



74AHC30; 74AHCT30

8-input NAND gate

Rev. 8 — 28 April 2025

Product data sheet

1. General description

The 74AHC30; 74AHCT30 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC30; 74AHCT30 provides an 8-input NAND function.

2. Features and benefits

- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- Input levels:
 - For 74AHC30: CMOS level
 - For 74AHCT30: TTL level
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC30D 74AHCT30D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHC30PW 74AHCT30PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHC30BQ 74AHCT30BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74AHC30BZ 74AHCT30BZ	-40 °C to +125 °C	DHXQFN14	plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 14 terminals; 0.4 mm pitch; body 2 mm × 2 mm × 0.48 mm	SOT8014-1
74AHC30GU12	-40 °C to +125 °C	XQFN12	plastic, extremely thin quad flat package; no leads; 12 terminals; body 1.70 × 2.0 × 0.50 mm	SOT1174-1

nexperia

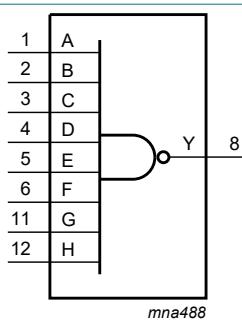
4. Marking

Table 2. Marking codes

Type number	Marking
74AHC30D	74AHC30D
74AHCT30D	74AHCT30D
74AHC30PW	AHC30
74AHCT30PW	AHCT30
74AHC30BQ	AHC30
74AHCT30BQ	AHT30
74AHC30BZ	A30
74AHCT30BZ	C30
74AHC30GU12	A3 [1]

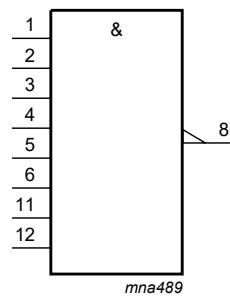
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



Pin numbers are shown for SO14, TSSOP14, DHVQFN14 and DHXQFN14 packages only

Fig. 1. Logic symbol



Pin numbers are shown for SO14, TSSOP14, DHVQFN14 and DHXQFN14 packages only

Fig. 2. IEC logic symbol

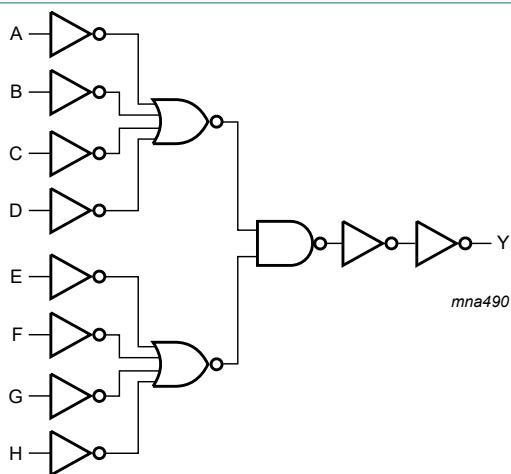
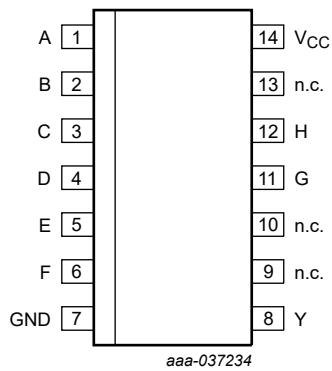


Fig. 3. Logic diagram

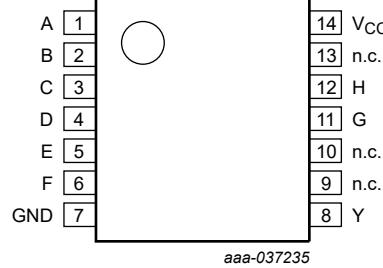
6. Pinning information

6.1. Pinning

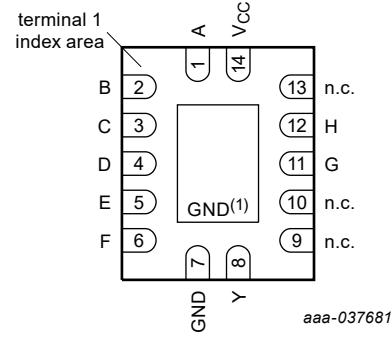
D package
SOT108-1 (SO14)



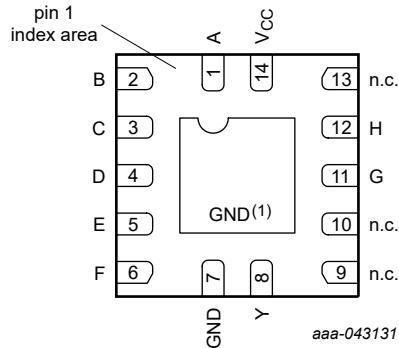
PW package
SOT402-1 (TSSOP14)



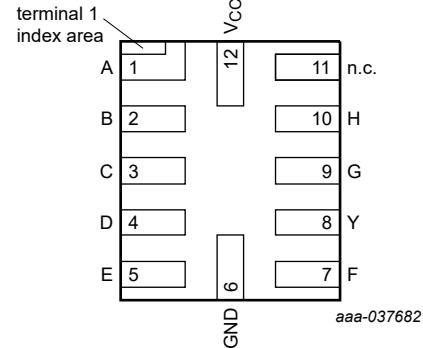
BQ package
SOT762-1 (DHVQFN14)



BZ package
SOT8014-1 (DHXQFN14)



GU12 package
SOT1174-1 (XQFN12)



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	SO14, TSSOP14, DHVQFN14 and DHXQFN14	XQFN12	
A	1	1	data input
B	2	2	data input
C	3	3	data input
D	4	4	data input
E	5	5	data input
F	6	7	data input
GND	7	6	ground (0 V)
Y	8	8	data output
n.c.	9	-	not connected
n.c.	10	-	not connected
G	11	9	data input
H	12	10	data input
n.c.	13	11	not connected
V _{CC}	14	12	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input								Output
A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	[1]	-20	- mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-20	+20 mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	-25	+25	mA
I_{CC}	supply current		-	+75	mA
I_{GND}	ground current		-75	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C			
		SOT108-1 (SO14)	[2]	-	500 mW
		SOT402-1 (TSSOP14)			
		SOT762-1 (DHVQFN14)		-	250 mW
		SOT8014-1 (DHXQFN14)			
		SOT1174-1 (XQFN12)		-	

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC30			74AHCT30			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3$ V ± 0.3 V	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0$ V ± 0.5 V	-	-	20	-	-	20	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC30										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -50 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -50 µA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -50 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I _O = -8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 µA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2.0	-	20	-	40	µA
C _I	input capacitance	V _I = V _{CC} or GND	-	3	10	-	10	-	10	pF
C _O	output capacitance		-	4	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHCT30										
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
		$I_O = -50 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -8.0 \text{ mA}$	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
		$I_O = 50 \mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	$V_I = 5.5 \text{ V or GND}; V_{CC} = 0 \text{ V to } 5.5 \text{ V}$	-	-	0.1	-	1.0	-	2.0	μA
I_{CC}	supply current	$V_I = V_{CC} \text{ or GND}; I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}; \text{ other pins at } V_{CC} \text{ or GND}; I_O = 0 \text{ A}; V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance	$V_I = V_{CC} \text{ or GND}$	-	3	10	-	10	-	10	pF
C_O	output capacitance		-	4	-	-	-	-	-	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Fig. 5](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC30										
t_{pd}	propagation delay	A, B, C, D, E, F, G, H to Y; see Fig. 4 and Fig. 5 [2]								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	5.0	9.5	1.0	11.0	1.0	12.0	ns
		$C_L = 50 \text{ pF}$	-	6.7	12.0	1.0	14.5	1.0	15.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	3.6	6.5	1.0	7.5	1.0	8.0	ns
		$C_L = 50 \text{ pF}$	-	4.9	8.0	1.0	9.5	1.0	10.5	ns
C_{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz}$; $V_i = \text{GND to } V_{CC}$	[3]	-	10	-	-	-	-	pF
74AHCT30; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$										
t_{pd}	propagation delay	A, B, C, D, E, F, G, H to Y; see Fig. 4 and Fig. 5 [2]								
		$C_L = 15 \text{ pF}$	-	3.3	6.5	1.0	7.5	1.0	8.0	ns
		$C_L = 50 \text{ pF}$	-	4.7	8.5	1.0	9.5	1.0	10.5	ns
C_{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz}$; $V_i = \text{GND to } V_{CC}$	[3]	-	12	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage ($V_{CC} = 3.3 \text{ V}$ and $V_{CC} = 5.0 \text{ V}$).

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

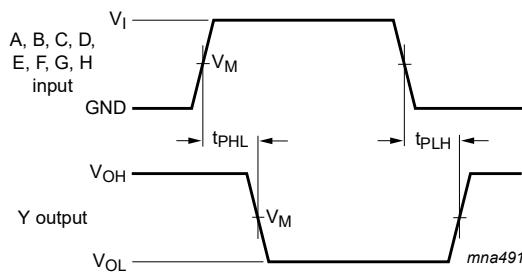
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$$\Sigma(C_L \times V_{CC}^2 \times f_o) = \text{sum of the outputs.}$$

11.1. Waveforms and test circuit



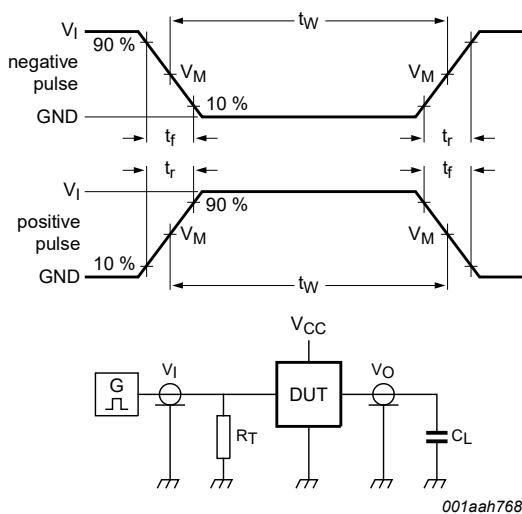
Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 4. Input to output propagation delays

Table 9. Measurement points

Type	Input	Output
	V_M	V_M
74AHC30	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT30	1.5 V	$0.5 \times V_{CC}$



Test data is given in [Table 10](#).

Definitions test circuit:

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator;

C_L = load capacitance including jig and probe capacitance.

Fig. 5. Test circuit for measuring switching times

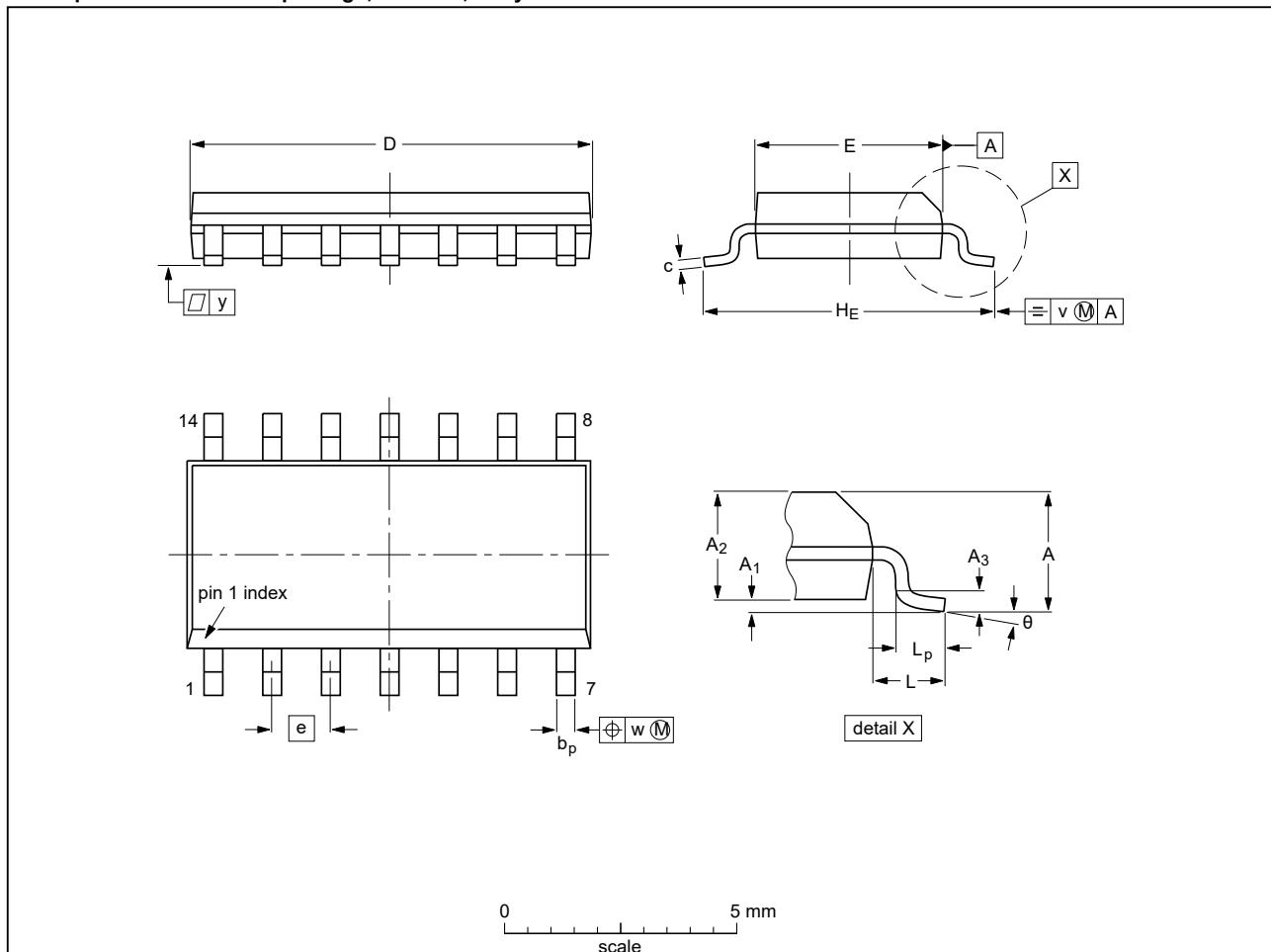
Table 10. Test data

Type	Input		Load	Test
	V_I	t_r, t_f		
74AHC30	V_{CC}	$\leq 3.0 \text{ ns}$	15 pF, 50 pF	t_{PLH}, t_{PHL}
74AHCT30	3.0 V	$\leq 3.0 \text{ ns}$	15 pF, 50 pF	t_{PLH}, t_{PHL}

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit	A	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	v	w	y	θ	
mm	max	1.75	0.25		0.51	0.25	8.75	4.0		6.2		1.27		0.2	0.25	0.1	8°
	nom				0.25				1.27		1.05						
	min		0.10	1.25		0.31	0.10	8.55	3.8		5.8	0.4					0°
inches	max	0.069	0.010		0.020	0.010	0.344	0.16		0.244		0.05		0.008	0.01	0.004	8°
	nom				0.01				0.05		0.041						
	min		0.004	0.049		0.012	0.004	0.337	0.15		0.228	0.016					0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot108-1 po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT108-1		MS-012			 	03-02-19 23-10-27

Fig. 6. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

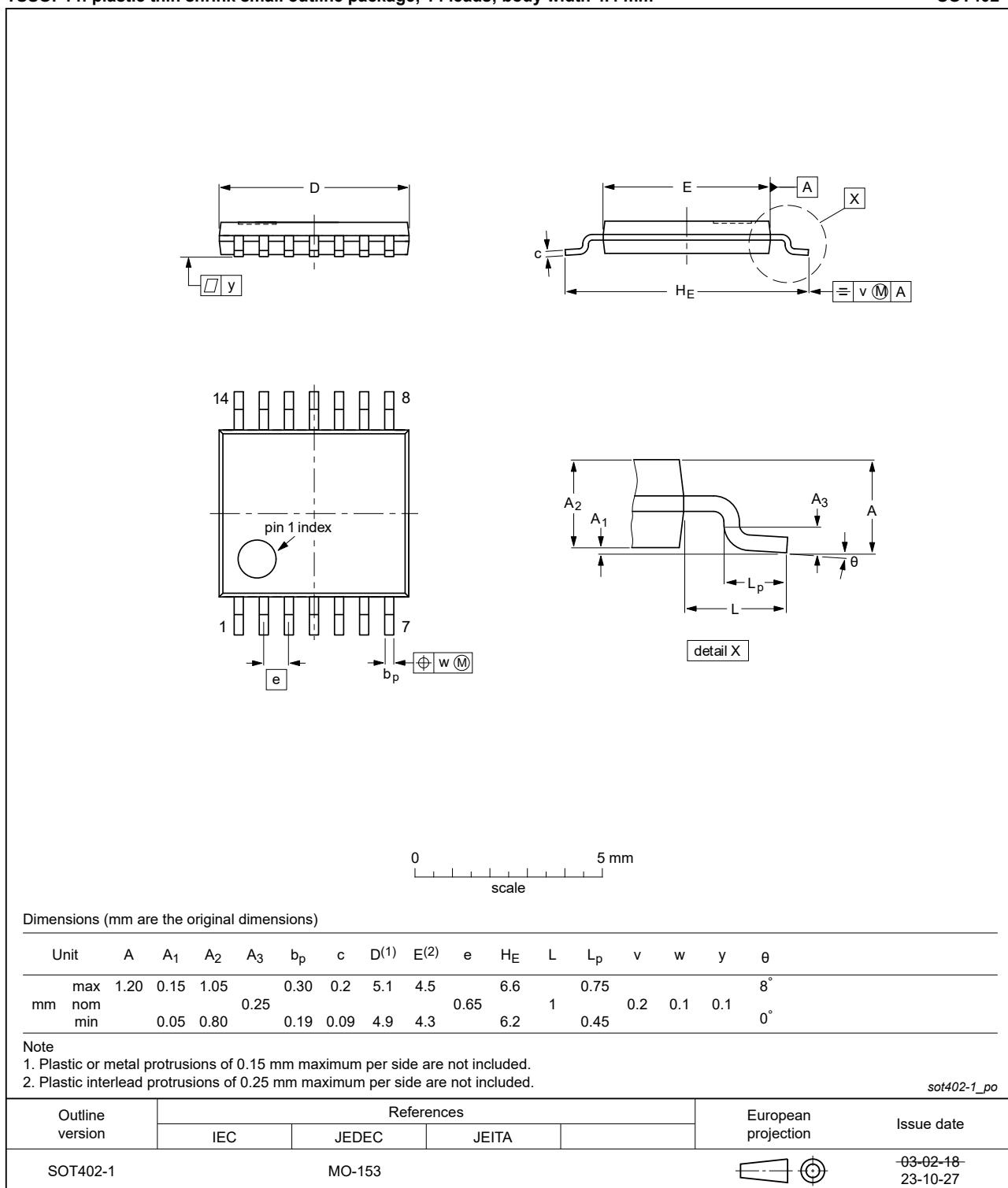


Fig. 7. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

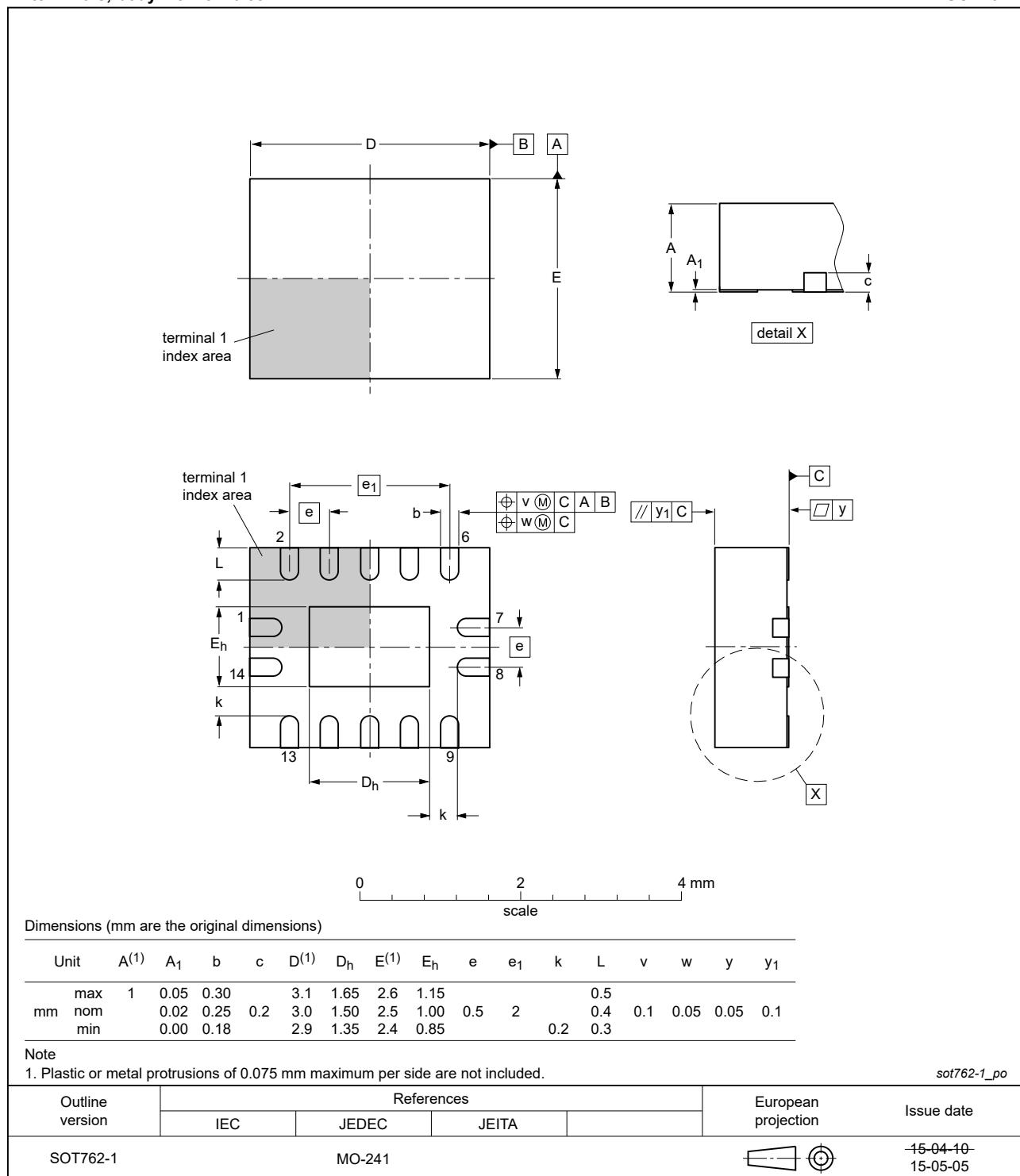


Fig. 8. Package outline SOT762-1 (DHVQFN14)

DHXQFN14: plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 14 terminals; 0.4 mm pitch; body 2 mm x 2 mm x 0.48 mm

SOT8014-1

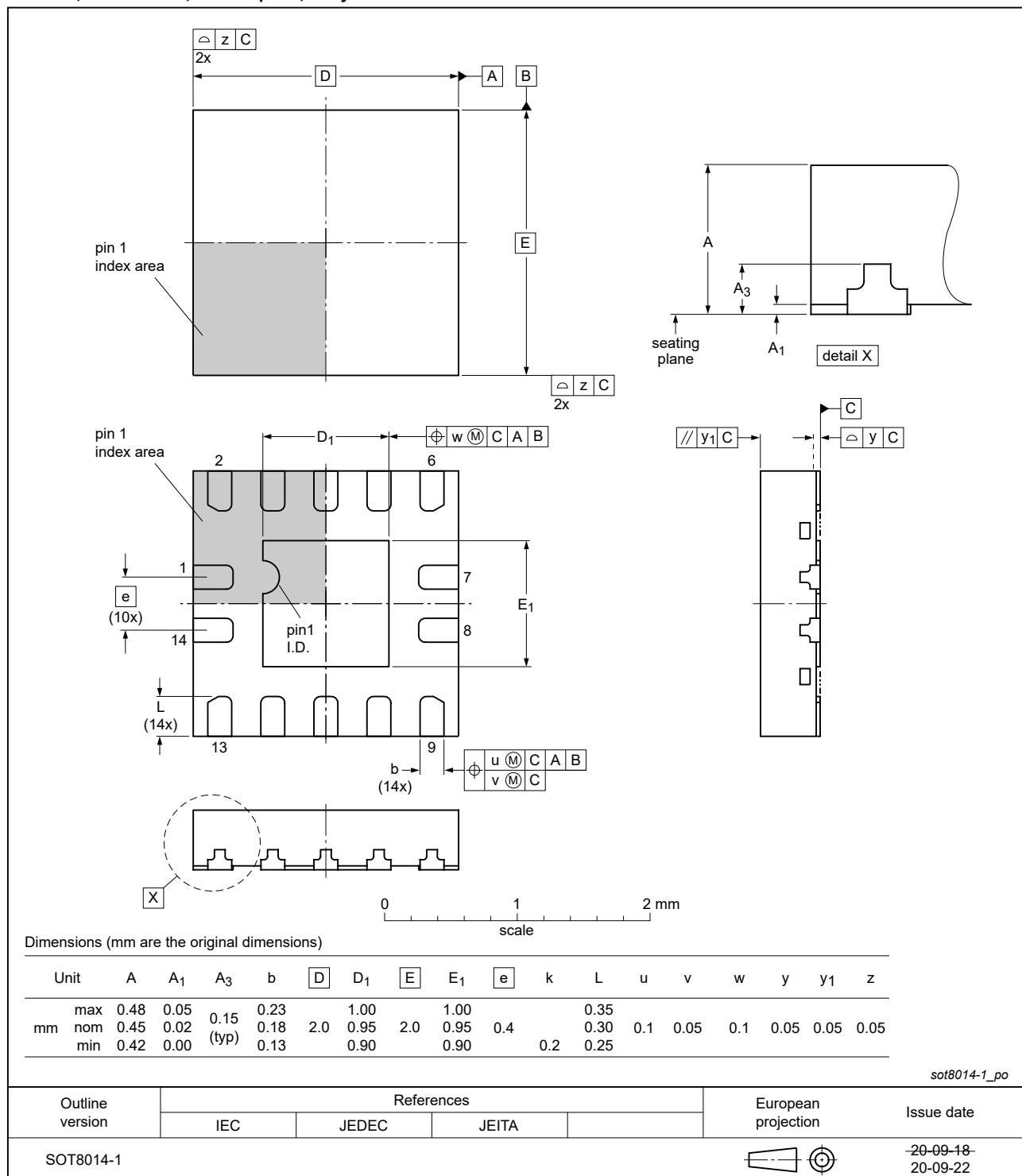


Fig. 9. Package outline SOT8014-1 (DHXQFN14)

XQFN12: plastic, extremely thin quad flat package; no leads;
12 terminals; body 1.70 x 2.00 x 0.50 mm

SOT1174-1

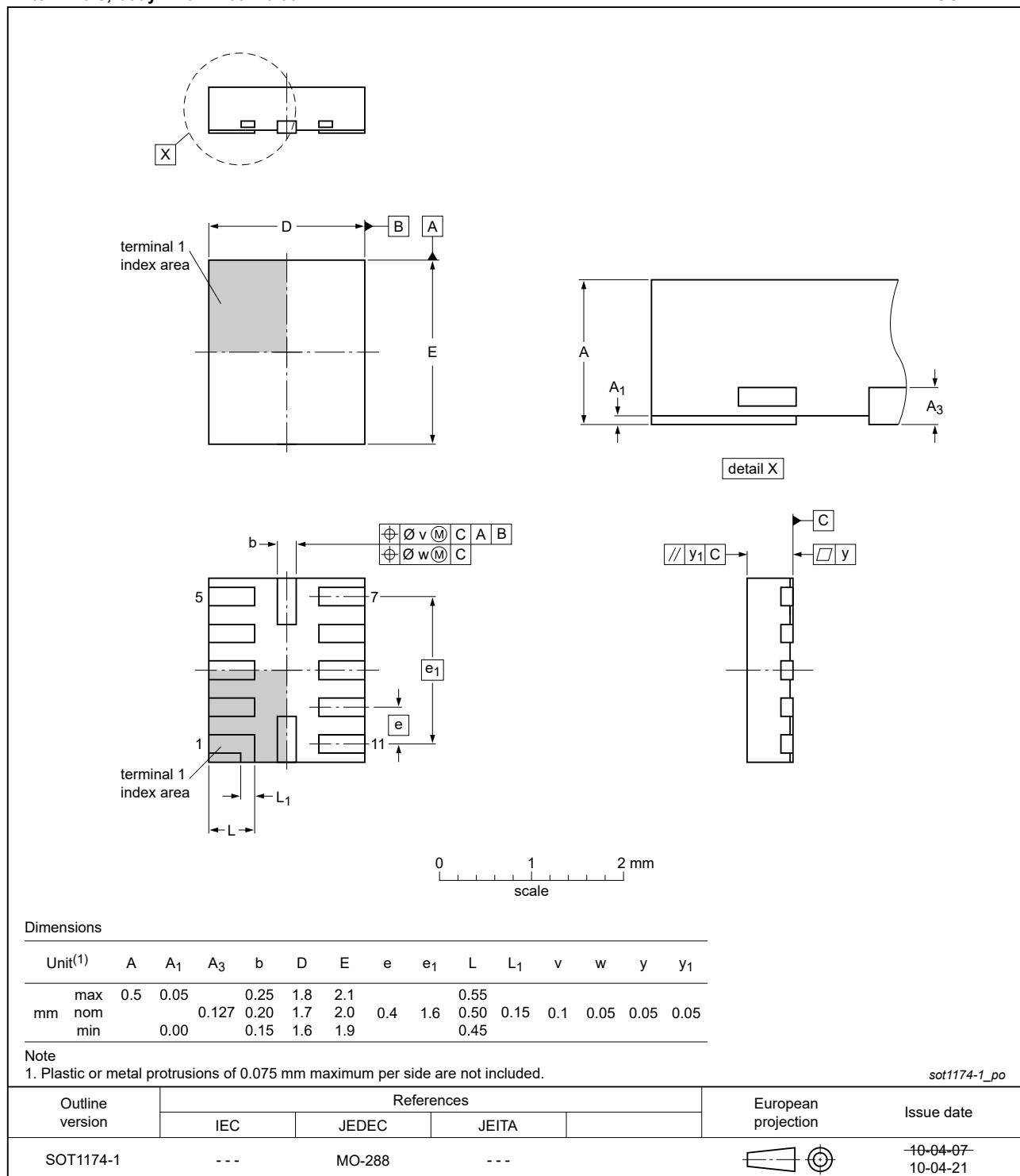


Fig. 10. Package outline SOT1174-1 (XQFN12)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
LSTTL	Low-power Schottky Transistor-Transistor Logic
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT30 v.8	20250428	Product data sheet	-	74AHC_AHCT30 v.7
Modifications:	<ul style="list-style-type: none"> Type numbers 74AHC30BZ and 74AHCT30BZ (SOT8014-1/DHXFNQ14) added. 			
74AHC_AHCT30 v.7	20240307	Product data sheet	-	74AHC_AHCT30 v.6
Modifications:	<ul style="list-style-type: none"> Fig. 6, Fig. 7: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. 			
74AHC_AHCT30 v.6	20231009	Product data sheet	-	74AHC_AHCT30 v.5
Modifications:	<ul style="list-style-type: none"> Section 2: ESD specification updated according to the latest JEDEC standard. 			
74AHC_AHCT30 v.5	20200506	Product data sheet	-	74AHC_AHCT30 v.4
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Table 5: Derating values for P_{tot} total power dissipation have been updated. 			
74AHC_AHCT30 v.4	20150722	Product data sheet	-	74AHC_AHCT30 v.3
Modifications:	<ul style="list-style-type: none"> Added type number 74AHC30GU12. 			
74AHC_AHCT30 v.3	20090626	Product data sheet	-	74AHC_AHCT30 v.2
Modifications:	<ul style="list-style-type: none"> Section 3: DHVQFN14 package added. Section 8: derating values added for DHVQFN14 package. Section 12: outline drawing added for DHVQFN14 package. 			
74AHC_AHCT30 v.2	20080530	Product data sheet	-	74AHC_AHCT30 v.1
74AHC_AHCT30 v.1	19991130	Product specification	-	-

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT30_Q100 v.4	20240307	Product data sheet	-	74AHC_AHCT30_Q100 v.3
Modifications:	<ul style="list-style-type: none"> Fig. 6, Fig. 7: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. 			
74AHC_AHCT30_Q100 v.3	20231009	Product data sheet	-	74AHC_AHCT30_Q100 v.2

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	<ul style="list-style-type: none">• #unique_18: ESD specification updated according to the latest JEDEC standard.			
74AHC_AHCT30_Q100 v.2	20200506	Product data sheet	-	74AHC_AHCT30_Q100 v.1
Modifications:	<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.• Legal texts have been adapted to the new company name where appropriate.• Table 5: Derating values for P_{tot} total power dissipation have been updated.• Package outline drawing of SOT762-1 (Fig. 8) updated.			
74AHC_AHCT30_Q100 v.1	20131120	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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