19-3375; Rev 0; 7/04

Dual SPDT Analog Switches with Over-Rail Signal Handling

General Description

The MAX4850/MAX4850H/MAX4852/MAX4852H family of dual SPDT (single-pole/double-throw) switches operate from a single +2V to +5.5V supply and can handle signals greater than the supply rail. These switches feature low 3.5Ω or 3.5Ω/7Ω on-resistance with low on-capacitance, making them ideal for switching audio and data signals.

The MAX4850/MAX4850H are configured with two SPDT switches and feature two comparators for headphone detection or mute/send key functions. The MAX4852 has two SPDT switches with no comparators for low 1µA supply current.

For over-rail applications, these devices offer either the pass-through or high-impedance option. For the MAX4850/MAX4852, the signal (up to 5.5V) passes through the switch without distortion even when the positive supply rail is exceeded. For the MAX4850H/MAX4852H, the switch input becomes high impedance when the input signal exceeds the supply rail.

The MAX4850/MAX4850H/MAX4852/MAX4852H are available in the space-saving (3mm x 3mm), 16-pin TQFN package and operate over the extended temperature range of -40°C to +85°C.

Applications

USB Switching

Audio-Signal Routing

Cellular Phones

Notebook Computers

PDAs and Other Handheld Devices

Features

- **USB 2.0 Full Speed (12MB) and USB 1.1 Signal Switching Compliant**
- **Switch Signals Greater than V_{CC}**
- **0.1ns Differential Skew**
- **3.5Ω/7Ω On-Resistance**
- **135MHz -3dB Bandwidth**
- **+2V to +5.5V Supply Range**
- **1.8V Logic Compatible**
- **Low Supply Current**
  1µA (MAX4852)
  5µA (MAX4850)
  10µA (MAX4850H/MAX4852H)
- **Available in a Space-Saving (3mm x 3mm), 16-Pin TQFN Package**

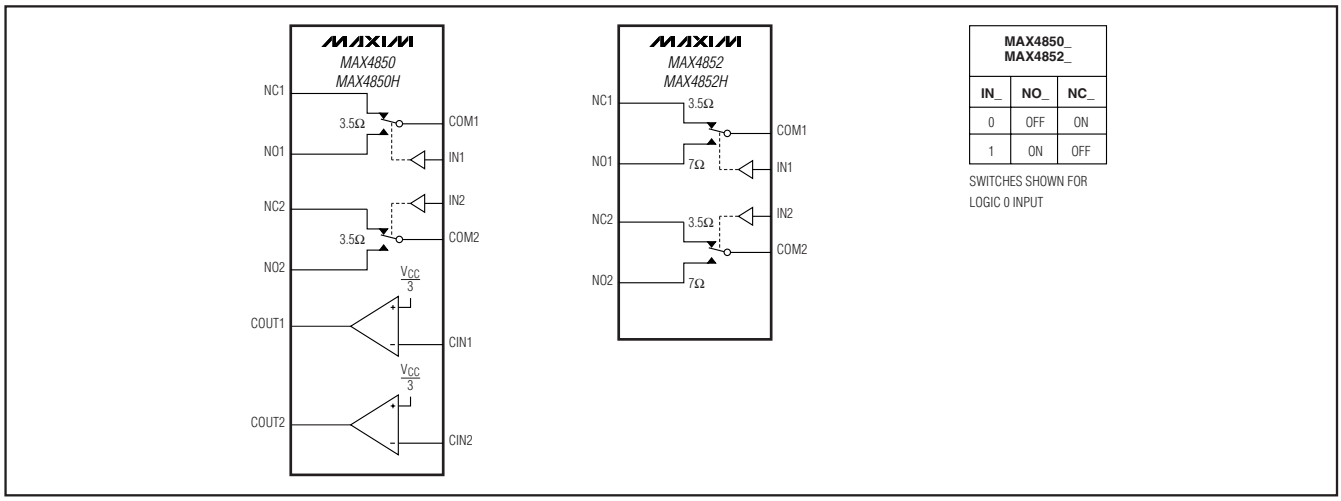
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4850ETE	-40°C to +85°C	16 TQFN-EP*	ABU
MAX4850HETE	-40°C to +85°C	16 TQFN-EP*	ABV
MAX4852ETE	-40°C to +85°C	16 TQFN-EP*	ABZ
MAX4852HETE	-40°C to +85°C	16 TQFN-EP*	ACA

**EP = Exposed paddle.*

Pin Configurations and Selector Guide appear at end of data sheet.

Block Diagrams/Truth Table



Dual SPDT Analog Switches with Over-Rail Signal Handling

Detailed Description

The MAX4850/MAX4850H/MAX4852/MAX4852H are low on-resistance, low-voltage, analog switches that operate from a +2V to +5.5V single supply and are fully specified for nominal 3.0V applications. These devices feature over-rail signal capability that allows signals up to 5.5V with supply voltages down to 2.0V. These devices are configured as dual SPDT switches.

These switches have low 50pF on-channel capacitance, which allows for 12Mbps switching of the data signals for USB 2.0 full speed/1.1 applications. The MAX485__ are designed to switch D+ and D- USB signals with a guaranteed skew of less than 1ns (see Figure 1), as measured from 50% of the input signal to 50% of the output signal.

The MAX4850_ feature a comparator that can be used for headphone or mute detection. The comparator threshold is internally generated to be approximately 1/3 of V_{CC}.

Applications Information

Digital Control Inputs

The logic inputs (IN_) accept up to +5.5V even if the supply voltages are below this level. For example, with a +3.3V V_{CC} supply, IN_ can be driven low to GND and high to +5.5V, allowing for mixing of logic levels in a system. Driving IN_ rail-to-rail minimizes power consumption. For a +2V supply voltage, the logic thresholds are 0.5V (low) and 1.4V (high); for a +5V supply voltage, the logic thresholds are 0.8V (low) and 1.8V (high).

Analog Signal Levels

The on-resistance of these switches changes very little for analog input signals across the entire supply voltage range (see *Typical Operating Characteristics*). The switches are bidirectional, so NO_, NC_, and COM_ can be either inputs or outputs.

Comparator

The positive terminal of the comparator is internally set to $V_{CC}/3$. When the negative terminal (CIN_) is below the threshold ($V_{CC}/3$), the comparator output (COUT_) goes high. When CIN_ rises above $V_{CC}/3$, COUT_ goes low.

The comparator threshold allows for detection of headphones since headphone audio signals are typically biased to $V_{CC}/2$.

Power-Supply Sequencing

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V_{CC} before applying analog signals, especially if the analog signal is not current-limited.

Dual SPDT Analog Switches with Over-Rail Signal Handling

Test Circuits/Timing Diagrams

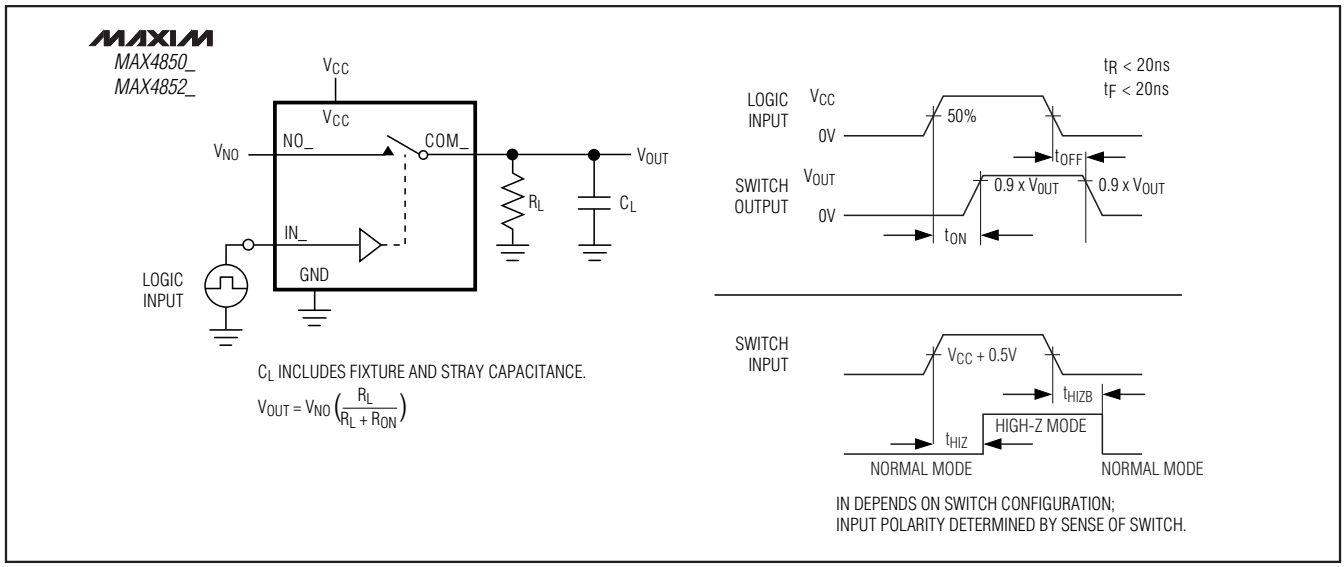


Figure 1. Switching Time

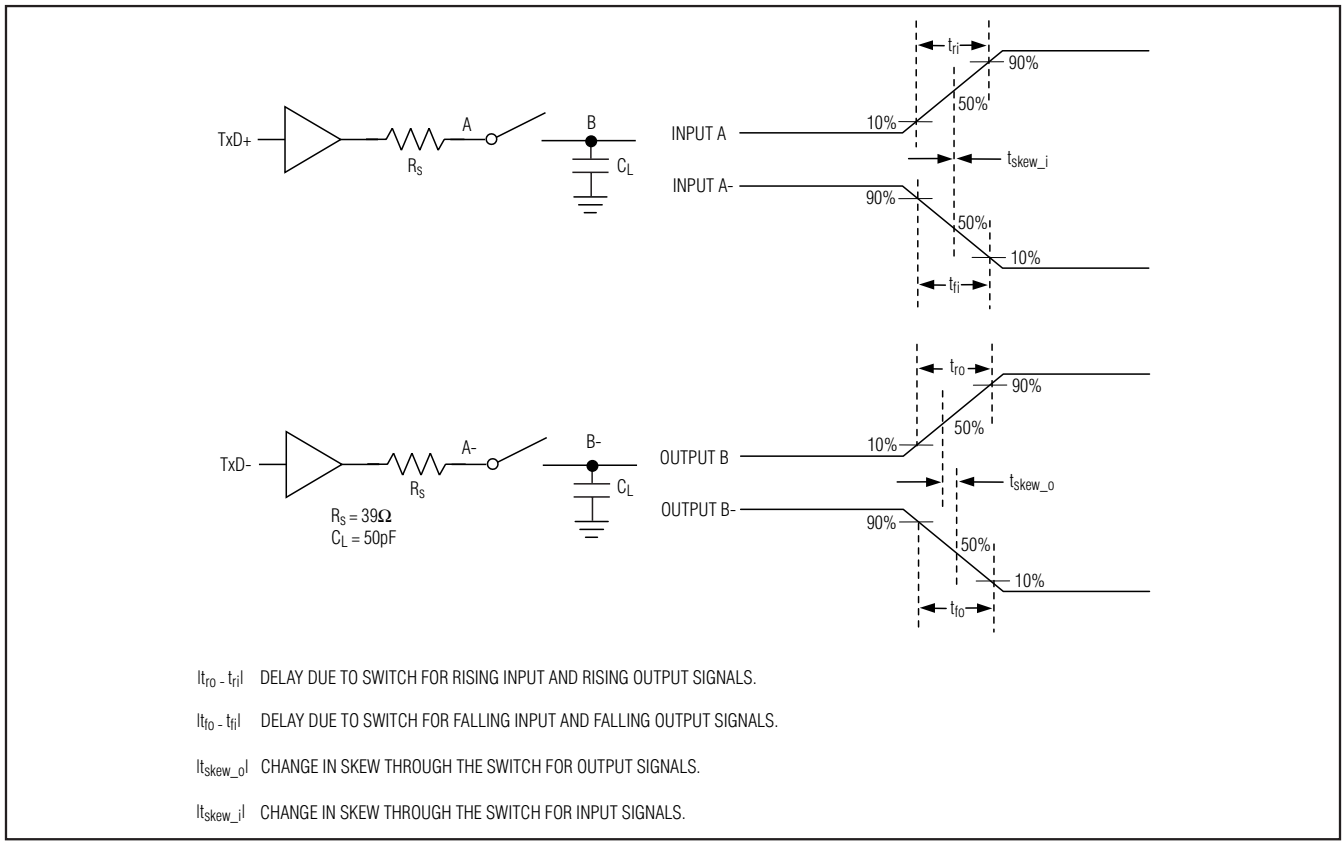


Figure 2. Input/Output Skew Timing Diagram

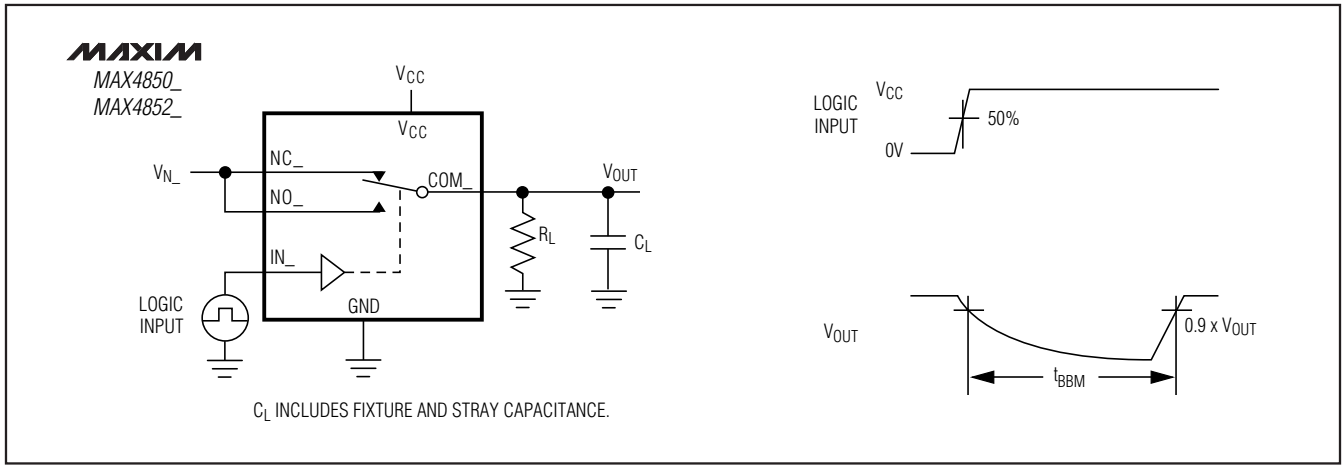


Figure 3. Break-Before-Make Interval

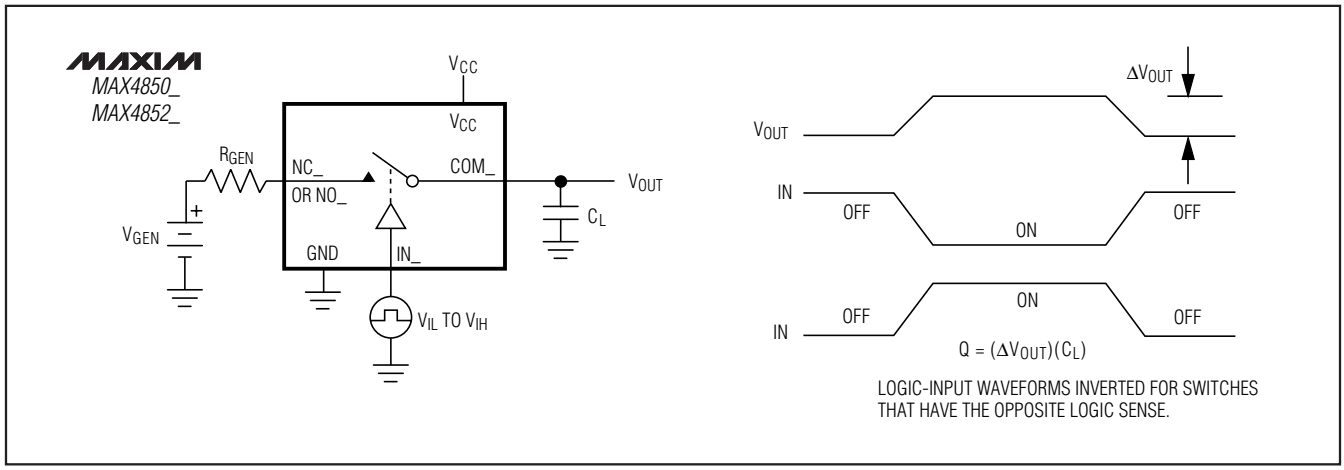


Figure 4. Charge Injection

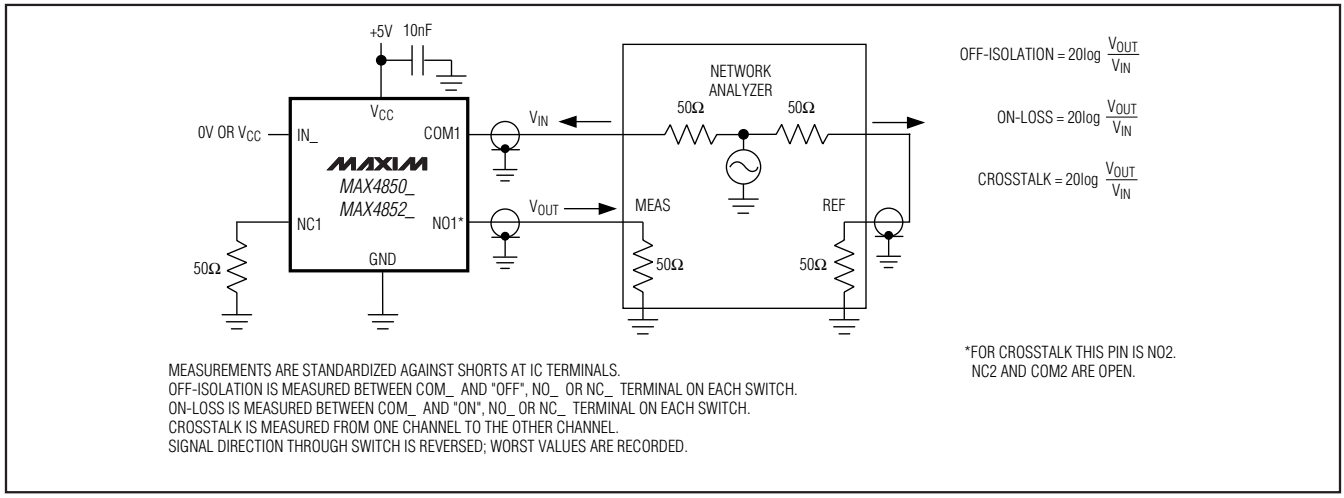


Figure 5. On-Loss, Off-Isolation, and Crosstalk

Dual SPDT Analog Switches with Over-Rail Signal Handling

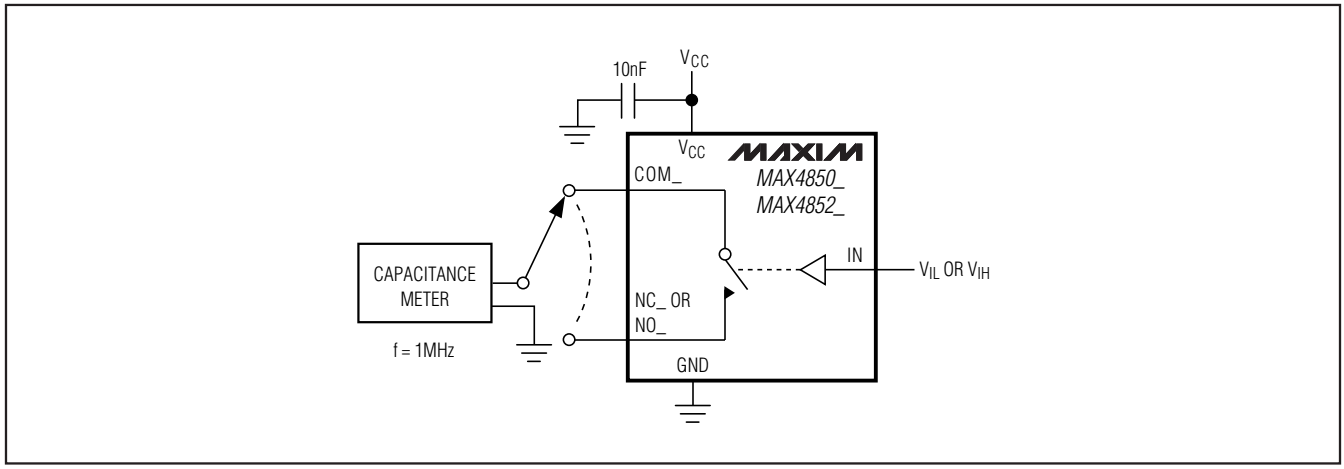


Figure 6. Channel Off-/On-Capacitance

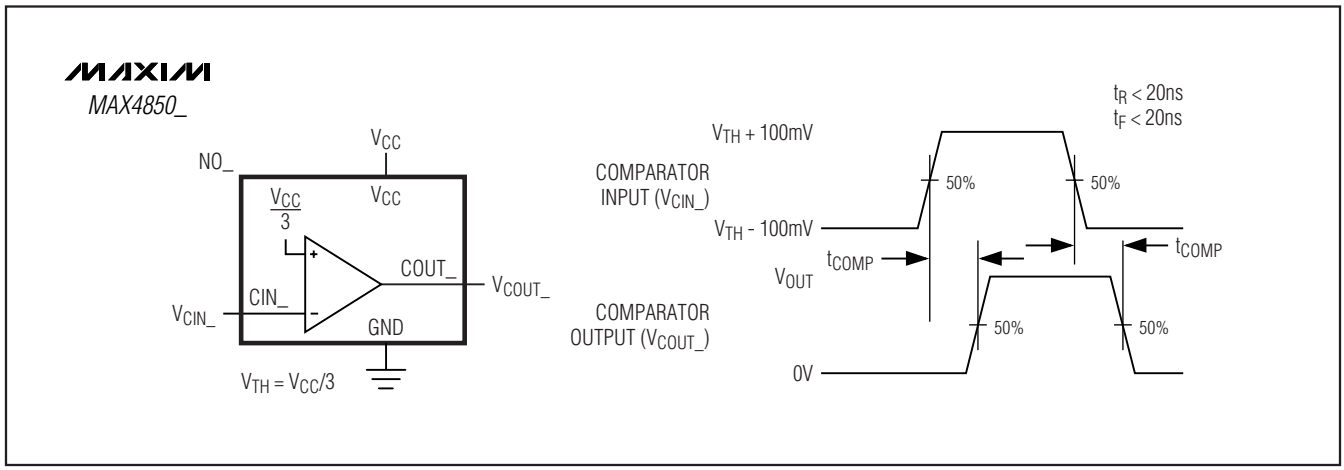
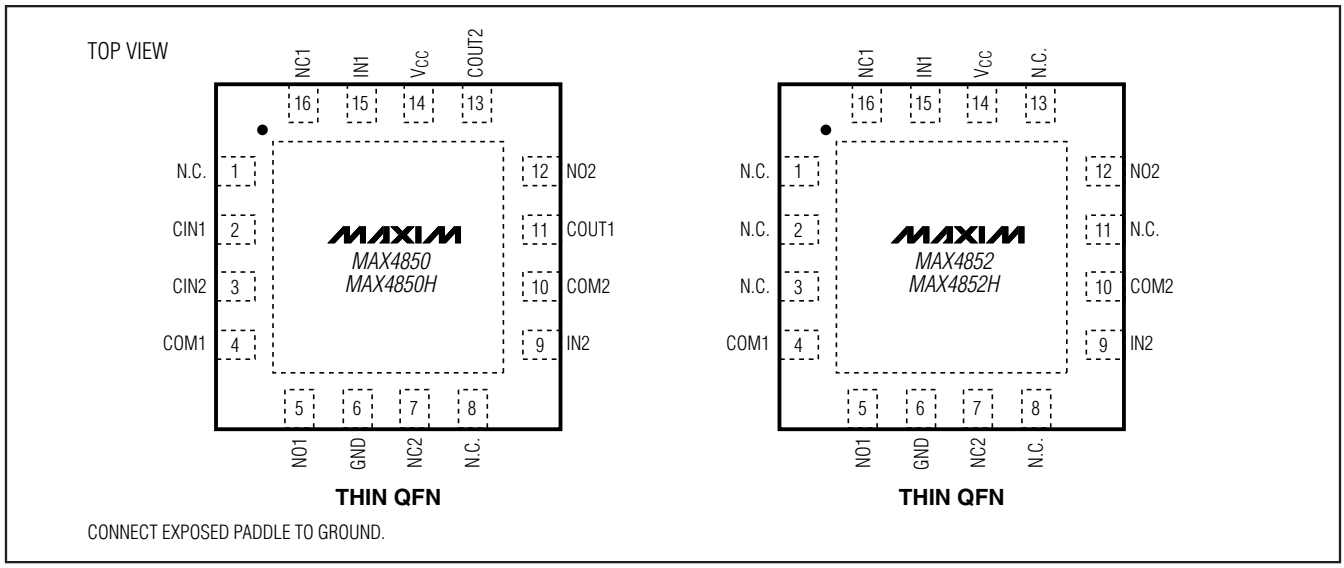


Figure 7. Comparator Switching Time

Dual SPDT Analog Switches with Over-Rail Signal Handling

Pin Configurations



CONNECT EXPOSED PADDLE TO GROUND.

Selector Guide

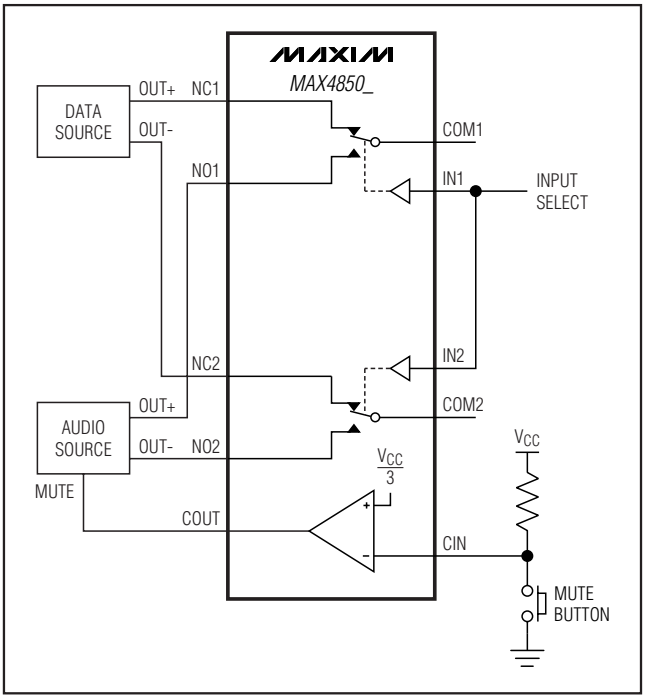
PART	R_{ON} NC_/NO_ (Ω)	COMPARATORS	OVER-RAIL HANDLING
MAX4850	3.5/3.5	2	Input signal passes through the switch
MAX4850H	3.5/3.5	2	High-impedance switch input
MAX4852	3.5/7	—	Input signal passes through the switch
MAX4852H	3.5/7	—	High-impedance switch input

Chip Information

TRANSISTOR COUNT: 735

PROCESS: CMOS

Typical Operating Circuit

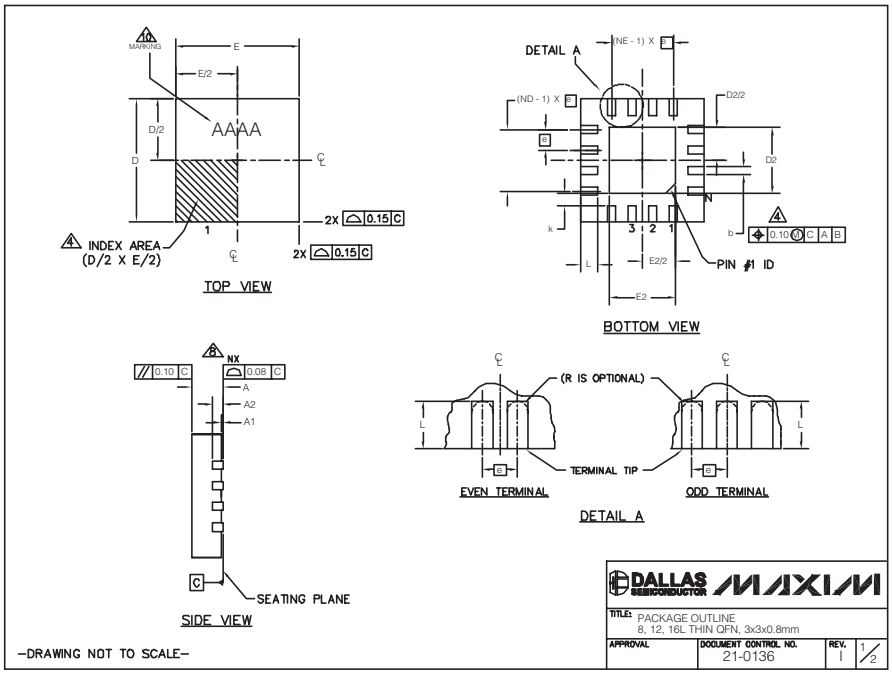


Dual SPDT Analog Switches with Over-Rail Signal Handling

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

12x16L QFN THIN.EPS



PKG	8L 3x3			12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N	8			12			16		
ND	2			3			4		
NE	2			3			4		
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633-5	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS .
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
12. WARPAGE NOT TO EXCEED 0.10mm.

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE
8, 12, 16L THIN QFN, 3x3x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0136
REV. I
2/2
-DRAWING NOT TO SCALE-