Rev 0; 12/07

3.3V Margining Clock Oscillator with LVPECL/LVDS Output

General Description

The DS4M125/DS4M133/DS4M200 are margining clock oscillators with LVPECL or LVDS outputs. They are designed to fit in a 5mm x 3.2mm ceramic package with an AT-cut fundamental-mode crystal to form a complete clock oscillator. The circuit can generate the following frequencies and their ±5% frequency deviations: 125MHz, 133.33MHz, and 200MHz. The DS4M125/DS4M133/DS4M200 employ a low-jitter PLL to generate the frequencies. The typical phase jitter is less than 0.9ps RMS from 12kHz to 20MHz.

Frequency margining is a circuit operation to change the output frequency to 5% higher or 5% lower than the nominal frequency. Frequency margining is accomplished through the margining select pin, MS. This three-state input pin accepts a three-level voltage signal to control the output frequency. In a low-level state, the output frequency is set to the nominal frequency. When set to a high-level state, the frequency output is set to the nominal frequency plus 5%. When set to the mid-level state, the frequency output is equal to the nominal frequency minus 5%. If left open, the MS pin is pulled low by an internal 100kΩ (nominal) pulldown resistor.

The DS4M125/DS4M133/DS4M200 are available with either an LVPECL or LVDS output. The output can be disabled by pulling the OE pin low. When disabled, both OUTP and OUTN levels of the LVPECL driver go to the LVPECL bias voltage, while the output of the LVDS driver is a logical one. The OE input is an active-high logic signal and has an internal 100kΩ pullup resistor. When OE is in a logic-high state, the OUTP and OUTN outputs are enabled.

The devices operate from a single 3.3V supply voltage.

Applications

Memory Clocks

RAID Systems

Features

- **Frequency Margining: ±5%**
- **Nominal Clock Output Frequencies: 125MHz, 133.33MHz, and 200MHz**
- **Jitter < 0.9ps RMS from 12kHz to 20MHz**
- **LVPECL or LVDS Output**
- **3.3V Operating Voltage**
- **Operating Temperature Range: -40°C to +85°C**
- **Supply Current: < 100mA at 3.3V**
- **Excellent Power-Supply Noise Rejection**
- **5mm x 3.2mm Ceramic LCCC Package**
- **Output Enable/Disable**

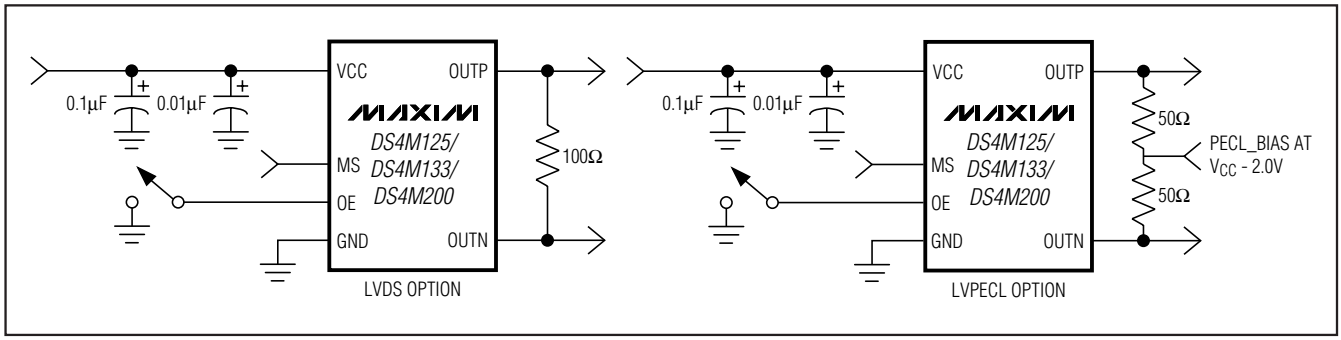
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS4M125P+33	-40°C to +85°C	10 LCCC
DS4M125D+33	-40°C to +85°C	10 LCCC
DS4M133P+33	-40°C to +85°C	10 LCCC
DS4M133D+33	-40°C to +85°C	10 LCCC
DS4M200P+33	-40°C to +85°C	10 LCCC
DS4M200D+33	-40°C to +85°C	10 LCCC

+Denotes a lead(Pb)-free package. The lead finish is JESD97 category e4 (Au over Ni) and is compatible with both lead-based and lead-free soldering processes.

Pin Configuration and Selector Guide appear at end of data sheet.

Typical Operating Circuit



3.3V Margining Clock Oscillator with LVPECL/LVDS Output

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage Range (V_{CC}) .....-0.3V to +4.0V
Continuous Power Dissipation (T_A = +70°C) 330mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+125°C
Storage Temperature Range .....-55°C to +85°C
Soldering Temperature
(3 passes max of reflow).....Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.135V to 3.465V, T_A = -40°C to +85°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range		V_{CC}	(Note 1)	3.135	3.3	3.465	V
Operating Current		I_{CC_D}	LVDS, output loaded or unloaded		52	75	mA
		I_{CC_PU}	LVPECL, output unloaded		49	70	
		I_{CC_PI}	LVPECL, output loaded		74	100	
Inactive Current		I_{CC_OEZ}	$V_{OE} = V_{IL}$		52	85	mA
OUTPUT FREQUENCY SPECIFICATIONS							
Frequency	DS4M125	f_O	MS = 0, OE = 1		125		MHz
	DS4M133		MS = 0, OE = 1		133.33		
	DS4M200		MS = 0, OE = 1		200		
Frequency Stability		$\Delta f_{TOTAL}/f_O$	Over temperature range, aging, load, supply, and initial tolerance (Note 3)	-50		+50	ppm
Frequency Stability Over Temperature		$\Delta f_{TEMP}/f$	V_{CC} = 3.3V	-35		+35	ppm
Initial Tolerance		$\Delta f_{INITIAL}/f_V$	V_{CC} = 3.3V, T_A = +25°C		±20		ppm
Frequency Change Due to ΔV_{CC}		$\Delta f_{VCC}/f$	V_{CC} = 3.3V ±5%	-3		+3	ppm/V
Frequency Change Due to Load Variation		$\Delta f_{LOAD}/f_O$	±10% variation in termination resistance		±1		ppm
Aging (15 Years)		Δf_{AGING}		-7		+7	ppm
Phase Jitter		J_{RMS}	Integrated phase RMS; 12kHz to 80MHz, V_{CC} = 3.3V, T_A = +25°C		< 0.9		ps
Accumulated Deterministic Jitter Due to Reference Spurs			No margin 155.52MHz output		0.6		ps
Accumulated Deterministic Jitter Due to Power-Supply Noise			10kHz		12.9		ps
			100kHz (Note 4)		26.3		
			200kHz (Note 4)		20.1		
			1MHz (Note 4)		6.4		
Startup Time		t_{STRT}			1.0		ms
Frequency Switch Time		t_{SWITCH}			0.5		ms
Input-Voltage High (OE)		V_{IH}	(Note 5)	0.7 x V_{CC}		V_{CC}	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.135V to 3.465V, T_A = -40°C to +85°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input-Voltage Low (OE)	V_{IL}	(Note 5)	0		0.3 x V_{CC}	V
Input-Leakage High (OE)	I_{LEAKH}	OE voltage = VCC	-5		+5	µA
Input-Leakage Low (OE)	I_{LEAKL}	OE voltage = GND	-20		-50	µA
Input-Leakage High (MS)	I_{LEAKH}	MS voltage = VCC	20		50	µA
Input-Leakage Low (MS)	I_{LEAKL}	MS voltage = GND	-5		+5	µA
Input Voltage: High Level (MS)	V_{IH}	(Note 5)	0.75 x V_{CC} + 0.15V		V_{CC}	V
Input Voltage: Mid Level (MS)	V_{IM}	(Note 5)	0.25 x V_{CC} + 0.15V		0.75 x V_{CC} - 0.15V	V
Input Voltage: Low Level (MS)	V_{IL}	(Note 5)	0		0.25 x V_{CC} - 0.15V	V
LVDS						
Output High Voltage	V_{OH}	100Ω differential load (Notes 2, 5)			1.475	V
Output Low Voltage	V_{OL}	100Ω differential load (Notes 2, 5)	0.925			V
Differential Output Voltage	$\|V_{OD}\|$	100Ω differential load	250		425	mV
Change in V_{OD} for Complementary States	$\Delta\|V_{OD}\|$	100Ω differential load			25	mV
Offset Output Voltage	V_{OS}	100Ω differential load (Note 2)	1.125		1.275	V
Change in V_{OS} for Complementary States	$\Delta\|V_{OS}\|$	100Ω differential load			150	mV
Differential Output Impedance	R_{OLVDS}		80		140	Ω
Output Current	$L_{VSSLVDSO}$	OUTN or OUTP shorted to ground and measure the current in the shorting path			40	mA
	L_{LVDSO}	OUTN and OUTP shorted together and measure the change in I_{CC}		6.5		
Output Rise Time (Differential)	t_{RLVDSO}	20% to 80%		175		ps
Output Fall Time (Differential)	t_{FLVDSO}	80% to 20%		175		ps
Duty Cycle	D_{CYCLE_LVDS}		45		55	%
Propagation Delay from OE Going LOW to Logical 1 at OUTP	t_{PA1}	(Figure 2)			200	ns
Propagation Delay from OE Going HIGH to Output Active	t_{P1A}	(Figure 2)			200	ns

3.3V Margining Clock Oscillator with LVPECL/LVDS Output

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.135V to 3.465V, T_A = -40°C to +85°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVPECL						
Output High Voltage (Note 2)	V_{OH}	Output connected to 50Ω at PECL_BIAS at V_{CC} - 2.0V	V_{CC} - 1.085		V_{CC} - 0.88	V
Output Low Voltage (Note 2)	V_{OL}	Output connected to 50Ω at PECL_BIAS at V_{CC} - 2.0V	V_{CC} - 1.825		V_{CC} - 1.62	V
Differential Voltage	V_{DIFF_PECL}	Output connected to 50Ω at PECL_BIAS at V_{CC} - 2.0V	0.595	0.710		V
Rise Time	t_{R-PECL}	20% to 80%		200		ps
Fall Time	t_{F-PECL}	80% to 20%		200		ps
Duty Cycle	D_{CYCLE_PECL}		45		55	%
Propagation Delay from OE Going LOW to Output Three-Stated	t_{PAZ}	(Figure 3)			200	ns
Propagation Delay from OE Going HIGH to Output Active	t_{PZA}	(Figure 3)			200	ns

Note 1: Limits at -40°C are guaranteed by design and are not production tested. Typical values are at +25°C and 3.3V, unless otherwise noted.

Note 2: AC parameters are guaranteed by design and characterization and are not production tested.

Note 3: Frequency stability is calculated as: $\Delta f_{TOTAL} = \Delta f_{INITIAL} + \Delta f_{TEMP} + (\Delta f_{VCC} \times 0.165) + \Delta f_{LOAD} + \Delta f_{AGING}$.

Note 4: Supply induced jitter is measured with a 50mV_{P-P} sine wave forced on V_{CC}. Deterministic jitter is calculated by measuring the power of the resulting tone seen on a spectrum analyzer.

Note 5: Voltage referenced to ground.

SINGLE-SIDEBAND PHASE NOISE AT $f_O = f_{NOM}$

f_M =	SINGLE-SIDEBAND PHASE NOISE AT $f_O = f_{NOM}$ (dBc/Hz)		
	125MHz	133.33MHz	200MHz
10Hz	-70	-75	-70
100Hz	-100	-105	-100
1kHz	-118	-121	-115
10kHz	-118	-122	-117
100kHz	-124	-126	-122
1MHz	-142	-141	-138
10MHz	-150	-150	-150
20MHz	-150	-150	-150

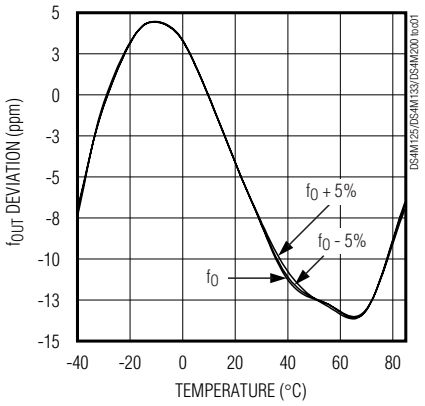
Pin Description

PIN	NAME	FUNCTION
1	OE	Active-High Output Enable. Has an internal pullup 100kΩ resistor.
2	MS	Margin Select. Three-level input with a 100kΩ pulldown resistor.
3	GND	Ground
4	OUTP	Positive Output for LVPECL or LVDS
5	OUTN	Negative Output for LVPECL or LVDS
6	VCC	Supply Voltage
7–10	N.C.	No Connection. Must be floated.
—	EP	Exposed Paddle. The exposed pad must be used for thermal relief. This pad must be connected to ground.

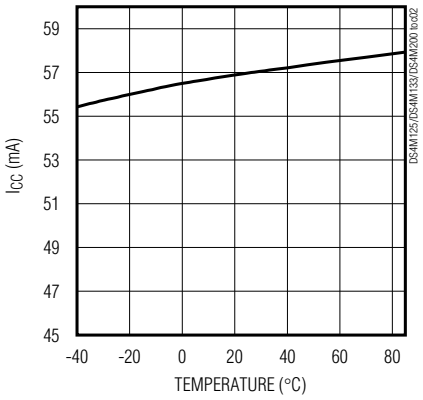
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

FREQUENCY vs. TEMPERATURE



CURRENT vs. TEMPERATURE



3.3V Margining Clock Oscillator with LVPECL/LVDS Output

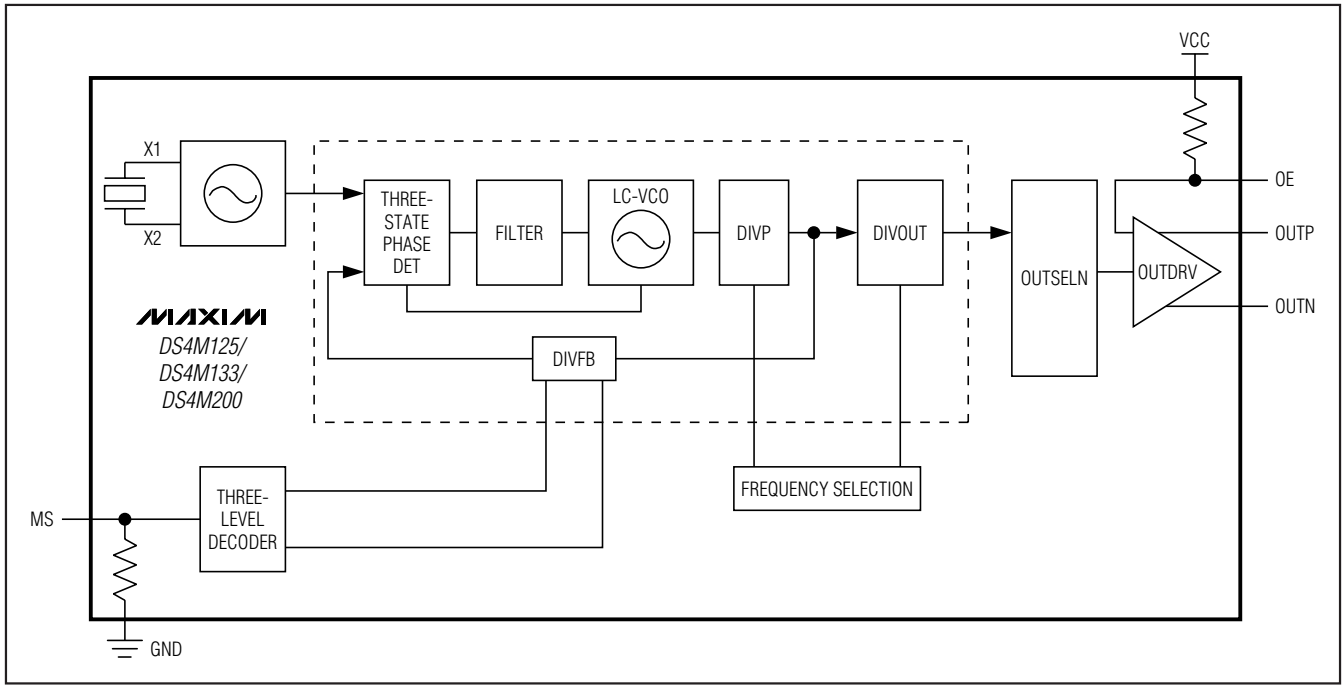


Figure 1. Functional Diagram

Detailed Description

The DS4M125/DS4M133/DS4M200 consist of an oscillator designed to oscillate with a fundamental-mode crystal and a PLL to synthesize the base frequency with its ±5% deviations. The output interface is either LVPECL or LVDS.

The ±5% frequency deviation is controlled through a three-level margining select (MS) pin. This three-state input pin accepts a three-level voltage signal to control the output frequency. In a low-level state, the output frequency is set to the nominal frequency. When set to a high-level state, the frequency output is set to the nominal frequency plus 5%. When set to the mid-level state, the frequency output is equal to the nominal frequency minus 5%. The MS pin has an internal 100kΩ pulldown resistor. When the pin is left floating, the devices output a nominal frequency.

The devices are available with either LVDS or LVPECL output drivers. When the OE signal is low, the LVPECL output driver is turned off and the output voltage goes to the PECL_BIAS level of V_{CC} - 2.0V, while the LVDS outputs are a logical one. The OE pin has an internal 100kΩ pullup resistor. When the pin is left floating, the device output is active.

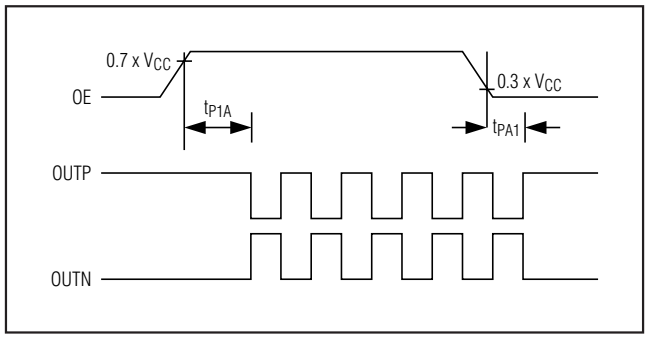


Figure 2. LVDS Output Timing Diagram When OE Is Enabled and Disabled

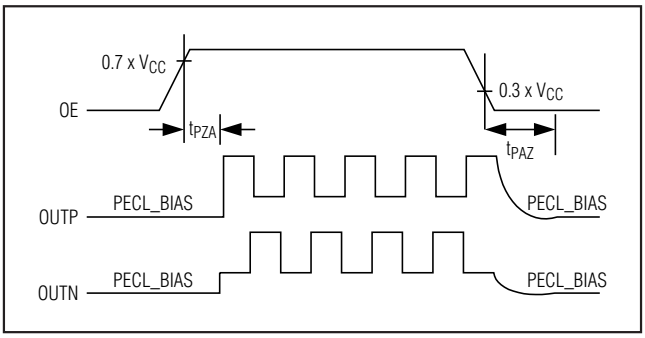


Figure 3. LVPECL Output Timing Diagram When OE Is Enabled and Disabled

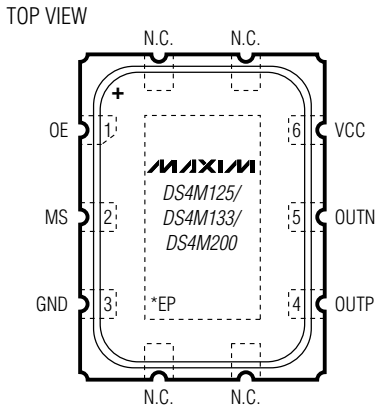
3.3V Margining Clock Oscillator with LVPECL/LVDS Output

Selector Guide

PART	FREQUENCY (NOM) (MHz)	OUTPUT TYPE	TOP MARK
DS4M125P+33	125	LVPECL	MEP
DS4M125D+33	125	LVDS	MED
DS4M133P+33	133.33	LVPECL	MFP
DS4M133D+33	133.33	LVDS	MFD
DS4M200P+33	200	LVPECL	MJP
DS4M200D+33	200	LVDS	MJD

+Denotes a lead-free package. The lead finish is JESD97 category e4 (Au over Ni) and is compatible with both lead-based and lead-free soldering processes. A + appears anywhere on the top mark.

Pin Configuration



LCCC
(5.00mm × 3.20mm × 1.49mm)

*EXPOSED PAD

Chip Information

SUBSTRATE CONNECTED TO GROUND

PROCESS: BiPOLAR SiGe

Thermal Information

THETA-JA (°C/W)
90

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10 LCCC	L1053+H2	**21-0389**