# MULTIFUNCTION 3-CHANNEL LED DRIVERS

**Check for Samples: TPS68401, TPS68402**

## FEATURES

- **Multifunction LED Driver With Three Independent Channels**
- **Integrated High Efficiency 1x / 1.5x Charge Pump With Automatic or Manual Gain Change**
- **3 x 25.5-mA Total Output Current**
- **3 x 25.5-mA Total Output Current**
- **Three Independent Program Execution Engines (3 x 16 Instructions)**
- **8-Bit PWM With Exponential Control Option**
- **8-Bit Current DAC Control**
- **200-nA Typical Shutdown Current**
- **Automatic Power-Save Mode**
- **Autonomous Operation Without External Control**
- **Trigger I/O for Synchronizing Multiple Devices**
- **One or Two General Purpose Output Controlled Via Serial Interface**
- **$I^2C$ Interface**
- **Operating Temperature Range: -30ºC to 85ºC**

## APPLICATIONS

- **LED Control for Portable Applications**
- **Accent Lighting (Mood, Personalization, etc.)**
- **Function Indication (Charge, Messages, etc.)**
- **Keypad Illumination / Backlight (White or RGB)**
- **Display Backlight**

## DESCRIPTION

The TPS68401/TPS68402 is an advanced lighting management unit for handheld devices. It has three independent channels optimized for driving RGB LEDs. The built-in fractional charge pump boosts the input voltage to power the LEDs at low input voltage. Channel one can optionally be supplied directly from the battery voltage to reduce power consumption and improve efficiency.

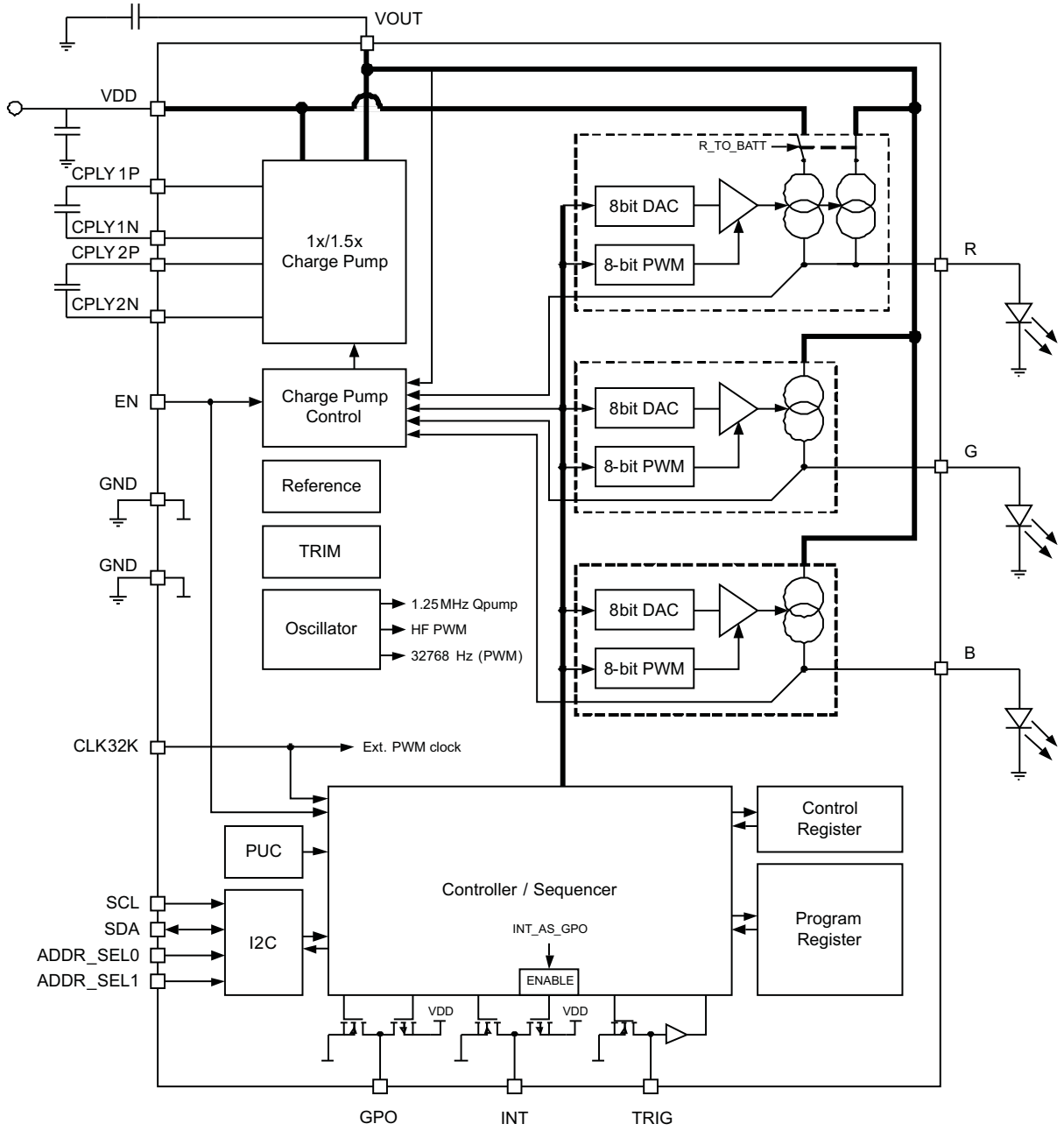
At the heart of the device is a programmable state machine which executes a lighting program consisting of up to 16 instructions per channel. Once the program is loaded through the $I^2C$ interface the device is fully independent from the main processor resulting in significant system-level power savings. The device can issue an interrupt to the main processor via the INT pin.

The TRIG I/O allows synchronization between multiple devices. A general-purpose output pin is provided which is addressable through the serial interface. In addition, the INT pin can also be configured as general-purpose output.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## FUNCTIONAL BLOCK DIAGRAM

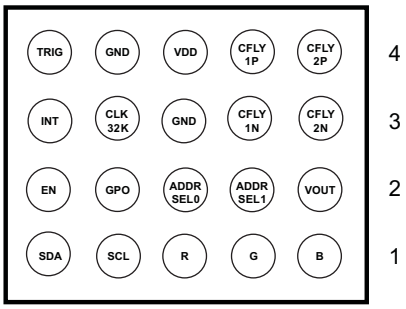


## ORDERING INFORMATION

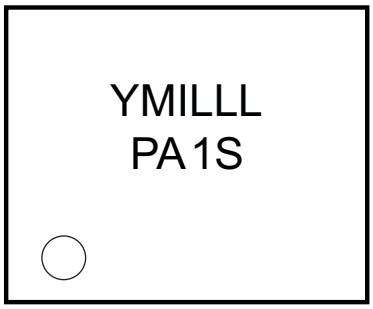
| $T_A$ | PACKAGE | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|
| -30°C to 85°C | YFF | TPS68401C4YFFR | TPS68401C4YFF |
| | RHF | TPS68402A0RHFR | 24RHF |

## TERMINAL FUNCTIONS

NanoFree YFF PACKAGE
(BOTTOM VIEW )

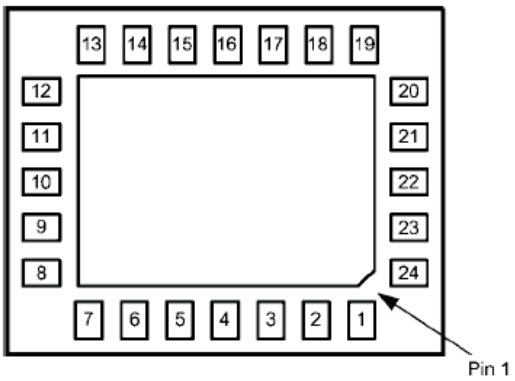



PACKAGE MARKING

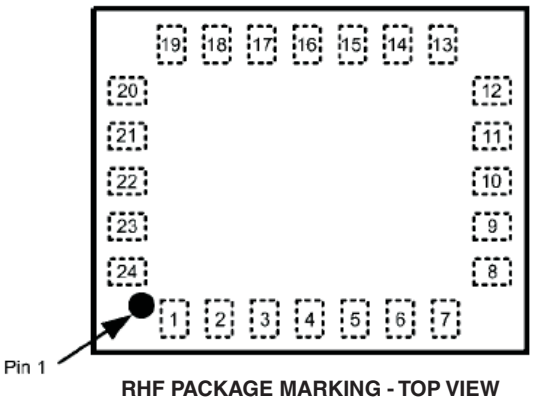



YM = YEAR / MONTH DATE CODE
LLLL = LOT TRACE CODE
S = ASSEMBLY SITE CODE
A = MAJOR DIE REVISION
1 = MINOR DIE REVISION
P = PREPRODUCTION INDICATOR
0 = Pin A1 (Filled Solid)

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| CFLY1P | 4B | | Positive terminal of charge pump fly capacitor |
| CFLY1N | 3B | | Negative terminal of charge pump fly capacitor |
| CFLY2P | 4A | | Positive terminal of charge pump fly capacitor |
| CFLY2N | 3A | | Negative terminal of charge pump fly capacitor |
| VDD | 4C | | Power pin |
| GND | 4D | | Ground |
| VOUT | 2A | | Charge pump output |
| R | 1C | O | Current source output, Channel 1 (Red) |
| G | 1B | O | Current source output, Channel 2 (Green) |
| B | 1A | O | Current source output, Channel 3 (Blue) |
| SCL | 1D | I | $I^2C$ Serial interface clock input |
| SDA | 1E | I/O | $I^2C$ Serial interface data input/output (open drain) |
| CLK32K | 3D | I | 32.768-kHz clock input – If no clock present on power-up or after RESET, uses internal oscillator |
| EN | 2E | I | Chip enable (active high) |
| ADDR_SEL0 | 2C | I | $I^2C$ address select input |
| ADDR_SEL1 | 2B | I | $I^2C$ address select input |
| INT | 3E | O | Interrupt output (open drain, active low); Can be configured as push-pull GPO |
| TRIG | 4E | I/O | Trigger input / output (open drain, active low) |
| GPO | 2D | O | General purpose output |
| GND | 3C | | Ground |




RHF PACKAGE - BOTTOM VIEW




RHF PACKAGE MARKING - TOP VIEW

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| CFLY2P | 1 | | Positive terminal of charge pump fly capacitor |
| CFLY1P | 2 | | Positive terminal of charge pump fly capacitor |
| VDD | 3 | | Power pin |
| GND | 4 | | Ground |
| CLK32K | 5 | I | 32.768-kHz clock input. If no clock present on power-up or after RESET, uses internal oscillator. |
| INT | 6 | O | Interrupt output (open drain, active low); Can be configured as push-pull GPO. |
| TRIG | 7 | I/O | Trigger input/output (open drain, active low) |
| N/C | 8 | | Not connected |
| N/C | 9 | | Not connected |
| N/C | 10 | | Not connected |
| N/C | 11 | | Not connected |
| N/C | 12 | | Not connected |
| SDA | 13 | I/O | $I^2C$ Serial interface data input/output (open drain) |
| EN | 14 | I | Chip enable (active high) |
| SCL | 15 | I | $I^2C$ Serial interface clock input |
| GPO | 16 | O | General purpose output. |
| R | 17 | O | Current source output, Channel 1 (Red) |
| G | 18 | O | Current source output, Channel 2 (Green) |
| B | 19 | O | Current source output, Channel 3 (Blue) |
| ADDR_SEL0 | 20 | I | $I^2C$ address select input |
| ADDR_SEL1 | 21 | I | $I^2C$ address select input |
| VOUT | 22 | | Charge pump output |
| CFLY2N | 23 | | Negative terminal of charge pump fly capacitor |
| CFLY1N | 24 | | Negative terminal of charge pump fly capacitor |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)(2)

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{OUT}$ | $V_{DD}$ (unregulated input battery voltage) | | -0.3 to 6 | V |
| | Input/Output voltage range (with respect to PGND) | INT, GPO, R, G, B, CFLY1N, CFLY1P, CFLY2N, CFLY2P, ADDR_SEL0, ADDR_SEL1 | -0.3 to VDD+0.3 (6.0 max) | V |
| | | SDA, SCL, EN, TRIG, CLK32K | | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | | 100 | °C/W |
| $P_D$ | Continuous power dissipation | | Internally limited | W |
| $T_J$ | Operating junction temperature | | -30 to 125 | °C |
| $T_{stg}$ | Storage temperature | | -65 to 150 | °C |
| | ESD rating | (HBM) Human body model | ±2000 | V |
| | | (CDM) Charged device model | ±100 | |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Unregulated input battery voltage | 2.7 | 3.6 | 5.5 | V |
| INT, GPO, ADDR_SEL0, ADDR_SEL1 | | 0 | | 5.5 | V |
| SDA, SCL, EN, TRIG | | 0 | | 1.8 | V |
| CLK_32K | External clock frequency | 16 | 32 | 64 | kHz |
| $T_A$ | Operating ambient temperature | -30 | | 85 | °C |
| | Flying capacitor | | 0.47 | | µF |
| | Input capacitor ($V_{DD}$) | | 1 | | µF |
| | Output capacitor ($V_{OUT}$) | | 1 | | µF |
| | SCA, SDA pull-up resistor value | | 10 | | kΩ |
| | INT pull-up resistor value | | 10 | | kΩ |

## ELECTRICAL CHARACTERISTICS

$V_{BAT}$ = 3.6 V ±5%, $T_A$ = 25ºC (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| $I_{DD}$ | Shutdown current | EN = 0 | | 0.2 | 2.0 | µA |
| | Standby current | EN = 1; CHIP_EN = 0<br>Ext. 32-kHz clock not running | | 1 | 2.0 | µA |
| | | EN = 1; CHIP_EN = 0<br>Ext. 32-kHz clock running | | 1 | 2.0 | |
| | Normal mode supply current | EN = 1, CHIP_EN = 1<br>Ext. 32-kHz clock running<br>C/P, G & B channel disabled<br>R_TO_BATT = 1 (R channel enabled)<br>[CLK_DET_EN : INT_CLK_EN] = 00b<br>(clock detection disabled)<br>$I_{LED}$ = 5 mA, 50% duty cycle | | 180 | | µA |
| | | EN = 1, CHIP_EN = 1<br>C/P and LED drivers disabled<br>[CLK_DET_EN : INT_CLK_EN] = 10b<br>(automatic clock source selection)<br>PWRSAVE_EN = 0 | | 190 | | |
| | | EN = 1, CHIP_EN = 1<br>C/P in 1x mode, no load(1),<br>LED drivers disabled<br>Ext. 32-kHz clock running | | 70 | | |
| | | EN = 1, CHIP_EN = 1<br>C/P in 1.5x mode, no load(1),<br>LED drivers disabled | | 1700 | | |
| | | EN = 1, CHIP_EN = 1<br>C/P in 1x mode, no load(1),<br>LED drivers enabled<br>Ext. 32-kHz clock running | | 650 | | |
| | | EN = 1, CHIP_EN = 1<br>C/P in 1x mode, 5-mA load LED drivers enabled<br>Ext. 32-kHz clock running | | 800 | | |
| | Power save current | EN = 1, CHIP_EN = 1<br>CLK32K active | | 10 | | µA |
| | | EN = 1, CHIP_EN = 1<br>Internal oscillator running | | 190 | | |
| **STARTUP** | | | | | | |
| $t_{STARTUP}$ | Startup time | STANDBY to NORMAL mode | | 500 | 1000 | µs |
| **BOOST VOLTAGE ($V_{OUT}$)** | | | | | | |
| $V_{OUT}$ | Output voltage | 1x mode, no load(1) | | | $V_{DD}$ | V |
| | | 1.5x mode, $V_{DD}$ = 3.6 V, no load(1) | | 4.55 | | |
| $V_{HYS}$ | Automatic gain change hysteresis | C/P in automatic mode, no load(1) | | 200 | | mV |
| $I_{OUT}$ | Continuous output current | | | 150 | | mA |
| | Max output current | $V_{OUT}$ < 1V | | 150 | | |
| | | $V_{OUT}$ > 1V | 150 | 250 | | |
| $f_S$ | Switching frequency | | | 1.25 | | MHz |
| $Z_O$ | Open loop output impedance | 1x mode ($V_{DD}$ - $V_{OUT}$) / $I_{OUT}$ | | 1.1 | | Ω |
| | | 1.5x mode(2) | | 4.1 | | |
| $t_{ON}$ | Turn on time from 1x to 1.5x mode. | $V_{DD}$ = 3.6 V | | 50 | | µs |
| | Turn on time from off to 1.5x mode. | $V_{OUT}$ = 0 V | | 100 | | |

(1) No-load measurement condition is as follows: DAC setting = default (17.5 mA); PWM = 0; Output connected to ground via 150-Ω resistor.

(2) Charge pump Impedance is measured at $V_{DD}$ = 3 V, $I_{OUT}$ = 50 mA follows: [$V_{OUT}$ ($I_{OUT}$ = 0) – $V_{OUT}$ ($I_{OUT}$)] / $I_{OUT}$

## ELECTRICAL CHARACTERISTICS (continued)

$V_{BAT}$ = 3.6 V ±5%, $T_A$ = 25ºC (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INTERNAL OSCILLATOR** | | | | | | |
| $f_{OSC}$ | Internal oscillator frequency | $T_A$ = 25 ºC | -4 | | 4 | % |
| | | -30 ºC ≤ $T_A$ ≤ 85 ºC | -7 | | 7 | |
| **OUTPUT CHANNELS (R,G,B)** | | | | | | |
| $V_{LED}$ | LED forward voltage | | 1.5 | | | |
| $V_{DRP}$ | Driver saturation voltage | $I_{R,G,B}$ = 17.5 mA(3) | | 50 | 100 | mV |
| $I_{R,G,B}$ | LED current | Per channel | 0 | | 25.5 | mA |
| | LED current resolution | | | 8 | | Bit |
| | LED current accuracy | $I_{R,G,B}$ = 17.5 mA | -4 | | 4 | % |
| | LED current matching | $I_{R,G,B}$ = 17.5 mA, $V_f$ = 3.0 V | | 1 | 2 | % |
| $f_{PWM}$ | PWM frequency | PWM_HF = 1<br>Internal high frequency oscillator | | 558 | | Hz |
| | | PWM_HF = 0<br>Internal clock or CLK_32K | | 256 | | |
| $I_{LEAK}$ | Pin leakage current | $T_A$ = 25 ºC | | 0.1 | | µA |
| | | -30 ºC ≤ $T_A$ ≤ 85 ºC | | | 1 | |
| $PWM_{RES}$ | PWM resolution | | 8 | | | Bit |
| **LOGIC INPUT LEVELS (EN)** | | | | | | |
| $V_{IL}$ | Input low level | | | | 0.5 | V |
| $V_{IH}$ | Input high level | | 1.2 | | | V |
| $I_{IH}$, $I_{IL}$ | Input bias current | $V_{EN}$ = 0 V to 1.65 V | -1 | | 1 | µA |
| $t_{delay}$ | Input delay | EN pin low to high | | 2 | | µs |
| **LOGIC INPUT LEVELS (SCL, SDA, TRIG, CLK_32K)** | | | | | | |
| $V_{IL}$ | Input low level | $V_{EN}$ = 1.65 V to 3.6 V | | | 0.2 x $V_{EN}$ | V |
| $V_{IH}$ | Input high level | $V_{EN}$ = 1.65V to 3.6 V | 0.8 x $V_{EN}$ | | | V |
| $I_{IH}$, $I_{IL}$ | Input bias current | | -1.0 | | 1.0 | µA |
| $f_{SCL}$ | $I^2C$ clock frequency | | | | 400 | kHz |
| **LOGIC INPUT LEVELS (ADD_SEL0, ADD_SEL1)** | | | | | | |
| $V_{IL}$ | Input low level | | | | 0.2 x $V_{DD}$ | V |
| $V_{IH}$ | Input high level | | 0.8 x $V_{DD}$ | | | V |
| $I_{IH}$, $I_{IL}$ | Input bias current | VADD_SEL0, ADD_SEL1 = 3.6 V | -1.0 | | 1.0 | µA |
| **LOGIC OUTPUT LEVELS (SDA, TRIG, INT pin as INT)** | | | | | | |
| $V_{OL}$ | Output low level | $I_{OUT}$ = 3 mA through pull-up | | 0.3 | 0.5 | V |
| $I_{IL}$ | Output leakage current | INT pin as INT (open drain), INT = high, $V_{INT}$ = 0 V to 1.65 V | | | 1.0 | µA |
| **LOGIC OUTPUT LEVELS (GPO, INT pin as GPO)** | | | | | | |
| $V_{OL}$ | Output low level | $I_{OUT}$ = 3 mA | | 0.3 | 0.5 | V |
| $V_{OH}$ | Output high level | $I_{OUT}$ = -2 mA | $V_{DD}$ - 0.5 | $V_{DD}$ - 0.3 | | V |

(3) $I_{OUT}$ at $V_{DRP}$ = 0.9 x $I_{OUT}$ at ($V_{DD}$ - $V_{LED}$) = 1 V

## DESCRIPTION OF CHARGE PUMP OPERATION

The TPS68401/TPS68402 includes a regulated fractional charge pump with bypass mode. It is used to boost the supply voltage for the output drivers when the battery voltage is close to or below the forward bias voltage of the LEDs. In 1.5x mode $V_{OUT}$ is boosted to 1.5x $V_{DD}$ or 4.55 V, whichever value is lower. In 1x (bypass) mode the output is connected directly to the input supply.

The charge pump is controlled with two CP_MODE bits in the CONFIG register. When disabled, $V_{OUT}$ is connected to ground through a 300-kΩ resistive path. The user can manually select 1x and 1.5x mode or select automatic mode. When automatic mode is enabled, the charge pump will operate in bypass mode as long as the input supply voltage is sufficient to drive the LEDs. Dropout voltage of all three channels is monitored and charge pump gain is set to 1.5x if any one driver does not have enough headroom to drive the LED. When the part enters Power Save mode the output capacitor is connected to the input supply through a resistive path. See Power Save mode description for details.

The mode selection logic utilizes digital filtering to prevent glitches of the supply voltage from triggering gain changes. If R-driver current source is connected to battery (CONFIG register, bit R_TO_BATT set to 1) voltage monitoring is disabled in R output, but still functional in G and B output.

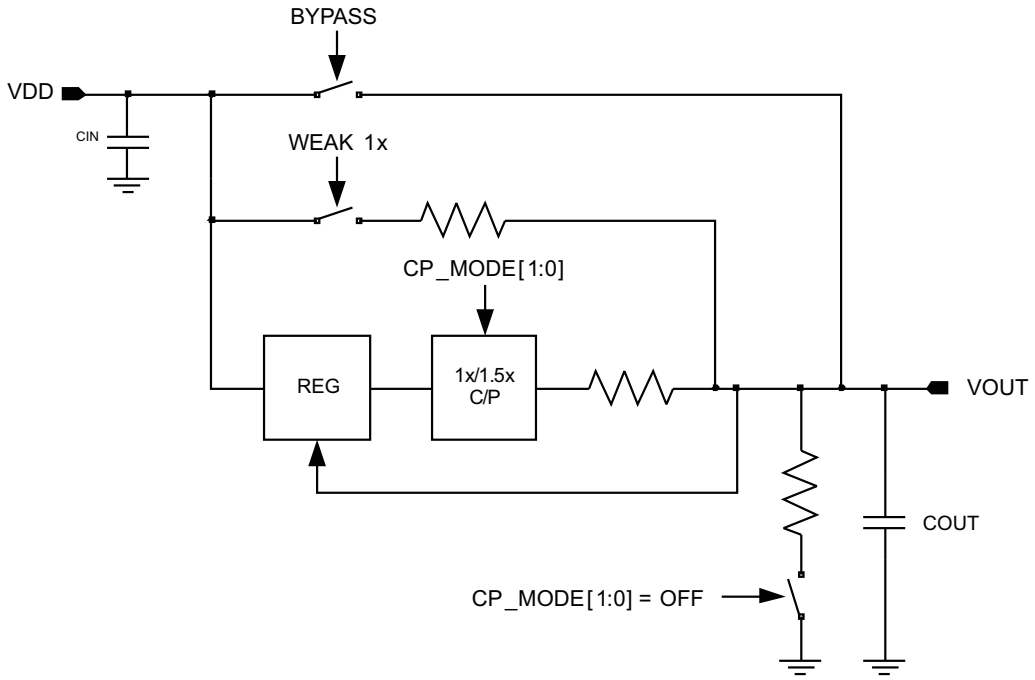



**Figure 1. Functional Model of Charge Pump**

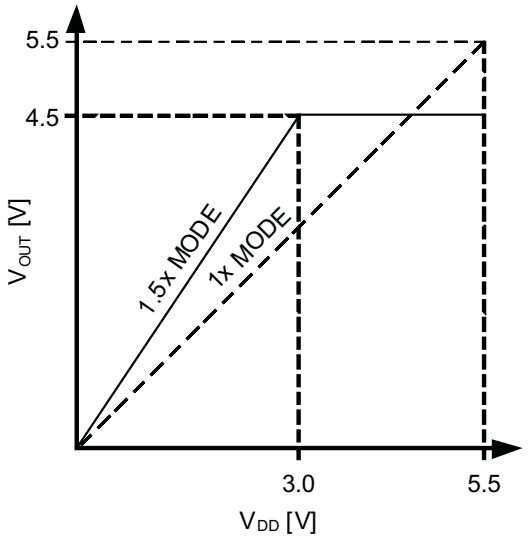



**Figure 2. Charge Pump Output Voltage**

## LED DRIVER OPERATIONAL DESCRIPTION

The TPS68401/TPS68402 has three independent constant current LED drivers with 8-bit PWM control. Output current is programmed through the $I^2C$ register and ranges from 0 mA to 25.5 mA with 8-bit resolution. PWM duty cycle is controlled either by program instructions or R/G/B PWM registers. Green and blue channels are always connected to the charge pump output $V_{OUT}$. The red channel is connected to either $V_{OUT}$ or $V_{DD}$ depending on R_TO_BAT bit setting of the CONFIG register. If red channel is connected to $V_{DD}$, automatic charge pump gain control is not used for this output. Connecting the red channel to $V_{DD}$ provides better efficiency when driving LEDs with low VF or the supply voltage is high enough to drive a LED with high VF.

PWM frequency is either 256 Hz or 558 Hz and is selected through PWM_HF bit in the CONFIG register. Linear and logarithmic PWM duty-cycle-to-input response is selectable through the LOG_EN bit of the ENABLE register. LOG_EN bit controls PWM response for all three channels. Logarithmic response is approximated by piece-wise-linear function as shown below.

When the external clock source is selected for driving the PWM, PWM frequency scales with the external clock frequency. Nominal 256-Hz PWM frequency requires external clock frequency of 32.768 kHz.

## PWM CONTROL

**Table 1. PWM Value and Output in LIN and EXP Mode**

| PWM REGISTER VALUE | PWM OUTPUT | | PWM REGISTER VALUE | PWM OUTPUT | |
|---|---|---|---|---|---|
| | LIN | EXP | | LIN | EXP |
| 0 | 0 | 0 | 128 | 128 | 64 |
| 1 | 1 | 0 | 129 | 129 | 65 |
| 2 | 2 | 1 | 130 | 130 | 66 |
| 3 | 3 | 1 | 131 | 131 | 67 |
| 4 | 4 | 2 | 132 | 132 | 68 |
| 5 | 5 | 2 | 133 | 133 | 69 |
| ... | ... | ... | ... | ... | ... |
| 61 | 61 | 30 | 189 | 189 | 125 |
| 62 | 62 | 31 | 190 | 190 | 126 |
| 63 | 63 | 31 | 191 | 191 | 127 |
| 64 | 64 | 32 | 192 | 192 | 129 |
| 65 | 65 | 32 | 193 | 193 | 131 |
| 66 | 66 | 33 | 194 | 194 | 133 |
| ... | ... | ... | ... | ... | ... |
| 125 | 125 | 62 | 253 | 253 | 251 |
| 126 | 126 | 63 | 254 | 254 | 253 |
| 127 | 127 | 63 | 255 | 255 | 255 |

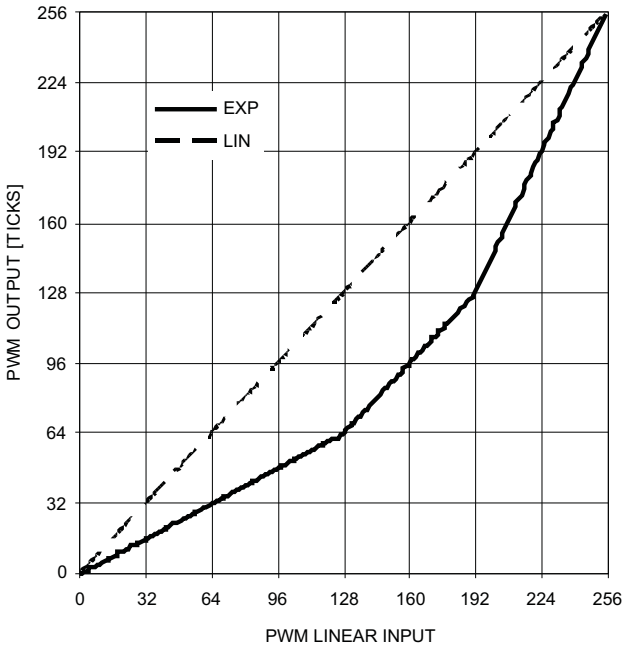



**Figure 3. Graph of PWM Output vs. PWM Input**

**Table 2. LED Channel Output Current Control**

| REGISTER | BITS | VALUE | CHANNEL CURRENT |
|---|---|---|---|
| R_CURRENT, G_CURRENT, B_CURRENT | 7:0 | 0x00 | 0.0 mA |
| | | 0x01 | 0.1 mA |
| | | ↕ | ↕ |
| | | 0xAE | 17.4 mA |
| | | 0xAF | 17.5 mA |
| | | 0xB0 | 17.6 mA |
| | | ↕ | ↕ |
| | | 0xFE | 25.4 mA |
| | | 0xFF | 25.5 mA |

## DATA TRANSMISSION

TPS68401/TPS68402 features an $I^2C$ slave interface for communication to a controlling microprocessor. SDA, SCL, CLK_32K and TRIG pins input levels are defined by EN pin. EN pin is used as voltage reference for logic inputs and therefore no dedicated VIO pin is required.

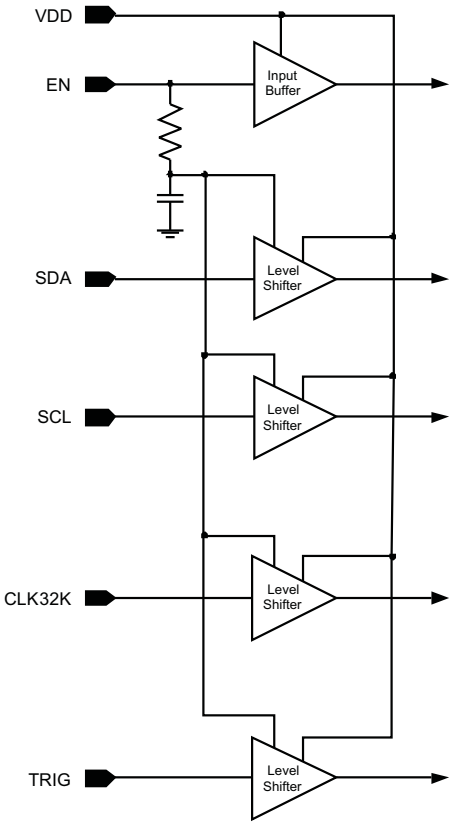



**Figure 4. Internal Logic Level Shifters**

## SUBADDRESS DEFINITION

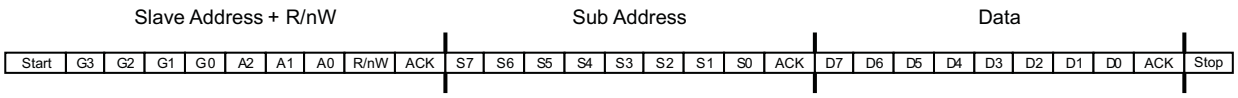



**Figure 5. Subaddress in I²C Transmission**

Start – Start Condition

G(3:0) – Group ID: Address fixed at 0110b

A(2:0) – Device address: Device address is selectable via ADDR_SEL input pin.

R/nW – Read / not Write select bit

ACK – Acknowledge

S(7:0) – Subaddress: defined per register map

D(7:0) – Data; Data to be loaded into the device

Stop – Stop condition

**Table 3. Subaddress Bits Defined by ADDR_SEL Inputs**

| ADDR_SEL [1:0] | A [2:0] |
|---|---|
| 00 | 010 |
| 01 | 011 |
| 10 | 100 |
| 11 | 101 |

The address bits used in the slave address portion of the I²C transaction are defined by the device pins ADDR_SEL1 and ADDR_SEL0 (combined as ADDR_SEL [1:0] above). The table above gives the values of the address bits for all combinations of ADDR_SEL1 and ADDR_SEL0.

## I²C BUS OPERATION

The I²C bus is a communications link between a controller and a series of slave terminals. The link is established using a two-wired bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data line is bi-directional for data communication between the controller and the slave terminals. Each device has an open drain output to transmit data on the serial data line. An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission.

Data transmission is initiated with a start bit from the controller as shown in Figure 6. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device will receive serial data on the SDA input and check for valid address and control information. If the appropriate group and address bits are set for the device, then the device will issue an acknowledge pulse and prepare the receive subaddress data. Subaddress data is decoded and responded to as per the Register Map section of this document. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge is issued after the reception of valid address, sub-address and data words. The I²C interface will auto-sequence through register addresses, so that multiple data words can be sent for a given I²C transmission.

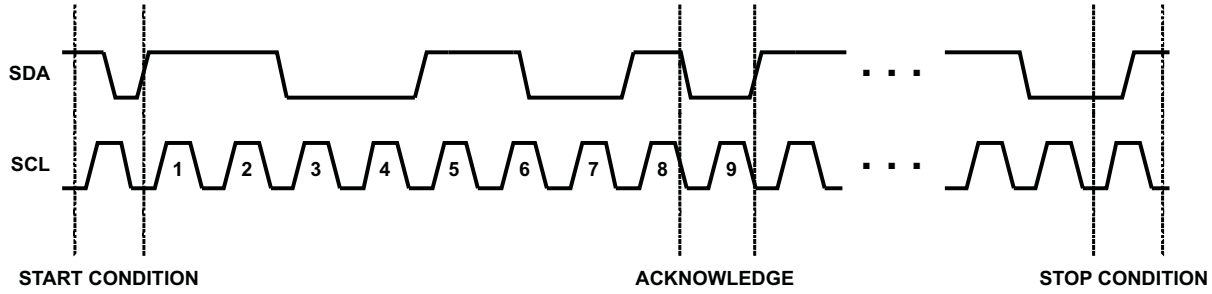



**Figure 6. I²C Start / Stop / Acknowledge Protocol**

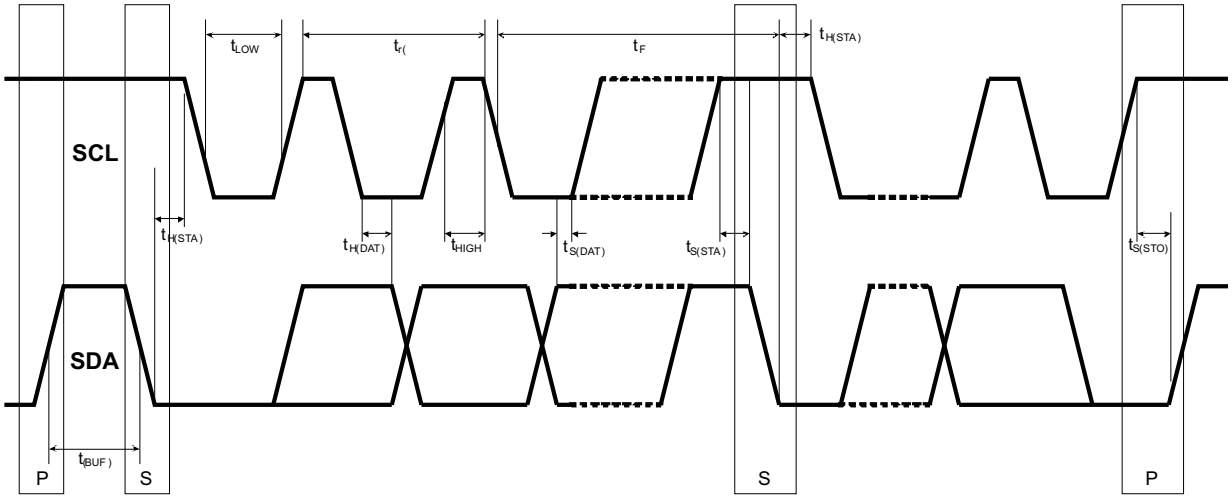



**Figure 7. I²C Data Transmission Timing**

## DATA TRANSMISSION TIMING

$V_{BAT}$ = 3.6 ±5%, $T_A$ = 25 ºC, $C_L$ = 100 pF (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{(SCL)}$ | Serial clock frequency | | | | 100 | KHz |
| | | | | | 400 | |
| $t_{(BUF)}$ | Bus free time between stop and start condition | SCL = 100 kHz | 4.7 | | | µs |
| | | SCL = 400 kHz | 1.3 | | | |
| $t_{(SP)}$ | Tolerable spike width on bus | SCL = 100 kHz | | | 50 | ns |
| | | SCL = 400 kHz | | | | |
| $t_{LOW}$ | SCL low time | SCL = 100 kHz | 4.7 | | | µs |
| | | SCL = 400 kHz | 1.3 | | | |
| $t_{HIGH}$ | SCL high time | SCL = 100 kHz | 4 | | | µs |
| | | SCL = 400 kHz | 0.6 | | | |
| $t_{S(DAT)}$ | SDA → SCL setup time | SCL = 100 kHz | 250 | | | ns |
| | | SCL = 400 kHz | 100 | | | |
| $t_{S(STA)}$ | Start condition setup time | SCL = 100 kHz | 4.7 | | | µs |
| | | SCL = 400 kHz | 0.6 | | | |
| $t_{S(STO)}$ | Stop condition setup time | SCL = 100 kHz | 4 | | | µs |
| | | SCL = 400 kHz | 0.6 | | | |
| $t_{H(DAT)}$ | SDA → SCL hold time | SCL = 100 kHz | 0 | | 3.45 | µs |
| | | SCL = 400 kHz | 0 | | 0.9 | |
| $t_{H(STA)}$ | Start condition hold time | SCL = 100 kHz | 4 | | | µs |
| | | SCL = 400 kHz | 0.6 | | | |
| $t_{r(SCL)}$ | Rise time of SCL Signal | SCL = 100 kHz | | | 1000 | ns |
| | | SCL = 400 kHz | | | 300 | |
| $t_{f(SCL)}$ | Fall time of SCL Signal | SCL = 100 kHz | | | 300 | ns |
| | | SCL = 400 kHz | | | 300 | |
| $t_{r(SDA)}$ | Rise time of SDA Signal | SCL = 100 kHz | | | 1000 | ns |
| | | SCL = 400 kHz | | | 300 | |
| $t_{f(SDA)}$ | Fall time of SDA Signal | SCL = 100 KHz | | | 300 | ns |
| | | SCL = 400 kHz | | | 300 | |

## FUNCTIONAL DESCRIPTION OF DEVICE PINS

### ADDR_SEL0 AND ADDR_SEL1 PINS

ADDR_SEL0 and ADDR_SEL1 pins define the chip $I^2C$ address. Pins are referenced to $V_{DD}$ signal level. See Data Transmission section for $I^2C$ address definitions.

### GENERAL PURPOSE OUTPUT PIN

The TPS68401/TPS68402 has one dedicated general purpose output pin (GPO) with digital CMOS output. High-level output voltage is defined by $V_{DD}$ and no pull-up resistor is needed. GPO output is controlled by GPO bit of the GPO register.

### INT PIN

The INT pin is used to issue an interrupt to a host processor when END instruction is executed and the INT bit is set (see Instruction Description section for details). The INT pin can also be configured as a GPO pin by setting the INT_AS_GPO bit of the GPO register. When configured as INT pin it has an open drain output and requires an external pull-up resistor. As GPO pin it has a digital CMOS output, high-level output voltage is defined by $V_{DD}$, and no pull-up resistor is needed. In GPO mode the output is controlled by the INT bit of the GPO register.

### TRIG PIN

TRIG pin is used to send and receive trigger pulses between multiple TPS68401/TPS68402 devices for pattern synchronization. TRIG is an open drain output and requires an external pull-up resistor. External trigger input signal must be at least two 32-kHz clock cycles long to be recognized. Trigger output signal is three 32-kHz clock cycles long. If TRIG pin is not used on application, it should be connected to GND.

### CLK_32K PIN

CLK_32K pin is used for connecting external 32.768-kHz clock to TPS68401/TPS68402. Connecting several devices to the same clock source ensures synchronous instruction execution. When external clock source is used the internal oscillator is shut down during automatic power save mode to achieve lowest possible current consumption. An external clock source is not required for device operation. If external clock is not used, CLK_32K pin should be connected to GND.

### CLK_32K EXTERNAL CLOCK DETECTION

The instruction execution engine and PWM are clocked either by an internal 32.768-kHz or an external clock. The user can manually select internal or external clock or enable automatic clock source selection. In automatic mode the TPS68401/TPS68402 monitors the CLK32K pin; If external clock frequency is < 15 kHz, stuck-at-zero, or stuck-at-one, the clock detector indicates that no external clock is present and switches to internal clock source. It switches back to external clock source once the external clock is detected again. In any mode (manual or automatic selection) the clock source can be checked by reading the EXT_CLK_USED bit of the STATUS register. Clock source selection is controlled by CONFIG register bits INT_CLK_EN and CLK_DET_EN. External clock detection is disabled in POWER SAVE mode.

When external clock source is selected, instruction timing and PWM frequency scale with the external clock frequency. Nominal external clock frequency is 32.768 kHz.

## MODES OF OPERATION

### RESET

In the RESET mode all the internal registers are reset to the default values. Reset is initiated if 0xFFh is written into the RESET register or internal power-up clear (PUC) is activated. PUC will activate when supply voltage is connected to $V_{DD}$ pin or when the supply voltage drops below the nPUC_VIL level. Once $V_{DD}$ rises above nPUC_VIH, PUC is released and the chip will continue to the STANDBY mode. CHIP_EN control bit is low after PUC by default.

### SHUTDOWN

Whenever the EN pin is pulled low the device enters SHUTDOWN mode. All functions are disabled, including the serial interface. This is the lowest power mode.

### STANDBY

STANDBY mode is entered if the CHIP_EN bit of the ENABLE register is set to 0 and reset is not active. Registers can be written to in this mode with the exception of the EXEC bits of the ENABLE register (R_EXEC[1:0], G_EXEC[1:0], B_EXEC[1:0]). Control bits are effective after start up.

### STARTUP

When CHIP_EN bit of the ENABLE register is written 1 and EN pin is high, the chip executes the internal startup sequence to power up analog blocks ($V_{REF}$, bias, oscillator etc.). If the chip temperature rises too high, the over temperature shutdown (OTS) disables the chip and automatically re-enters STARTUP mode, until no thermal shutdown event is present.

### NORMAL

During NORMAL mode the user controls the chip using the control registers. If EN pin is set low, the CHIP_EN bit is reset to 0.

## POWER SAVE

In POWER SAVE mode analog blocks are disabled to minimize power consumption. See the Power Save Mode section for further information.

## MODE TRANSITIONS

Setting the CHIP_EN bit of the ENABLE register to 0 resets the program counters (PC) but does not change the LED controller operational mode (see NORMAL MODE settings). Pulling the EN pin low resets the CHIP_EN bit and PC but does not affect operational mode (see NORMAL MODE settings).

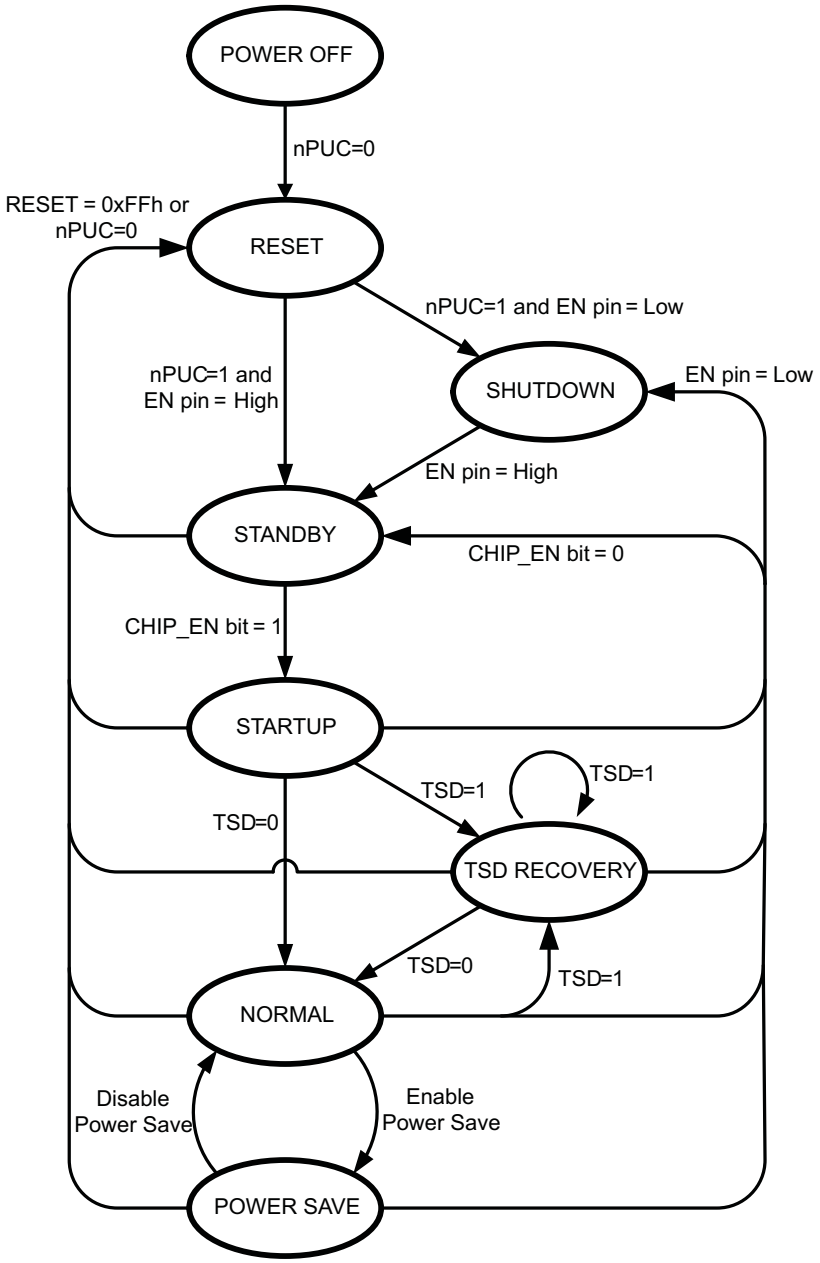



**Figure 8. Device Startup Flow and Modes of Operation**

## POWER SAVE MODE

Automatic power save mode is enabled when PWRSAVE_EN bit in the CONFIG register is set to 1. In power save mode all analog blocks are powered down with exception of charge pump protection circuits, provided external clock source is used to run the PWM. If internal clock source has been selected, only charge pump and LED drivers are disabled and the digital part of the LED controller remains active. In both cases charge pump enters a special 1x mode to keep the output at battery level. During program execution the device can enter power save if there is no PWM activity in R, G and B outputs for > 50ms. To prevent the device from entering power-save mode for short periods of time the device does a command look-ahead. In every instruction cycle R, G, B commands are analyzed, and if there is sufficient time left with no PWM activity, device will enter power save mode. In power save mode program execution continues uninterruptedly. When a command that requires PWM activity is executed, the device starts up automatically. The following table describes commands and conditions that can activate power save mode. All channels (R, G, and B) need to meet power save condition in order to enable power save.

POWER SAVE MODE can only be entered when no channel is in the LOAD MODE, all PWM values are zero or channel is disabled, and C/P mode is either OFF or Automatic.

**Table 4. Requirements for Power Save By Command**

| COMMAND | POWER SAVE REQUIREMENT |
|---|---|
| WAIT | Enter power save only if PWM is zero and wait is greater then 50 ms. |
| RAMP | Enter power save only if ramp ends with PWM set to zero and there is 50 ms before the next command. |
| TRIGGER | Enter power save only if PWM is zero while waiting for trigger. |
| END | Enter power save only if PWM is zero or reset bit of command is set to 1. |
| SET | Enter power save only if PWM is set to zero and the next command generates at least a 50-ms wait. |
| Other | Cannot enter power save mode |

## LED CONTROLLER OPERATIONAL MODES (NORMAL MODE)

In NORMAL MODE, operation of the red, green, and blue LED controller is defined independently by the OP_MODE, and respective R/G/B_PC, R/G/B_PWM, and R/G/B_CURRENT registers. The R/G/B CURRENT registers define the maximum output current for the respective channel. MODE control bits are synchronized to a 32-kHz clock.

In the following, PC denotes either R_PC, G_PC, or B_PC program counter. MODE denotes either R_MODE, G_MODE, or B_MODE bits of the OP_MODE register.

### DISABLED MODE

LED output current is set to 0 and PC counter is reset.

### LOAD MODE

The device can store 16 16-bit commands for each channel (R, G, B). Due to the 8-bit format of the $I^2C$ protocol two writes are required to load a single instruction. The device supports auto-increment addressing to reduce program load time. Register address is incremented after each 8 data bits which allows the whole program memory to be written in a single $I^2C$ write sequence. Program memory is defined in the register table. Read / write access to program memory is allowed only in LOAD mode and only to the channel in LOAD mode. LOAD mode resets respective channel's PC. Program execution on all other channels is halted and PWM value remains static while at least one channel is in LOAD mode. Program execution continues when all channels are out of LOAD program mode.

### RUN MODE

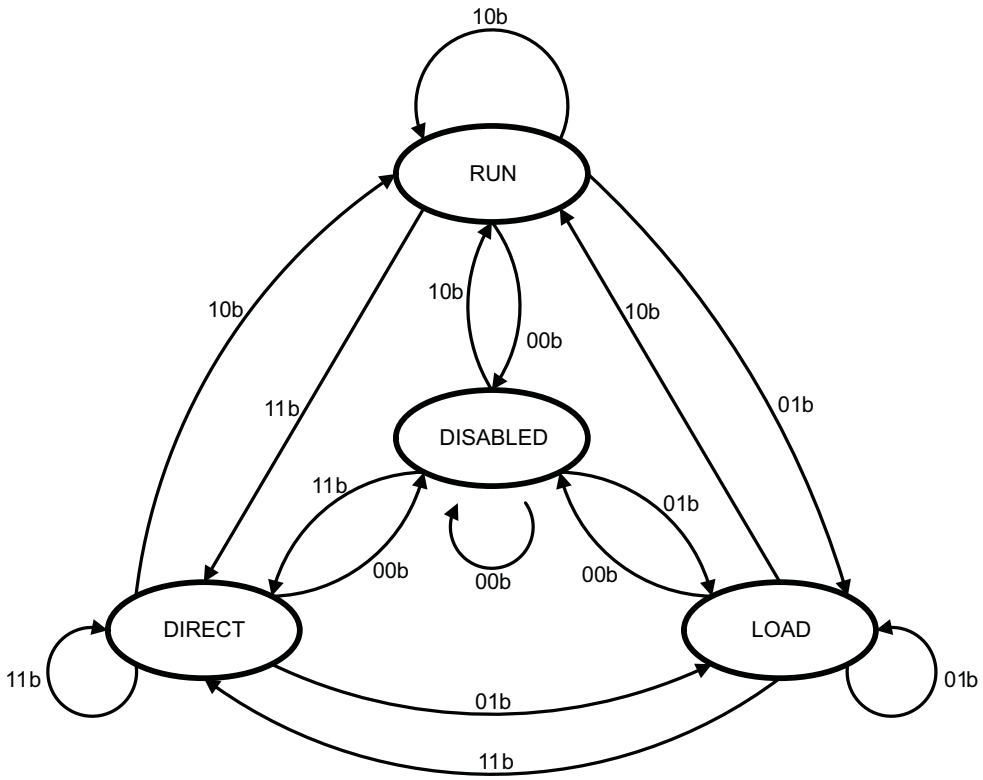
In RUN mode the LED controller executes instructions stored in program memory. Execution is controlled by the R, G, and B program counters (R_PC, G_PC, B_PC) and the ENABLE register. For details refer to RUN MODE OPTIONS section. Program start position can be determined by writing to the PC registers. If program counter runs to end (15) the next command will be executed from program location 0. If internal PWM clock source is selected in RUN mode, the LED controller must be disabled (MODE = 00b) before disabling the chip (with CHIP_EN bit or EN pin) to ensure that the sequence starts from the correct program counter (PC) value when restarting the sequence. PC registers are synchronized to a 32-kHz clock.

### DIRECT MODE

In DIRECT mode the LED channels can be controlled independently through the $I^2C$ interface. For each channel there is a PWM control register (R_PWM, G_PWM, B_PWM) which contains the PWM duty cycle. If the charge pump is set to automatic 1x / 1.5x mode selection, PWM values need to be written 0 before disabling the drivers (MODE = 00b) to ensure proper automatic gain change operation.

### MODE TRANSITIONS

A transition between operational modes aborts the instruction being executed (if any), resets the PC and sets the PWM duty cycle to 0. The channel current setting is not affected.




NORMAL MODE

Bit settings refer to the R/G/B_MODE[1:0] bits of the OP_MODE register.

**Figure 9. Operational Modes of LED Controller in NORMAL Mode of Operation**

## RUN MODE SETTINGS

Run mode is set independently for each channel in the ENABLE register. In the following PC denotes either R_PC, G_PC, or B_PC program counter. EXEC denotes either R_EXEC, G_EXEC, or B_EXEC bits of the ENABLE register.

### HOLD

Wait until current command is finished then stop while EXEC[1:0] = 00b (Hold). PC can be read or written only in this mode.

### STEP

Execute instruction defined by PC, increment PC and change EXEC[1:0] to 00b (Hold).

### CONTINUE

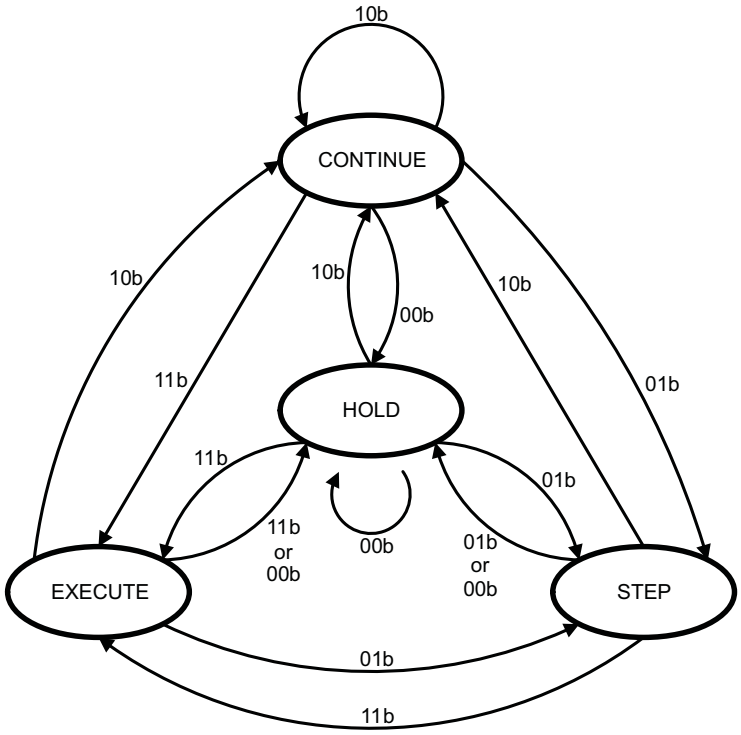
Start program execution at PC value, increment PC and continue.

### EXECUTE

Execute instruction defined by PC, do not update PC, change EXEC[1:0] to 00b (Hold).

### MODE TRANSITIONS

A transition between run modes does not abort the instruction being executed. PC is updated before mode transition. Note that PC is also incremented when transitioning out of EXECUTE mode.




RUN MODE

Bit settings refer to the R/G/B_EXEC[1:0] bits of the ENABLE register.

**Figure 10. Run Mode State Diagram**

## INSTRUCTION DESCRIPTION

The three channels are independent, except for the trigger connections between the channels. The following table describes the binary format used. In this implementation, there are 16 program steps available per channel.

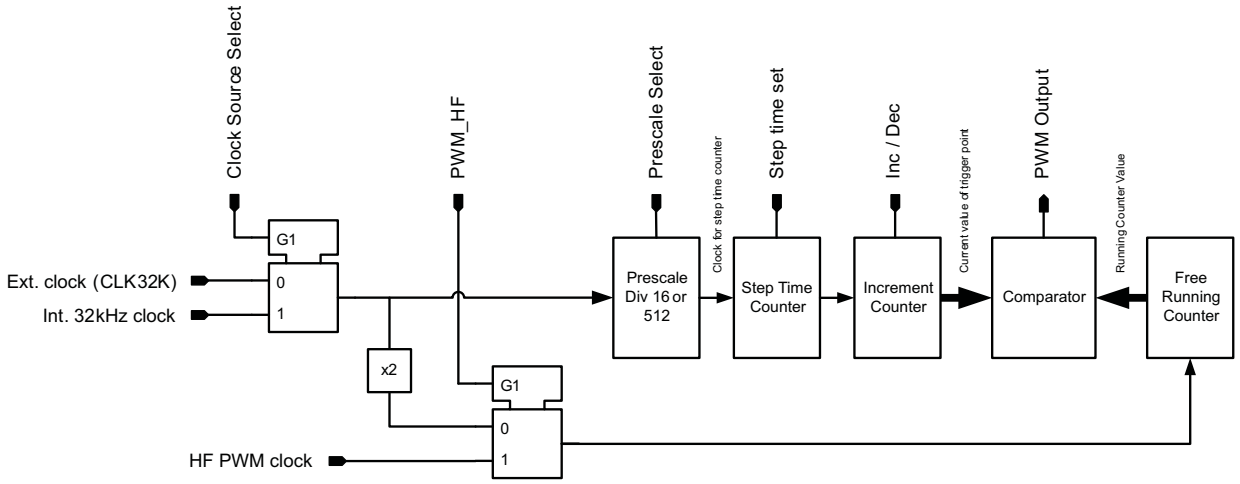



**Figure 11. Simplified Block Diagram of PWM**

## RAMP / WAIT

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| | prescale<br>0 = 16<br>1 = 512 | step time<br>1 to 63 | | | | | | sign<br>0= INC<br>1= DEC | number of steps<br>0 to 127 | | | | | | |

The ramp command generates a PWM ramp starting from the current value. At each ramp step the PWM value is incremented or decremented by one. Time for one step is defined by prescale and step time bits. The number of increments executed by the instruction is defined by number of steps which has a maximum value of 127 or half of full scale. If, during a ramp command, PWM reaches minimum / maximum (0 / 255), the ramp command will continue for the remaining number of steps without changing the PWM value (PWM value saturates). This enables the ramp command to be used as combined ramp and wait command in single instruction.

Ramp command can be used as a single step time wait instruction when increment is zero.

## SET PWM

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | x | x | x | x | x | x | x | x |
| | | | | | | | | PWM value | | | | | | | |

Set PWM output value from 0 to 255 in a single instruction.

## BRANCH

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | x | x | x | x | x | x | x | x | x | x | x | x | x |
| | | | loop count<br>0 to 63 (0 = loop forever) | | | | | | not used | | | step number | | | |

Loop instruction. Code between (step number) and BRANCH command will be executed (loop count + 1) times. Set (loop count) = 0 for infinite looping. Nested looping is supported. The number of nested loops is not limited.

## GO TO START

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Command resets program counter register and continues executing program from the 00H location.

## END

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | INT | RST | x | x | x | x | x | x | x | x | x | x | x |
| | | | interupt | reset | | | | | | | | | | | |
| | | | | 0 = Keep the current PWM value<br>1 = Set PWM value to 0 | | | | | | | | | | | |
| | | | 0 = Do not issue interrupt<br>1 = Issue interrupt and set corresponding status bit high. Interrupt is cleared by reading interrupt status register. | | | | | | | | | | | | |

Stops program execution. Set (interrupt) = 1 to issue an interrupt on the INT pin. If INT is used it must be cleared before pulling the EN pin low or writing CHIP_EN low.

## TRIGGER

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | EXT | x | x | B | G | R | EXT | x | x | B | G | R | x |
| | | | Wait for trigger<br>R=RED; G=GREEN; B=BLUE; EXT=EXTERNAL<br>1 = Wait for trigger from specified channel.<br>Own channel position is ignored.<br>0 = Continue without wait | | | | | | Issue trigger<br>R=RED; G=GREEN; B=BLUE; EXT=EXTERNAL<br>1 = Issue trigger for specified channel.<br>Own channel position is ignored.<br>0 = Continue without issuing trigger | | | | | | |

Used to synchronize channels and / or multiple units. The wait for trigger command is executed until all defined trigger have been received. An external trigger is ignored by the issuing channel / device. External trigger input signal must be at least two 32-kHz clock cycles long to be recognized. Trigger output signal is three 32-kHz clock cycles long. External trigger signal is active low, i.e. when trigger is send / received the pin is pulled to GND. Sent external trigger is masked, i.e. the device which has sent the trigger will not recognize it. If send and wait external trigger are used on the same command, the send external trigger is executed first, then the wait external trigger. Channel (R, G, or B) waiting for its own trigger is not allowed.

**Table 5. ADDRESS REGISTER MAP**

| REGISTER | ADDRESS (HEX) | NAME | DEFAULT VALUE | DESCRIPTION |
|---|---|---|---|---|
| 0 | 0 | ENABLE | 0000 0000 | Chip enable and execution control |
| 1 | 1 | OP_MODE | 0000 0000 | RGB operating mode control |
| 2 | 2 | R_PWM | 0000 0000 | Red channel PWM value |
| 3 | 3 | G_PWM | 0000 0000 | Green channel PWM value |
| 4 | 4 | B_PWM | 0000 0000 | Blue channel PWM value |
| 5 | 5 | R_CURRENT | 1010 1111 | Red channel current limit value |
| 6 | 6 | G_CURRENT | 1010 1111 | Green channel current limit value |
| 7 | 7 | B_CURRENT | 1010 1111 | Blue channel current limit value |
| 8 | 8 | CONFIG | 0000 0000 | Charge pump configuration |
| 9 | 9 | R_PC | 0000 0000 | Red channel program counter value |
| 10 | 0A | G_PC | 0000 0000 | Green channel program counter value |
| 11 | 0B | B_PC | 0000 0000 | Blue channel program counter value |
| 12 | 0C | STATUS | 0000 0000 | Clock and interrupt status |
| 13 | 0D | RESET | 0000 0000 | Device reset |
| 14 | 0E | GPO | 1000 0000 | GPO configuration and value |
| 15 | N/A | N/A | N/A | Register not implemented |
| 16 | 10 | PROG_MEM_R1_H | 0000 0000 | Red channel instruction 1 MSB |
| 17 | 11 | PROG_MEM_R1_L | 0000 0000 | Red channel instruction 1 LSB |
| ... | ... | ... | ... | ... |
| 46 | 2E | PROG_MEM_R16_H | 0000 0000 | Red channel instruction 16 MSB |
| 47 | 2F | PROG_MEM_R16_L | 0000 0000 | Red channel instruction 16 LSB |
| 48 | 30 | PROG_MEM_G1_H | 0000 0000 | Green channel instruction 1 MSB |
| 49 | 31 | PROG_MEM_G1_L | 0000 0000 | Green channel instruction 1 LSB |
| ... | ... | ... | ... | ... |
| 78 | 4E | PROG_MEM_G16_H | 0000 0000 | Green channel instruction 16 MSB |
| 79 | 4F | PROG_MEM_G16_L | 0000 0000 | Green channel instruction 16 LSB |
| 80 | 50 | PROG_MEM_B1_H | 0000 0000 | Blue channel instruction 1 MSB |
| 81 | 51 | PROG_MEM_B1_L | 0000 0000 | Blue channel instruction 1 LSB |
| ... | ... | ... | ... | ... |
| 110 | 6E | PROG_MEM_B16_H | 0000 0000 | Blue channel instruction 16 MSB |
| 111 | 6F | PROG_MEM_B16_L | 0000 0000 | Blue channel instruction 16 LSB |

## ENABLE REGISTER (ENABLE)

Address – 0x00h

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | LOG_EN | CHIP_EN | R_EXEC[1:0] | | G_EXEC[1:0] | | B_EXEC[1:0] | |
| READ/WRITE | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| LOG_EN | Enable logarithmic current adjustment mode |
| CHIP_EN | Chip enable: Forcing EN pin low resets CHIP_EN to zero. See state diagram for details. |
| R_EXEC[1:0] | Program execution control for red channel<br>00b – Hold: Finish current instruction, then stop until R_EXEC[1:0] changes.<br>01b – Step: Finish current instruction, increment R_PC and set EXEC to hold<br>10b – Continue: Execute command indicated by PC, then increment R_PC<br>11b – Execute: Execute command indicated by R_PC, then set R_EXEC[1:0] to 00b (Hold) |
| G_EXEC[1:0] | Program execution control for green channel<br>00b – Hold: Finish current instruction, then stop until G_EXEC[1:0] changes<br>01b – Step: Finish current instruction, increment R_PC and set EXEC to hold<br>10b – Continue: Execute command indicated by PC, then increment G_PC<br>11b – Execute: Execute command indicated by G_PC, then set G_EXEC[1:0] to 00b (Hold) |
| B_EXEC[1:0] | Program execution control for blue channel<br>00b – Hold: Finish current instruction, then stop until B_EXEC[1:0] changes<br>01b – Step: Finish current instruction, increment R_PC and set EXEC to hold<br>10b – Continue: Execute command indicated by PC, then increment B_PC<br>11b – Execute: Execute command indicated by B_PC, then set B_EXEC[1:0] to 00b (Hold) |

## OPERATION MODE REGISTER (OP_MODE)

Address – 0x01h

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | N/A | N/A | R_MODE[1:0] | | G_MODE[1:0] | | B_MODE[1:0] | |
| READ/WRITE | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| R_MODE[1:0] | Red channel operating mode<br>00b – Disable<br>01b – Load: Load program to instruction registers and reset R_PC<br>10b – Run: Execute commands according to R_EXEC[1:0] setting in ENABLE register<br>11b – Direct: Direct control (through R_PWM register) |
| G_MODE[1:0] | Green channel operating mode<br>00b – Disable<br>01b – Load: Load program to instruction registers and reset G_PC<br>10b – Run: Execute commands according to G_EXEC[1:0] setting in ENABLE register<br>11b – Direct: Direct control (through G_PWM register) |
| B_MODE[1:0] | Blue channel operating mode<br>00b – Disable<br>01b – Load: Load program to instruction registers and reset B_PC<br>10b – Run: Execute commands according to B_EXEC[1:0] setting in ENABLE register<br>11b – Direct: Direct control (through B_PWM register) |

## RED CHANNEL PWM CONTROL REGISTER (R_PWM)

Address – 0x02h

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | R_PWM[7:0] | | | | | | | |
| READ/WRITE | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| R_PWM[7:0] | Red channel PWM value used when R_MODE is Direct |

## GREEN CHANNEL PWM CONTROL REGISTER (G_PWM)

Address – 0x03h

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | G_PWM[7:0] | | | | | | | |
| READ/WRITE | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| G_PWM[7:0] | Green channel PWM value used when G_MODE is Direct |

## BLUE CHANNEL PWM CONTROL REGISTER (B_PWM)

Address – 0x04h

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | B_PWM[7:0] | | | | | | | |
| READ/WRITE | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| B_PWM[7:0] | Blue channel PWM value used when B_MODE is Direct |

## RED CHANNEL CURRENT CONTROL REGISTER (R_CURRENT)

Address – 0x05h

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | R_CURRENT[7:0] | | | | | | | |
| READ/WRITE | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| R_CURRENT[7:0] | Red channel current setting |
| | 0000 0000b - 0.0 mA |
| | 0000 0001b - 0.1 mA |
| | 0000 0002b - 0.2 mA |
| | ... |
| | 1010 1111b - 17.5 mA (default) |
| | ... |
| | 1111 1101b - 25.3 mA |
| | 1111 1110b - 25.4 mA |
| | 1111 1111b - 25.5 mA |

## GREEN CHANNEL CURRENT CONTROL REGISTER (G_CURRENT)

Address – 0x06h

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | G_CURRENT[7:0] | | | | | | | |
| READ/WRITE | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| G_CURRENT[7:0] | Green channel current setting |
| | 0000 0000b - 0.0 mA |
| | 0000 0001b - 0.1 mA |
| | 0000 0002b - 0.2 mA |
| | ... |
| | 1010 1111b - 17.5 mA (default) |
| | ... |
| | 1111 1101b - 25.3 mA |
| | 1111 1110b - 25.4 mA |
| | 1111 1111b - 25.5 mA |

## BLUE CHANNEL CURRENT CONTROL REGISTER (B_CURRENT)

Address – 0x07h

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | B_CURRENT[7:0] | | | | | | | |
| READ/WRITE | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| B_CURRENT[7:0] | Blue channel current setting |
| | 0000 0000b - 0.0 mA |
| | 0000 0001b - 0.1 mA |
| | 0000 0002b - 0.2 mA |
| | ... |
| | 1010 1111b - 17.5 mA (default) |
| | ... |
| | 1111 1101b - 25.3 mA |
| | 1111 1110b - 25.4 mA |
| | 1111 1111b - 25.5 mA |

## CONFIGURATION CONTROL REGISTER (CONFIG)

Address – 0x08h

| DATA BIT | D7(1) | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | N/A | PWM_HF | PWRSAVE_EN | CP_MODE[1:0] | | R_TO_BATT | CLK_DET_EN | INT_CLK_EN |
| READ/WRITE | N/A | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

(1) Bit D7 must be set to 0 at all times. Writing 1 may result in unexpected behavior.

| FIELD NAME | BIT DEFINITION |
|---|---|
| PWM_HF | Source clock for PWM blocks |
| | 0b - 256-Hz PWM frequency |
| | 1b - 558-Hz PWM frequency |

| FIELD NAME | BIT DEFINITION |
|---|---|
| PWRSAVE_EN | 0b - Power save mode disabled<br>1b – Power save mode enabled |
| CP_MODE[1:0] | Charge pump operating mode<br>00b – OFF<br>01b – Forced 1x mode<br>10b – Forced 1.5x mode<br>11b – Automatic mode selection |
| R_TO_BAT | Red channel source supply<br>0b – Red channel connected to charge pump output ($V_{OUT}$)<br>1b – Red channel connected to battery supply ($V_{DD}$) |
| [CLK_DET_EN INT_CLK_EN] | PWM clock source<br>00b - Use external clock source (CLK_32)<br>01b - Use internal clock source, clock detection disabled<br>10b - Automatically select clock source, clock detection enabled<br>11b - Use internal clock source, clock detection disabled |

## RED CHANNEL PROGRAM COUNTER REGISTER (R_PC)

Address – 0x09h

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | N/A | N/A | N/A | N/A | R_PC[3:0] (1) | | | |
| READ/WRITE | N/A | N/A | N/A | N/A | R/W | R/W | R/W | R/W |
| RESET VALUE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

(1) R_PC register can only be read or written to when R channel is in HOLD mode (R_EXEC[1:0] = 11b). In STANDBY mode R_PC can be written to but not read. Value is effective after startup. Any change of the R_MODE[1:0] bits reset the R_PC value. For read access device must be in NORMAL mode.

| FIELD NAME | BIT DEFINITION |
|---|---|
| R_PC[3:0] | Red channel program counter |

## GREEN CHANNEL PROGRAM COUNTER REGISTER (G_PC)

Address – 0x0Ah

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | N/A | N/A | N/A | N/A | G_PC[3:0] (1) | | | |
| READ/WRITE | N/A | N/A | N/A | N/A | R/W | R/W | R/W | R/W |
| RESET VALUE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

(1) G_PC register can only be read or written to when G channel is in HOLD mode (G_EXEC[1:0] = 11b). In STANDBY mode G_PC can be written to but not read. Value is effective after startup. Any change of the G_MODE[1:0] bits reset the G_PC value. For read access device must be in NORMAL mode.

| FIELD NAME | BIT DEFINITION |
|---|---|
| G_PC[3:0] | Green channel program counter |

## BLUE CHANNEL PROGRAM COUNTER REGISTER (B_PC)

Address – 0x0Bh

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | N/A | N/A | N/A | N/A | B_PC[3:0] (1) | | | |
| READ/WRITE | N/A | N/A | N/A | N/A | R/W | R/W | R/W | R/W |
| RESET VALUE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

(1) B_PC register can only be read or written to when B channel is in HOLD mode (B_EXEC[1:0] = 11b). In STANDBY mode B_PC can be written to but not read. Value is effective after startup. Any change of the B_MODE[1:0] bits reset the B_PC value. For read access device must be in NORMAL mode.

| FIELD NAME | BIT DEFINITION |
|---|---|
| B_PC[3:0] | Blue channel program counter |

## STATUS AND INTERUPT REGISTER (STATUS)

Address – 0x0Ch

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | N/A | N/A | CP_STATUS[1:0] | | EXT_CLK_USED | R_INT | G_INT | B_INT |
| READ/WRITE | N/A | N/A | R | R | R | R | R | R |
| RESET VALUE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| CP_STATUS[1:0] | Charge pump operating mode<br>00b – OFF<br>01b – Forced 1x mode<br>10b – Forced 1.5x mode<br>11b – Power save |
| EXT_CLK _USED | External clock selected<br>0b - Internal 32-Hz clock selected<br>1b - External 32-kHz clock selected |
| R_INT(1) | Red channel interrupt, set upon channel interrupt generation (END instruction), cleared on read |
| G_INT(1) | Green channel interrupt, set upon channel interrupt generation (END instruction), cleared on read |
| B_INT(1) | Blue channel interrupt, set upon channel interrupt generation (END instruction), cleared on read |

(1) Interrupt bits are cleared and INT output pin will go high-impedance (open drain output) after register read access.

## RESET CONTROL REGISTER (RESET)

Address – 0x0Dh

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | RESET[7:0] | | | | | | | |
| READ/WRITE | W | W | W | W | W | W | W | W |
| RESET VALUE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| RESET[7:0] | Forced reset state (reset all registers to default values). No $I^2C$ acknowledge will be generated when 0xFFh is written to the RESET register. $I^2C$ acknowledge will be generated for any other pattern written to the register. |

## GPO CONTROL REGISTER (GPO)

Address – 0x0Eh

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | ID | N/A | N/A | N/A | N/A | INT_AS_GPO | GPO | INT |
| READ/WRITE | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| INT_AS_GPO | INT pin GPO function enable<br>0b – INT pin functions as interrupt pin<br>1b – INT pin functions as GPO |
| GPO | GPO value<br>0b – Output low<br>1b – Output high |
| INT | INT value (when INT_AS_GPO is set to 1)<br>0b – Output low<br>1b – Output high |
| ID | ID bit |

## PROGRAM MEMORY REGISTERS (PROGRAM MEMORY R, G, B)

Address – 0x10h to 0x2F in pairs (Red)
– 0x30h to 0x4F in pairs (Green)
– 0x50h to 0x6F in pairs (Blue)

**NOTE**

Each program command is composed of two consecutive bytes in the register space. The most significant byte of the command is stored in the lower order address followed by the least significant byte.

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | CMD_Rn_H[7:0], CMD_Rn_L[7:0] | | | | | | | |
| READ/WRITE | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| CMD_Rn_H[7:0] | Red channel program command n, most significant byte; Address is 0x10h + 2n and 0 ≤ n ≤ 15. See program commands section for details. |
| CMD_Rn_L[7:0] | Red channel program command n, least significant byte; Address is 0x11h + 2n and 0 ≤ N ≤ 15. See program commands section for details. |

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | CMD_Gn_H[7:0], CMD_Gn_L[7:0] | | | | | | | |
| READ/WRITE | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| CMD_Gn_H[7:0] | Green channel program command n, most significant byte; Address is 0x30h + 2n and 0 ≤ n ≤ 15. See program commands section for details. |
| CMD_Gn_L[7:0] | Green channel program command n, least significant byte; Address is 0x31h + 2n and 0 ≤ n ≤ 15. See program commands section for details. |

| DATA BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| FIELD NAME | CMD_Bn_H[7:0], CMD_Bn_L[7:0] | | | | | | | |
| READ/WRITE | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| FIELD NAME | BIT DEFINITION |
|---|---|
| CMD_Bn_H[7:0] | Blue channel program command n, most significant byte; Address is 0x50h + 2n and 0 ≤ n ≤ 15. See program commands section for details. |
| CMD_Bn_L[7:0] | Blue channel program command n, least significant byte; Address is 0x51h + 2n and 0 ≤ n ≤ 15. See program commands section for details. |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS68401C4YFFR | ACTIVE | DSBGA | YFF | 20 | | Green (RoHS & no Sb/Br) | Call TI | Level-1-260C-UNLIM | -30 to 85 | | Samples |
| TPS68402A0RHFR | ACTIVE | VQFN | RHF | 24 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -30 to 85 | 68402 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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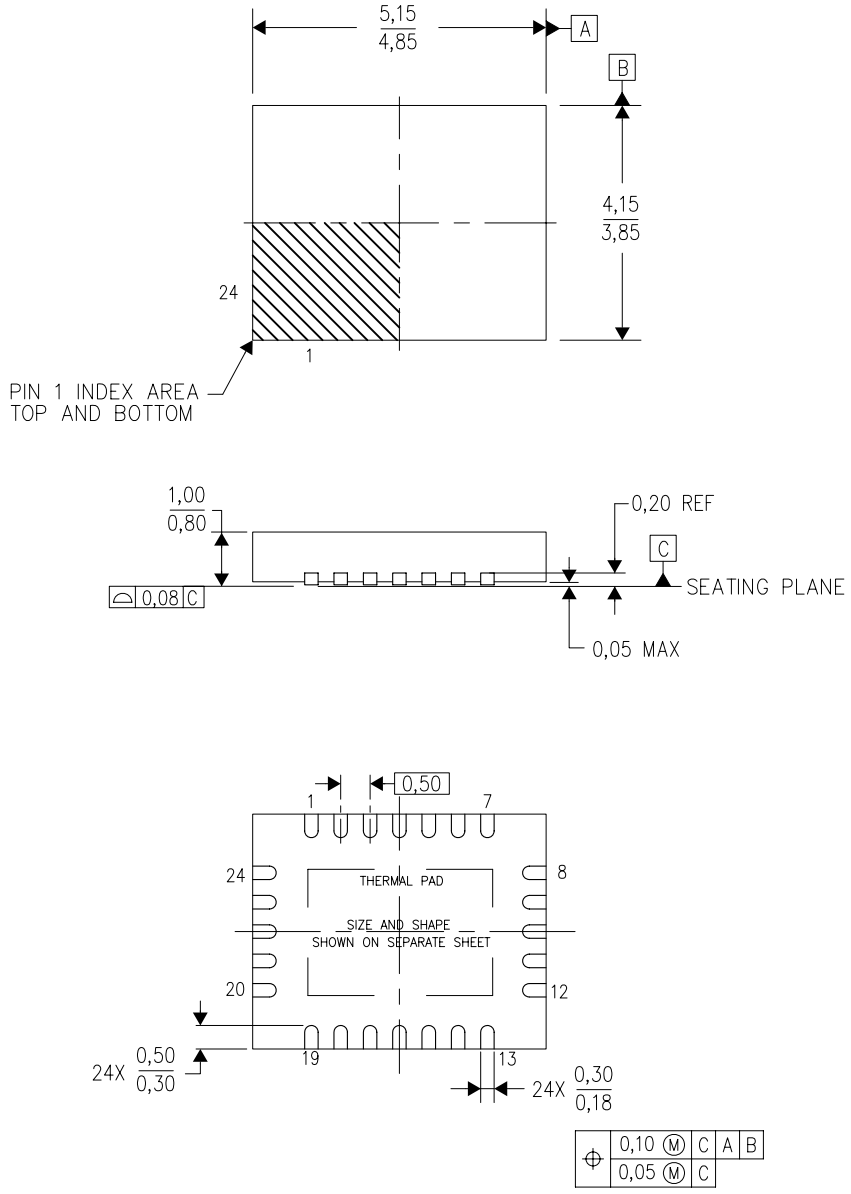
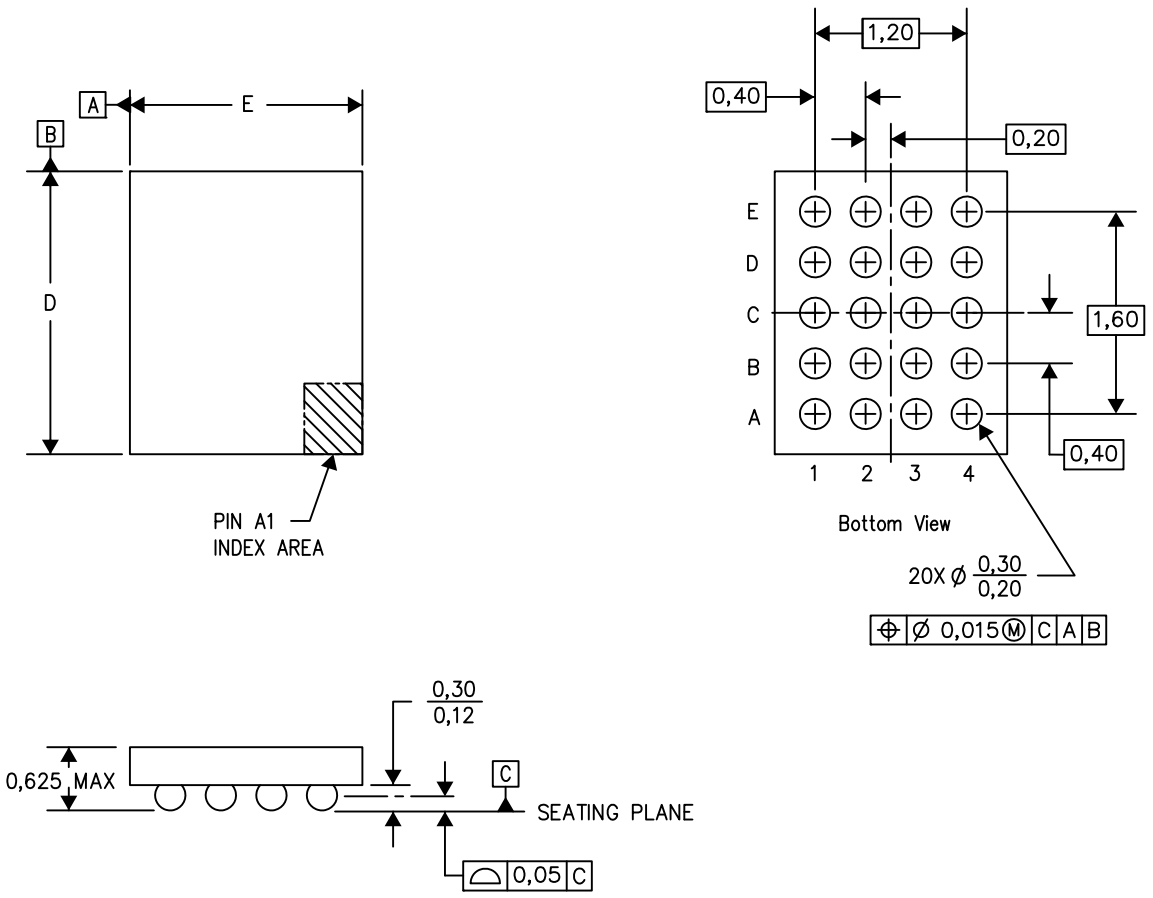



4204845–2/H 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

YFF (R–XBGA–N20) DIE–SIZE BALL GRID ARRAY




4207625–9/AO 12/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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