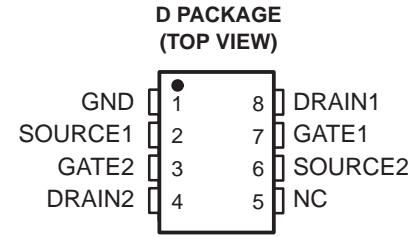


TPIC5223L
2-CHANNEL INDEPENDENT GATE-PROTECTED LOGIC-LEVEL
POWER DMOS ARRAY

SLIS043A – NOVEMBER 1994 – REVISED SEPTEMBER 1995

- Low $r_{DS(on)}$. . . 0.38 Ω Typ
- Voltage Output . . . 60 V
- Input Protection Circuitry . . . 18 V
- Pulsed Current . . . 3 A Per Channel
- Extended ESD Capability . . . 4000 V
- Direct Logic-Level Interface



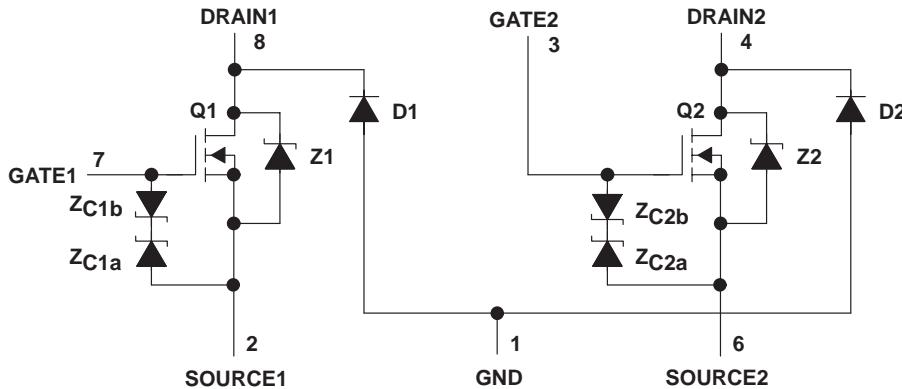
NC – No internal connection

description

The TPIC5223L is a monolithic gate-protected logic-level power DMOS array that consists of two electrically isolated independent N-channel enhancement-mode DMOS transistors. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-k Ω resistor.

The TPIC5223L is offered in a standard eight-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature of -40°C to 125°C .

schematic



NOTE A: For correct operation, no terminal may be taken below GND.

absolute maximum ratings over operating case temperature range (unless otherwise noted)[†]

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage range, V_{GS}	–9 V to 18 V
Continuous drain current, each output, $T_C = 25^\circ\text{C}$	1 A
Continuous source-to-drain diode current, $T_C = 25^\circ\text{C}$	1 A
Pulsed drain current, each output, I_{max} , $T_C = 25^\circ\text{C}$ (see Note 1 and Figure 15)	3 A
Continuous gate-to-source zener diode current, $T_C = 25^\circ\text{C}$	±50 mA
Pulsed gate-to-source zener-diode current, $T_C = 25^\circ\text{C}$	±500 mA
Single-pulse avalanche energy, E_{AS} , $T_C = 25^\circ\text{C}$ (see Figures 4 and 16)	108 mJ
Continuous total power dissipation, $T_C = 25^\circ\text{C}$ (see Figure 15)	0.95 W
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

TPIC5223L
2-CHANNEL INDEPENDENT GATE-PROTECTED LOGIC-LEVEL
POWER DMOS ARRAY

SLIS043A – NOVEMBER 1994 – REVISED SEPTEMBER 1995

electrical characteristics, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(\text{BR})\text{DSX}}$	Drain-to-source breakdown voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0$	60			V
$V_{GS(\text{th})}$	Gate-to-source threshold voltage	$I_D = 1 \text{ mA}$, $V_{DS} = V_{GS}$, See Figure 5	1.5	2.05	2.2	V
$V_{(\text{BR})\text{GS}}$	Gate-to-source breakdown voltage	$I_{GS} = 250 \mu\text{A}$	18			V
$V_{(\text{BR})\text{SG}}$	Source-to-gate breakdown voltage	$I_{SG} = 250 \mu\text{A}$	9			V
$V_{(\text{BR})}$	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = 250 μA	100			V
$V_{DS(\text{on})}$	Drain-to-source on-state voltage	$I_D = 1 \text{ A}$, $V_{GS} = 5 \text{ V}$, See Notes 2 and 3		0.375	0.425	V
$V_{F(\text{SD})}$	Forward on-state voltage, source-to-drain	$I_S = 1 \text{ A}$, $V_{GS} = 0$ (Z1, Z2), See Notes 2 and 3 and Figure 12		0.85	1.2	V
V_F	Forward on-state voltage, GND-to-drain	$I_D = 1 \text{ A}$ (D1, D2), See Notes 2 and 3		3		V
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = 48 \text{ V}$, $V_{GS} = 0$	$T_C = 25^\circ\text{C}$	0.05	1	μA
			$T_C = 125^\circ\text{C}$	0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	$V_{GS} = 15 \text{ V}$, $V_{DS} = 0$		20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	$V_{SG} = 5 \text{ V}$, $V_{DS} = 0$		10	100	nA
$I_{lk\text{g}}$	Leakage current, drain-to-GND	$V_{DGND} = 48 \text{ V}$	$T_C = 25^\circ\text{C}$	0.05	1	μA
			$T_C = 125^\circ\text{C}$	0.5	10	
$r_{DS(\text{on})}$	Static drain-to-source on-state resistance	$V_{GS} = 5 \text{ V}$, $I_D = 1 \text{ A}$, See Notes 2 and 3 and Figures 6 and 7	$T_C = 25^\circ\text{C}$	0.38	0.43	Ω
			$T_C = 125^\circ\text{C}$	0.61	0.65	
g_{fs}	Forward transconductance	$V_{DS} = 15 \text{ V}$, $I_D = 500 \text{ mA}$, See Notes 2 and 3 and Figure 9		1.2	1.49	S
C_{iss}	Short-circuit input capacitance, common source	$V_{DS} = 25 \text{ V}$, $f = 1 \text{ MHz}$,		150	190	pF
C_{oss}	Short-circuit output capacitance, common source			100	125	
C_{rss}	Short-circuit reverse transfer capacitance, common source			40	50	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, $T_C = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	$I_S = 500 \text{ mA}$, $V_{GS} = 0$, See Figures 1 and 14	$Z1$ and $Z2$	50		ns
			$D1$ and $D2$	210		
Q_{RR}	Total diode charge	$V_{DS} = 48 \text{ V}$, $di/dt = 100 \text{ A}/\mu\text{s}$	$Z1$ and $Z2$	50		nC
			$D1$ and $D2$	800		

TPIC5223L

2-CHANNEL INDEPENDENT GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY

SLIS043A – NOVEMBER 1994 – REVISED SEPTEMBER 1995

resistive-load switching characteristics, $T_C = 25^\circ\text{C}$

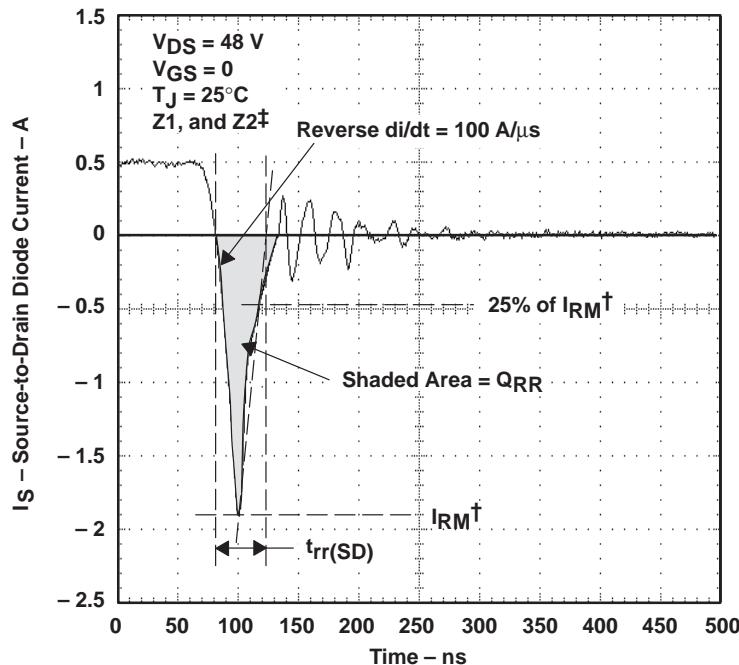
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	$V_{DD} = 25 \text{ V}$, $R_L = 50 \Omega$, $t_{f1} = 10 \text{ ns}$, $t_{f2} = 10 \text{ ns}$, See Figure 2	34	70		ns
$t_{d(off)}$		20	40		
t_{r1}		28	55		
t_{f2}		15	30		
Q_g	$V_{DS} = 48 \text{ V}$, $I_D = 500 \text{ mA}$, $V_{GS} = 5 \text{ V}$, See Figure 3	3.1	3.8		nC
$Q_{gs(th)}$		0.5	0.6		
Q_{gd}		1.9	2.3		
L_D		5			nH
L_S		5			
R_g		0.25			Ω

thermal resistance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	See Notes 4 and 7	130			°C/W
$R_{\theta JB}$		78.6			
$R_{\theta JP}$		34			

NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.
 5. Package mounted on a 24 in², 4-layer FR4 printed-circuit board.
 6. Package mounted in intimate contact with infinite heatsink.
 7. All outputs with equal power

PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current

‡ The above waveform is representative of D1 and D2 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION

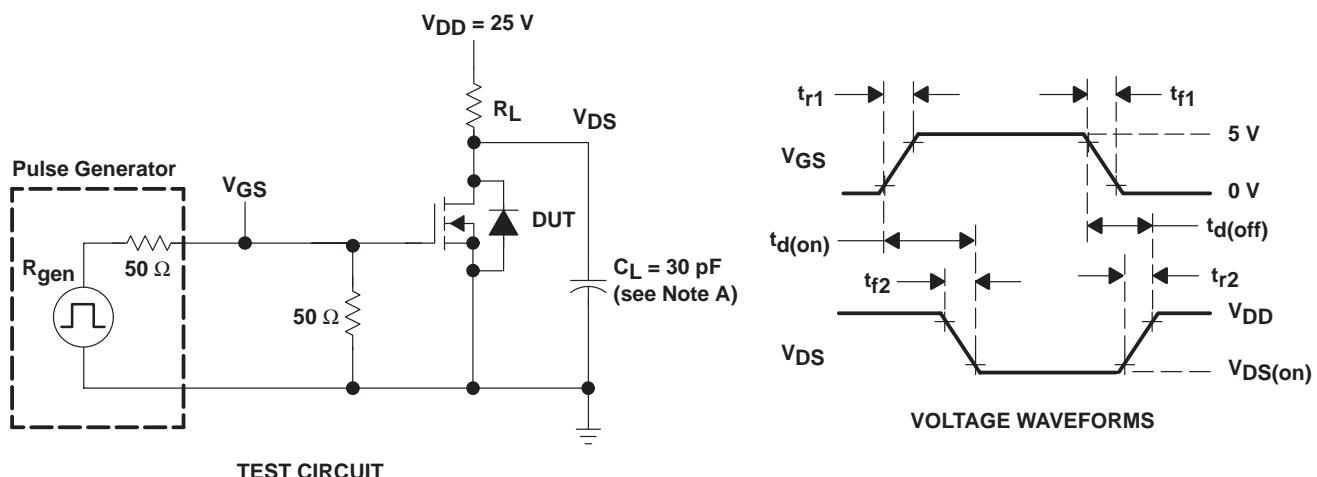


Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

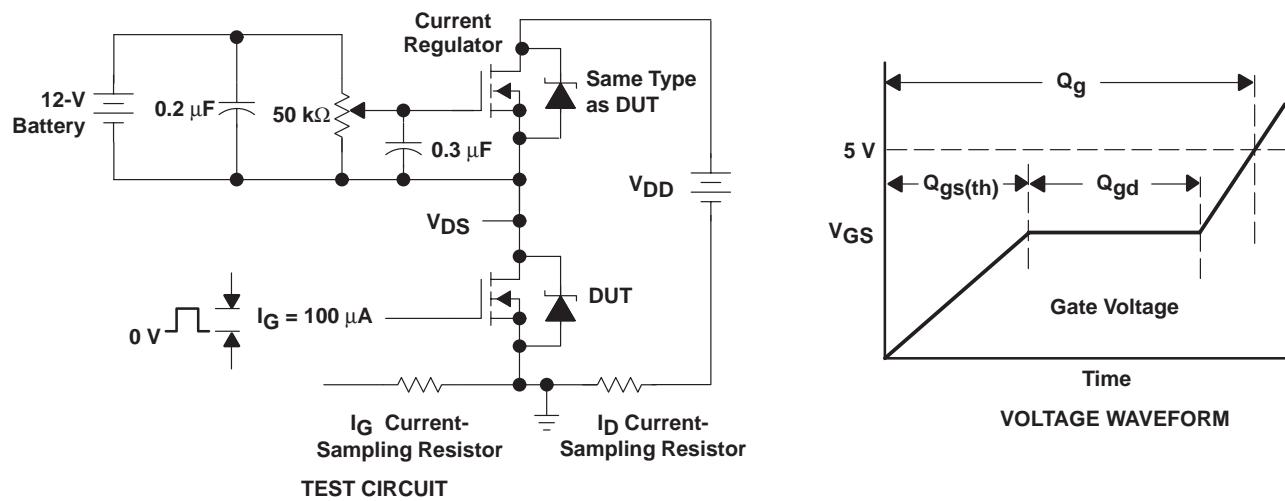
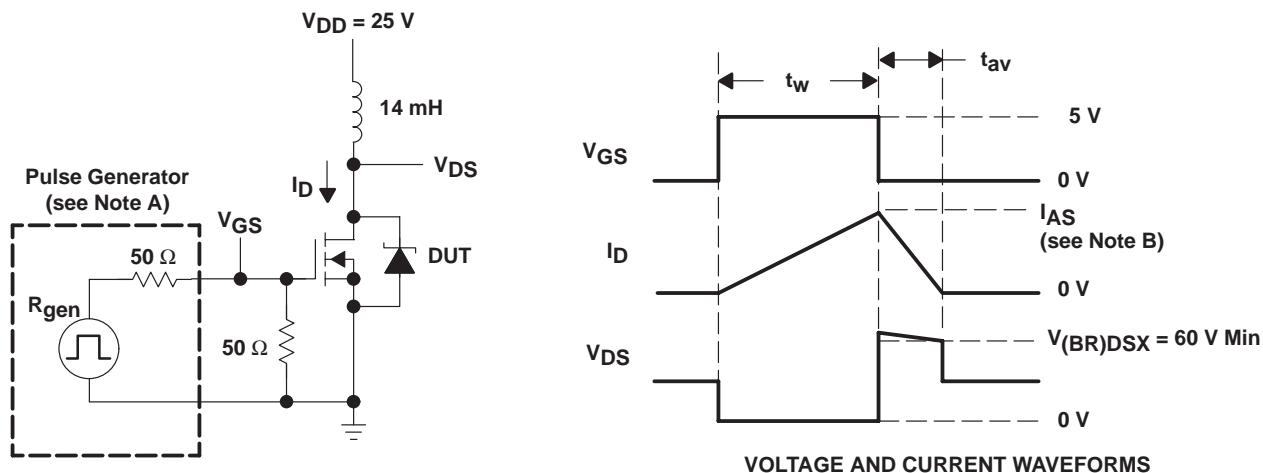


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 3$ A.

$$\text{Energy test level is defined as } E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 108 \text{ mJ, where } t_{av} = \text{avalanche time.}$$

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

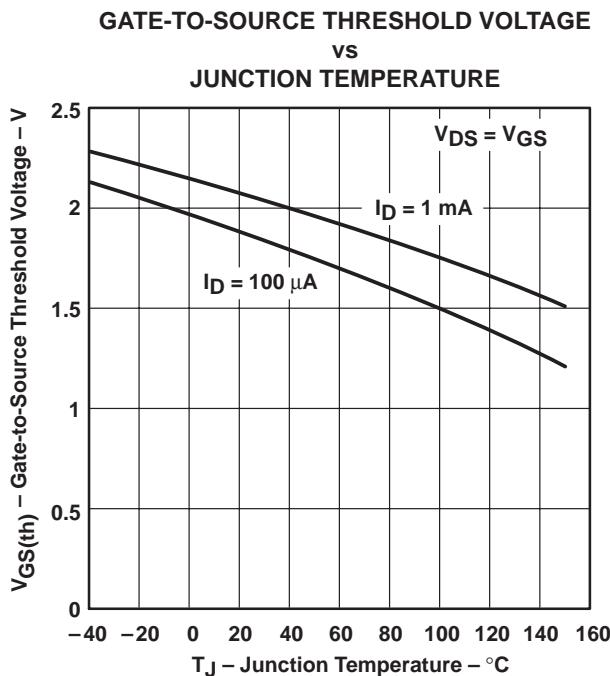


Figure 5

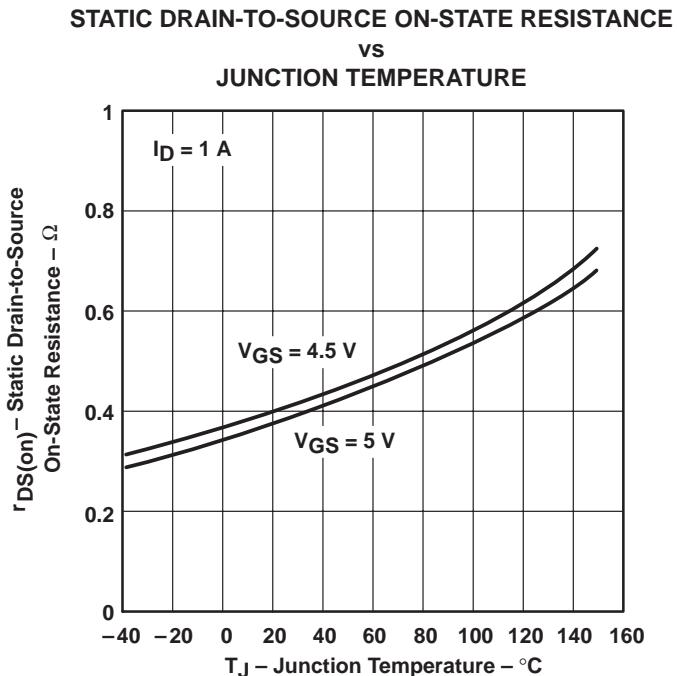


Figure 6

TYPICAL CHARACTERISTICS

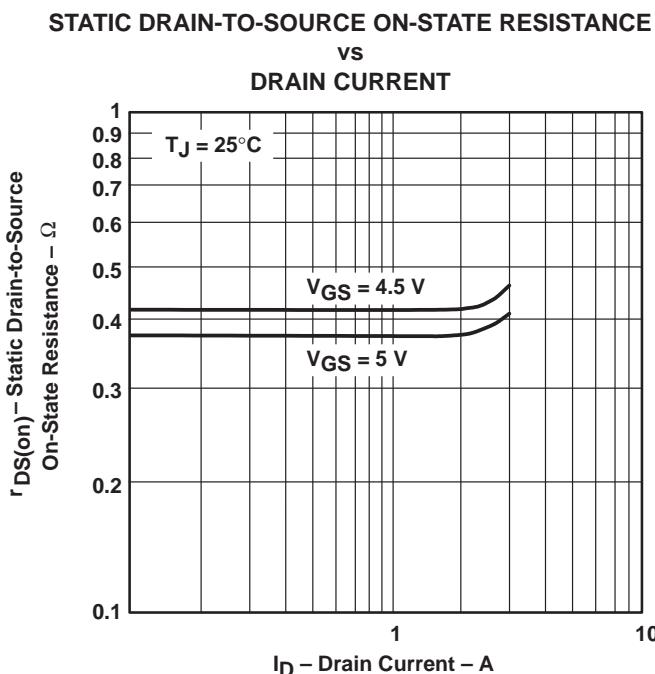


Figure 7

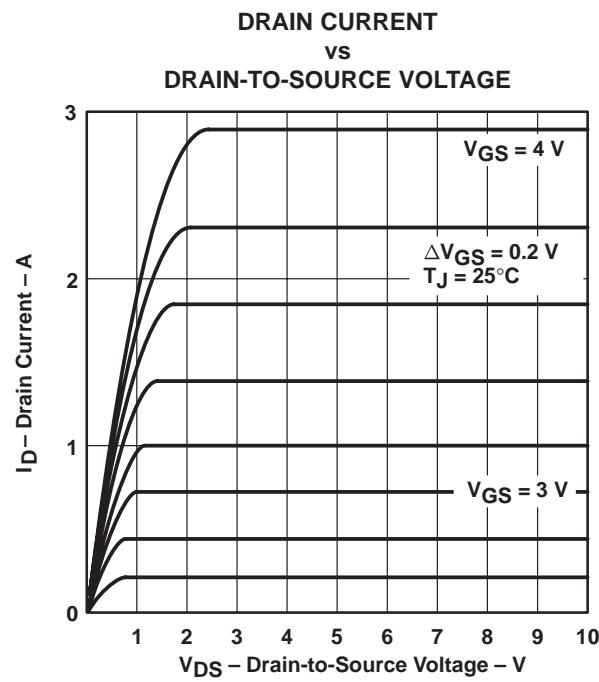


Figure 8

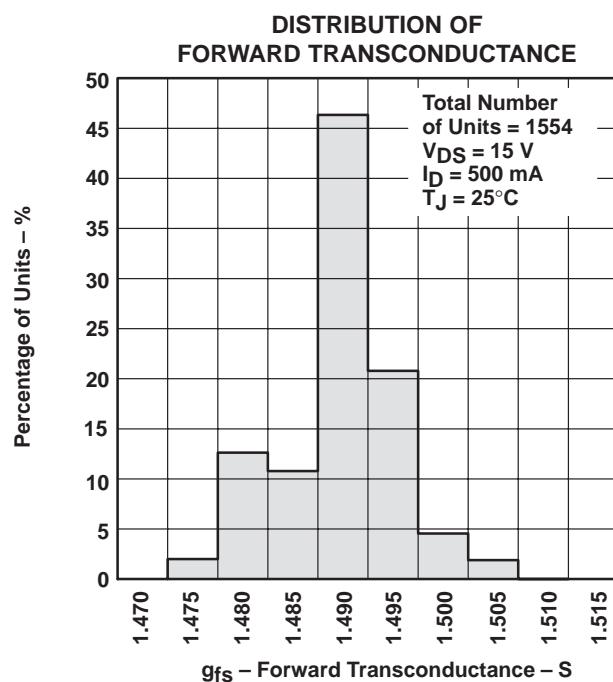


Figure 9

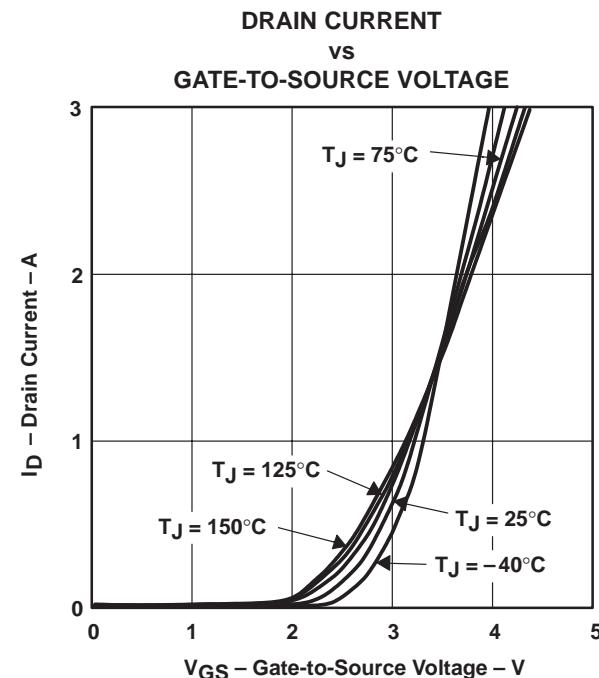


Figure 10

TYPICAL CHARACTERISTICS

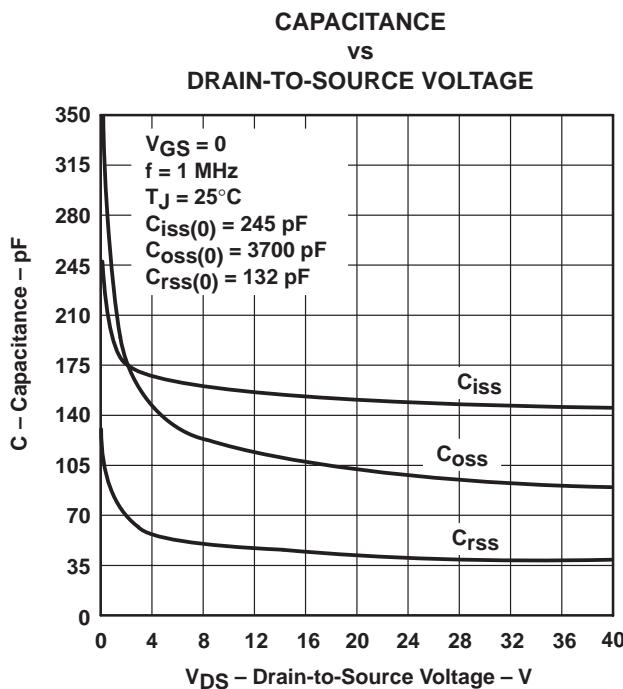


Figure 11

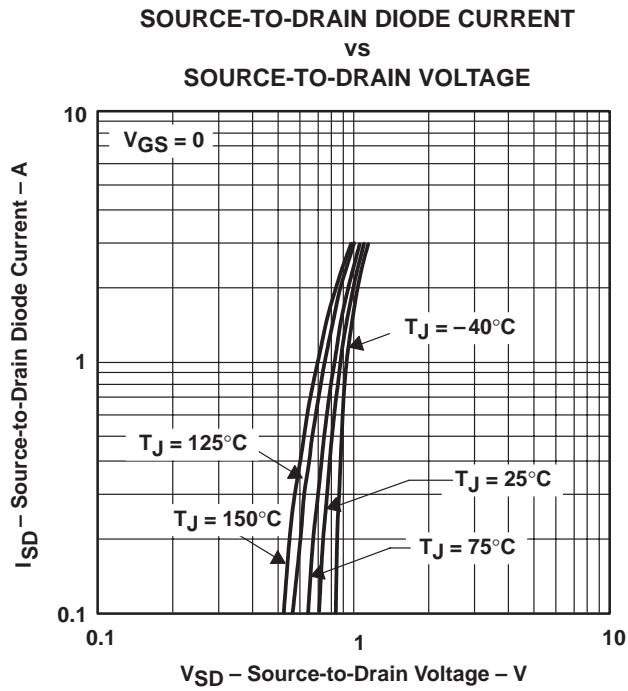


Figure 12

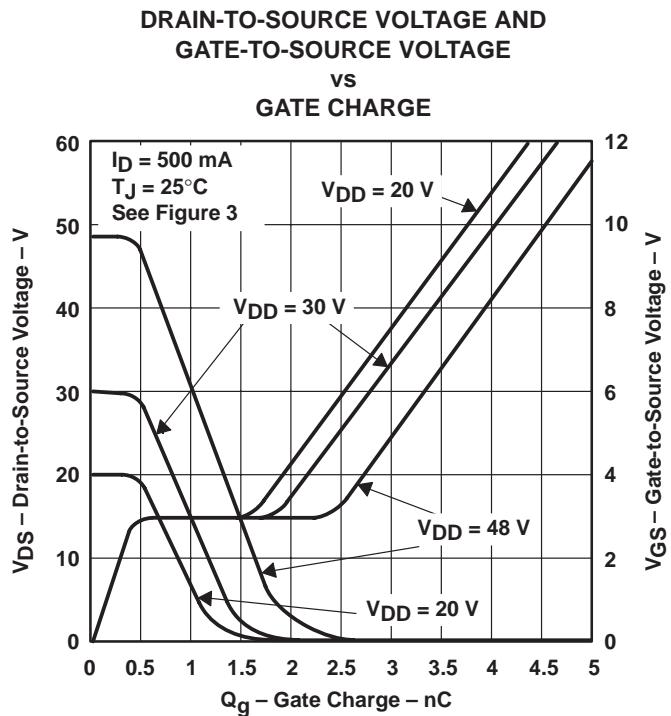


Figure 13

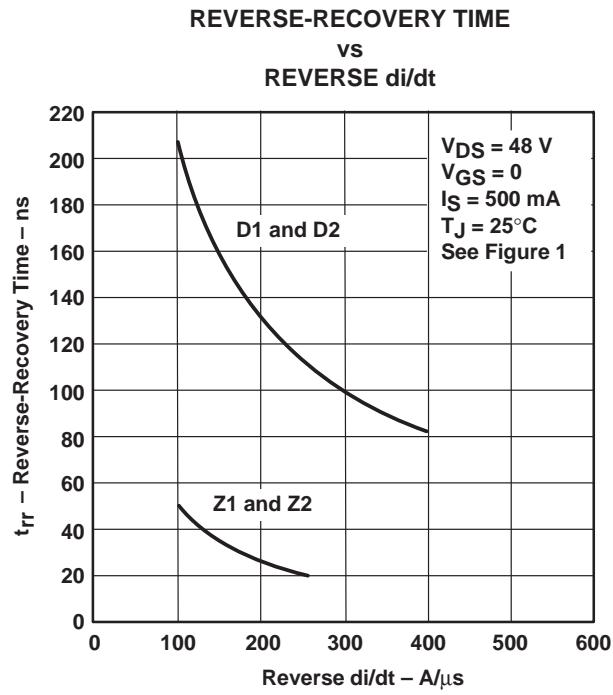
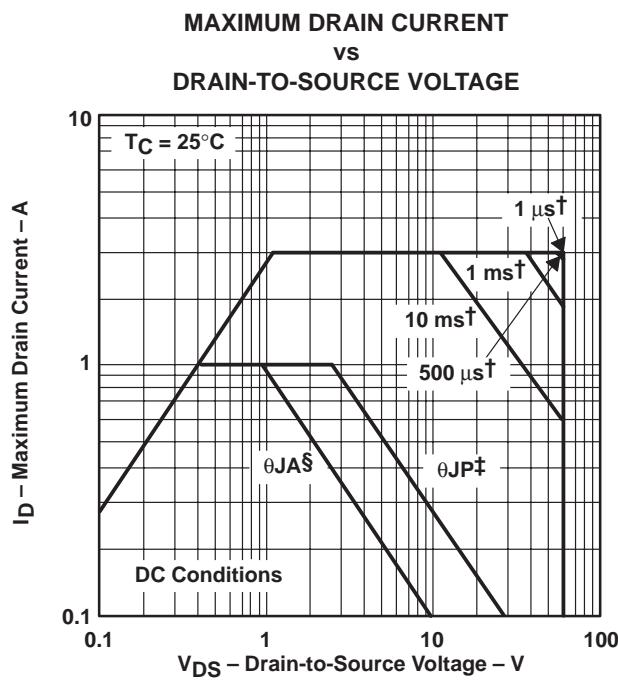


Figure 14

THERMAL INFORMATION



\dagger Less than 2% duty cycle

\ddagger Device mounted in intimate contact with infinite heatsink.

$\$$ Device mounted on FR4 printed-circuit board with no heatsink.

Figure 15

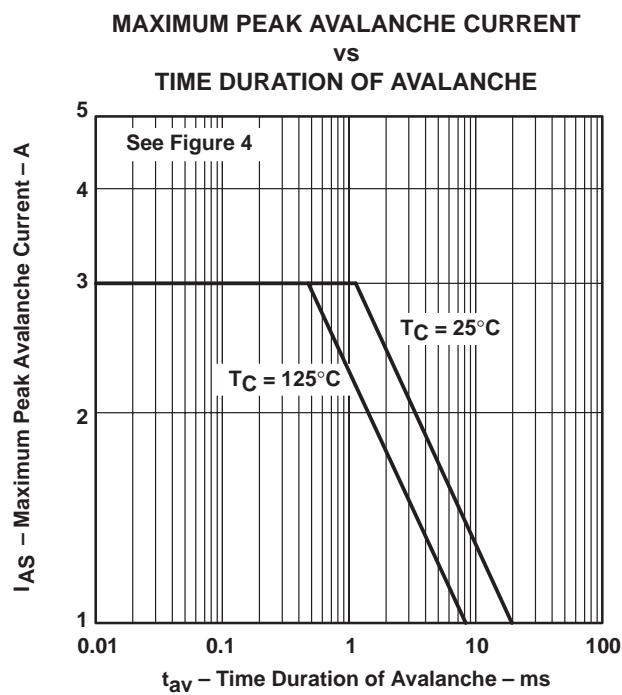
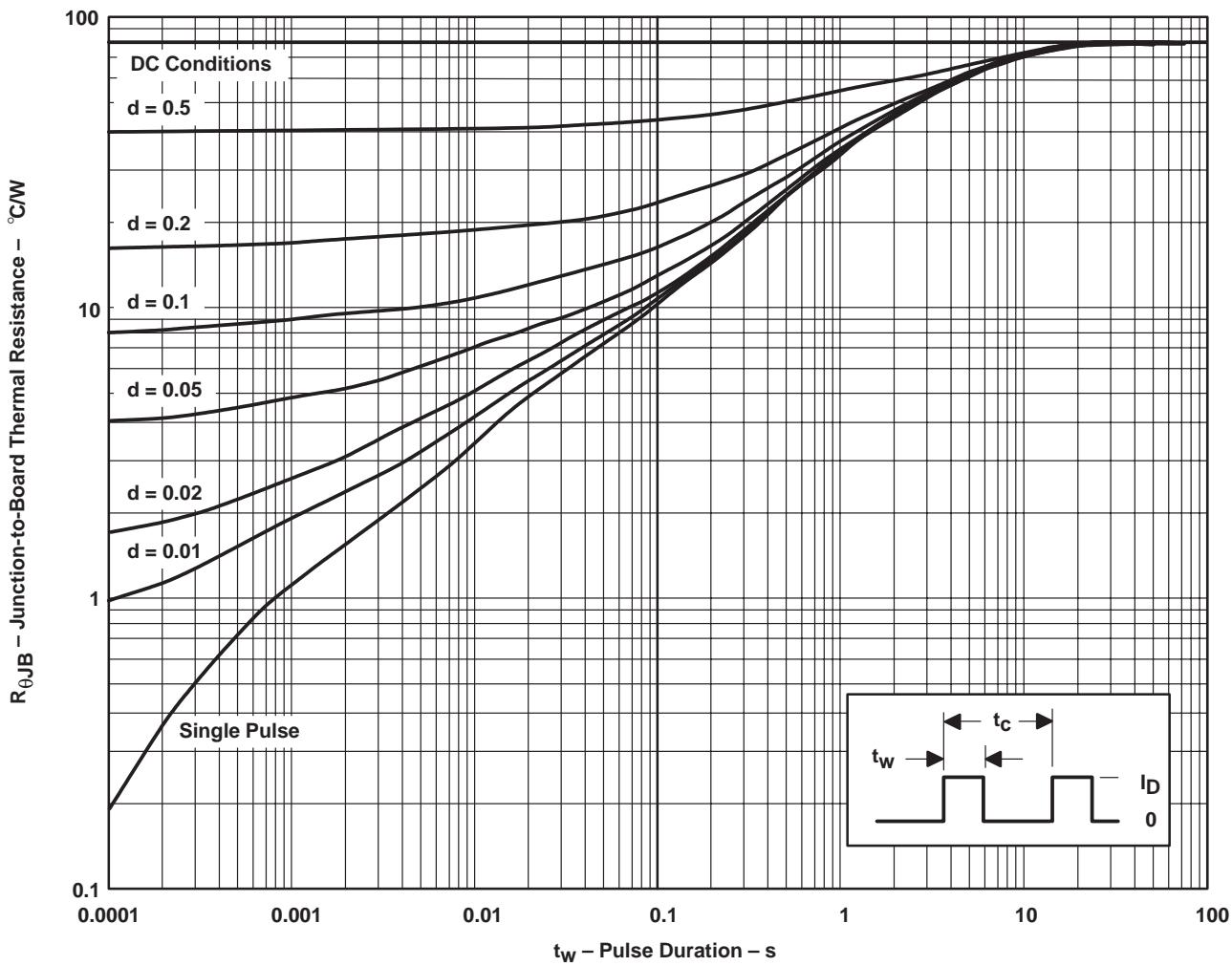


Figure 16

THERMAL INFORMATION

D PACKAGE[†]
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION

[†] Device mounted on 24 in², 4-layer FR4 printed-circuit board with no heatsink.

NOTE A: $Z_{\theta B}(t) = r(t) R_{\theta JB}$

t_W = pulse duration

t_c = cycle time

d = duty cycle = t_W/t_c

Figure 17

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPIC5223LD	OBsolete	SOIC	D	8		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

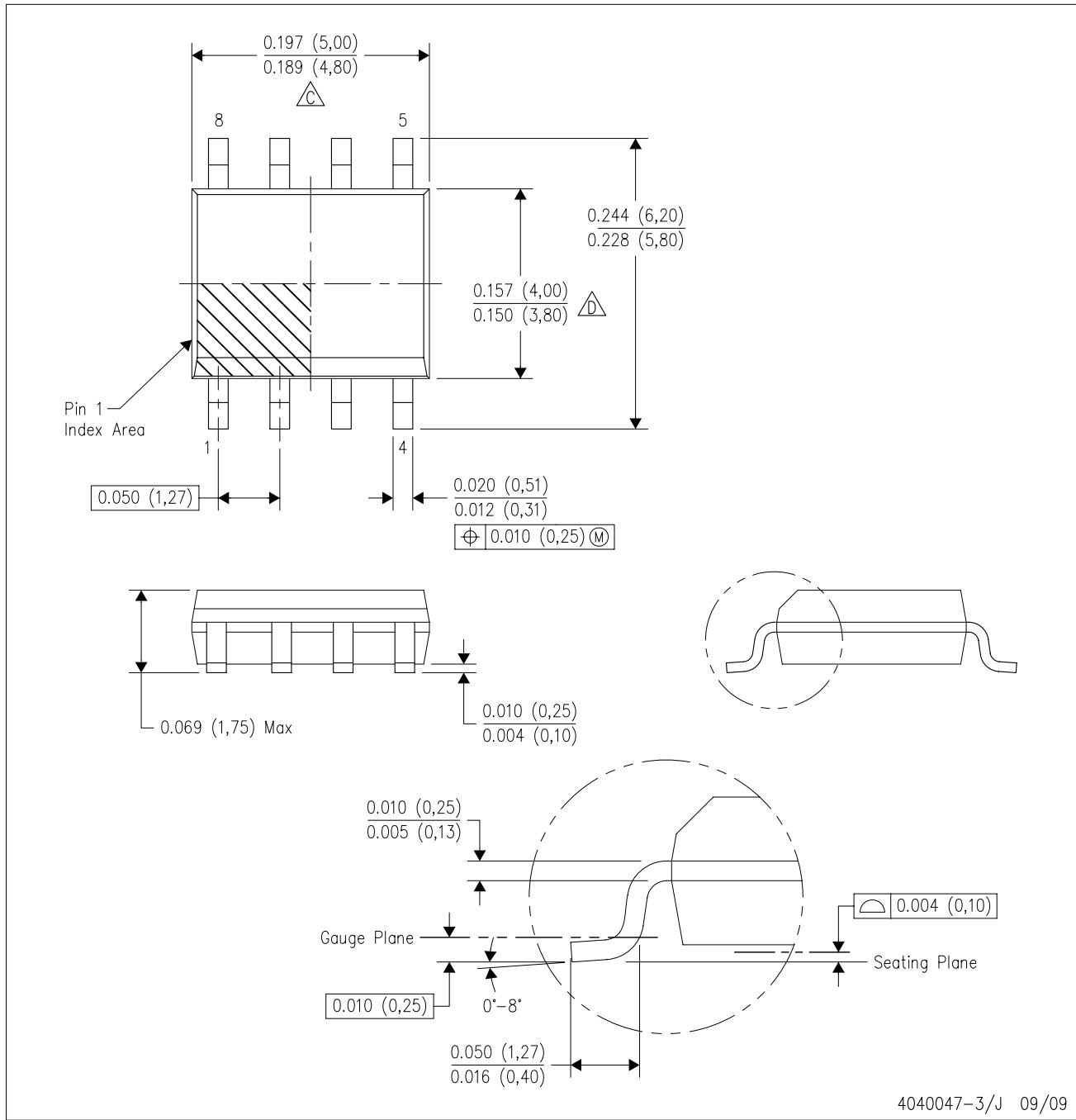
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

△D Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AA.

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