Clock Generator PLL with Integrated VCO

Data Sheet

ADF4360-9

FEATURES

Primary output frequency range: 65 MHz to 400 MHz
Auxiliary divider from 2 to 31, output from 1.1 MHz to 200 MHz
3.0 V to 3.6 V power supply
1.8 V logic compatibility
Integer-N synthesizer
Programmable output power level
3-wire serial interface
Digital lock detect
Software power-down mode

APPLICATIONS

System clock generation
Test equipment
Wireless LANs
CATV equipment

GENERAL DESCRIPTION

The ADF4360-9 is an integrated integer-N synthesizer and voltage-controlled oscillator (VCO). External inductors set the ADF4360-9 center frequency. This allows a VCO frequency range of between 65 MHz and 400 MHz.

An additional divider stage allows division of the VCO signal. The CMOS level output is equivalent to the VCO signal divided by the integer value between 2 and 31. This divided signal can be further divided by 2, if desired.

Control of all the on-chip registers is through a simple 3-wire interface. The device operates with a power supply ranging from 3.0 V to 3.6 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

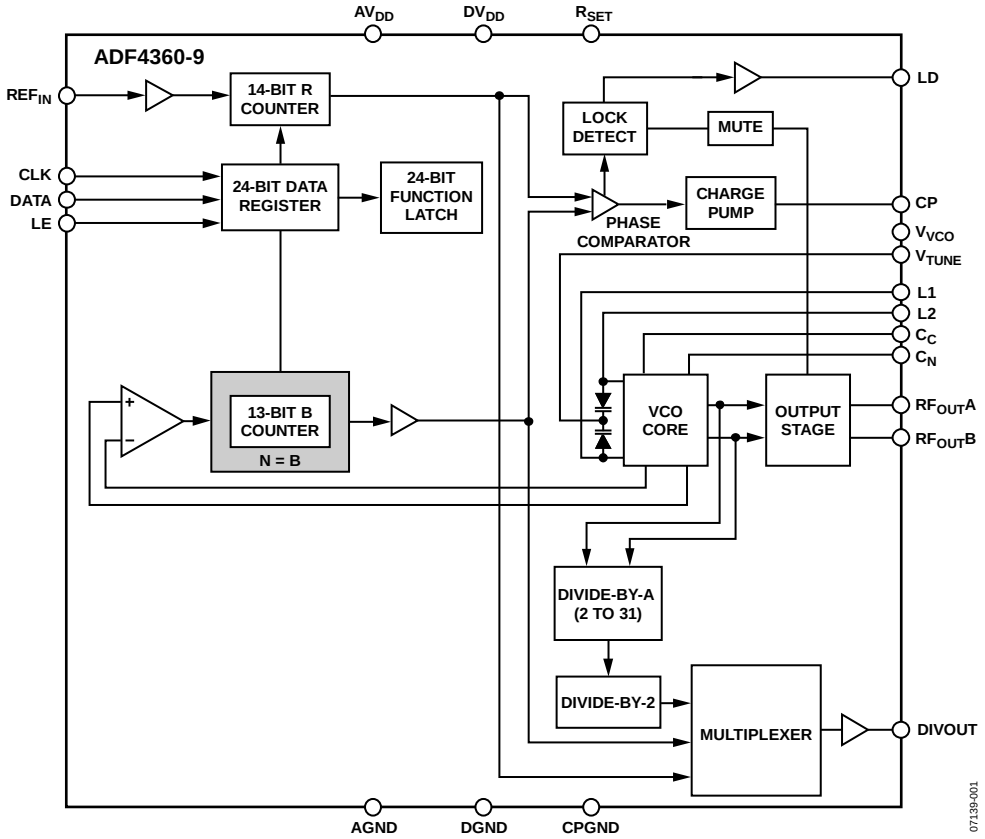

Figure 1.

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ADF4360-9* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADF4360-9 Evaluation Board

DOCUMENTATION

Data Sheet

- ADF4360-9: Clock Generator PLL with Integrated VCO Data Sheet

User Guides

- UG-106: Evaluation Board for the ADF4360-9
- UG-476: PLL Software Installation Guide

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADF4360 - Microcontroller No-OS Driver

TOOLS AND SIMULATIONS

- ADIsimPLL™
- ADIsimRF

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

DESIGN RESOURCES

- ADF4360-9 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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SAMPLE AND BUY

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DOCUMENT FEEDBACK

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REVISION HISTORY

5/2016—Rev. C to Rev. D

Changed ADF4360 Family to ADF4360-9 and ADSP-21xx to ADSP-2181 ... Throughout
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11/2012—Rev. B to Rev. C

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Updated Outline Dimensions ... 24

2/2012—Rev. A to Rev. B

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3/2008—Rev. 0 to Rev. A

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1/2008—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = DV_{DD} = V_{VCO} = 3.3 V ± 10%; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 1.

Parameter	B Version	Unit	Test Conditions/Comments
REF_{IN} CHARACTERISTICS			
REF_{IN} Input Frequency	10/250	MHz min/MHz max	For f < 10 MHz, use a dc-coupled, CMOS-compatible square wave, slew rate > 21 V/µs
REF_{IN} Input Sensitivity	0.7/AV_{DD}	V p-p min/V p-p max	AC-coupled
	0 to AV_{DD}	V max	CMOS-compatible
REF_{IN} Input Capacitance	5.0	pF max	
REF_{IN} Input Current	±60	µA max	
PHASE DETECTOR			
Phase Detector Frequency[2]	8	MHz max	
CHARGE PUMP			
I_{CP} Sink/Source[3]			With R_{SET} = 4.7 kΩ
High Value	2.5	mA typ	
Low Value	0.312	mA typ	
R_{SET} Range	2.7/10	kΩ min/kΩ max	
I_{CP} Three-State Leakage Current	0.2	nA typ	
Sink and Source Current Matching	2	% typ	1.25 V ≤ V_{CP} ≤ 2.5 V
I_{CP} vs. V_{CP}	1.5	% typ	1.25 V ≤ V_{CP} ≤ 2.5 V
I_{CP} vs. Temperature	2	% typ	V_{CP} = 2.0 V
LOGIC INPUTS			
Input High Voltage, V_{INH}	1.5	V min	
Input Low Voltage, V_{INL}	0.6	V max	
Input Current, I_{INH}/I_{INL}	±1	µA max	
Input Capacitance, C_{IN}	3.0	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	DV_{DD} − 0.4	V min	CMOS output chosen
Output High Current, I_{OH}	500	µA max	
Output Low Voltage, V_{OL}	0.4	V max	I_{OL} = 500 µA
POWER SUPPLIES			
AV_{DD}	3.0/3.6	V min/V max	
DV_{DD}	AV_{DD}		
V_{VCO}	AV_{DD}		
AI_{DD}[4]	5	mA typ	
DI_{DD}[4]	2.5	mA typ	
I_{VCO}[4, 5]	12.0	mA typ	I_{CORE} = 5 mA
I_{RFOUT}[4]	3.5 to 11.0	mA typ	RF output stage is programmable
Low Power Sleep Mode[4]	7	µA typ	
RF OUTPUT CHARACTERISTICS[5]			
Maximum VCO Output Frequency	400	MHz	I_{CORE} = 5 mA; depending on L1 and L2; see the Choosing the Correct Inductance Value section
Minimum VCO Output Frequency	65	MHz	
VCO Output Frequency	90/108	MHz min/MHz max	L1, L2 = 270 nH; see the Choosing the Correct Inductance Value section for other frequency values
VCO Frequency Range	1.2	Ratio	f_{MAX}/f_{MIN}
VCO Sensitivity	2	MHz/V typ	L1, L2 = 270 nH; see the Choosing the Correct Inductance Value section for other sensitivity values
Lock Time[6]	400	µs typ	To within 10 Hz of final frequency
Frequency Pushing (Open Loop)	0.24	MHz/V typ	
Frequency Pulling (Open Loop)	10	Hz typ	Into 2.00 VSWR load
Harmonic Content (Second)	−16	dBc typ	

Parameter	B Version	Unit	Test Conditions/Comments
Harmonic Content (Third)	−21	dBc typ	
Output Power[5, 7]	−9/0	dBm typ	Using tuned load, programmable in 3 dB steps; see Figure 35
Output Power[5, 8]	−14/−9	dBm typ	Using 50 Ω resistors to V_{VCO}, programmable in 3 dB steps; see Figure 33
Output Power Variation	±3	dB typ	
VCO Tuning Range	1.25/2.5	V min/V max	
VCO NOISE CHARACTERISTICS			
VCO Phase Noise Performance[9,10]	−91	dBc/Hz typ	At 10 kHz offset from carrier
	−117	dBc/Hz typ	At 100 kHz offset from carrier
	−139	dBc/Hz typ	At 1 MHz offset from carrier
	−140	dBc/Hz typ	At 3 MHz offset from carrier
	−147	dBc/Hz typ	At 10 MHz offset from carrier
Normalized In-Band Phase Noise [10, 11]	−218	dBc/Hz typ	
In-Band Phase Noise[10, 11]	−110	dBc/Hz typ	At 1 kHz offset from carrier
RMS Integrated Jitter[12]	1.4	ps typ	Measured at $RF_{OUT}A$
Spurious Signals Due to PFD Frequency[13]	−75	dBc typ	
DIVOUT CHARACTERISTICS[12]			
Integrated Jitter Performance (Integrated from 100 Hz to 1 GHz)			VCO frequency = 320 MHz to 380 MHz
DIVOUT = 180 MHz	1.4	ps rms	A = 2, A output selected
DIVOUT = 95 MHz	1.4	ps rms	A = 2, A/2 output selected
DIVOUT = 80 MHz	1.4	ps rms	A = 2, A/2 output selected
DIVOUT = 52 MHz	1.4	ps rms	A = 3, A/2 output selected (VCO = 312 MHz, PFD = 1.6 MHz)
DIVOUT = 45 MHz	1.4	ps rms	A = 4, A/2 output selected
DIVOUT = 10 MHz	1.6	ps rms	A = 18, A/2 output selected (VCO = 360 MHz, PFD = 1.6 MHz)
DIVOUT Duty Cycle			
A Output	1/A × 100	% typ	Divide-by-A selected
A/2 Output	50	% typ	Divide-by-A/2 selected

[1] Operating temperature range is −40°C to +85°C.
[2] Guaranteed by design. Sample tested to ensure compliance.
[3] I_{CP} is internally modified to maintain constant loop gain over the frequency range.
[4] T_A = 25°C; $AV_{DD} = DV_{DD} = V_{VCO}$ = 3.3 V.
[5] Unless otherwise stated, these characteristics are guaranteed for VCO core power = 5 mA. L1, L2 = 270 nH, 470 Ω resistors to GND in parallel with L1, L2.
[6] Jumping from 90 MHz to 108 MHz. PFD frequency = 200 kHz; loop bandwidth = 10 kHz.
[7] For more detail on using tuned loads, see the Output Matching section.
[8] Using 50 Ω resistors to V_{VCO} into a 50 Ω load.
[9] The noise of the VCO is measured in open-loop conditions. L1, L2 = 56 nH.
[10] The phase noise is measured with the EV-ADF4360-9EB1Z evaluation board and the Agilent E5052A signal source analyzer.
[11] f_{REFIN} = 10 MHz; f_{PFD} = 1 MHz; N = 360; loop bandwidth = 40 kHz. The normalized phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20logN (where N is the N divider value) and $10\log f_{PFD}$. $PN_{SYNTH} = PN_{TOT} - 10\log f_{PFD} - 20\log N$.
[12] The jitter is measured with the EV-ADF4360-9EB1Z evaluation board and the Agilent E5052A signal source analyzer. A low noise TCXO provides the REF_{IN} for the synthesizer, and the jitter is measured over the instrument's jitter measurement bandwidth. f_{REFIN} = 10 MHz; f_{PFD} = 1 MHz; N = 360; loop bandwidth = 40 kHz, unless otherwise noted.
[13] The spurious signals are measured with the EV-ADF4360-9EB1Z evaluation board and the Agilent E5052A signal source analyzer. The spectrum analyzer provides the REF_{IN} for the synthesizer; f_{REFIN} = 10 MHz at 0 dBm. f_{REFIN} = 10 MHz; f_{PFD} = 1 MHz; N = 360; loop bandwidth = 40 kHz.

TIMING CHARACTERISTICS[1]

AV_{DD} = DV_{DD} = V_{VCO} = 3.3 V ± 10%; AGND = DGND = 0 V; 1.8 V and 3 V logic levels used; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLK setup time
t_3	10	ns min	DATA to CLK hold time
t_4	25	ns min	CLK high duration
t_5	25	ns min	CLK low duration
t_6	10	ns min	CLK to LE setup time
t_7	20	ns min	LE pulse width

[1] Refer to the Power-Up section for the recommended power-up procedure for this device.

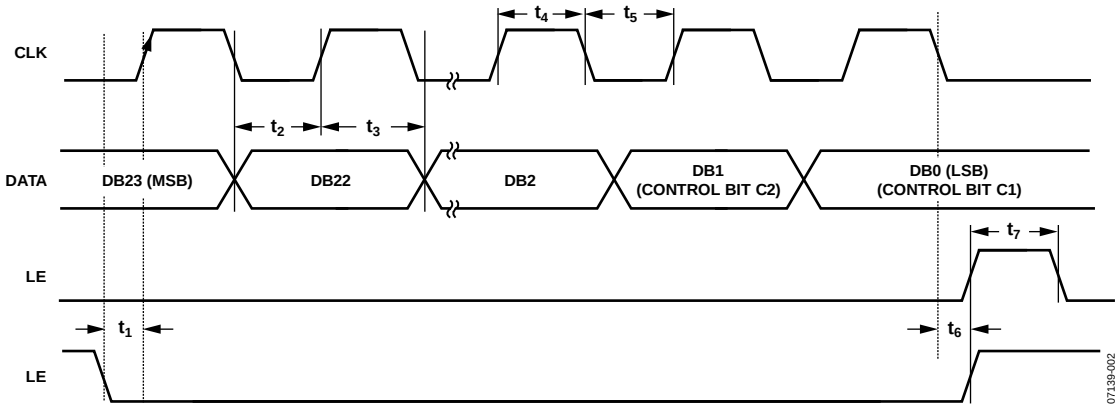

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND[1]	−0.3 V to +3.9 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_{VCO} to GND	−0.3 V to +3.9 V
V_{VCO} to AV_{DD}	−0.3 V to +0.3 V
Digital Input/Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog Input/Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
REF_{IN} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to + 85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA} Thermal Impedance	
Paddle Soldered	50°C/W
Paddle Not Soldered	88°C/W
Lead Temperature, Soldering Reflow	260°C

[1] GND = CPGND = AGND = DGND = 0 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

This device is a high performance RF integrated circuit with an ESD rating of <1 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

TRANSISTOR COUNT

The transistor count is 12,543 (CMOS) and 700 (bipolar).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

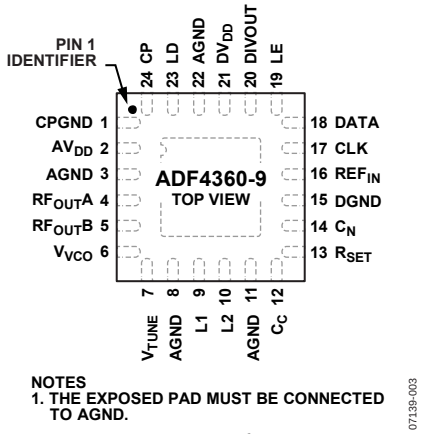

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
2	AV_{DD}	Analog Power Supply. This ranges from 3.0 V to 3.6 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AV_{DD} must have the same value as DV_{DD}.
3, 8, 11, 22	AGND	Analog Ground. This is the ground return path of the prescaler and VCO.
4	$RF_{OUT}A$	VCO Output. The output level is programmable from 0 dBm to −9 dBm. See the Output Matching section for a description of the various output stages.
5	$RF_{OUT}B$	VCO Complementary Output. The output level is programmable from 0 dBm to −9 dBm. See the Output Matching section for a description of the various output stages.
6	V_{VCO}	Power Supply for the VCO. This ranges from 3.0 V to 3.6 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. V_{VCO} must have the same value as AV_{DD}.
7	V_{TUNE}	Control Input to the VCO. This voltage determines the output frequency and is derived from filtering the CP output voltage.
9	L1	An external inductor to AGND should be connected to this pin to set the ADF4360-9 output frequency. L1 and L2 need to be the same value. A 470 Ω resistor should be added in parallel to AGND.
10	L2	An external inductor to AGND should be connected to this pin to set the ADF4360-9 output frequency. L1 and L2 need to be the same value. A 470 Ω resistor should be added in parallel to AGND.
12	C_C	Internal Compensation Node. This pin must be decoupled to ground with a 10 nF capacitor.
13	R_{SET}	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current for the synthesizer. The nominal voltage potential at the R_{SET} pin is 0.6 V. The relationship between I_{CP} and R_{SET} is $I_{CPmax} = 11.75/R_{SET}$ For example, R_{SET} = 4.7 kΩ and I_{CPmax} = 2.5 mA.
14	C_N	Internal Compensation Node. This pin must be decoupled to V_{VCO} with a 10 µF capacitor.
15	DGND	Digital Ground.
16	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and a dc equivalent input resistance of 100 kΩ (see Figure 16). This input can be driven from a TTL or CMOS crystal oscillator, or it can be ac-coupled.
17	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
18	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
19	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, and the relevant latch is selected using the control bits.
20	DIVOUT	This output allows the user to select VCO frequency divided by A or VCO frequency divided by 2A. Alternatively, the scaled RF, or the scaled reference frequency, can be accessed externally through this output.
21	DV_{DD}	Digital Power Supply. This ranges from 3.0 V to 3.6 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} must have the same value as AV_{DD}.
23	LD	Lock Detect. The output on this pin is logic high to indicate that the device is in lock. Logic low indicates loss of lock.
24	CP	Charge Pump Output. When enabled, this provides $\pm I_{CP}$ to the external loop filter, which in turn drives the internal VCO.
	EP	Exposed Pad. The exposed pad must be connected to AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

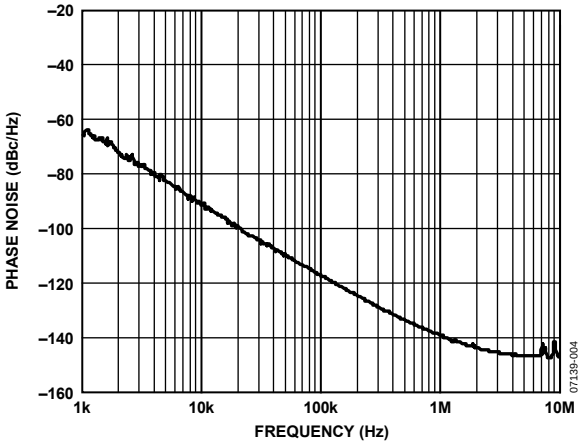

Figure 4. Open-Loop VCO Phase Noise at 218 MHz, L1, L2 = 56 nH

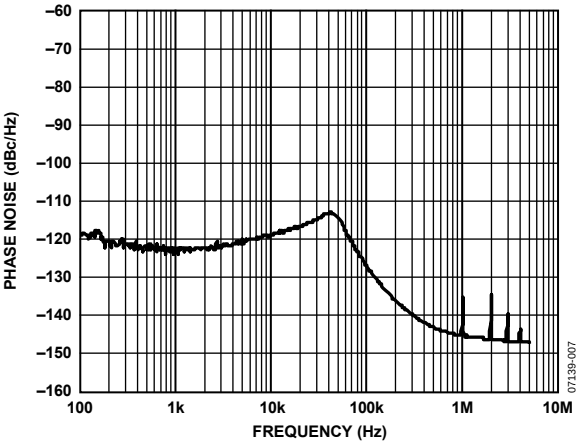

Figure 7. DIVOUT Phase Noise, 95 MHz, VCO = 380 MHz, PFD Frequency = 1 MHz, Loop Bandwidth = 40 kHz, Jitter = 1.3 ps, Divide-by-A/2 Selected, A = 2

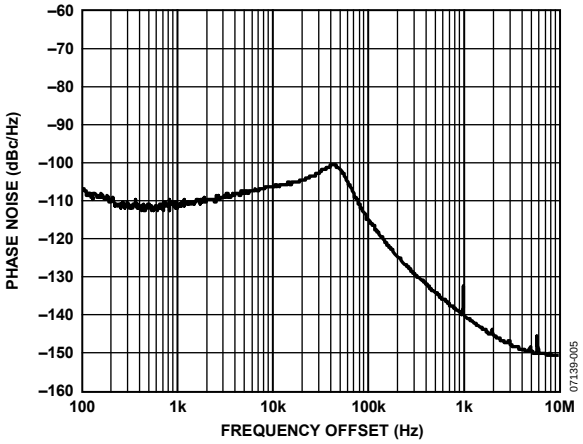

Figure 5. VCO Phase Noise, 360 MHz, 1 MHz PFD, 40 kHz Loop Bandwidth, RMS Jitter = 1.4 ps

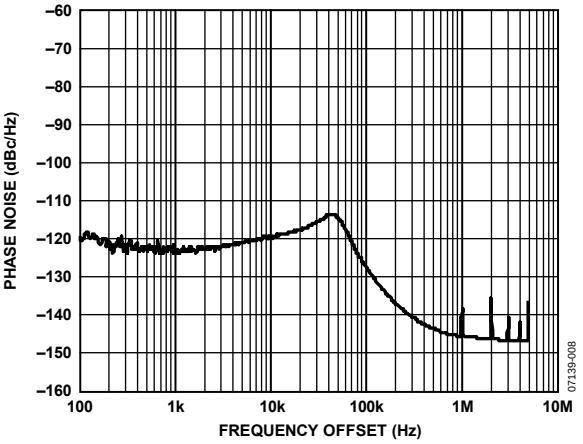

Figure 8. DIVOUT Phase Noise, 80 MHz, VCO = 320 MHz, PFD Frequency = 1 MHz, Loop Bandwidth = 40 kHz, Jitter = 1.3 ps, Divide-by-A/2 Selected, A = 2

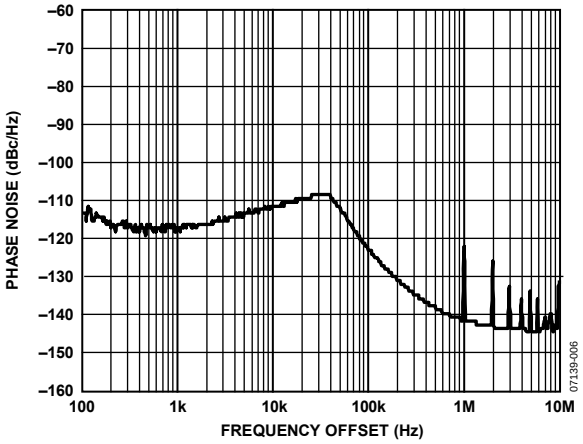

Figure 6. DIVOUT Phase Noise, 180 MHz, VCO = 360 MHz, PFD Frequency = 1 MHz, Loop Bandwidth = 40 kHz, Jitter = 1.3 ps, Divide-by-A Selected, A = 2

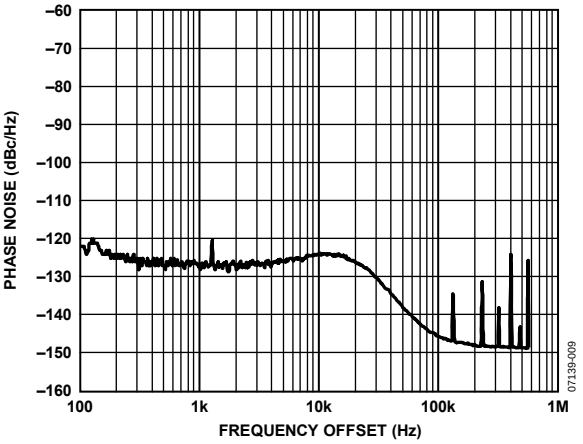

Figure 9. DIVOUT Phase Noise, 52 MHz, VCO = 312 MHz, PFD Frequency = 1.6 MHz, Loop Bandwidth = 40 kHz, Jitter = 1.4 ps, Divide-by-A/2 Selected, A = 3

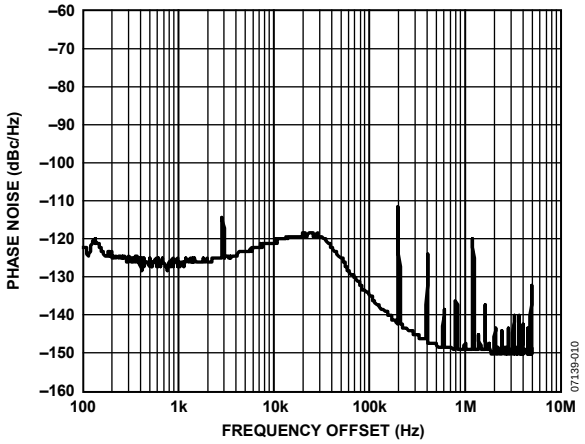

Figure 10. DIVOUT Phase Noise, 45 MHz, VCO = 360 MHz, PFD Frequency = 1.6 MHz, Loop Bandwidth = 60 kHz, Jitter = 1.4 ps, Divide-by-A/2 Selected, A = 2

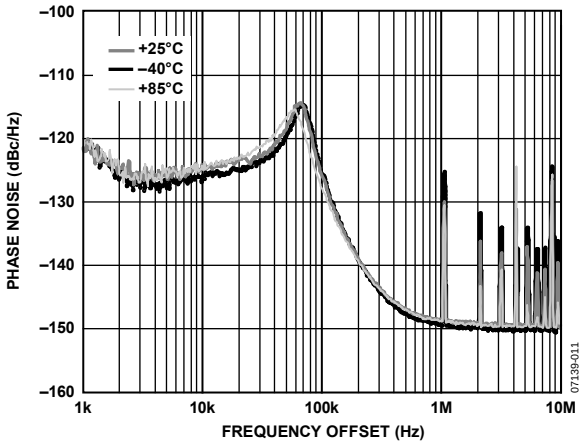

Figure 11. DIVOUT Phase Noise over Temperature, 52 MHz, VCO = 312 MHz, PFD Frequency = 1 MHz, Loop Bandwidth = 60 kHz, Divide-by-A/2 Selected, A = 3

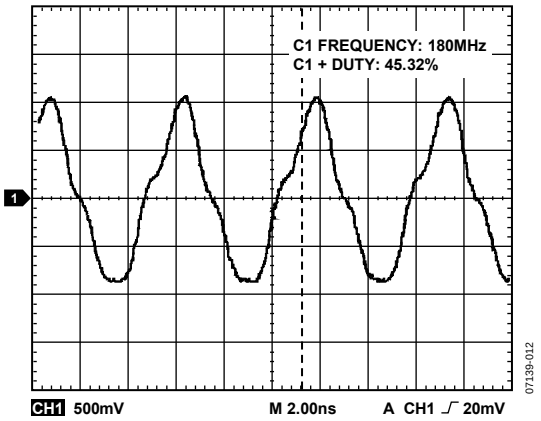

Figure 12. DIVOUT 180 MHz Waveform, VCO = 360 MHz, Divide-by-A Selected, A = 2, Duty Cycle = ~50%

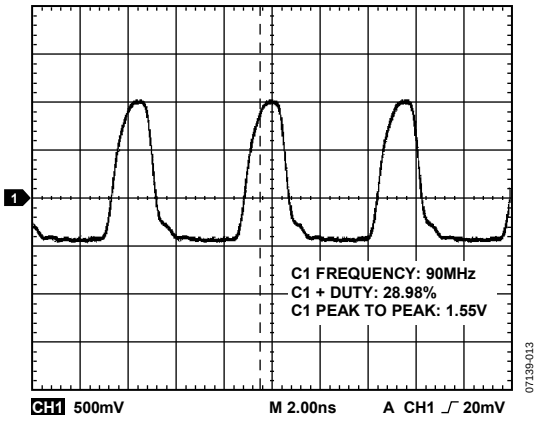

Figure 13. DIVOUT 90 MHz Waveform, VCO = 360 MHz, Divide-by-A Selected, A = 4, Duty Cycle = ~25%

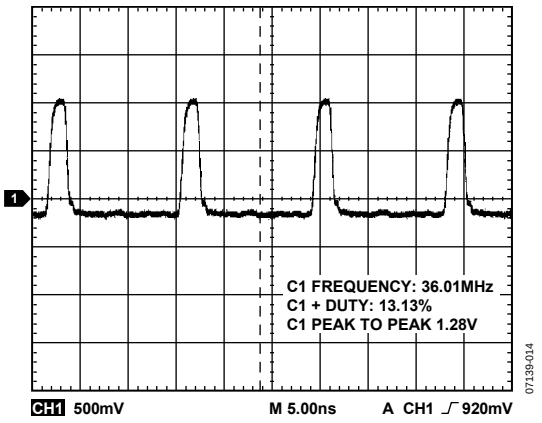

Figure 14. DIVOUT 36 MHz Waveform, VCO = 360 MHz, Divide-by-A Selected, A = 10, Duty Cycle = ~10%

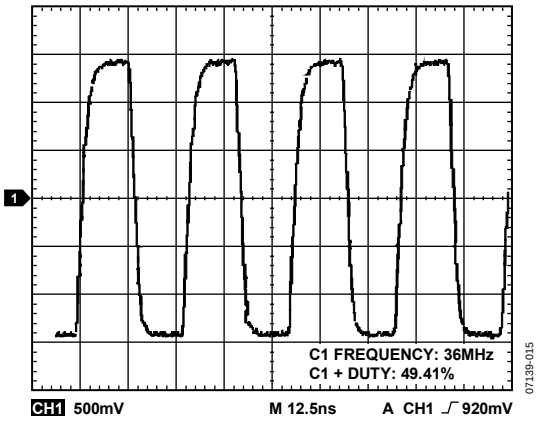

Figure 15. DIVOUT 36 MHz Waveform, VCO = 360 MHz, Divide-by-A/2 Selected, A = 5, Duty Cycle = ~50%

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 16. SW1 and SW2 are normally closed switches, and SW3 is normally open. When power-down is initiated, SW3 is closed, and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin at power-down.

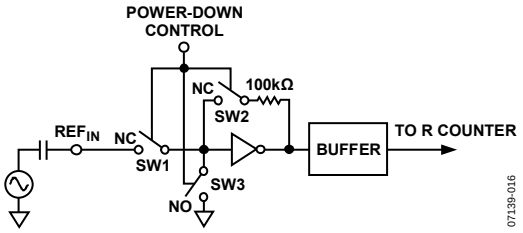

Figure 16. Reference Input Stage

N COUNTER

The CMOS N counter allows a wide division ratio in the PLL feedback counter. The counters are specified to work when the VCO output is 400 MHz or less. To avoid confusion, this is referred to as the B counter. It makes it possible to generate output frequencies that are spaced only by the reference frequency divided by R. The VCO frequency equation is

$$f_{VCO} = B \times f_{REFIN}/R$$

where:
f_{VCO} is the output frequency of the VCO.
B is the preset divide ratio of the binary 13-bit counter (3 to 8191).
f_{REFIN} is the external reference frequency oscillator.

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

PFD AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter (N = B) and produces an output proportional to the phase and frequency difference between them. Figure 17 is a simplified schematic. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the R counter latch, ABP2 and ABP1, control the width of the pulse (see Figure 25).

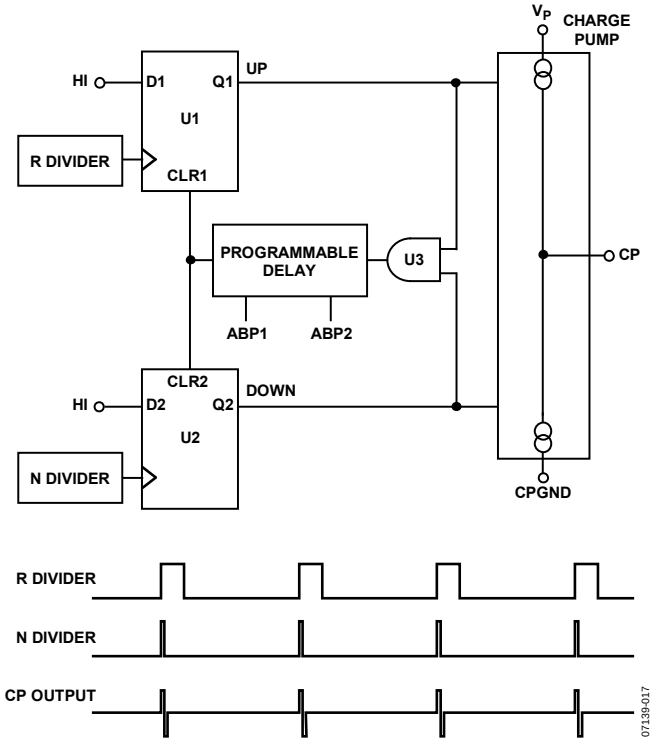

Figure 17. PFD Simplified Schematic and Timing (In Lock)

LOCK DETECT

The LD pin outputs a lock detect signal. Digital lock detect is active high. When lock detect precision (LDP) in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector cycles is <15 ns.

When LDP is set to 1, five consecutive cycles of <15 ns phase error are required to set the lock detect. It stays set high until a phase error of >25 ns is detected on any subsequent PD cycle.

INPUT SHIFT REGISTER

The digital section of the ADF4360-9 includes a 24-bit input shift register, a 14-bit R counter, and an 18-bit N counter, comprising a 5-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. The two LSBs, DB1 and DB0, are shown in Figure 2.

The truth table for these bits is shown in Table 5. Figure 22 shows a summary of how the latches are programmed. Note that the test modes latch is used for factory testing and should not be programmed by the user.

Table 5. C2 and C1 Truth Table

Control Bits		
C2	**C1**	**Data Latch**
0	0	Control
0	1	R Counter
1	0	N Counter (B)
1	1	Test Modes

VCO

The VCO core in the ADF4360-9 uses eight overlapping bands, as shown in Figure 18, to allow a wide frequency range to be covered without a large VCO sensitivity (K_V) and resultant poor phase noise and spurious performance.

The correct band is chosen automatically by the band select logic at power-up or whenever the N counter latch is updated. It is important that the correct write sequence be followed at power-up. The correct write sequence is as follows:

1. R Counter Latch
2. Control Latch
3. N Counter Latch

During band selection, which takes five PFD cycles, the VCO V_{TUNE} is disconnected from the output of the loop filter and connected to an internal reference voltage.

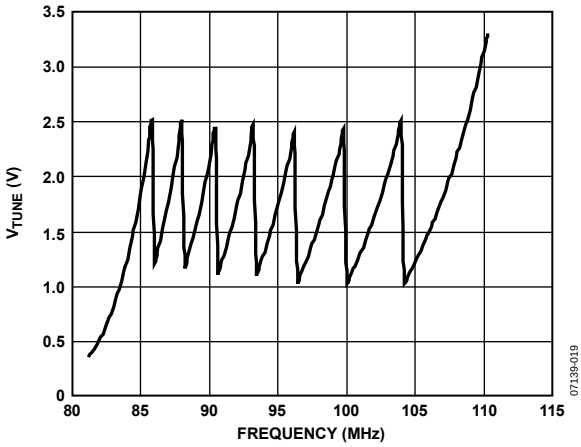

Figure 18. V_{TUNE}, ADF4360-9, L1 and L2 = 270 nH vs. Frequency

The R counter output is used as the clock for the band select logic and should not exceed 1 MHz. A programmable divider is provided at the R counter input to allow division by 1, 2, 4, or 8 and is controlled by the BSC1 bit and the BSC2 bit in the R counter latch. Where the required PFD frequency exceeds 1 MHz, the divide ratio should be set to allow enough time for correct band selection. For many applications, it is usually best to set this to 8.

After band selection, normal PLL action resumes. The value of K_V is determined by the value of the inductors used (see the Choosing the Correct Inductance Value section). The ADF4360-9 contains linearization circuitry to minimize any variation of the product of I_{CP} and K_V.

The operating current in the VCO core is programmable in four steps: 2.5 mA, 5 mA, 7.5 mA, and 10 mA. This is controlled by the PC1 bit and the PC2 bit in the control latch.

It is strongly recommended that only the 5 mA setting be used. However, in applications requiring a low VCO frequency, the high temperature coefficient of some inductors may lead to the VCO tuning voltage varying as temperature changes. The 7.5 mA VCO core power setting shows less tuning voltage variation over temperature in these applications and can be used, provided that 240 Ω resistors are used in parallel with Pin 9 and Pin 10, instead of the default 470 Ω.

OUTPUT STAGE

The RF$_{OUT}$A and RF$_{OUT}$B pins of the ADF4360-9 are connected to the collectors of an NPN differential pair driven by buffered outputs of the VCO, as shown in Figure 19. To allow the user to optimize the power dissipation vs. the output power requirements, the tail current of the differential pair is programmable via Bit PL1 and Bit PL2 in the control latch. Four current levels can be set: 3.5 mA, 5 mA, 7.5 mA, and 11 mA. These levels give output power levels of −9 dBm, −6 dBm, −3 dBm, and 0 dBm, respectively, using the correct shunt inductor to V_{DD} and ac coupling into a 50 Ω load. Alternatively, both outputs can be combined in a 1 + 1:1 transformer or a 180° microstrip coupler (see the Output Matching section).

Another feature of the ADF4360-9 is that the supply current to the RF output stage is shut down until the device achieves lock, as measured by the digital lock detect circuitry. This is enabled by the mute-till-lock detect (MTLD) bit in the control latch.

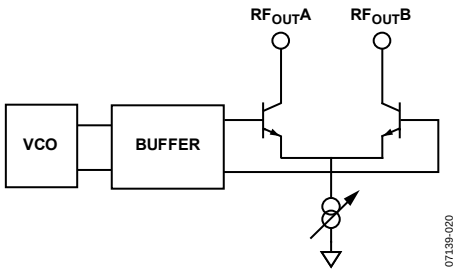

Figure 19. RF Output Stage

DIVOUT STAGE

The output multiplexer on the ADF4360-9 allows the user to access various internal points on the chip. The state of DIVOUT is controlled by D3, D2, and D1 in the control latch. The full truth table is shown in Figure 23. Figure 20 shows the DIVOUT section in block diagram form.

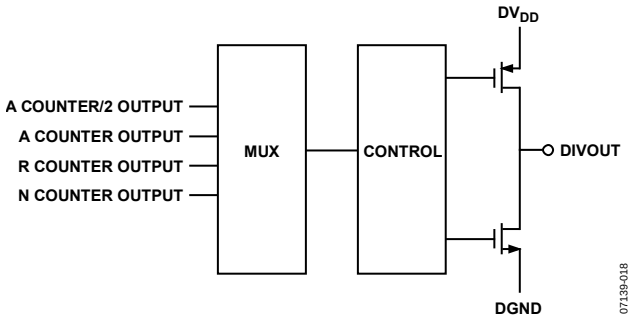

Figure 20. DIVOUT Circuit

The primary use of this pin is to derive the lower frequencies from the VCO by programming various divider values to the auxiliary A divider. Values ranging from 2 to 31 are possible. The duty cycle of this output is 1/A times 100%, with the logic high pulse width equal to the inverse of the VCO frequency. That is,

$$Pulse\ Width\ (\text{seconds}) = 1/f_{VCO}\ (\text{Frequency (Hz)})$$

See Figure 21 for a graphical description. By selecting the divide-by-2 function, this divided down frequency can in turn be divided by 2 again. This provides a 50% duty cycle in contrast to the A counter output, which may be more suitable for some applications (see Figure 21).

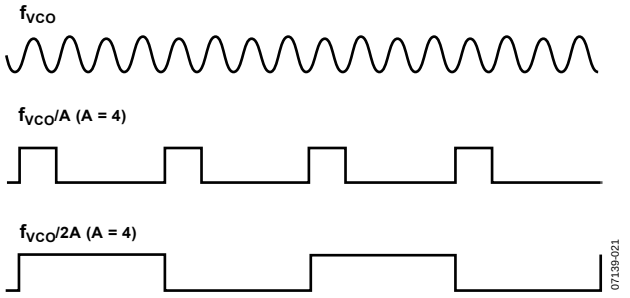

Figure 21. DIVOUT Waveforms

LATCH STRUCTURE

Figure 22 shows the three on-chip latches for the ADF4360-9. The two LSBs decide which latch is programmed.

CONTROL LATCH

RESERVED	RESERVED	POWER-DOWN 2	POWER-DOWN 1	CURRENT SETTING 2			CURRENT SETTING 1			OUTPUT POWER LEVEL		MUTE-TILL-LD	CP GAIN	CP THREE-STATE	PHASE DETECTOR POLARITY	DIVOUT CONTROL			COUNTER RESET	CORE POWER LEVEL		CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RSV	RSV	PD2	PD1	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	PL2	PL1	MTLD	CPG	CP	PDP	D3	D2	D1	CR	PC2	PC1	C2 (0)	C1 (0)

N COUNTER LATCH

RESERVED	RESERVED	CP GAIN	13-BIT B COUNTER													RESERVED	5-BIT DIVOUT					CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RSV	RSV	CPG	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	RSV	A5	A4	A3	A2	A1	C2 (1)	C1 (0)

R COUNTER LATCH

RESERVED	RESERVED	BAND SELECT CLOCK		TEST MODE BIT	LOCK DETECT PRECISION	ANTI-BACKLASH PULSE WIDTH		14-BIT REFERENCE COUNTER														CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RSV	RSV	BSC2	BSC1	TMB	LDP	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (1)

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Figure 22. Latch Structure

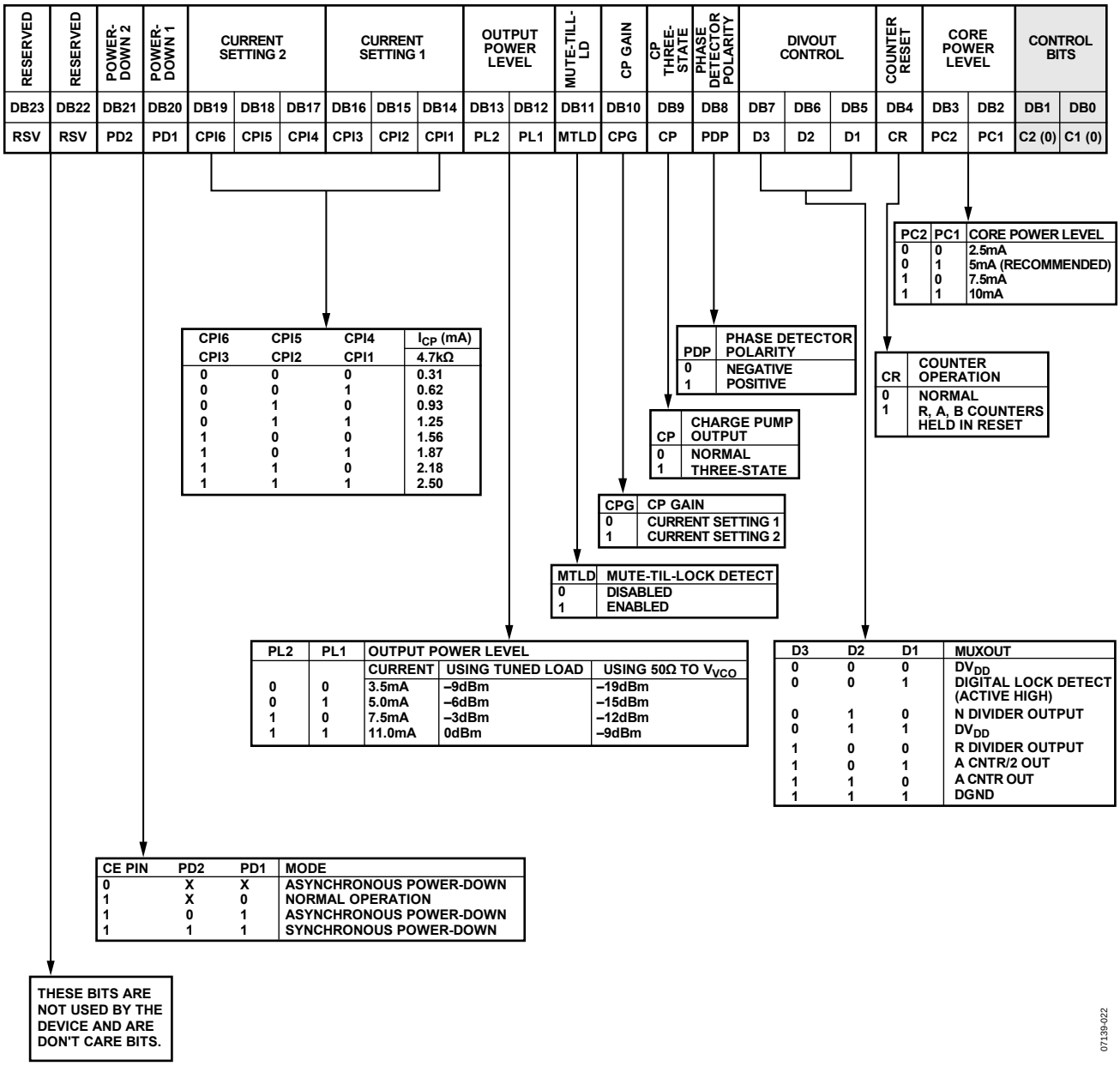


Figure 23. Control Latch

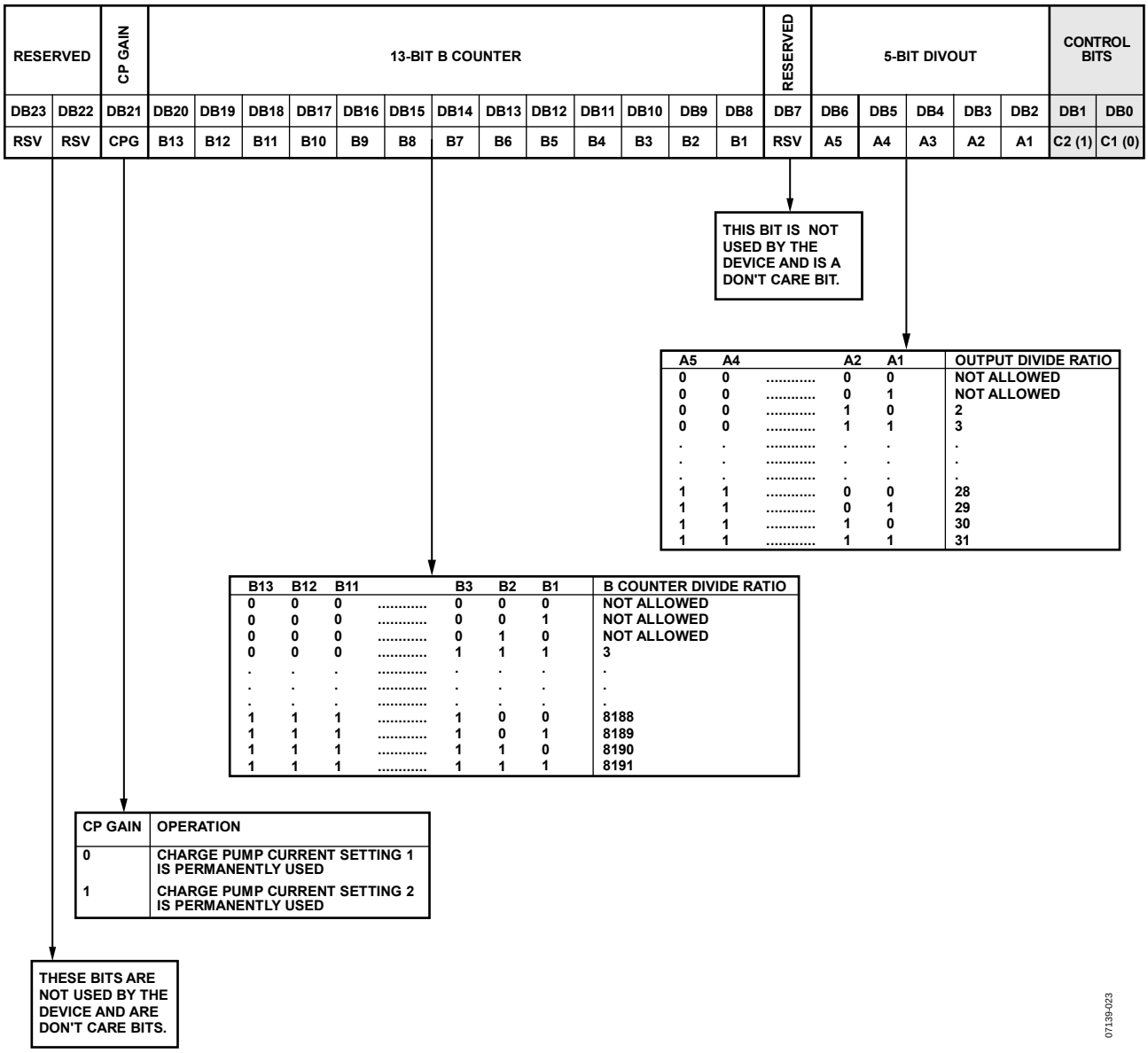


Figure 24. N Counter Latch

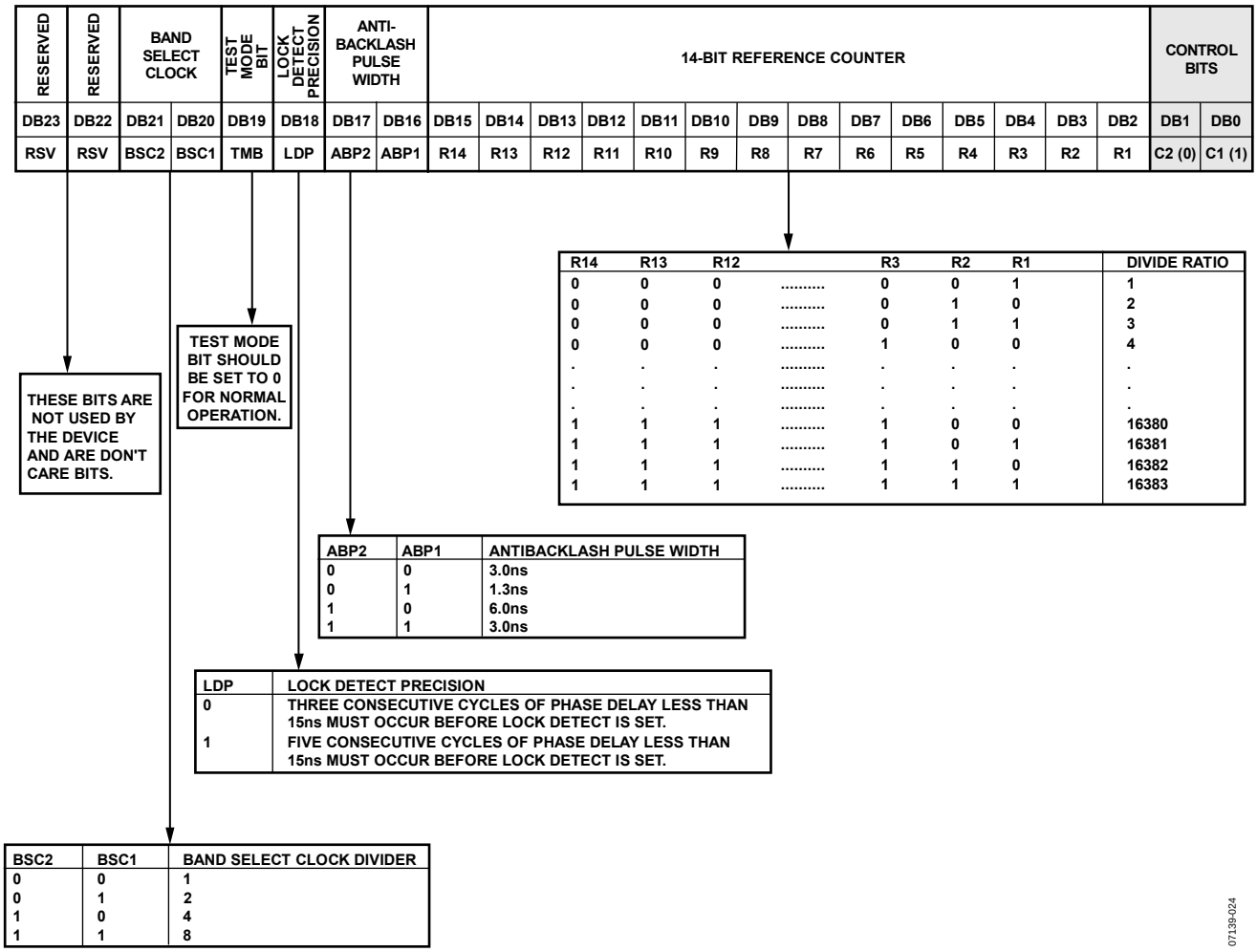


Figure 25. R Counter Latch

POWER-UP

Power-Up Sequence

The correct programming sequence for the ADF4360-9 after power-up is as follows:

1. R Counter Latch
2. Control Latch
3. N Counter Latch

Initial Power-Up

Initial power-up refers to programming the device after the application of voltage to the AV_{DD}, DV_{DD}, and V_{VCO} pins. On initial power-up, an interval is required between programming the control latch and programming the N counter latch. This interval is necessary to allow the transient behavior of the ADF4360-9 during initial power-up to settle.

During initial power-up, a write to the control latch powers up the device, and the bias currents of the VCO begin to settle. If these currents have not settled to within 10% of their steady-state value, and if the N counter latch is then programmed, the VCO may not oscillate at the desired frequency, which does not allow the band select logic to choose the correct frequency band, and the ADF4360-9 may not achieve lock. If the recommended interval is inserted, and the N counter latch is programmed, the band select logic can choose the correct frequency band, and the device locks to the correct frequency.

The duration of this interval is affected by the value of the capacitor on the C_N pin (Pin 14). This capacitor is used to reduce the close-in noise of the ADF4360-9 VCO. The recommended value of this capacitor is 10 µF. Using this value requires an interval of ≥15 ms between the latching in of the control latch bits and latching in of the N counter latch bits. If a shorter delay is required, the capacitor can be reduced. A slight phase noise penalty is incurred by this change, which is further explained in Table 6.

Table 6. C_N Capacitance vs. Interval and Phase Noise

C_N Value	Recommended Interval Between Control Latch and N Counter Latch	Open-Loop Phase Noise at 10 kHz Offset		
		L1 and L2 = 18.0 nH	L1 and L2 = 110.0 nH	L1 and L2 = 560.0 nH
10 µF	≥15 ms	−100 dBc/Hz	−97 dBc/Hz	−99 dBc/Hz
440 nF	≥600 µs	−99 dBc/Hz	−96 dBc/Hz	−98 dBc/Hz

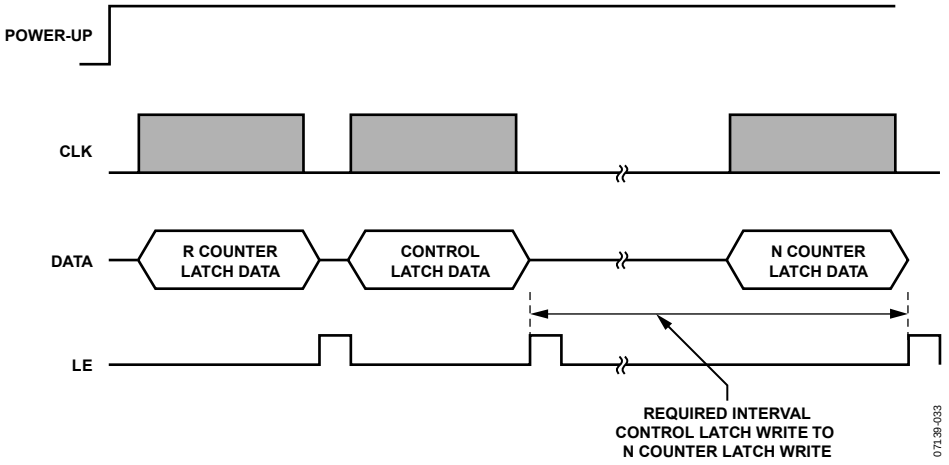


Figure 26. Power-Up Timing

Software Power-Up/Power-Down

If the device is powered down via the software (using the control latch) and powered up again without any change to the N counter latch during power-down, the device locks at the correct frequency because the device is already in the correct frequency band. The lock time depends on the value of capacitance on the C_N pin, which is <15 ms for 10 μF capacitance. The smaller capacitance of 440 nF on this pin enables lock times of <600 μs.

The N counter value cannot be changed while the device is in power-down because the device may not lock to the correct frequency on power-up. If it is updated, the correct programming sequence for the device after power-up is to the R counter latch, followed by the control latch, and finally the N counter latch, with the required interval between the control latch and N counter latch, as described in the Initial Power-Up section.

CONTROL LATCH

With (C2, C1) = (0, 0), the control latch is programmed. Figure 23 shows the input data format for programming the control latch.

Power-Down

DB21 (PD2) and DB20 (PD1) provide programmable power-down modes.

In the programmed asynchronous power-down, the device powers down immediately after latching a 1 into Bit PD1, with the condition that PD2 is loaded with a 0. In the programmed synchronous power-down, the device power-down is gated by the charge pump to prevent unwanted frequency jumps. Once the power-down is enabled by writing a 1 into Bit PD1 (on the condition that a 1 is also loaded in PD2), the device goes into power-down on the second rising edge of the R counter output, after LE goes high. When a power-down is activated (either synchronous or asynchronous mode), the following events occur:

- All active dc current paths are removed.
- The R, N, and timeout counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital lock detect circuitry is reset.
- The RF outputs are debiased to a high impedance state.
- The reference input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

Charge Pump Currents

CPI3, CPI2, and CPI1 in the ADF4360-9 determine Current Setting 1. CPI6, CPI5, and CPI4 determine Current Setting 2 (see the truth table in Figure 23).

Output Power Level

Bit PL1 and Bit PL2 set the output power level of the VCO (see the truth table in Figure 23).

Mute-Till-Lock Detect

DB11 of the control latch in the ADF4360-9 is the mute-till-lock detect bit. This function, when enabled, ensures that the RF outputs are not switched on until the PLL is locked.

CP Gain

DB10 of the control latch in the ADF4360-9 is the charge pump gain bit. When it is programmed to 1, Current Setting 2 is used. When programmed to 0, Current Setting 1 is used.

Charge Pump Three-State

This bit (DB9) puts the charge pump into three-state mode when programmed to a 1. For normal operation, it should be set to 0.

Phase Detector Polarity

The PDP bit in the ADF4360-9 sets the phase detector polarity. The positive setting enabled by programming a 1 is used when using the on-chip VCO with a passive loop filter or with an active noninverting filter. It can also be set to 0, which is required if an active inverting loop filter is used.

DIVOUT Control

The on-chip multiplexer is controlled by D3, D2, and D1 (see the truth table in Figure 23).

Counter Reset

DB4 is the counter reset bit for the ADF4360-9. When this is 1, the R counter and the A, B counters are reset. For normal operation, this bit should be 0.

Core Power Level

PC1 and PC2 set the power level in the VCO core. The recommended setting is 5 mA. The 7.5 mA setting is permissible in some applications (see the truth table in Figure 23).

N COUNTER LATCH

Figure 24 shows the input data format for programming the N counter latch.

5-Bit Divider

A5 to A1 program the output divider. The divide range is 2 (00010) to 31 (11111). If unused, this divider should be set to 0. The output or the output divided by 2 is available at the DIVOUT pin.

Reserved Bits

DB23, DB22, and DB7 are spare bits and are designated as reserved. They should be programmed to 0.

B Counter Latch

B13 to B1 program the B counter. The divide range is 3 (00 … 0011) to 8191 (11 … 111).

Overall Divide Range

The overall VCO feedback divide range is defined by B.

CP Gain

DB21 of the N counter latch in the ADF4360-9 is the charge pump gain bit. When it is programmed to 1, Current Setting 2 is used. When programmed to 0, Current Setting 1 is used. This bit can also be programmed through DB10 of the control latch. The bit always reflects the latest value written to it, whether this is through the control latch or the N counter latch.

R COUNTER LATCH

With (C2, C1) = (0, 1), the R counter latch is programmed. Figure 25 shows the input data format for programming the R counter latch.

R Counter

R1 to R14 set the counter divide ratio. The divide range is 1 (00 … 001) to 16,383 (111 … 111).

Antibacklash Pulse Width

DB16 and DB17 set the antibacklash pulse width.

Lock Detect Precision

DB18 is the lock detect precision bit. This bit sets the number of reference cycles with <15 ns phase error for entering the locked state. With LDP at 1, five cycles are taken; with LDP at 0, three cycles are taken.

Test Mode Bit

DB19 is the test mode bit (TMB) and should be set to 0. With TMB = 0, the contents of the test mode latch are ignored and normal operation occurs, as determined by the contents of the control latch, R counter latch, and N counter latch. Note that test modes are for factory testing only and should not be programmed by the user.

Band Select Clock

These bits (DB20 and DB21) set a divider for the band select logic clock input. The output of the R counter is, by default, the value used to clock the band select logic; if this value is too high (>1 MHz), a divider can be switched on to divide the R counter output to a smaller value (see Figure 25). A value of 8 is recommended.

Reserved Bits

DB23 to DB22 are spare bits that are designated as reserved. They should be programmed to 0.

APPLICATIONS INFORMATION

CHOOSING THE CORRECT INDUCTANCE VALUE

The ADF4360-9 can be used at many different frequencies simply by choosing the external inductors to give the correct output frequency. Figure 27 shows a graph of both minimum and maximum frequency vs. the external inductor value. The correct inductor should cover the maximum and minimum frequencies desired. The inductors used are 0603 CS or 0805 CS type from Coilcraft. To reduce mutual coupling, the inductors should be placed at right angles to one another.

The lowest center frequency of oscillation possible is approximately 65 MHz, which is achieved using 560 nH inductors. This relationship can be expressed by

$$f_O = \frac{1}{2\pi\sqrt{9.3\ \text{pF}(0.9\ \text{nH} + L_{EXT})}}$$

where:
f_O is the center frequency.
L_{EXT} is the external inductance.

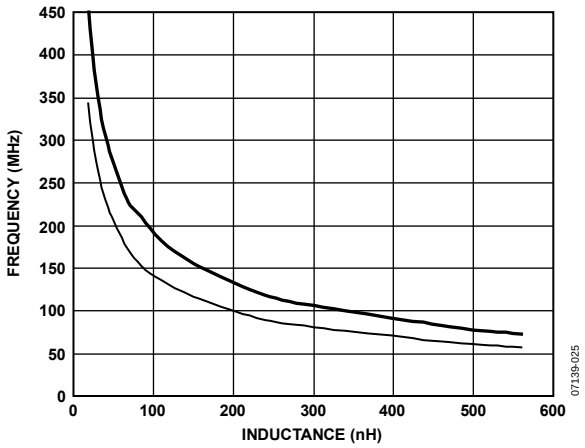


Figure 27. Output Center Frequency vs. External Inductor Value

The approximate value of capacitance at the midpoint of the center band of the VCO is 9.3 pF, and the approximate value of internal inductance due to the bond wires is 0.9 nH. The VCO sensitivity is a measure of the frequency change vs. the tuning voltage. It is a very important parameter for the low-pass filter. Figure 28 shows a graph of the tuning sensitivity (in MHz/V) vs. the inductance (nH). It can be seen that as the inductance increases, the sensitivity decreases. This relationship can be derived from the previous equation; that is, because the inductance increased, the change in capacitance from the varactor has less of an effect on the frequency.

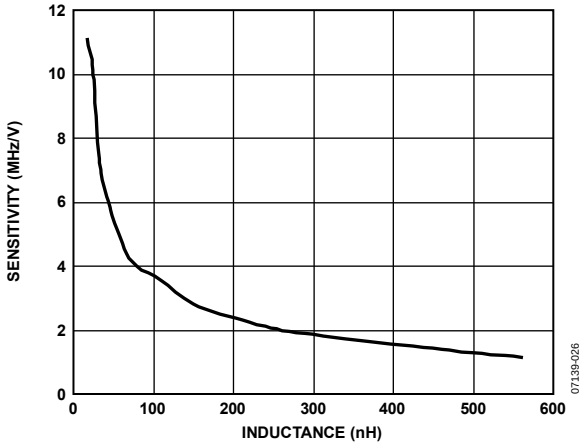


Figure 28. Tuning Sensitivity vs. Inductance

ENCODE CLOCK FOR ADC

Analog-to-digital converters (ADCs) require a sampling clock for their operation. Generally, this is provided by TCXO or VCXOs, which can be large and expensive. The frequency range is usually quite limited. An alternative solution is the ADF4360-9, which can be used to generate a CMOS clock signal suitable for use in all but the most demanding converter applications.

Figure 29 shows an ADF4360-9 with a VCO frequency of 320 MHz and a DIVOUT frequency of 80 MHz. Because a 50% duty cycle is preferred by most sampling clock circuitry, the A/2 mode is selected. Therefore, A is programmed to 2, giving an overall divide value of 4. The AD9215-80 is a 10-bit, 80 MSPS ADC that requires an encode clock jitter of 6 ps or less. The ADF4360-9 takes a 10 MHz TCXO frequency and divides this to 1 MHz; therefore, R = 10 is programmed and N = 320 is programmed to achieve a VCO frequency of 320 MHz. The resultant 80 MHz CMOS signal has a jitter of <1.5 ps, which is more than adequate for the application.

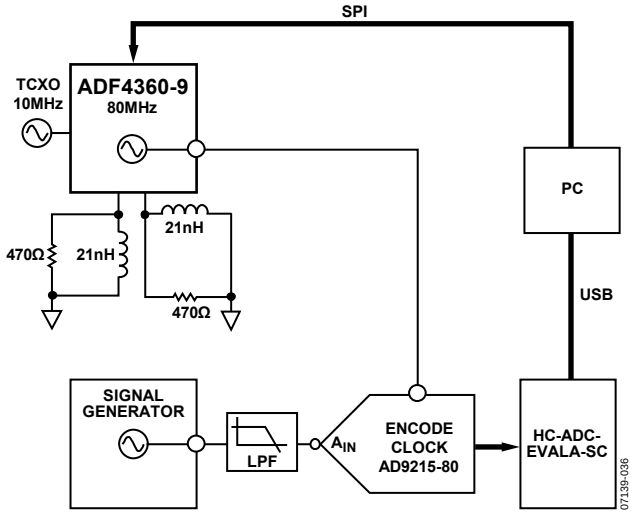


Figure 29. The ADF4360-9 Used as an Encode Clock for an ADC

GSM TEST CLOCK

Figure 30 shows the ADF4360-9 used to generate three different frequencies at DIVOUT. The frequencies required are 45 MHz, 80 MHz, and 95 MHz. This is achieved by generating 360 MHz, 320 MHz, and 380 MHz and programming the correct A divider ratio. Because a 50% duty cycle is required, the A/2 DIVOUT mode is selected. This means that A values of 4, 2, and 2 are selected, respectively, for each of the output frequencies previously mentioned.

The low-pass filter was designed using ADIsimPLL™ for a channel spacing of 1 MHz and an open-loop bandwidth of 40 kHz. Larger PFD frequencies can be used to reduce in-band noise and, therefore, rms jitter. However, for the purposes of this example, 1 MHz is used. The measured rms jitter from this circuit at each frequency is less than 1.5 ps.

Two 21 nH inductors are required for the specified frequency range. The reference frequency is from a 20 MHz TCXO from Fox; therefore, an R value of 20 is programmed. Taking into account the high PFD frequency and its effect on the band select logic, the band select clock divider is enabled. In this case, a value of 8 is chosen. A very simple shunt resistor and dc-blocking capacitor complete the RF output stage. Because these outputs are not used, they are terminated in 50 Ω resistors. This is recommended for circuit stability. Leaving the RF outputs open is not recommended.

The CMOS level output frequency is available at DIVOUT. If the frequency has to drive a low impedance load, a buffer is recommended.

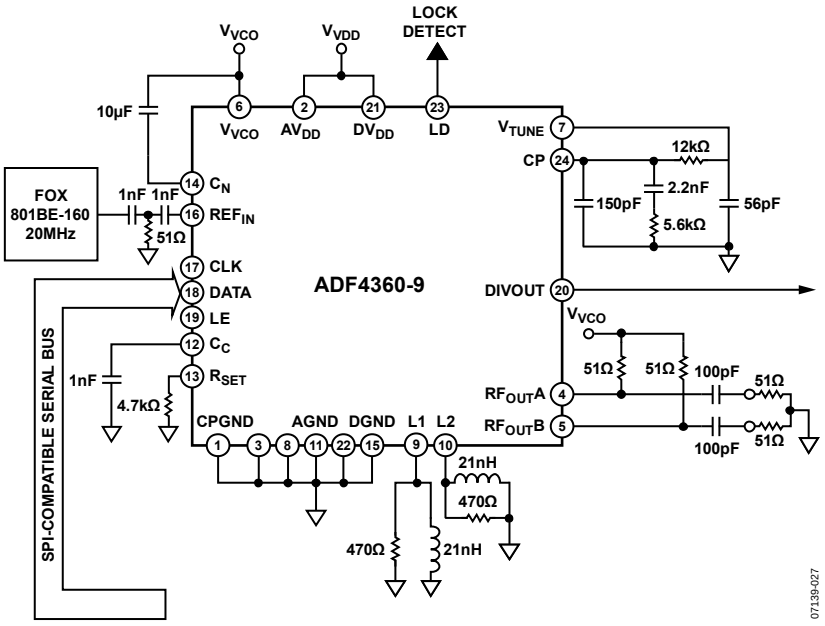


Figure 30.GSM Test Clock

INTERFACING

The ADF4360-9 has a simple SPI-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When LE goes high, the 24 bits that are clocked into the appropriate register on each rising edge of CLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 5 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible is 833 kHz, or one update every 1.2 µs. This is more than adequate for systems that have typical lock times in hundreds of microseconds.

ADuC812 Interface

Figure 31 shows the interface between the ADF4360-9 and the ADuC812 MicroConverter®. Because the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontrollers. The MicroConverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4360-9 needs a 24-bit word, which is accomplished by writing three 8-bit bytes from the MicroConverter to the device. After the third byte is written, the LE input should be brought high to complete the transfer.

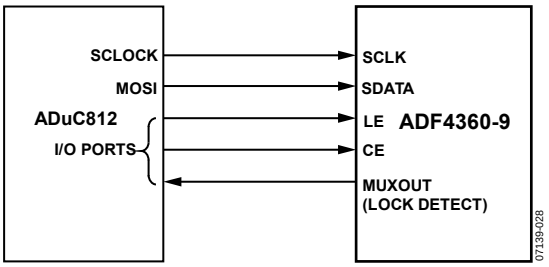


Figure 31. ADuC812 to ADF4360-9 Interface

I/O port lines on the ADuC812 are used to detect lock (MUXOUT configured as lock detect and polled by the port input). When operating in the described mode, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 166 kHz.

ADSP-2181 Interface

Figure 32 shows the interface between the ADF4360-9 and the ADSP-2181 digital signal processor. The ADF4360-9 needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the ADSP-2181 is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated.

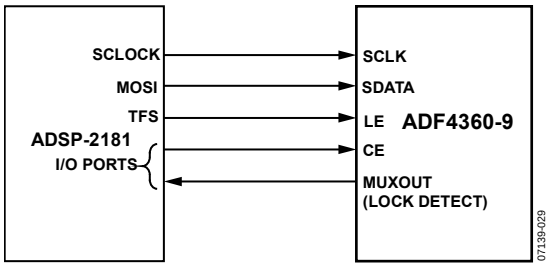


Figure 32. ADSP-2181 to ADF4360-9 Interface

Set up the word length for 8 bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the 8-bit bytes, enable the autobuffered mode, and write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The leads on the chip scale package (CP-24-2) are rectangular. The printed circuit board (PCB) pad for these should be 0.1 mm longer than the package lead length and 0.05 mm wider than the package lead width. The lead should be centered on the pad to ensure that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the PCB should be at least as large as this exposed pad. On the PCB, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern to ensure that shorting is avoided.

Thermal vias can be used on the PCB thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated into the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 ounce of copper to plug the via.

The user should connect the printed circuit thermal pad to AGND. This is internally connected to AGND.

OUTPUT MATCHING

There are a number of ways to match the VCO output of the ADF4360-9 for optimum operation; the most basic is to use a 51 Ω resistor to V_{VCO}. A dc bypass capacitor of 100 pF is connected in series, as shown in Figure 33. Because the resistor is not frequency dependent, this provides a good broadband match. The output power in the circuit in Figure 33 typically gives −9 dBm output power into a 50 Ω load.

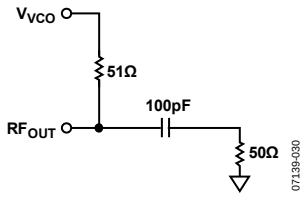


Figure 33. Simple Output Stage

A better solution is to use a shunt inductor (acting as an RF choke) to V_{VCO}. This gives a better match and, therefore, more output power.

Experiments have shown that the circuit shown in Figure 34 provides an excellent match to 50 Ω over the operating range of the ADF4360-9. This gives approximately 0 dBm output power across the specific frequency range of the ADF4360-9 using the recommended shunt inductor, followed by a 100 pF dc-blocking capacitor.

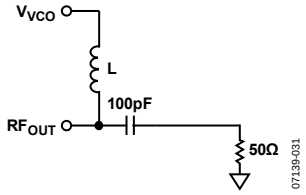


Figure 34. Optimum Output Stage

The recommended value of this inductor changes with the VCO center frequency. Figure 35 shows a graph of the optimum inductor value vs. center frequency.

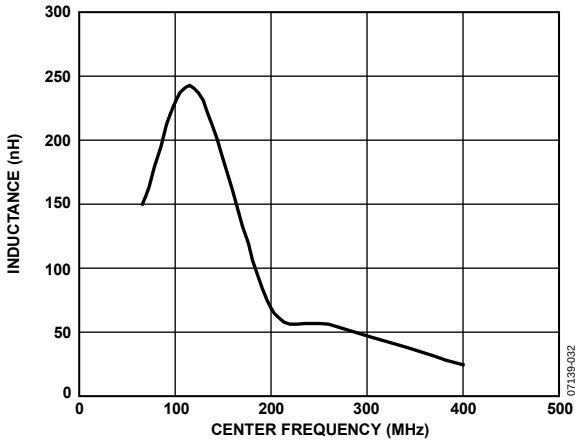
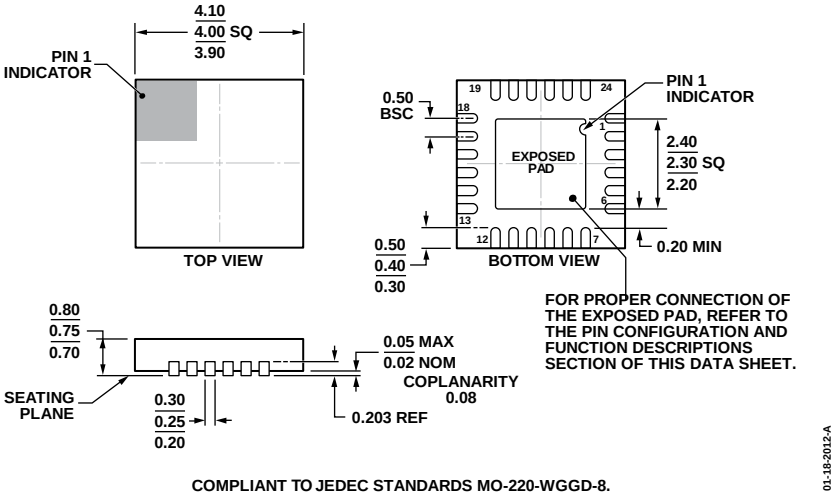


Figure 35. Optimum Shunt Inductor vs. Center Frequency

Both complementary architectures can be examined using the EV-ADF4360-9EB1Z evaluation board. If the user does not need the differential outputs available on the ADF4360-9, the user should either terminate the unused output with the same circuitry as much as possible or combine both outputs using a balun. Alternatively, instead of the LC balun, both outputs can be combined using a 180° rat-race coupler.

If the user is only using DIVOUT and does not use the RF outputs, it is still necessary to terminate both RF output pins with a shunt inductor/resistor to V_{VCO} and also a dc bypass capacitor and a 50 Ω load. The circuit in Figure 33 is probably the simplest and most cost-effective solution. It is important that the load on each pin be balanced because an unbalanced load is likely to cause stability problems. Terminations should be identical as much as possible.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8.

Figure 36. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Frequency Range	Package Option
ADF4360-9BCPZ	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	65 MHz to 400 MHz	CP-24-14
ADF4360-9BCPZRL	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	65 MHz to 400 MHz	CP-24-14
ADF4360-9BCPZRL7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	65 MHz to 400 MHz	CP-24-14
EV-ADF4360-9EB1Z		Evaluation Board		

[1] Z = RoHS Compliant Part.