

AUDIO DIFFERENTIAL LINE RECEIVER 0dB (G = 1)

Check for Samples: [INA2134-EP](#)

FEATURES

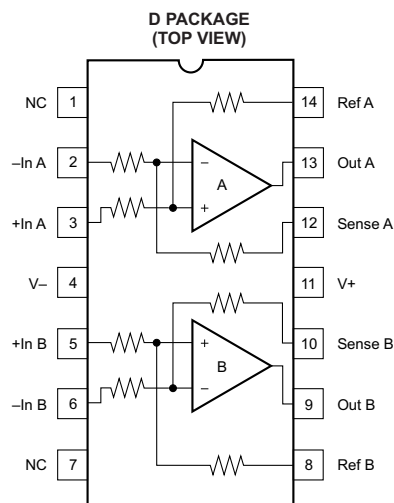
- Single and Dual Versions
- Low Distortion: 0.0005% at $f = 1$ kHz
- High Slew Rate: 14 V/ms
- Fast Settling Time: 3 ms to 0.01%
- Wide Supply Range: ± 4 V to ± 18 V
- Low Quiescent Current: 3.1 mA max
- High CMRR: 90 dB
- Fixed Gain = 0 dB (1V/V)
- Dual 14-Pin SOIC Package

APPLICATIONS

- Audio Differential Line Receiver
- Summing Amplifier
- Unity-Gain Inverting Amplifier
- Psuedoground Generator
- Instrumentation Building Block
- Current Shunt Monitor
- Voltage-Controlled Current Source
- Ground Loop Eliminator

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military ($-55^{\circ}\text{C}/125^{\circ}\text{C}$) Temperature Range⁽¹⁾
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability



NC = No Connection

(1) Additional temperature ranges available - contact factory

DESCRIPTION

The INA2134 is a differential line receiver consisting of high performance op amps with onchip precision resistors. The device is fully specified for high performance audio applications and has excellent ac specifications, including low distortion (0.0005% at 1 kHz) and high slew rate (14 V/ms), assuring good dynamic response. In addition, wide output voltage swing and high output drive capability allow use in a wide variety of demanding applications. The dual version features completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

The INA2134 on-chip resistors are laser trimmed for accurate gain and optimum common-mode rejection. Furthermore, excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. Operation is guaranteed from ± 4 V to ± 18 V (8-V to 36-V total supply).

The INA2134 comes in a 14-pin SOIC surface-mount package and is specified for operation over the military temperature range, -55°C to 125°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



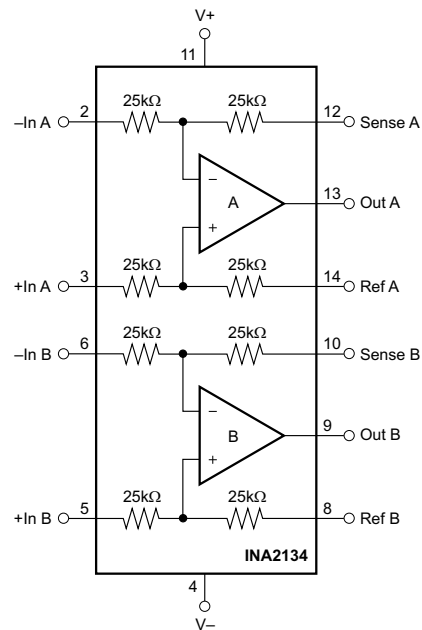
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE	TOP-SIDE MARKING	ORDERABLE PART NUMBER	VID NUMBER	TRANSPORT MEDIA
–55°C to 125°C	SOIC-14 – D	INA2134M	INA2134MDREP	V62/12613-01XE	Tape and Reel, large
			INA2134MDEP	V62/12613-02XE	Tube

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	VALUE	UNIT
Supply voltage, V+ to V-	40	V
Input voltage range	±80	V
Output short-circuit (to ground) ⁽²⁾	Continuous	
Operating temperature	–55 to 125	°C
Storage temperature	–65 to 150	°C
Junction temperature	150	°C
Lead temperature (soldering, 10 s)	300	°C
ESD Rating	Human Body Model (HBM)	500 V
	Machine Model (MM)	100 V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) One channel per package.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		INA2134	UNITS
		D	
		14 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	73.1	°C/W
θ_{JC}	Junction-to-case thermal resistance	31.1	
θ_{JB}	Junction-to-board thermal resistance ⁽³⁾	27.6	
ψ_{JT}	Junction-to-top characterization parameter ⁽⁴⁾	3.2	
ψ_{JB}	Junction-to-board characterization parameter ⁽⁵⁾	27.3	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (4) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (5) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $R_L = 2\text{ k}\Omega$, and Ref pin connected to Ground (unless otherwise noted).

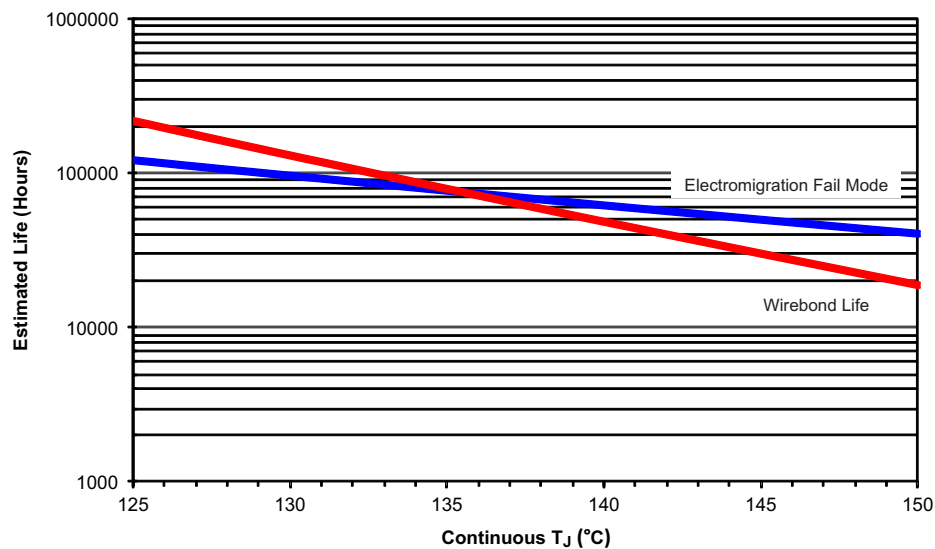
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE					
Total harmonic distortion + noise, $f = 1\text{ kHz}$	$V_{IN} = 10\text{ Vrms}$		0.0005		%
Noise floor ⁽¹⁾	20 kHz BW		-100		dBu
Headroom ⁽¹⁾	THD+N < 1%		23		dBu
FREQUENCY RESPONSE					
Small-signal bandwidth			3.1		MHz
Slew rate			14		V/ μs
Settling time: 0.1%	10-V step, $C_L = 100\text{ pF}$		2		μs
0.01%	10-V step, $C_L = 100\text{ pF}$		3		μs
Overload recovery time	50% overdrive		3		μs
Channel separation (dual), $f = 1\text{ kHz}$			117		dB
OUTPUT NOISE VOLTAGE⁽²⁾					
$f = 20\text{ Hz to } 20\text{ kHz}$			7		μVrms
$f = 1\text{ kHz}$			52		$\text{nV}/\sqrt{\text{Hz}}$
OFFSET VOLTAGE⁽³⁾					
Input offset voltage	$V_{CM} = 0\text{ V}$		± 100	± 1000	μV
vs Temperature	$-55^\circ\text{C to } 125^\circ\text{C}$		± 2		$\mu\text{V}/^\circ\text{C}$
vs Power supply	$V_S = \pm 4\text{ V to } \pm 18\text{ V}, -55^\circ\text{C to } 125^\circ\text{C}$		± 5	± 60	$\mu\text{V/V}$
INPUT					
Common-mode voltage range: Positive	$V_O = 0\text{ V}$	$2(V+) - 5$	$2(V+) - 4$		V
Negative	$V_O = 0\text{ V}$	$2(V-) + 5$	$2(V-) + 2$		V
Differential voltage range		See Typical Curve			
Common-mode rejection	$V_{CM} = \pm 31\text{ V}, R_S = 0\text{ }\Omega$	74	90		dB
	$V_{CM} = \pm 31\text{ V}, R_S = 0\text{ }\Omega, -55^\circ\text{C to } 125^\circ\text{C}$	72	85		dB
Impedance: ⁽⁴⁾ Differential			50		k Ω
Common-mode			50		k Ω

- (1) $\text{dBu} = 20\log(\text{Vrms}/0.7746)$.
- (2) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.
- (3) Includes effects of amplifier's input bias and offset currents.
- (4) 25-k Ω resistors are ratio matched, but have $\pm 25\%$ absolute value.

ELECTRICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $R_L = 2\text{ k}\Omega$, and Ref pin connected to Ground (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAIN						
Initial				1		V/V
Error		$V_O = -16\text{ V to }16\text{ V}$		± 0.02	± 0.1	%
	vs Temperature	$V_O = -16\text{ V to }16\text{ V}, -55^\circ\text{C to }125^\circ\text{C}$		± 2	± 3.5	%
	Nonlinearity	$V_O = -16\text{ V to }16\text{ V}$		0.0001		%
OUTPUT						
Voltage output:	Positive	Specified temperature range	$(V+) - 2$	$(V+) - 1.8$		V
	Negative		$(V-) + 2$	$(V-) + 1.6$		V
	Positive		$(V+) - 2.45$	$(V+) - 2.1$		V
	Negative		$(V-) + 2.45$	$(V-) + 1.8$		V
Current limit, continuous to common				± 60		mA
Capacitive load (stable operation)				500		pF
POWER SUPPLY						
Rated voltage				± 18		V
Voltage range			± 4		± 18	V
Quiescent current (per amplifier)		$I_O = 0\text{ A}$		± 2.4	± 2.9	mA
		$I_O = 0\text{ A}, -55^\circ\text{C to }125^\circ\text{C}$		± 2.7	± 3.1	mA
TEMPERATURE RANGE						
Specified temperature range			-55		125	$^\circ\text{C}$
Operating temperature range			-55		125	$^\circ\text{C}$
Storage temperature range			-65		150	$^\circ\text{C}$

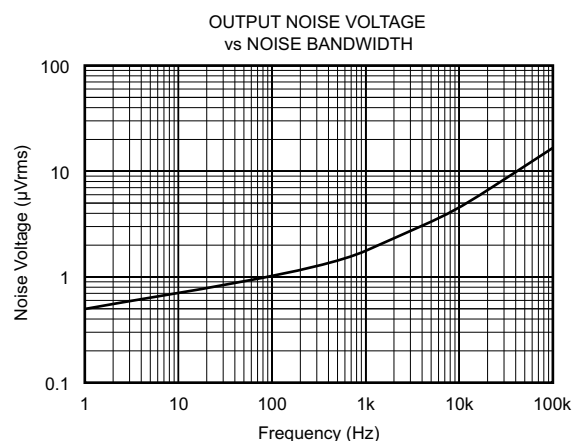
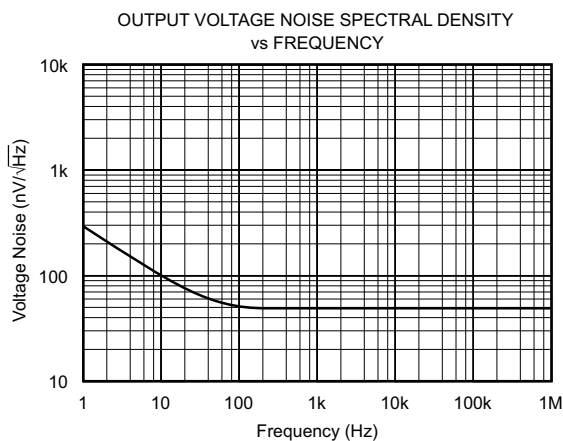
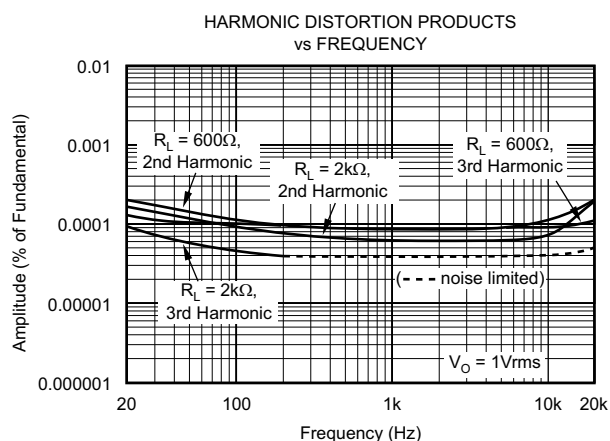
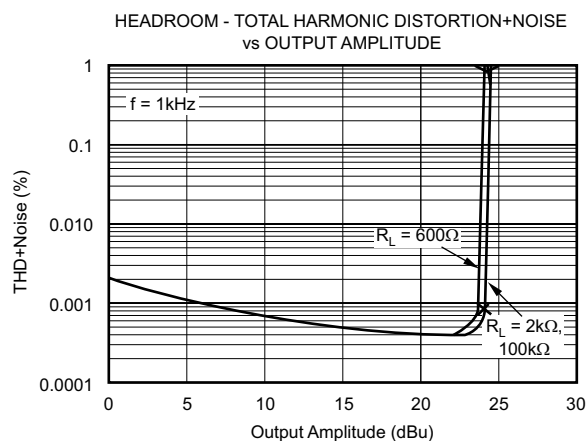
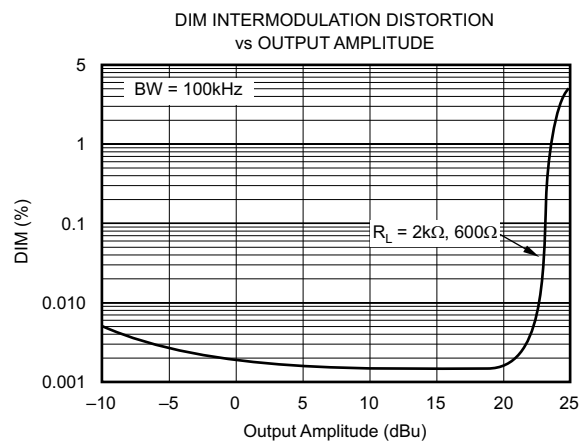
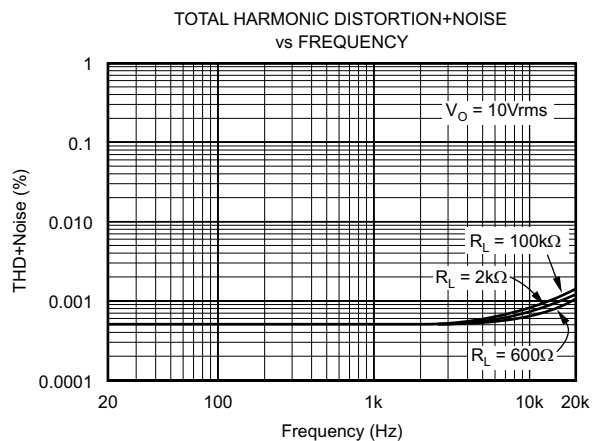


- See datasheet for absolute maximum and minimum recommended operating conditions.
- Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
- The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

Figure 1. INA2134 Electromigration Fail Mode/Wirebond Life Derating Chart

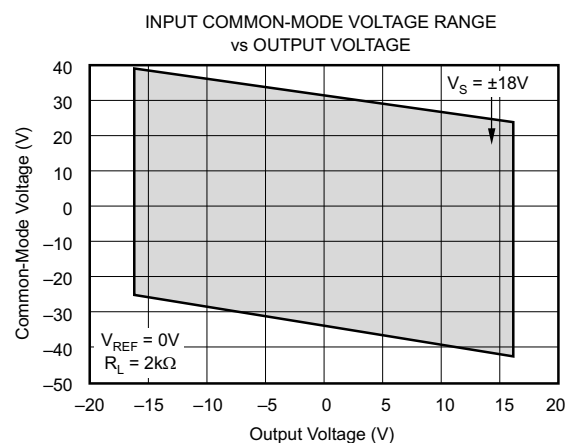
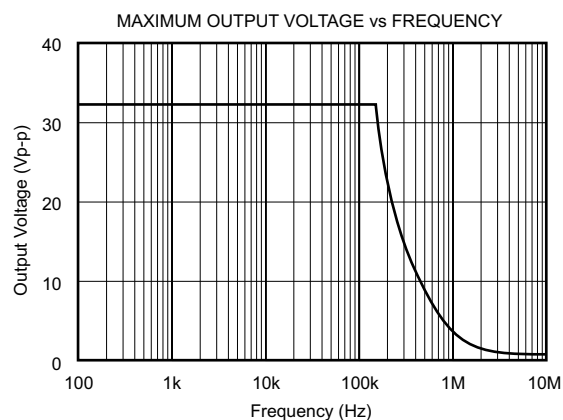
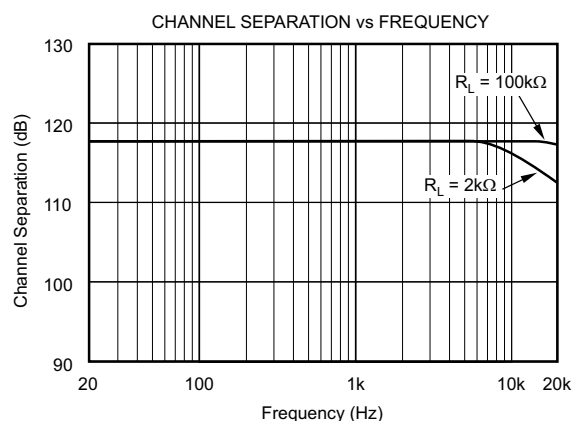
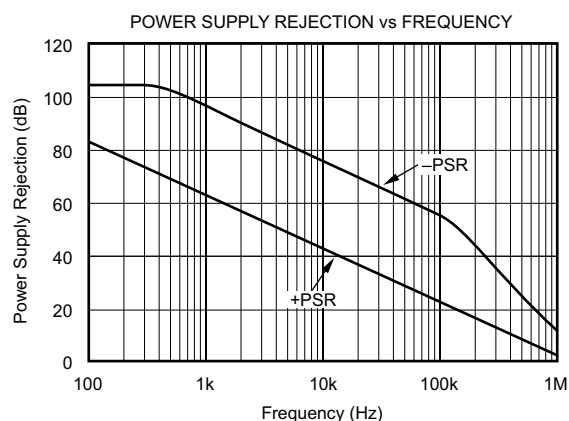
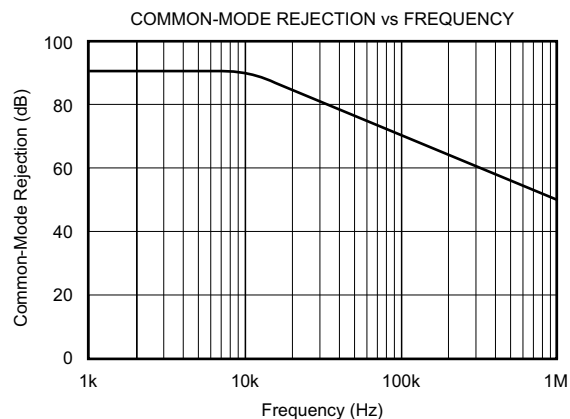
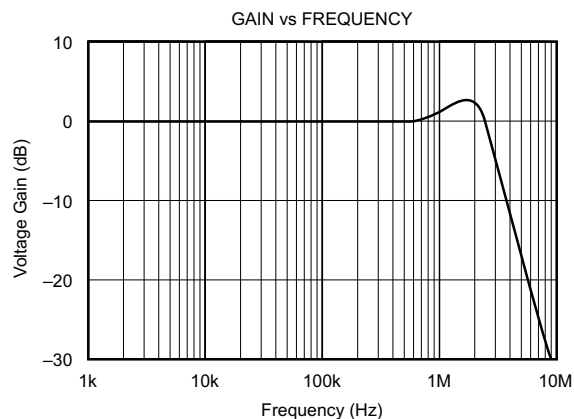
TYPICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$ (unless otherwise noted).



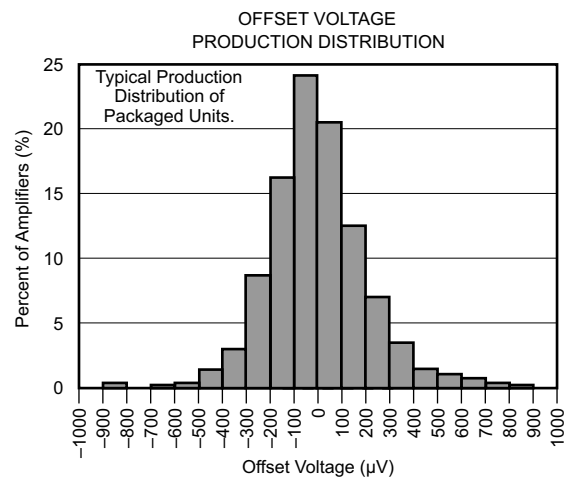
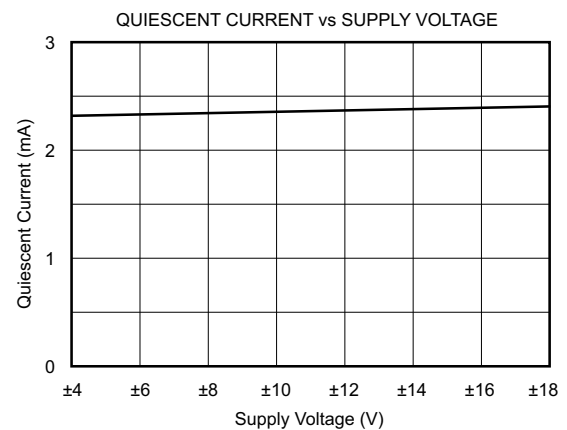
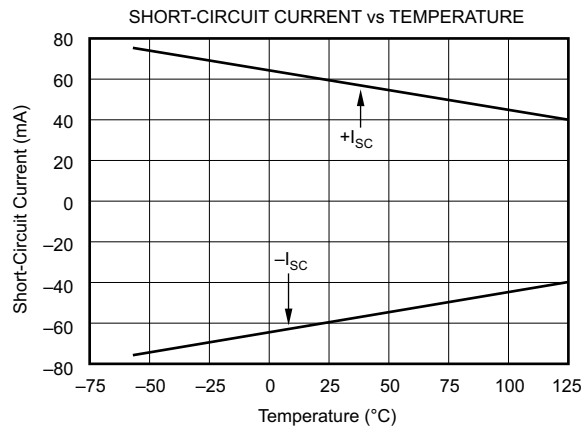
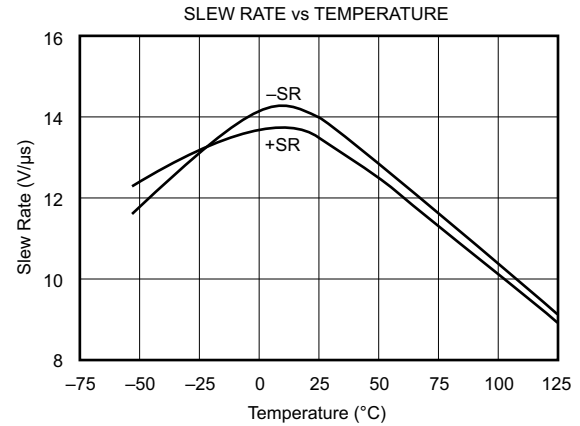
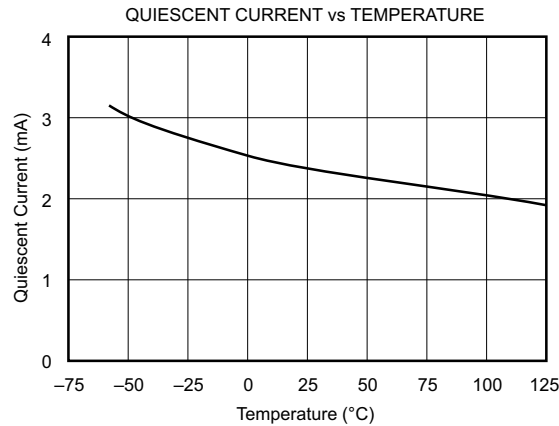
TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$ (unless otherwise noted).



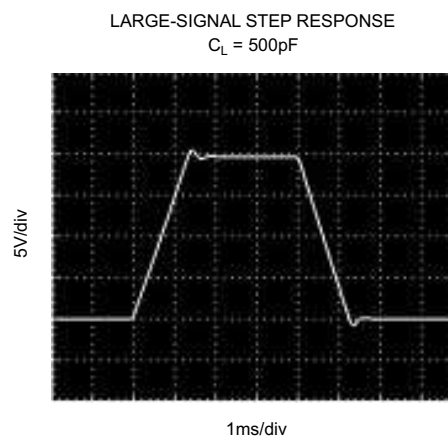
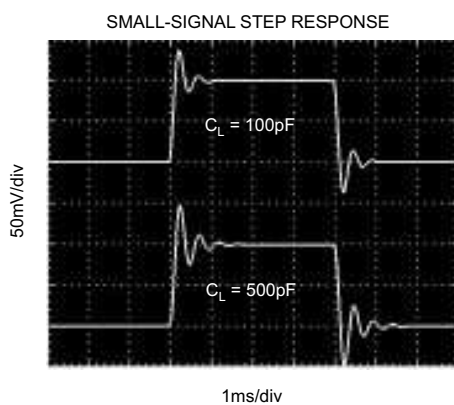
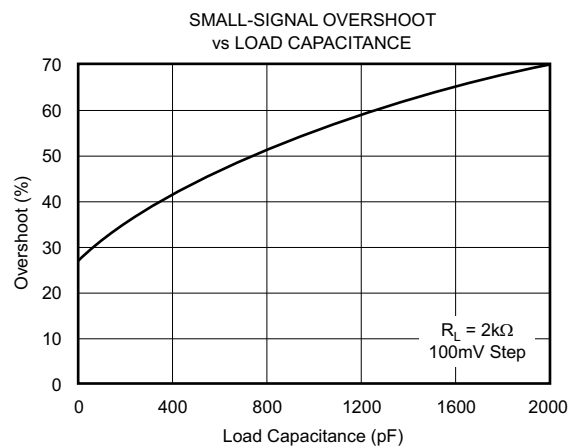
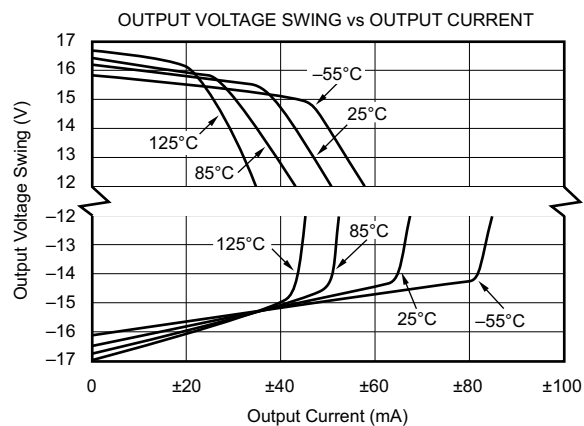
TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$ (unless otherwise noted).



TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$ (unless otherwise noted).



APPLICATION INFORMATION

Basic Connection

Figure 2 shows the basic connections required for operation of the INA2134. Decoupling capacitors are strongly recommended in applications with noisy or high impedance power supplies. The capacitors should be placed close to the device pins as shown in Figure 2. All circuitry is completely independent in the dual version assuring lowest crosstalk and normal behavior when one amplifier is overdriven or short-circuited.

As shown in Figure 2, the differential input signal is connected to pins 2 and 3. The source impedances connected to the inputs must be nearly equal to assure good common mode rejection. A 10-Ω mismatch in source impedance will degrade the common-mode rejection of a typical device to approximately 74 dB. If the source has a known impedance mismatch, an additional resistor in series with the opposite input can be used to preserve good common-mode rejection.

Do not interchange pins 1 and 3 or pins 2 and 5, even though nominal resistor values are equal. These resistors are laser trimmed for precise resistor ratios to achieve accurate gain and highest CMR. Interchanging these pins would not provide specified performance.

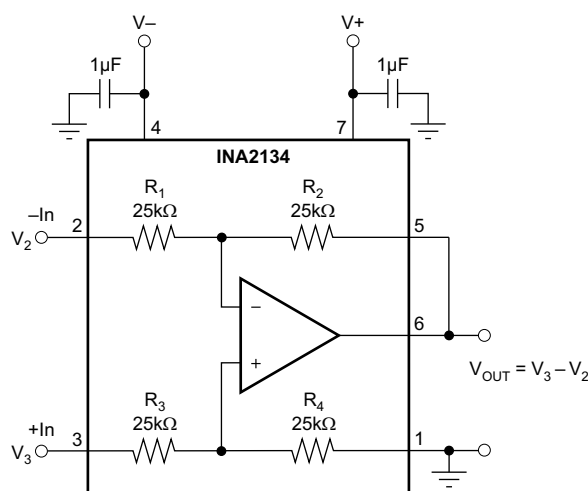


Figure 2. Precision Difference Amplifier (Basic Power Supply and Signal Connections)

Audio Performance

The INA2134 was designed for enhanced ac performance. Very low distortion, low noise, and wide bandwidth provide superior performance in high quality audio applications. Laser-trimmed matched resistors provide optimum common-mode rejection (typically 90 dB), especially when compared to circuits implemented with an operational amplifier and discrete precision resistors. In addition, high slew rate (14 V/μs) and fast settling time (3 ms to 0.01%) ensure good dynamic performance.

The INA2134 has excellent distortion characteristics. THD+Noise is below 0.002% throughout the audio frequency range. Up to approximately 10-kHz distortion is below the measurement limit of commonly used test equipment. Furthermore, distortion remains relatively flat over its wide output voltage swing range (approximately 1.7 V from either supply).

Offset Voltage Trim

The INA2134 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 3 shows an optional circuit for trimming the output offset voltage. The output is referred to the output reference terminal (pin 1), which is normally grounded. A voltage applied to the Ref terminal will be summed with the output signal. This can be used to null offset voltage as shown in Figure 3. The source impedance of a signal applied to the Ref terminal should be less than 10 Ω to maintain good common-mode rejection.

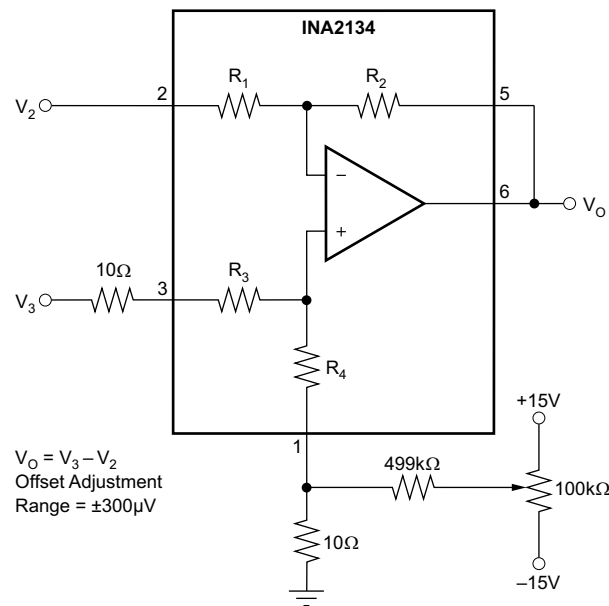


Figure 3. Offset Adjustment

Other Applications

The difference amplifier is a highly versatile building block that is useful in a wide variety of applications. See the INA105 data sheet ([SBOS145](#)) for additional applications ideas, including:

- Current Receiver with Compliance to Rails
- Precision Unity-Gain Inverting Amplifier
- $\pm 10\text{-V}$ Precision Voltage Reference
- $\pm 5\text{-V}$ Precision Voltage Reference
- Precision Unity-Gain Buffer
- Precision Average Value Amplifier
- Precision $G = 2$ Amplifier
- Precision Summing Amplifier
- Precision $G = 1/2$ Amplifier
- Precision Bipolar Offsetting
- Precision Summing Amplifier with Gain
- Instrumentation Amplifier Guard Drive Generator
- Precision Summing Instrumentation Amplifier
- Precision Absolute Value Buffer
- Precision Voltage-to-Current Converter with Differential Inputs
- Differential Input Voltage-to-Current Converter for Low I_{OUT}
- Isolating Current Source
- Differential Output Difference Amplifier
- Isolating Current Source with Buffering Amplifier for Greater Accuracy
- Window Comparator with Window Span and Window Center Inputs
- Precision Voltage-Controlled Current Source with Buffered Differential Inputs and Gain
- Digitally Controlled Gain of ± 1 Amplifier

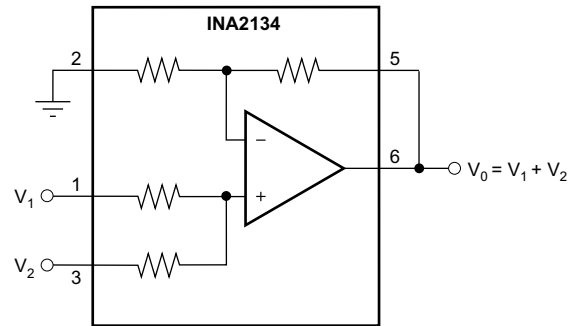


Figure 4. Precision Summing Amplifier

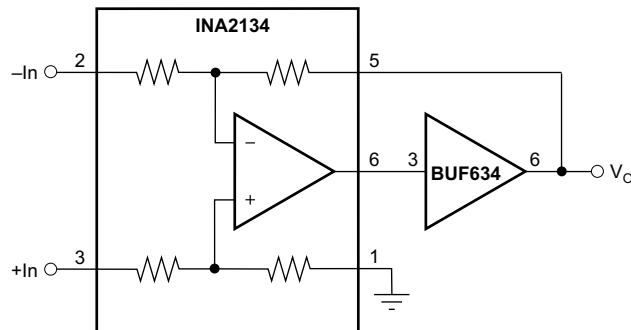


Figure 5. Boosting Output Current

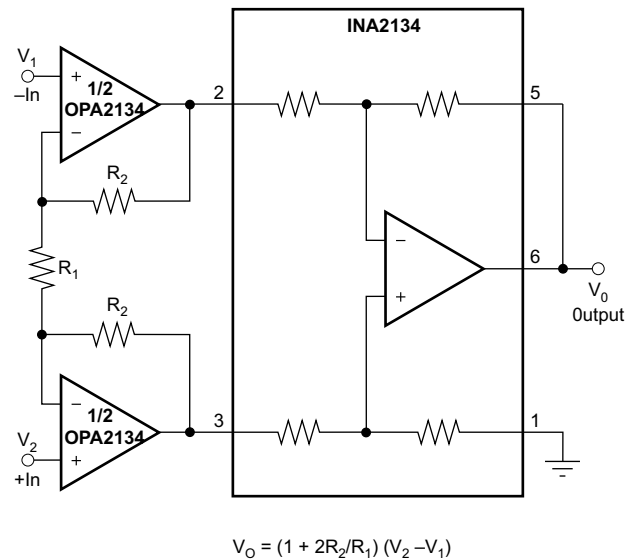


Figure 6. High Input Impedance Instrumentation Amplifier

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA2134MDREP	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	INA2134M
INA2134MDREP.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	INA2134M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

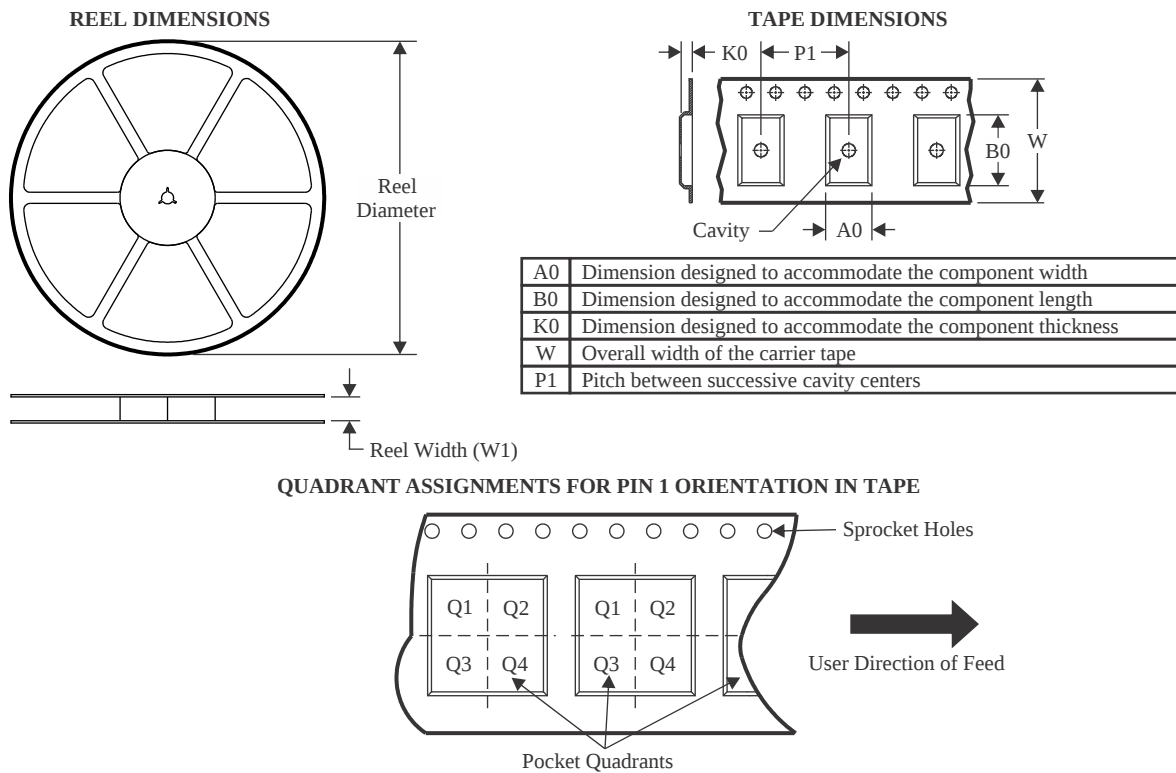
OTHER QUALIFIED VERSIONS OF INA2134-EP :

- Catalog : [INA2134](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

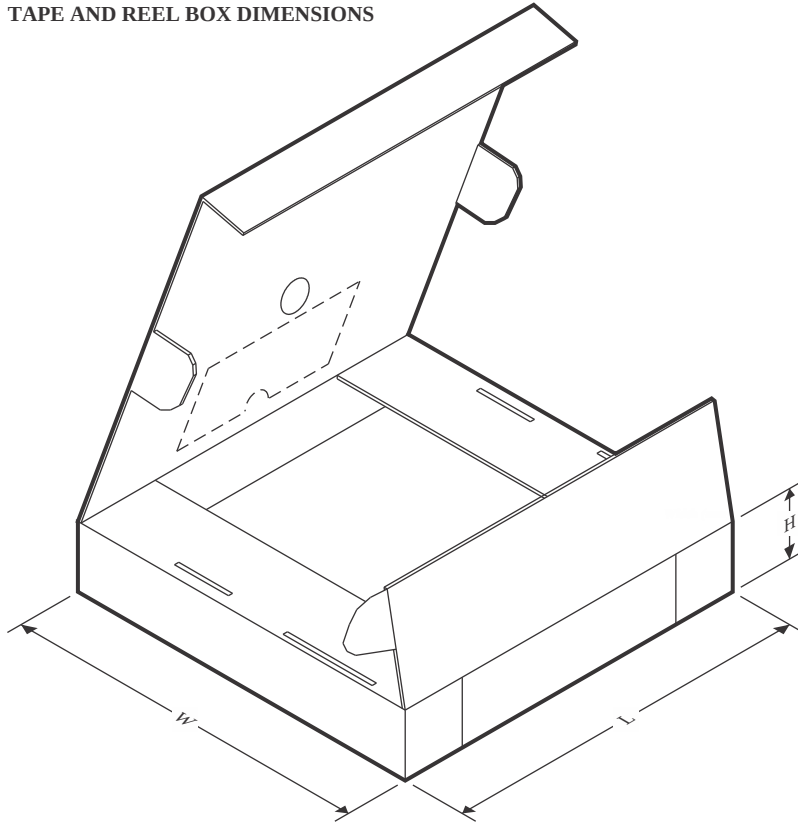
TAPE AND REEL INFORMATION



*All dimensions are nominal

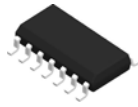
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA2134MDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

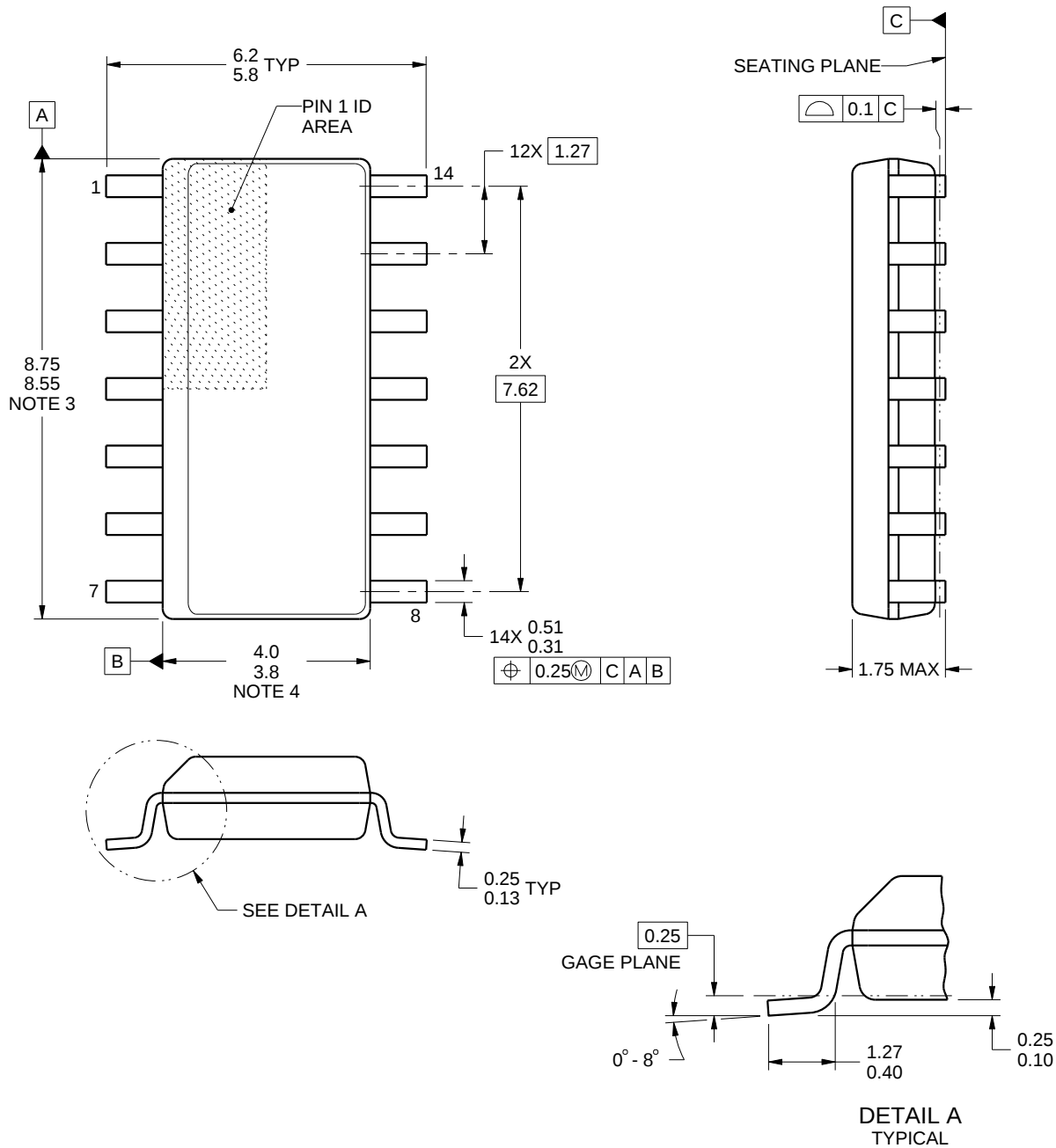


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA2134MDREP	SOIC	D	14	2500	353.0	353.0	32.0

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

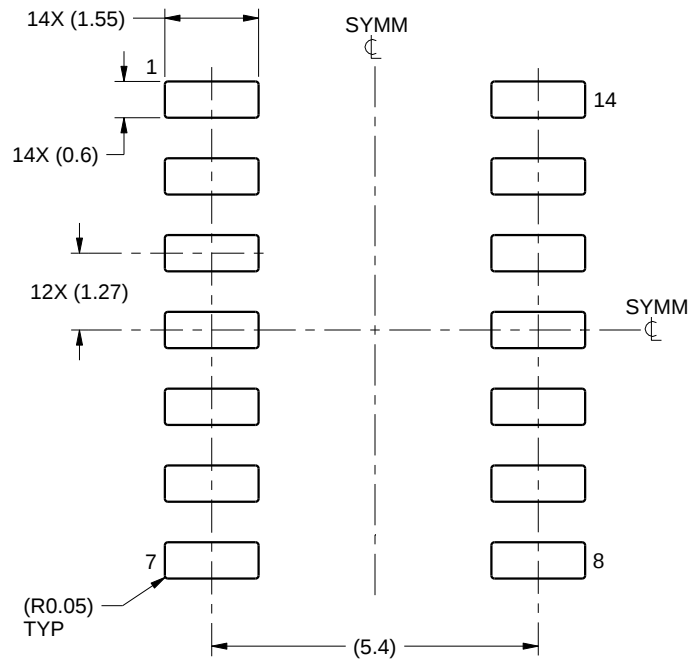
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

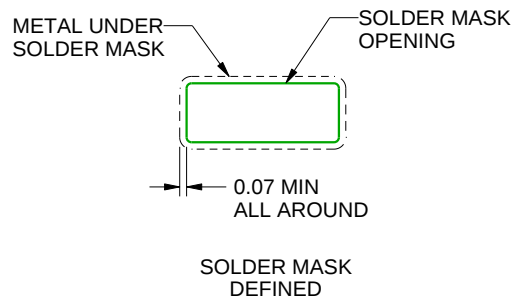
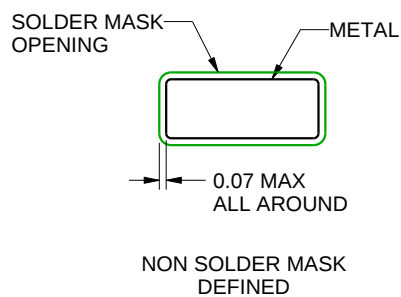
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

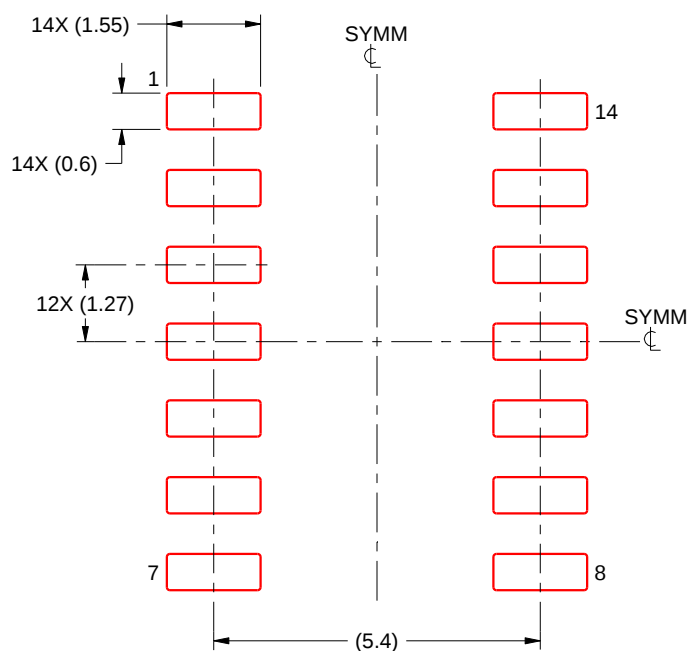
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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