



## LatticeECP3™ Video Protocol Board – Revision C

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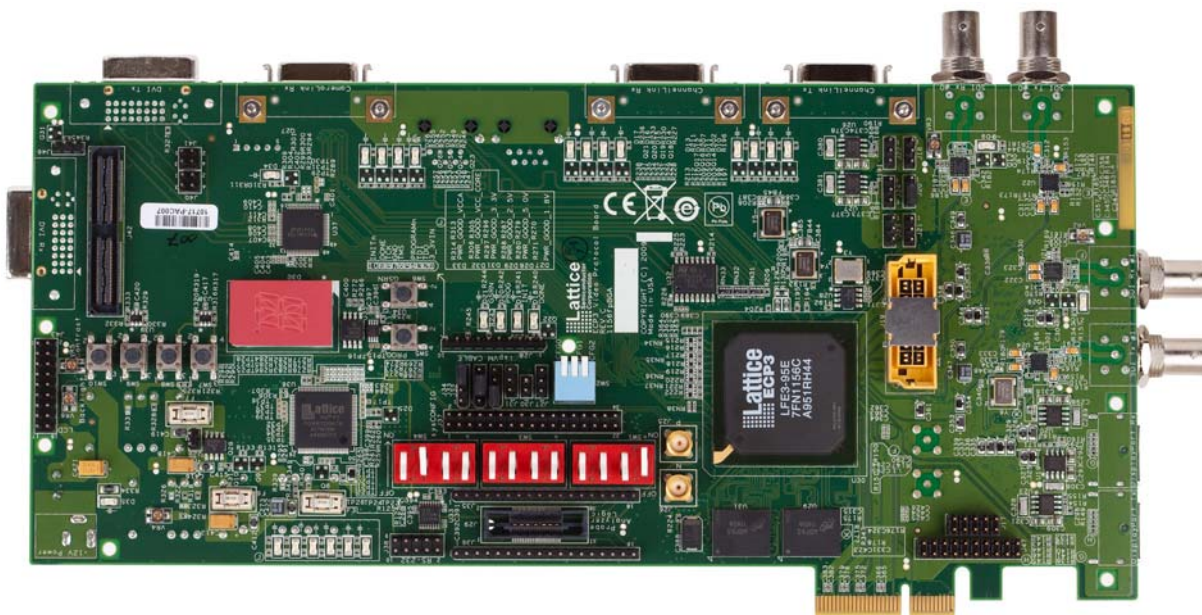
### User's Guide

## Introduction

The LatticeECP3™ FPGA family includes many features for video applications. For example, DisplayPort, SMPTE standards (SD-SDI, HD-SDI and 3G-SDI), DVB-ASI, DVI and HDMI can be implemented with 16 channels of embedded SERDES/PCS. 7:1 LVDS video interfaces like ChannelLink and CameraLink can be supported by the generic DDRX2 mode on the I/O pins. When configuring to TRLVDS mode, the I/O pins on banks 0 and 1 can also be used to receive the TMDS signals of DVI or HDMI video standard.

This user's guide describes revision C of the LatticeECP3 Video Protocol Board featuring the LatticeECP3 LFE3-95E-7FN1156C FPGA device. The stand-alone evaluation PCB provides a functional platform for development and rapid prototyping of many different video applications.

**Figure 1. LatticeECP3 Video Protocol Board – Revision C**



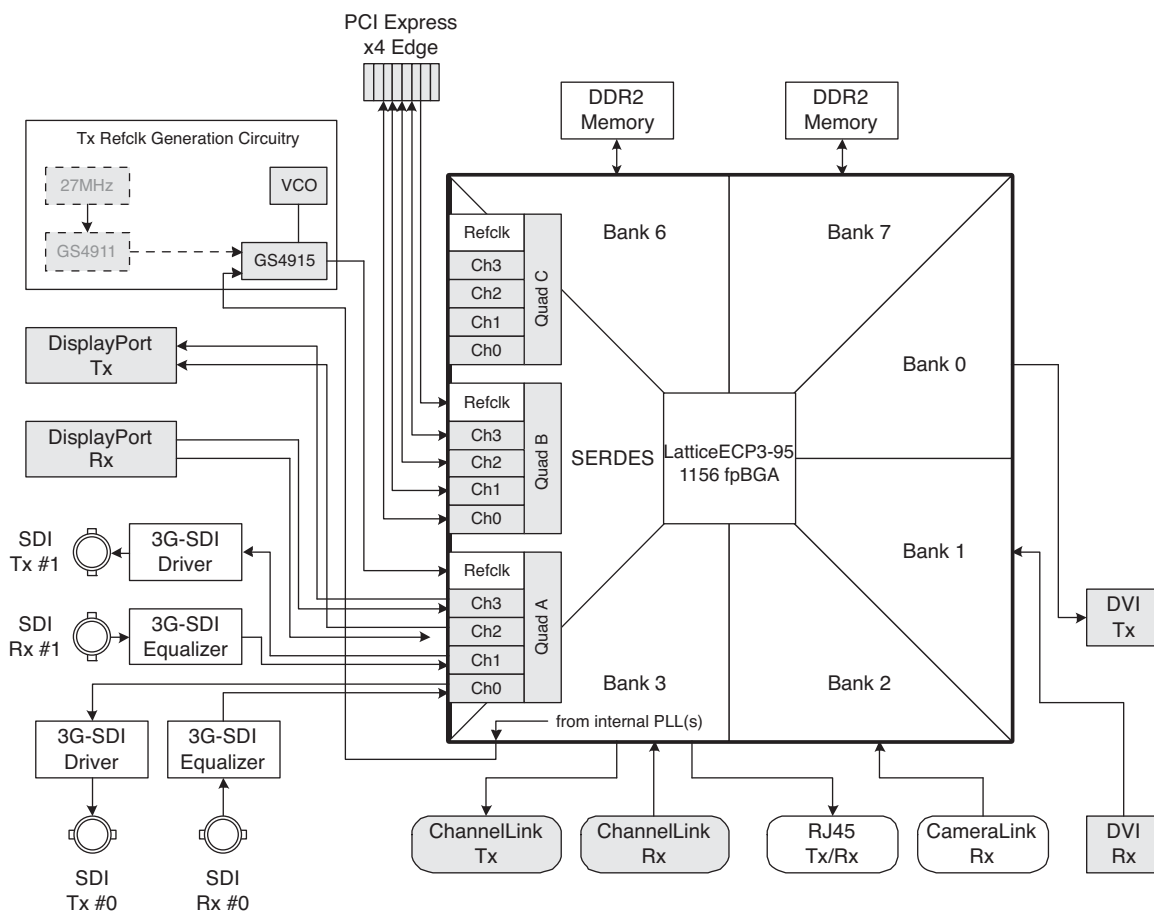
## Features

- Video interfaces for interconnection to video standard equipment
- Allow the demonstration of SD/HD/3G-SDI, DisplayPort and PCI Express (x4) interfaces using SERDES channels
- High speed Mezzanine connector connected to SERDES channels for future expansion
- Allows the demonstration of LVDS video standards – ChannelLink and CameraLink
- Allows control of SERDES PCS registers using the Serial Client Interface (ORCAstra)
- Allows the demonstration of receiving TMDS signals using the DVI interface
- On-board Boot Flash with Serial SPI Flash memory device
- Shows interoperation with high performance DDR2 memory components
- Driver-based “run-time” device configuration capability via an ORCAstra or RS232 interface
- SMAs for external high-speed clock / PLL inputs
- Switches, LEDs and LCD display header for demo purposes
- Mictor connector for using Logic Analyzer in the debugging phase

- Input connection for lab-power supply
- Power connections and power sources
- ispVM™ programming support
- On-board and external reference clock sources
- Various high-speed layout structures
- User-defined input and output points
- Performance monitoring via test headers, LEDs and switches

The contents of this user's guide include top-level functional descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, diodes and switches and a complete set of schematics of the board. Figure 2 shows the functional partitioning of the board.

**Figure 2. LatticeECP3 Video Protocol Board – Revision C Functional Partition**



## Differences Between the Revision B and Revision C Boards

The major changes in revision C are summarized below:

1. The Revision C board includes eight pull-up resistors, R362-R369, to the DVI Rx signals placed close to the LatticeECP3 device. These resistors are used for termination of the DVI's TMDS signals and are not included on the Revision B board.

- The Revision C board includes eight pull-up resistors, R370-R377, to the DDR2 memory's DQS signals. These resistors are placed close to the LatticeECP3 device. These resistors are not included on the Revision B board.
- The Revision C board includes R75 between the P and N reference clocks of SERDES Quad C (Mezzanine daughter board) for future use. No resistor is populated. This resistor is not included on the Revision B board.
- On the Revision C board, the Gennum clock generators (GS4911) on U2 and U3 are not populated.

## LatticeECP3 Device

This board features a LatticeECP3 FPGA with a 1.2V core supply. It can accommodate all pin compatible LatticeECP3 devices in the 1156-ball fpBGA (1mm pitch) package. A complete description of this device can be found in the [LatticeECP3 Family Data Sheet](#).

## Applying Power to the Board

The LatticeECP3 Video Protocol Board is ready to power on. This board can be supplied with power from an AC wall-type transformer power supply shipped with the board. Or it can be supplied from a bench top supply via terminal screw connections. It also has provisions to be supplied from the PCI Express edge fingers from a host board.

To supply power from the factory-supplied wall transformer, simply connect the output connection of the power cord to J15 and plug wall-transformer into an AC wall outlet.

## Supply Power from Bench Power Supply

The evaluation board incorporates an alternate scheme to provide power to the board. The board is equipped to accept a main supply via the TB1 connection. This connection is intended to be used with a bench top supply adjusted to provide a nominal 12V DC.

All input power sources and on-board power supplies are fused with surface mounted fuses. Table 1 shows these fuses and the corresponding powers.

**Table 1. Board Power Supply Fuses**

| Fuse # | Rating | Voltage | Usage                                                                                                                                                                                                                        |
|--------|--------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| F1     | 3A     | 2.5V    | EEPROM, DDR2 regulator, Bank 1, 2 and 3 I/Os, DIP switches                                                                                                                                                                   |
| F2     | 3A     | 1.8V    | Bank 6, Bank 7 I/Os, DDR2 regulator, DDR2 memory, Gennum clock chips                                                                                                                                                         |
| F3     | 3A     | 5.0V    | Cable driver/equalizer power regulator, Gennum clock chips power regulators, DisplayPort power output regulators, Mezzanine connector, DVI power output for EDID, LCD module                                                 |
| F4     | 3A     | 1.2V    | LatticeECP3 SERDES                                                                                                                                                                                                           |
| F5     | 10A    | 12V     | Main power supply                                                                                                                                                                                                            |
| F6     | 10A    | 1.2V    | LatticeECP3 Core                                                                                                                                                                                                             |
| F7     | 10A    | 3.3V    | LatticeECP3 V <sub>CCAUX</sub> , PLL, JTAG, Bank 0 and 8 I/Os, SPI Flash memory, push-button debouncer, DVI transmitter, RS-232 driver/receiver, zero delay clock buffer, clock oscillators, MachXO™, cable driver/equalizer |

The Lattice ispPAC® Power Manager II device, the ispPAC-POWR1220AT8, is used for monitoring various voltages on the board. There are six LEDs used to indicate the status of the monitoring voltages. If the monitoring voltage is not in the +/- 5% voltage window, the corresponding LED will flash; otherwise, the LED will stay ON. Table 2 shows these six voltages and the corresponding LEDs.

**Table 2. Board Power Supply Monitoring Indicators**

| Power              | LED # | Voltage Range | In Range | Out of Range |
|--------------------|-------|---------------|----------|--------------|
| LatticeECP3 SERDES | D33   | 1.2V +/- 5%   | On       | Flash        |
| LatticeECP3 Core   | D32   | 1.2V +/- 5%   | On       | Flash        |
| 3.3V               | D31   | 3.3V +/- 5%   | On       | Flash        |
| 2.5V               | D29   | 2.5V +/- 5%   | On       | Flash        |
| 5.0V               | D28   | 5.0V +/- 5%   | On       | Flash        |
| 1.8V               | D27   | 1.8V +/- 5%   | On       | Flash        |

External power can be alternatively connected through TB1 rather than the wall transformer power pack.

**Table 3. Board Supply Disconnects**

|     |                                                                                                                                           |
|-----|-------------------------------------------------------------------------------------------------------------------------------------------|
| TB1 | Screw terminal for 12V DC<br>+12V: Pin1 (closer to the wall transformer power jack J15) 12V DC<br>GND: Pin2 (closer to the LCD connector) |
|-----|-------------------------------------------------------------------------------------------------------------------------------------------|

## PCI Express Power Interface

Power can be sourced to the board via the PCB edge-finger (CN1). This interface allows the user to provide power from a PCI Express host board.

## Configuration/Programming Headers

Two programming headers are provided on the board for accessing to the LatticeECP3 JTAG port and sysCONFIG™ port. The JTAG connector is a 1x10 header and the sysCONFIG connector is a 2x17 header.

**Table 4. sysCONFIG Connector Pinout (J37)**

| Net Name | LatticeECP3 Pin | Header Pin | Net Name | LatticeECP3 Pin | Header Pin |
|----------|-----------------|------------|----------|-----------------|------------|
| CCLK     | C34             | 1          | GND      | —               | 2          |
| SISPI    | F33             | 3          | D6       | J34             | 4          |
| CSSPI0N  | D34             | 5          | 3.3V     | —               | 6          |
| CSSP1N   | E34             | 7          | INITN    | C33             | 8          |
| DONE     | G31             | 9          | PROGRAMN | B34             | 10         |
| D7       | F32             | 11         | GND      | —               | 12         |
| D6       | J34             | 13         | GND      | —               | 14         |
| D5       | H34             | 15         | GND      | —               | 16         |
| D4       | G32             | 17         | GND      | —               | 18         |
| D3       | G33             | 19         | GND      | —               | 20         |
| D2       | H33             | 21         | GND      | —               | 22         |
| D1       | G34             | 23         | GND      | —               | 24         |
| D0       | E32             | 25         | GND      | —               | 26         |
| CSN      | F31             | 27         | WRITE    | E31             | 28         |
| CS1      | G30             | 29         | CFG0     | B33             | 30         |
| 3.3V     | —               | 31         | CFG1     | F30             | 32         |
| GND      | —               | 33         | CFG2     | D32             | 34         |

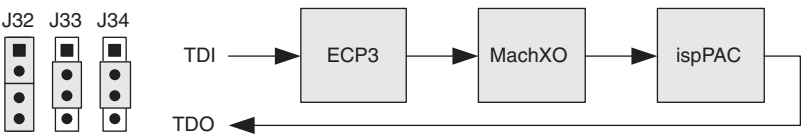
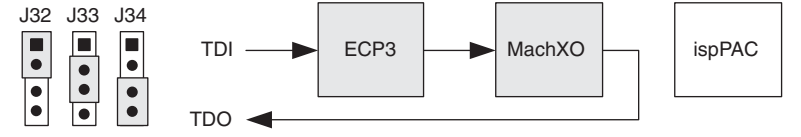
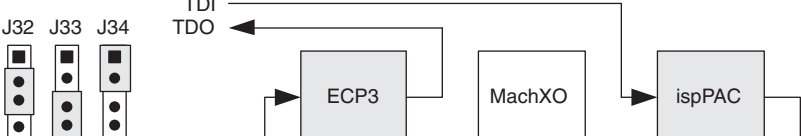
J28 is a 10-pin JTAG connector used in conjunction with the ispVM download cable to program and control the Lattice devices on this board.

**Table 5. ispVM JTAG Connector (J28)**

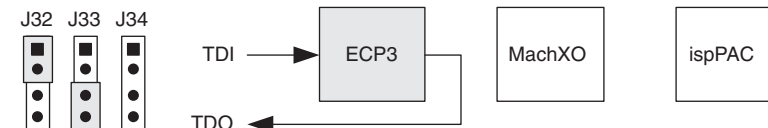
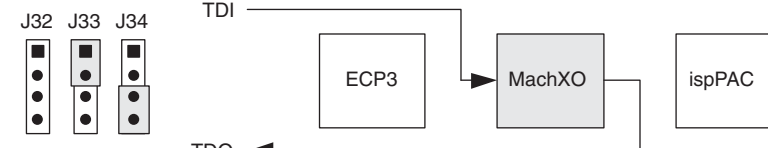
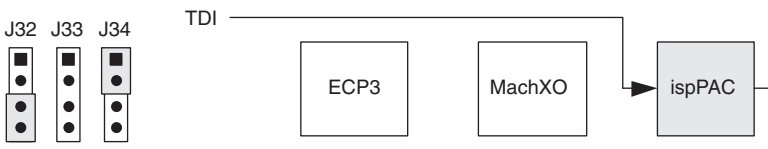
| Pin #  | Description |
|--------|-------------|
| Pin 1  | VCC         |
| Pin 2  | TDO         |
| Pin 3  | TDI         |
| Pin 4  | PROGRAMN    |
| Pin 5  | NC          |
| Pin 6  | TMS         |
| Pin 7  | GND         |
| Pin 8  | TCK         |
| Pin 9  | DONE        |
| Pin 10 | INITN       |

This board includes three Lattice programmable devices that can be programmed in a daisy chain (U30 = LatticeECP3-95, U1 = MachXO™ LCMXO256, and U36 = ispPAC-POWR1220AT8). Other than the LatticeECP3-95, the JTAG connector provides access to the JTAG ports of the ispPAC-POWR1220AT8 and the MachXO. With proper jumper selection, the JTAG ports of these devices can be chained together for programming. Table 6 shows the jumper settings of J32, J33 and J34 used to configure the JTAG connections.

**Table 6. JTAG Connection Settings (J32, J33, J34)**

| Jumper Settings | JTAG Connection                                                                      |
|-----------------|--------------------------------------------------------------------------------------|
| 1               |   |
| 2               |  |
| 3               |  |
| 4               |  |

**Table 6. JTAG Connection Settings (J32, J33, J34) (Continued)**

| Jumper Settings | JTAG Connection                                                                    |
|-----------------|------------------------------------------------------------------------------------|
| 5               |  |
| 6               |  |
| 7               |  |

There are several LEDs on the board to indicate the LatticeECP3 programming status. They are listed in Table 7.

**Table 7. LED Indicators for Configuration Status**

| LED # | Color | Function                                                                                                                |
|-------|-------|-------------------------------------------------------------------------------------------------------------------------|
| D19   | Red   | LED illuminated to indicate that the programming was aborted or reinitialized driving the INITN output low.             |
| D18   | Green | LED illuminated to indicate the successful completion of configuration by releasing the open collector DONE output pin. |
| D20   | Red   | LED illuminated to indicate that PROGRAMN is low.                                                                       |
| D21   | Red   | LED illuminated to indicate that GSRN is low.                                                                           |

The PROGRAMN pin of the LatticeECP3-95 is connected to a push-button switch (SW5). Depressing this button drives a logic level “0” to the PROGRAMN pin. This will force the LatticeECP3 into the configuration mode and initiate the configuration sequence.

The FPGA CFG pins are set on the board for a particular programming mode via the SW2 DIP switch. JTAG programming is independent of the MODE pins and is always available to the user. Pushing down the switch will turn it on and set the CFG value to 0.

**Table 8. CFG Mode Selections**

| CFG2 (SW2-1) | CFG1 (SW2-2) | CFG0 (SW2-3) | Selected Configuration Mode         |
|--------------|--------------|--------------|-------------------------------------|
| 0 (ON)       | 0 (ON)       | 0 (ON)       | SPI Flash Mode (available on-board) |
| 0 (ON)       | 1 (OFF)      | 0 (ON)       | SPIm                                |
| 1 (OFF)      | 0 (ON)       | 0 (ON)       | Master Serial                       |
| 1 (OFF)      | 0 (ON)       | 1 (OFF)      | Slave Serial                        |
| 1 (OFF)      | 1 (OFF)      | 0 (ON)       | Master Parallel                     |
| 1 (OFF)      | 1 (OFF)      | 1 (OFF)      | Slave Parallel                      |

## On-Board Flash Memory

One SPI (16-pin TSSOP 64M) Flash memory device (U32) is on board for non-volatile configuration memory storage. The CFG [2:0] setting must be [000] for the LatticeECP3 to enable the SPI Flash mode.

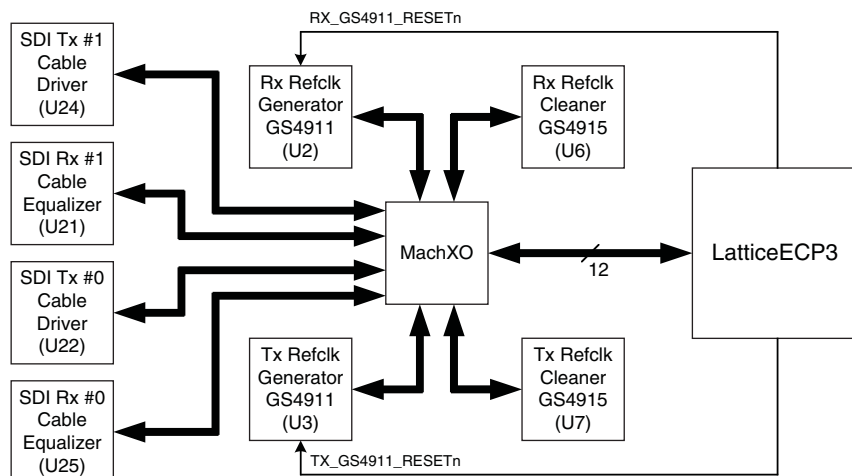
## Video Clock Management and SDI Cable Driver/Equalizer

Industry standard video clocks are generated and managed via Genum chipsets. These chipsets are used to generate both transmit and receive reference clocks for LatticeECP3 SERDES. The GS4911 clock generator device produces multiple video standard reference clocks from an on-board 27MHz crystal. The GS4915 clock cleaner is used to reduce clock jitter to produce a clean clock for video signal quality using a high-performance VCO. The Genum clock devices are used to generate clocks for SD/HD/3G-SDI applications. Since the PLL in LatticeECP3 FPGAs is designed to support all the frequencies required by SD/HD/3G-SDI, the GS4911 clock generator is no longer needed. The two GS4911 devices found on the Revision B board are included on the Revision C board but not populated.

Two cable drivers and two cable equalizers are placed on-board for SD/HD/3G-SDI applications that require delivering video signal over 75 ohm coaxial cable.

The control and status pins of the Genum chipsets and the cable drivers/equalizers are connected to the MachXO I/O pins. By using the signals connected between the MachXO and LatticeECP3, the Genum chipsets and cable drivers/equalizers can be controlled from the design in the LatticeECP3. Figure 3 shows the block diagram of the control/status buses of the connections between these devices. The MachXO pins connected to these devices are shown in Tables 9 to 12.

**Figure 3. Block Diagram of Genum Chipsets and Cable Driver/Equalizer Controls**



**Table 9. MachXO Pin Connections to GS4911 Devices (GS4911 Devices are Not Populated on the Revision C Board)**

| Signal Type | GS4911 Pin Name           | U2 (for Rx Refclk)     | U3 (for Tx Refclk)     | Pull-low/high |
|-------------|---------------------------|------------------------|------------------------|---------------|
| Control     | VID_STD0                  | K2                     | G13                    | High          |
|             | VID_STD1                  | L1                     | H13                    | Low           |
|             | VID_STD2                  | L2                     | J13                    | High          |
|             | VID_STD3                  | M1                     | J14                    | Low           |
|             | VID_STD4                  | M2                     | K13                    | High          |
|             | VID_STD5                  | N1                     | K14                    | Low           |
|             | /GENLOCK                  | M3                     | M13                    | High          |
|             | ASR_SEL0                  | H2                     | —                      | Low           |
|             | ASR_SEL1                  | G2                     | —                      | Low           |
|             | ASR_SEL2                  | F2                     | —                      | Low           |
|             | JTAG / HOSTn <sup>1</sup> | N11                    | N11                    | —             |
|             | SCLK_TCLK <sup>1</sup>    | P13                    | P13                    | —             |
|             | SDIN_TDI                  | —                      | N12                    | —             |
|             | SDOUT_TDO                 | P12                    | —                      | —             |
|             | CSn_TMS                   | P11                    | P14                    | —             |
|             | /RESET                    | D17 (from LatticeECP3) | D12 (from LatticeECP3) | Low           |
| Status      | LOCK_LOST                 | —                      | L14                    | —             |
|             | REF_LOST                  | —                      | L13                    | —             |
|             | TIMING_OUT_1              | K1                     | F14                    | —             |
|             | TIMING_OUT_2              | J2                     | F13                    | —             |
|             | TIMING_OUT_3              | J1                     | E14                    | —             |
|             | TIMING_OUT_4              | —                      | E13                    | —             |

1. These are the signals controlled by the same MachXO I/O pins.

**Table 10. MachXO Pin Connections to GS4915 Devices**

| Signal Type | GS4915 Pin Name | U6 (for Rx Refclk) | U7 (for Tx Refclk) | Pull-low/high |
|-------------|-----------------|--------------------|--------------------|---------------|
| Control     | /RESET          | F1                 | D14                | High          |
|             | IPSEL           | E2                 | D13                | Low           |
|             | BYPASS          | E1                 | C14                | Low           |
|             | /AUTOBYPASS     | C2                 | C13                | Low           |
|             | FCTRL0          | D1                 | B14                | Low           |
|             | FCTRL1          | D2                 | C12                | Low           |
|             | DOUBLE          | C1                 | A13                | Low           |
|             | SKEW_EN         | B1                 | A12                | Low           |
| Status      | LOCK            | B11                | B12                | —             |

**Table 11. MachXO Pin Connections to LMH0303 or GS2978 Cable Driver Devices**

| Signal Type | Driver Pin Name   | U22 (for Tx #0) | U24 (for Tx #1) | Pull-low/high |
|-------------|-------------------|-----------------|-----------------|---------------|
| Control     | SD / HDn          | N5              | N14             | Low           |
|             | ENABLE (/DISABLE) | N6              | M14             | High          |
|             | /RSTI             | N7              | —               | High          |
| Status      | /FAULT            | N13             | N13             | —             |

**Table 12. MachXO Pin Connections GS2974 Cable Equalizer Devices**

| Signal Type | Driver Pin Name | U25 (for Rx #0)                 | U21 (for Rx #1)                 | Pull-low/high |
|-------------|-----------------|---------------------------------|---------------------------------|---------------|
| Control     | BYPASS          | P3                              | P8                              | Low           |
|             | MUTE            | P4                              | N8                              | Low           |
|             | MCLADJ          | Controlled by potentiometer VR3 | Controlled by potentiometer VR2 | —             |
| Status      | /CD             | N3                              | P9                              | —             |

**Table 13. MachXO Pin Connections to LatticeECP3**

| Net Name      | MachXO Pin | LatticeECP3 Pin |
|---------------|------------|-----------------|
| ECP3_XO_SIG0  | B10        | AM31            |
| ECP3_XO_SIG1  | A9         | AL31            |
| ECP3_XO_SIG2  | A7         | AN31            |
| ECP3_XO_SIG3  | A6         | AP31            |
| ECP3_XO_SIG4  | A5         | AM32            |
| ECP3_XO_SIG5  | B4         | AN32            |
| ECP3_XO_SIG6  | A3         | AB33            |
| ECP3_XO_SIG7  | B3         | AB34            |
| ECP3_XO_SIG8  | A2         | Y31             |
| ECP3_XO_SIG9  | C3         | Y32             |
| ECP3_XO_SIG10 | A1         | Y33             |
| ECP3_XO_SIG11 | B2         | Y34             |

The status pins of these devices can also be observed from LED indicators. Table 13 shows the these LEDs with the associated signals.

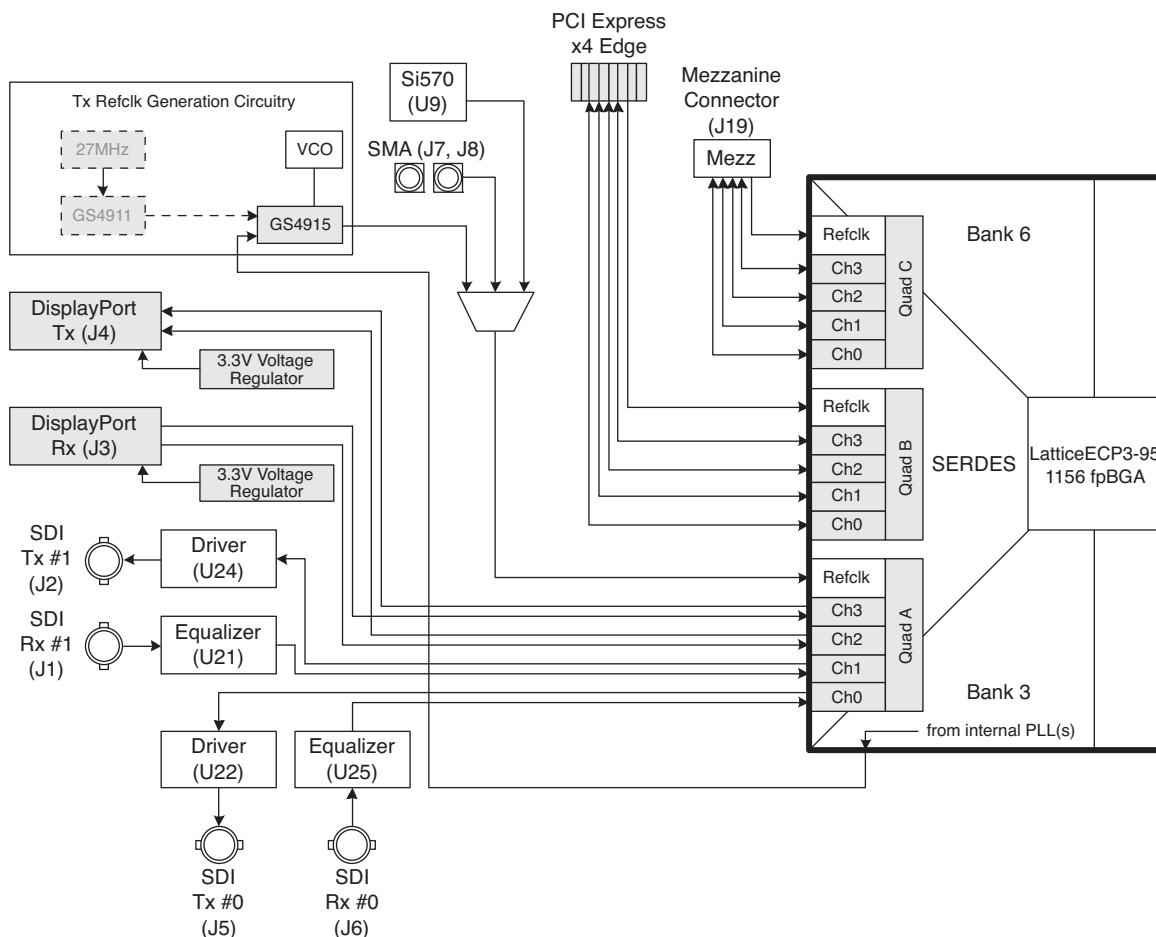
**Table 14. LED Indicators for Video Clocking and Cable Equalizer Status**

| LED # | Color  | Function                 | Description                                                                                                                                                    |
|-------|--------|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D4    | Red    | Rx GS4911 REF LOST       | LED illuminates to indicate that no reference signal is applied or the FSYNC, VSYNC, HSYNC input reference signals do not meet the min/max timing requirement. |
| D1    |        | Tx GS4911 REF LOST       |                                                                                                                                                                |
| D3    |        | Rx GS4911 LOCK LOST      | LED illuminates to indicate the GS4911 clock output is not genlocked to the input reference signals.                                                           |
| D2    |        | Tx GS4911 LOCK LOST      |                                                                                                                                                                |
| D5    | Green  | Rx GS4915 LOCK           | LED illuminates to indicate that the GS4915 output clock is locked to the input clock selected by IPSEL.                                                       |
| D6    |        | Tx GS4915 LOCK           |                                                                                                                                                                |
| D9    | Orange | SDI Rx #0 Carrier Detect | LED illuminates to indicate that the equalizer has detected the presence of a good input video signal.                                                         |
| D8    |        | SDI Rx #1 Carrier Detect |                                                                                                                                                                |

## SERDES

There are three SERDES quads available for the LatticeECP3-95. Each quad include four SERDES channels. These 12 SERDES channels are used for implementing high-speed serial link interfaces. Figure 4 shows the how these channels are used.

**Figure 4. Block Diagram of SERDES Usage**



The power supply of the input and output buffers of the SERDES quads can be individually set to either 1.2V or 1.5V. This is done by headers J18, J20~J24. Table 15 shows the jumper settings of these headers for applying either 1.2V or 1.5V power to the SERDES input and output buffers.

**Table 15. Jumper Settings for SERDES I/O Buffer (J18, J20~J24)**

| Header | Buffer                      | Jumper Setting | Function                           |
|--------|-----------------------------|----------------|------------------------------------|
| J24    | Quad A Input (SDI/DP)       | 1-2            | Set PCSA_VCCIB (J24 pin 2) to 1.2V |
|        |                             | 2-3            | Set PCSA_VCCIB (J24 pin 2) to 1.5V |
| J20    | Quad A Output (SDI/DP)      | 1-2            | Set PCSA_VCCOB (J20 pin 2) to 1.2V |
|        |                             | 2-3            | Set PCSA_VCCOB (J20 pin 2) to 1.5V |
| J23    | Quad B Input (PCI Express)  | 1-2            | Set PCSB_VCCIB (J23 pin 2) to 1.2V |
|        |                             | 2-3            | Set PCSB_VCCIB (J23 pin 2) to 1.5V |
| J21    | Quad B Output (PCI Express) | 1-2            | Set PCSB_VCCOB (J21 pin 2) to 1.2V |
|        |                             | 2-3            | Set PCSB_VCCOB (J21 pin 2) to 1.5V |
| J22    | Quad C Input (Mezzanine)    | 1-2            | Set PCSC_VCCIB (J22 pin 2) to 1.2V |
|        |                             | 2-3            | Set PCSC_VCCIB (J22 pin 2) to 1.5V |
| J18    | Quad C Output (Mezzanine)   | 1-2            | Set PCSC_VCCOB (J18 pin 2) to 1.2V |
|        |                             | 2-3            | Set PCSC_VCCOB (J18 pin 2) to 1.5V |

### Quad A (3G-SDI and DisplayPort Video Interfaces)

Quad 0 is used for SDI and DisplayPort video protocols. Channel 0 and 1 of quad 0 are used for SD/HD/3G-SDI. The SD/HD/3G-SDI video signal is a signal-ended video signal transmitting through 75-ohm coaxial cable connecting through BNC connectors. Two cable drivers and two cable equalizers are placed on board for using longer coaxial cable. Channels 2 and 3 are used for support Displayport up to two data lanes.

Table 16 shows the ECP3 connections for the SD/HD/3G-SDI video interface connectors.

**Table 16. SD/HD/3G-SDI Connections (J1, J2, J5 and J6)**

| Connector | Description | Cable Driver/Equalizer | SERDES Pin Names | LatticeECP3 Pin # |
|-----------|-------------|------------------------|------------------|-------------------|
| J5        | SDI Tx #0   | Driver (U22)           | PCSA_HDOUT[P:N]0 | AP21, AN21        |
| J6        | SDI Rx #0   | Equalizer (U25)        | PCSA_HDIN[P:N]0  | AL21, AK21        |
| J2        | SDI Tx #1   | Driver (U24)           | PCSA_HDOUT[P:N]1 | AP20, AN20        |
| J1        | SDI Rx #1   | Equalizer (U21)        | PCSA_HDIN[P:N]1  | AL20, AK20        |

There are two instances of Gennum clocking circuitry on this board, one for Rx side and the other for Tx side. Since the specification of the high-speed video output stream jitter is critical, it is important to have a clean reference clock for the Tx side serializer. The reference clock of the SERDES channel can come from different a path, but the clock coming in through the dedicated reference clock pins will have the lowest jitter.

The dedicated reference clock pins of quad 0 can be sourcing from the following clocks:

- Clock generated by the on-board Gennum clocking chipsets
- Clock generated by the Silicon Labs Si570
- External differential clock coming through the two SMA connectors

Other than generating from the Gennum chipsets, the transmit reference clock can also receive input clock from an external clock source via a pair of SMA connectors, or from the on-board Silicon Labs Si570. To avoid PCB trace stub and minimize the jitter of the Tx reference clock, two zero-ohm resistors are used for selecting the clock from one of the three clock sources. Figure 5 shows how these two zero-ohm resistors are installed to select a difference clock source. See the schematic in Appendix A (Figure 16) for the detailed clock multiplexing circuitry.

**Figure 5. Resistors for Quad 0 Reference Clock Selection**

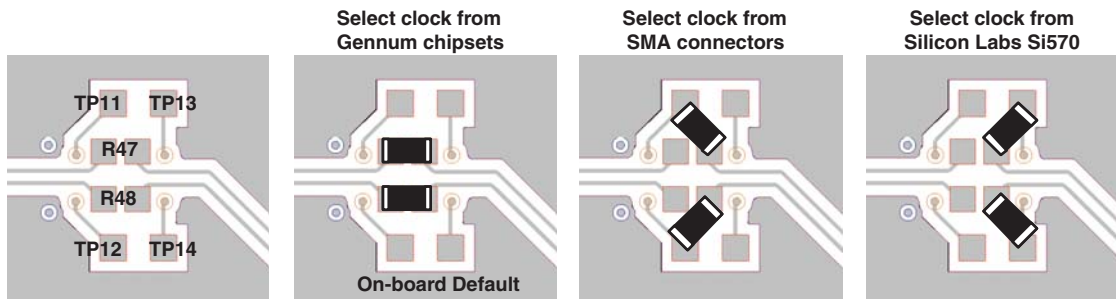


Figure 6 shows the block diagram of the DisplayPort circuitry on this board. Since only two channels in SERDES Quad 0 are used, the DisplayPort video interface on this board can only support up to two lanes. Two instances of 3.3V voltage regulators are used for providing power to the off-board DisplayPort devices when necessary.

Figure 6. Block Diagram of the DisplayPort Video Interface

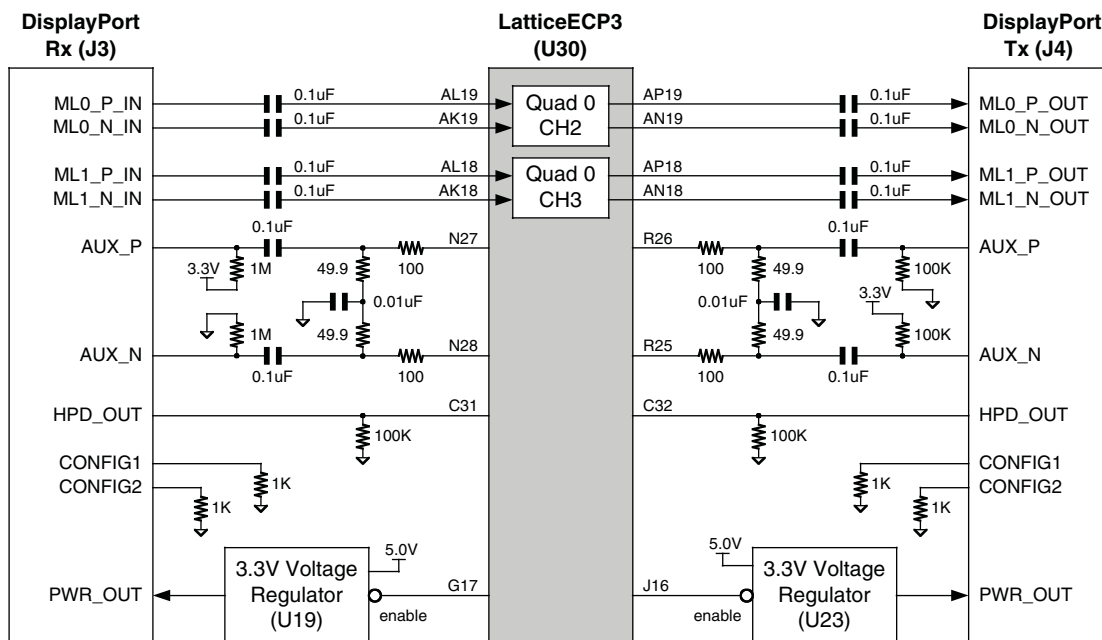


Table 17 shows the pin connections of the DisplayPort video interface.

Table 17. DisplayPort Connections (J3 and J4)

| Connector           | Pin Name      | Pin #     | LatticeECP3 Pin Name | LatticeECP3 Pin # |
|---------------------|---------------|-----------|----------------------|-------------------|
| DisplayPort Tx (J4) | ML0_[P:N]_OUT | 1 and 2   | PCSA_HDOUT[P:N]2     | AP19, AN19        |
|                     | ML1_[P:N]_OUT | 4 and 6   | PCSA_HDOUT[P:N]3     | AL18, AK18        |
|                     | AUX_[P:N]     | 15 and 17 | PR31[A:B]            | R26, R25          |
|                     | HPD_IN        | 18        | PT143B               | C32               |
| DisplayPort Rx (J3) | ML0_[P:N]_IN  | 10 and 12 | PCSA_HDIN[P:N]2      | AL19, AK19        |
|                     | ML1_[P:N]_IN  | 7 and 8   | PCSA_HDIN[P:N]3      | AL18, AK18        |
|                     | AUX_[P:N]     | 15 and 17 | PR22[A:B]            | N27, N28          |
|                     | HPD_OUT       | 18        | PT145B               | C31               |

## Quad B (PCI Express x4)

This board is equipped to communicate directly as an add-on card to a PCI Express host. It is designed with edge-fingers (CN1) to fit directly into a x1 host receptacle. Power can be supplied directly from the PCI Express host via the edge-finger connections.

All channels of Quad 1 are connected to the PCI Express Edge connector (CN1) for implementing a PCI Express x4 interface. The dedicated reference clock input pins and a reset control signal are also connected to the PCI Express edge connector.

Table 18. SERDES PCI Express Interconnections

| PCI Express Name | PCI Express Pin # | LatticeECP3 Pin Name | LatticeECP3 Pin # | AC Coupling | PCI Express Pin Description        |
|------------------|-------------------|----------------------|-------------------|-------------|------------------------------------|
| PERp0            | A16               | PCSB_HDOUTP0         | AP17              | C365        | Receiver differential pair, Lane 0 |
| PERn0            | A17               | PCSB_HDOUTN0         | AN17              | C366        |                                    |

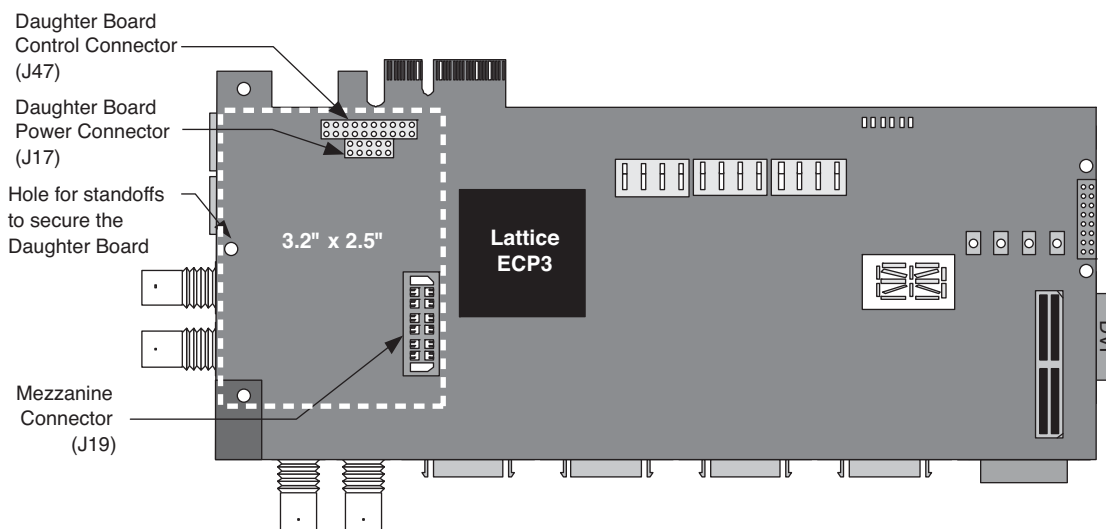
**Table 18. SERDES PCI Express Interconnections (Continued)**

| PCI Express Name | PCI Express Pin # | LatticeECP3 Pin Name | LatticeECP3 Pin # | AC Coupling | PCI Express Pin Description           |
|------------------|-------------------|----------------------|-------------------|-------------|---------------------------------------|
| PERp1            | A21               | PCSB_HDOUTP1         | AP16              | C372        | Receiver differential pair, Lane 1    |
| PERn1            | A22               | PCSB_HDOUTN1         | AN16              | C375        |                                       |
| PERp2            | A25               | PCSB_HDOUTP2         | AP15              | C376        | Receiver differential pair, Lane 2    |
| PERn2            | A26               | PCSB_HDOUTN2         | AN15              | C379        |                                       |
| PERp3            | A29               | PCSB_HDOUTP3         | AP14              | C382        | Receiver differential pair, Lane 3    |
| PERn3            | A30               | PCSB_HDOUTN3         | AN14              | C383        |                                       |
| PETp0            | B14               | PCSB_HDINP0          | AL17              | None        | Transmitter differential pair, Lane 0 |
| PETn0            | B15               | PCSB_HDINN0          | AK17              | None        |                                       |
| PETp1            | B19               | PCSB_HDINP1          | AL16              | None        | Transmitter differential pair, Lane 1 |
| PETn1            | B20               | PCSB_HDINN1          | AK16              | None        |                                       |
| PETp2            | B23               | PCSB_HDINP2          | AL15              | None        | Transmitter differential pair, Lane 2 |
| PETn2            | B24               | PCSB_HDINN2          | AK15              | None        |                                       |
| PETp3            | B27               | PCSB_HDINP3          | AL14              | None        | Transmitter differential pair, Lane 3 |
| PETn3            | B28               | PCSB_HDINN3          | AK14              | None        |                                       |
| REFCLK+          | A13               | PCSB_REFCLKP         | AH15              | None        | Reference clock (differential pair)   |
| REFCLK-          | A14               | PCSB_REFCLKN         | AH16              | None        |                                       |
| PERST#           | A11               | PT109A               | J21               | None        | Fundamental reset                     |

## Quad C (Daughter Board Expansion)

All channels of Quad 2 are connected to a high-speed Molex Mezzanine connector for working with a 3.2 x 2.5" daughter board. Users can design a daughter board for implementing anything that requires the SERDES quad, such as the high-speed HDMI/DVI video interface.

**Figure 7. Daughter Board Connection**



Other than the four input/output Quad 2 SERDES channels and the differential reference clock pair, there are three differential pairs of general purpose I/Os connected between the Mezzanine connector and the LatticeECP3 device. These signals can be used for the control or status signals of the daughter board. A 4-pin power connector is used to provide power to the daughter board. Tables 19 and 20 show the pin connections of the Mezzanine and the power connectors. Table 21 shows the pin connections between the LatticeECP3 and the daughter board con-

trol connector.

**Table 19. Mezzanine Connections (J19)**

| J19 Pin # | LatticeECP3 Pin Name | LatticeECP3 Pin # | Description                             |
|-----------|----------------------|-------------------|-----------------------------------------|
| 1         | PCSC_HDINP3          | AL22              | SERDES Quad 2 Channel 3 Input           |
| 2         | PCSC_HDINN3          | AK22              |                                         |
| 3         | PCSC_HDINP2          | AL23              | SERDES Quad 2 Channel 2 Input           |
| 4         | PCSC_HDINN2          | AK23              |                                         |
| 5         | PCSC_HDINP1          | AL24              | SERDES Quad 2 Channel 1 Input           |
| 6         | PCSC_HDINN1          | AK24              |                                         |
| 7         | PCSC_HDINP0          | AL25              | SERDES Quad 2 Channel 0 Input           |
| 8         | PCSC_HDINN0          | AK25              |                                         |
| 9         | PR25A                | P28               | User-defined Differential Signal Pair 1 |
| 10        | PR25B                | P27               |                                         |
| 11        | PR28A                | R28               | User-defined Differential Signal Pair 2 |
| 12        | PR28B                | R27               |                                         |
| 13        | PCSC_HDOUDP3         | AL22              | SERDES Quad 2 Channel 3 Output          |
| 14        | PCSC_HDOUDN3         | AK22              |                                         |
| 15        | PCSC_HDOUDP2         | AL23              | SERDES Quad 2 Channel 2 Output          |
| 16        | PCSC_HDOUDN2         | AK23              |                                         |
| 17        | PCSC_HDOUDP1         | AL24              | SERDES Quad 2 Channel 1 Output          |
| 18        | PCSC_HDOUDN1         | AK24              |                                         |
| 19        | PCSC_HDOUDP0         | AL25              | SERDES Quad 2 Channel 0 Output          |
| 20        | PCSC_HDOUDN0         | AK25              |                                         |
| 21        | PCSC_REFCLKP         | AH22              | SERDES Quad 2 Reference Clock           |
| 22        | PCSC_REFCLKN         | AH23              |                                         |
| 23        | PR19A                | N26               | User-defined Differential Signal Pair 0 |
| 24        | PR19B                | P26               |                                         |

**Table 20. Daughter Board Power Connections (J17)**

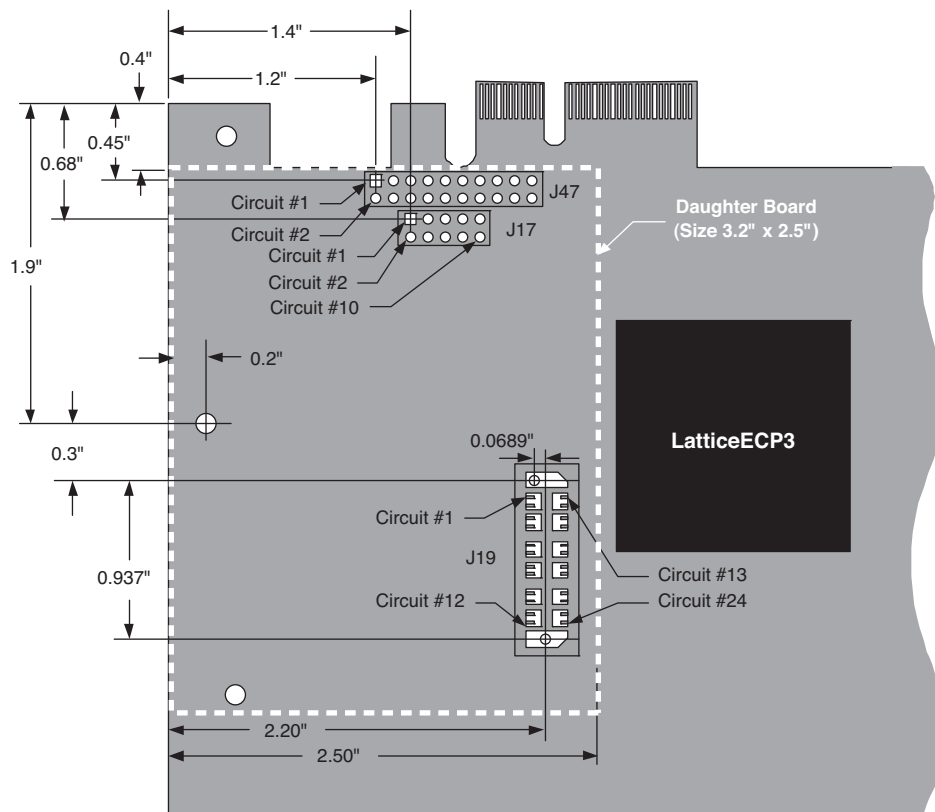
| J17 Pin Number | Voltage | Maximum Current |
|----------------|---------|-----------------|
| 2, 4           | 5.0V    | ~8A             |
| 6, 8           | 3.3V    | ~8A             |
| 10             | 1.8V    | ~2A             |
| 1, 3, 5, 7, 9  | GND     |                 |

**Table 21. Daughter Board Control Signals Connections (J47)**

| J47 Pin Number | LatticeECP3 Pin Number | Signal Name | J47 Pin Number | LatticeECP3 Pin Number | Signal Name |
|----------------|------------------------|-------------|----------------|------------------------|-------------|
| 1              | AM8                    | MZ_CTRL0    | 2              | AM7                    | MZ_CTRL1    |
| 3              | AK8                    | MZ_CTRL2    | 4              | AK7                    | MZ_CTRL3    |
| 5              | AG9                    | MZ_CTRL4    | 6              | AF9                    | MZ_CTRL5    |
| 7              | AK6                    | MZ_CTRL6    | 8              | AE9                    | MZ_CTRL7    |
| 9              | AH7                    | MZ_CTRL8    | 10             | AL3                    | MZ_CTRL9    |
| 11             | AJ3                    | MZ_CTRL10   | 12             | AJ2                    | MZ_CTRL11   |
| 13             | AN8                    | MZ_CTRL12   | 14             | AN7                    | MZ_CTRL13   |
| 15             | AH9                    | MZ_CTRL14   | 16             | AE3                    | MZ_CTRL15   |
| 17             | AE4                    | MZ_CTRL16   | 18             | AD3                    | MZ_CTRL17   |
| 19             | AD4                    | MZ_CTRL18   | 20             | AA8                    | MZ_CTRL19   |

Figure 8 shows the mechanical dimensions required for designing a daughter board.

**Figure 8. Mechanical Drawing of the Daughter Board Connection**



## ChannelLink and CameraLink Video Interfaces

There are two LVDS video interfaces on the board, ChannelLink and CameraLink. Both interfaces include a receive channel, but only the ChannelLink interface includes a transmit channel. All of these channels use the same on-board 3M MDR-26 (p/n 10226-1210VE) connectors. However, since the pinouts of these two interfaces are different, different 3M Mini D Ribbon (MDR) cables must be used. The cables are listed below. They look the same but have different pinouts.

- 3M ChannelLink Cable: 14526-EZ8B-XXX-07C
- 3M CameraLink Cable: 14X26-SZLB-XXX-0LC

Other than the ChannelLink and CameraLink LVDS signals, some of the LVDS signals are also connected to the two RJ45 connectors on J44 and J45. Tables 22 to 25 show the connections of these LVDS connectors.

**Table 22. ChannelLink Tx Connections (J9)**

| Signal Name | J9 Pin # | LatticeECP3 Pin # | LatticeECP3 Pin Type | External Resistor |
|-------------|----------|-------------------|----------------------|-------------------|
| TX OUT0+    | 15       | AM29              | True LVDS Output     | None              |
| TX OUT0-    | 14       | AN29              |                      |                   |
| TX OUT1+    | 5        | AL30              | True LVDS Output     | None              |
| TX OUT1-    | 4        | AM30              |                      |                   |
| TX OUT2+    | 7        | AJ31              | True LVDS Output     | None              |
| TX OUT2-    | 6        | AK31              |                      |                   |
| TX OUT3+    | 13       | AA28              | True LVDS Output     | None              |
| TX OUT3-    | 12       | AA27              |                      |                   |
| TX CLKOUT+  | 23       | AH33              | True LVDS Output     | None              |
| TX CLKOUT-  | 22       | AJ33              |                      |                   |

**Table 23. ChannelLink Rx Connections (J10)**

| Signal Names | J10 Pin # | LatticeECP3 Pin# | LatticeECP3 Pin Type | External Resistor   |
|--------------|-----------|------------------|----------------------|---------------------|
| RX IN0+      | 12        | V31              | LVDS Input           | R65 (100 $\Omega$ ) |
| RX IN0-      | 13        | V30              |                      |                     |
| RX IN1+      | 22        | W34              | LVDS Input           | R63 (100 $\Omega$ ) |
| RX IN1-      | 23        | W33              |                      |                     |
| RX IN2+      | 20        | W32              | LVDS Input           | R60 (100 $\Omega$ ) |
| RX IN2-      | 21        | W31              |                      |                     |
| RX IN3+      | 14        | W29              | LVDS Input           | R58 (100 $\Omega$ ) |
| RX IN3-      | 15        | W28              |                      |                     |
| RX CLKIN+    | 4         | U28              | LVDS Input           | R61 (100 $\Omega$ ) |
| RX CLKIN-    | 5         | V28              |                      |                     |

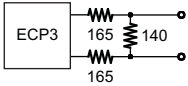
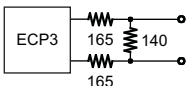
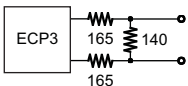
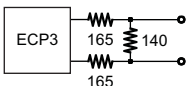
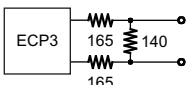
**Table 24. RJ45 Connections (J44 and J45)**

| Signal Name | Pin#    | LatticeECP3 Pin# | LatticeECP3 Pin Type | External Resistor   |
|-------------|---------|------------------|----------------------|---------------------|
| RJ45_OUT_P0 | 1 (J44) | W27              | True LVDS Output     | None                |
| RJ45_OUT_N0 | 2 (J44) | W26              |                      |                     |
| RJ45_OUT_P1 | 3 (J44) | AA25             | True LVDS Output     | None                |
| RJ45_OUT_N1 | 6 (J44) | AA26             |                      |                     |
| RJ45_OUT_P2 | 4 (J44) | W30              | Emulated LVDS Output | None                |
| RJ45_OUT_N2 | 5 (J44) | W29              |                      |                     |
| RJ45_OUT_P3 | 7 (J44) | Y26              | True LVDS Output     | None                |
| RJ45_OUT_N3 | 8 (J44) | Y25              |                      |                     |
| RJ45_IN_P0  | 1 (J45) | AM34             | LVDS Input           | R65 (100 $\Omega$ ) |
| RJ45_IN_N0  | 2 (J45) | AM33             |                      |                     |
| RJ45_IN_P1  | 3 (J45) | AC32             | LVDS Input           | R63 (100 $\Omega$ ) |
| RJ45_IN_N1  | 6 (J45) | AC31             |                      |                     |

**Table 24. RJ45 Connections (J44 and J45) (Continued)**

| Signal Name | Pin#    | LatticeECP3 Pin# | LatticeECP3 Pin Type | External Resistor   |
|-------------|---------|------------------|----------------------|---------------------|
| RJ45_IN_P2  | 4 (J45) | AA34             | LVDS Input           | R60 (100 $\Omega$ ) |
| RJ45_IN_N2  | 5 (J45) | AA33             |                      |                     |
| RJ45_IN_P3  | 7 (J45) | P30              | LVDS Input           | R58 (100 $\Omega$ ) |
| RJ45_IN_N3  | 8 (J45) | R29              |                      |                     |

**Table 25. CameraLink Rx Connections (J12)**

| Signal Name | J12 Pin # | LatticeECP3 Pin# | LatticeECP3 Pin Type | External Resistor                                                                              |
|-------------|-----------|------------------|----------------------|------------------------------------------------------------------------------------------------|
| X0+         | 12        | U32              | LVDS Input           | R80 (100 $\Omega$ )                                                                            |
| X0-         | 25        | U31              |                      |                                                                                                |
| X1+         | 11        | U34              | LVDS Input           | R76 (100 $\Omega$ )                                                                            |
| X1-         | 24        | U33              |                      |                                                                                                |
| X2+         | 10        | T34              | LVDS Input           | R71 (100 $\Omega$ )                                                                            |
| X2-         | 23        | T33              |                      |                                                                                                |
| X3+         | 8         | T32              | LVDS Input           | R68 (100 $\Omega$ )                                                                            |
| X3-         | 21        | T31              |                      |                                                                                                |
| XCLK+       | 9         | U26              | LVDS Input           | R70 (100 $\Omega$ )                                                                            |
| XCLK-       | 22        | U27              |                      |                                                                                                |
| SerTC+      | 20        | N30              | Emulated LVDS Output | RN33A<br>  |
| SerTC-      | 7         | N29              |                      |                                                                                                |
| SerTFG+     | 6         | P32              | LVDS Input           | R206 (100 $\Omega$ )                                                                           |
| SerTFG-     | 19        | P31              |                      |                                                                                                |
| CC1+        | 5         | R34              | Emulated LVDS Output | RN32A<br> |
| CC1-        | 18        | R33              |                      |                                                                                                |
| CC2+        | 17        | R31              | Emulated LVDS Output | RN32B<br> |
| CC2-        | 4         | R30              |                      |                                                                                                |
| CC3+        | 3         | P34              | Emulated LVDS Output | RN31A<br> |
| CC3-        | 16        | P33              |                      |                                                                                                |
| CC4+        | 15        | N34              | Emulated LVDS Output | RN31B<br> |
| CC4-        | 2         | N33              |                      |                                                                                                |

## DVI Video Interface

There are two DVI video connectors on this board, one for DVI receive and the other for DVI transmit. The I/Os on the banks 0 and 1 of LatticeECP3 support the TRLVDS (Transition Reduced LVDS) I/O standard and can be used to receive video signals with TMDS standard such as DVI and HDMI. These I/Os can support a maximum band-

width of up to 1Gbps. The TMDS signals of DVI Rx connector (J16). For DVI Tx, the TMDS transmitter TFP410 from TI is used to convert and encode the parallel R, G, B pixel data to TMDS signals. These TMDS signals are then connected to J14.

Tables 26 and 27 show the LatticeECP3 pin connections to these two DVI connectors.

**Table 26. DVI Rx Connections (J16)**

| J16 Pin # | Pin Name        | LatticeECP3 Pin # | Description             |
|-----------|-----------------|-------------------|-------------------------|
| 18        | TMDS_Data0+     | C16               | TMDS Blue Data Channel  |
| 17        | TMDS_Data0-     | D16               |                         |
| 10        | TMDS_Data1+     | A16               | TMDS Green Data Channel |
| 9         | TMDS_Data1-     | B16               |                         |
| 2         | TMDS_Data2+     | C17               | TMDS Red Data Channel   |
| 1         | TMDS_Data2-     | D17               |                         |
| 23        | TMDS_Clock0+    | J17               | TMDS Clock Channel      |
| 24        | TMDS_Clock0-    | H17               |                         |
| 6         | DDC_Clock       | D14               | DVI Rx DDC Clock        |
| 7         | DDC_Data        | J15               | DVI Rx DDC Data         |
| 16        | Hot Plug Detect | F13               | DVI Rx Hot Plug Detect  |

**Table 27. DVI Tx Connections (J14)**

| J14 Pin # | J14 Pin Name           | TFP410 Pin | TFP410 Pin # | LatticeECP3 Pin # | Description             |
|-----------|------------------------|------------|--------------|-------------------|-------------------------|
| 18 and 17 | TMDS_Data0+TMDS_Data0- | DATA7      | 54           | A4 (MSB)          | TMDS Blue Data Channel  |
|           |                        | DATA6      | 55           | A5                |                         |
|           |                        | DATA5      | 58           | G12               |                         |
|           |                        | DATA4      | 59           | G13               |                         |
|           |                        | DATA3      | 60           | A12               |                         |
|           |                        | DATA2      | 61           | B12               |                         |
|           |                        | DATA1      | 62           | J14               |                         |
|           |                        | DATA0      | 63           | H13 (LSB)         |                         |
| 10 and 9  | TMDS_Data1+TMDS_Data1- | DATA15     | 44           | B3 (MSB)          | TMDS Green Data Channel |
|           |                        | DATA14     | 45           | A2                |                         |
|           |                        | DATA13     | 46           | D5                |                         |
|           |                        | DATA12     | 47           | C6                |                         |
|           |                        | DATA11     | 50           | B4                |                         |
|           |                        | DATA10     | 51           | A3                |                         |
|           |                        | DATA9      | 52           | D6                |                         |
|           |                        | DATA8      | 53           | C5 (LSB)          |                         |
| 2 and 1   | TMDS_Data2+TMDS_Data2- | DATA23     | 36           | C3 (MSB)          | TMDS Red Data Channel   |
|           |                        | DATA22     | 37           | C4                |                         |
|           |                        | DATA21     | 38           | D3                |                         |
|           |                        | DATA20     | 39           | C2                |                         |
|           |                        | DATA19     | 40           | B1                |                         |
|           |                        | DATA18     | 41           | B2                |                         |
|           |                        | DATA17     | 42           | E4                |                         |
|           |                        | DATA16     | 43           | D4 (LSB)          |                         |
| 6         | DDC_Clock              | —          | —            | C14               | DVI Tx DDC Clock        |

**Table 27. DVI Tx Connections (J14) (Continued)**

| J14 Pin # | J14 Pin Name | TFP410 Pin | TFP410 Pin # | LatticeECP3 Pin # | Description     |
|-----------|--------------|------------|--------------|-------------------|-----------------|
| 7         | DDC_Data     | —          | —            | G15               | DVI Tx DDC Data |
| —         | —            | IDCKP      | 57           | K14               | —               |
| —         | —            | DE         | 2            | D13               | —               |
| —         | —            | VSYNC      | 5            | J13               | —               |
| —         | —            | HSYNC      | 4            | H14               | —               |
| —         | —            | ISEL/RSTN  | 13           | G21               | —               |
| —         | —            | BSEL/SCL   | 15           | B13               | —               |
| —         | —            | DSEL/SDA   | 14           | A13               | —               |

## RS-232 Interface

A 2x5 header (J38) provides a RS-232 port connection to the LatticeECP3 device via a RS-232 transceiver MAX232. Either the DB25 or DB9 cable can be connected to this header for providing a RS-232 port with industrial standard pinout. Table 28 shows the pin connections of this header.

**Table 28. RS-232 Interface Header Pin Connections (J38)**

| J38 Pin # | Pin Name | Net Name  | LatticeECP3 Pin # | J38 Pin # | Pin Name | Net Name | LatticeECP3 Pin # |
|-----------|----------|-----------|-------------------|-----------|----------|----------|-------------------|
| 1         | N.C.     | —         | —                 | 2         | N.C.     | —        | —                 |
| 3         | TXD      | RS232_TXD | F12 (Input)       | 4         | N.C.     | —        | —                 |
| 5         | RXD      | RS232_RXD | E11 (Output)      | 6         | N.C.     | —        | —                 |
| 7         | N.C.     | —         | —                 | 8         | N.C.     | —        | —                 |
| 9         | N.C.     | GND       | —                 | 10        | N.C.     | —        | —                 |

## LCD Interface

A 2x9 header (J43) provides a connection to LCD modules such as the 20-character x 2 line LCD module LCM-S02002DSR or LCM-S02002DSR (with backlight LED) from Lumex. The board includes two variable resistors for LCD adjustments. VR6 adjusts the backlight and VR5 provides contrast adjustment. A user design must be included in the FPGA to drive this feature. This header can also be used for probe points for observing FPGA pins. Pin 1 and Pin 2 of header J43 are dummy pins that connect to nothing. When installing the Lumex LCD module, these two pins should be skipped. Table 29 shows the pin connections of this header.

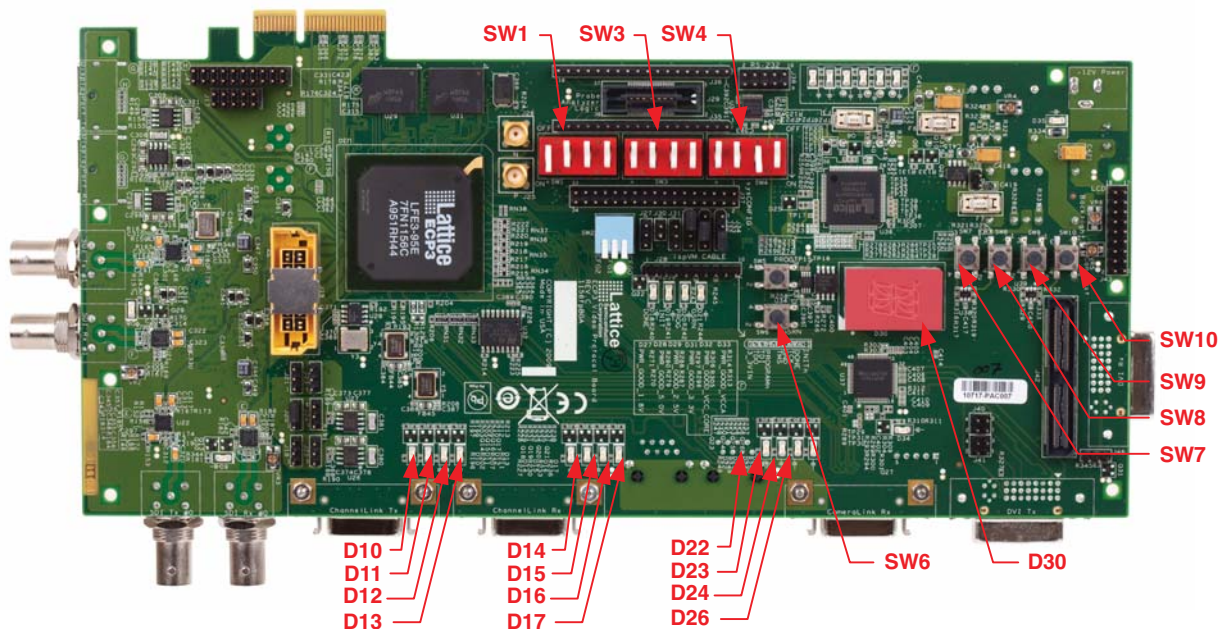
**Table 29. LCD Interface Header Pin Connections (J43)**

| J43 Pin# | LatticeECP3 Pin # | LCM-S02002 Pin # | Net Names         | J43 Pin# | LatticeECP3 Pin # | LCM-S02002 Pin# | Net Names       |
|----------|-------------------|------------------|-------------------|----------|-------------------|-----------------|-----------------|
| 1        | —                 | —                | N.C. (Dummy)      | 2        | —                 | —               | N.C. (Dummy)    |
| 3        | —                 | 1                | GND               | 4        | —                 | 2               | 5V              |
| 5        | —                 | 3                | VO (Contrast)     | 6        | H15               | 4               | LCD5 / LCD_RS   |
| 7        | A8                | 5                | LCD0 / LCD_R/W    | 8        | E17               | 6               | LCD6 / LCD_E    |
| 9        | A9                | 7                | LCD1 / LCD_DB0    | 10       | B14               | 8               | LCD7 / LCD_DB1  |
| 11       | A7                | 9                | LCD2 / LCD_DB2    | 12       | A14               | 10              | LCD8 / LCD_DB3  |
| 13       | E15               | 11               | LCD3 / LCD_DB4    | 14       | E13               | 12              | LCD9 / LCD_DB5  |
| 15       | D15               | 13               | LCD4 / LCD_DB6    | 16       | E12               | 14              | LCD10 / LCD_DB7 |
| 17       | —                 | 15               | ANODE (Backlight) | 18       | —                 | 16              | GND             |

## Switches and LEDs

There are many on-board DIP switches, push-button switches, discrete LEDs and a 16-segment LED display that can be used to provide static inputs and outputs for a design. Figure 9 shows the locations of these components.

**Figure 9. Switch and LED Locations**



## DIP Switches (SW1, SW3 and SW4)

There are three SPDT toggle-DIP switches on this board. Each of these switches includes four positions to make a total number of 12 static input signals to a design. Table 30 shows the pin connections and colors of these LEDs.

**Table 30. DIP Switch Connections**

| Switch # | Position # | Signal   | LatticeECP3 Pin # | LatticeECP3 I/O Bank (Voltage) |
|----------|------------|----------|-------------------|--------------------------------|
| SW1      | 1          | SWITCH1  | Y5                | Bank 6 (1.8V)                  |
|          | 2          | SWITCH2  | Y4                |                                |
|          | 3          | SWITCH3  | Y9                |                                |
|          | 4          | SWITCH4  | Y10               |                                |
| SW3      | 1          | SWITCH5  | AD2               |                                |
|          | 2          | SWITCH6  | AD1               |                                |
|          | 3          | SWITCH7  | AC6               |                                |
|          | 4          | SWITCH8  | AC7               |                                |
| SW4      | 1          | SWITCH9  | AM1               |                                |
|          | 2          | SWITCH10 | AM2               |                                |
|          | 3          | SWITCH11 | AE1               |                                |
|          | 4          | SWITCH12 | AE2               |                                |

## Push-button Switches (SW6, SW7, SW8, SW9 and SW10)

Five push-buttons can also be used to provide inputs that require pulses. There are de-bouncers between the push-buttons and the LatticeECP3 to remove the glitches of the push-button signals. When pressing these push-buttons, logic 0 will be sent to the connected LatticeECP3 pins. Table 31 shows the corresponding pin connections between the push-buttons and the LatticeECP3 pins.

**Table 31. Push-button Switch Connections**

| Signal | Switch # | LatticeECP3 Pin # | LatticeECP3 I/O Bank (Voltage) |
|--------|----------|-------------------|--------------------------------|
| GSRN   | SW6      | J20               | Bank 1 (2.5V)                  |
| PB4    | SW7      | U4                | Bank 7 (1.8V)                  |
| PB3    | SW8      | U5                |                                |
| PB2    | SW9      | P1                |                                |
| PB1    | SW10     | P2                |                                |

## Discrete LEDs (D10~D17, D22~D24, and D26)

There are 12 discrete LEDs for use as status indicators. These 12 LEDs are divided into three groups, (D10, D11, D12, D13), (D14, D15, D16, D17) and (D22, D23, D24, D26). Each group has four LEDs and each LED is in a different color. Table 32 shows the pin connections and colors of these LEDs.

**Table 32. Discrete LED Connections**

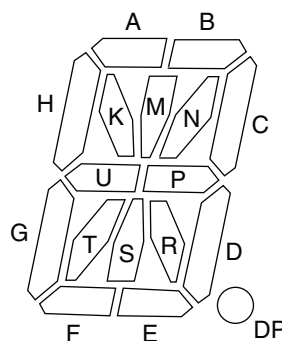
| Signal | LED # | LatticeECP3 Pin # | ECP3 I/O Bank (Voltage) | Color  |
|--------|-------|-------------------|-------------------------|--------|
| LED12  | D10   | AA31              | Bank 3 (2.5V)           | Blue   |
| LED11  | D11   | AN34              |                         | Green  |
| LED10  | D12   | AN33              |                         | Orange |
| LED9   | D13   | AP33              |                         | Red    |
| LED8   | D14   | AP32              |                         | Blue   |
| LED7   | D15   | AL32              |                         | Green  |
| LED6   | D16   | AK32              |                         | Orange |
| LED5   | D17   | N32               | Bank 2 (2.5V)           | Red    |
| LED4   | D22   | N31               |                         | Blue   |
| LED3   | D23   | T29               |                         | Green  |
| LED2   | D24   | T28               |                         | Orange |
| LED1   | D26   | T27               |                         | Red    |

## 16-Segment LED Display (D30)

The LatticeECP3 general-purpose I/O pins are connected to a 16-segment display, as shown in Table 33. These pins can be driven low to illuminate the display segments.

**Table 33. 16-Segment LED Display Connections**

| Segment | LatticeECP3 Pin |
|---------|-----------------|
| A       | H20             |
| B       | A18             |
| C       | G18             |
| D       | D18             |
| DP      | B18             |
| E       | L19             |
| F       | C19             |
| G       | J19             |
| H       | K19             |
| K       | G19             |
| M       | H19             |
| N       | K20             |
| P       | F19             |
| R       | H18             |
| S       | J18             |
| T       | D19             |
| U       | E18             |



## Logic Analyzer Connector and Test Points

For debugging purposes, all unused LatticeECP3 I/Os are connected to connectors/headers for debugging a design using test equipment such as logic analyzers or scopes.

### Logic Analyzer Connector

An on-board Mictor connector is connected to many LatticeECP3 I/Os to make it easy to use a logic analyzer for debugging the FPGA design. The Mictor connector pins are connected to different I/O banks with different Vccio voltages. Users may need to configure the threshold voltage of the logic analyzer pod to match the signals being monitored. Other than connecting to the Mictor connector, these LatticeECP3 pins are also connected to two standard 100-mil pitch headers for use with logic analyzers or scopes that do not support Mictor connection. Table 34 shows the LatticeECP3 pin connections to the Mictor connector and the two headers.

**Table 34. Logic Analyzer Connections (J29, J35 and J36)**

| J29 Pin # | Signal | J35 Pin # | J36 Pin # | LatticeECP3 Pin # | LatticeECP3 I/O Bank (Voltage) |
|-----------|--------|-----------|-----------|-------------------|--------------------------------|
| 1         | —      | —         | —         | —                 | —                              |
| 2         | —      | —         | —         | —                 | —                              |
| 3         | —      | —         | —         | GND               | —                              |
| 4         | —      | —         | —         | —                 | —                              |
| 5         | LA1    | —         | 1         | D33               | Bank 8 (3.3V)                  |
| 6         | LA2    | 1         | —         | D31               |                                |
| 7         | LA3    | —         | 2         | K15               | Bank 0 (3.3V)                  |
| 8         | LA4    | 2         | —         | C13               |                                |

**Table 34. Logic Analyzer Connections (J29, J35 and J36) (Continued)**

| J29 Pin # | Signal | J35 Pin # | J36 Pin # | LatticeECP3 Pin # | LatticeECP3 I/O Bank (Voltage) |
|-----------|--------|-----------|-----------|-------------------|--------------------------------|
| 9         | LA5    | —         | 3         | J22               | Bank 1 (2.5V)                  |
| 10        | LA6    | 3         | —         | J23               |                                |
| 11        | LA7    | —         | 4         | F22               |                                |
| 12        | LA8    | 4         | —         | G23               |                                |
| 13        | LA9    | —         | 5         | A24               |                                |
| 14        | LA10   | 5         | —         | B24               |                                |
| 15        | LA11   | —         | 6         | H22               |                                |
| 16        | LA12   | 6         | —         | H23               |                                |
| 17        | LA13   | —         | 7         | K23               |                                |
| 18        | LA14   | 7         | —         | K24               |                                |
| 19        | LA15   | —         | 8         | C28               |                                |
| 20        | LA16   | 8         | —         | D28               |                                |
| 21        | LA17   | —         | 9         | G26               |                                |
| 22        | LA18   | 9         | —         | AA2               | Bank 6 (1.8V)                  |
| 23        | LA19   | —         | 10        | AJ6               |                                |
| 24        | LA20   | 10        | —         | AL8               |                                |
| 25        | LA21   | —         | 11        | AM5               |                                |
| 26        | LA22   | 11        | —         | AM6               |                                |
| 27        | LA23   | —         | 12        | AN6               |                                |
| 28        | LA24   | 12        | —         | AL7               |                                |
| 29        | LA25   | —         | 13        | AM4               |                                |
| 30        | LA26   | 13        | —         | AP5               |                                |
| 31        | LA27   | —         | 14        | AP6               |                                |
| 32        | LA28   | 14        | —         | —                 | —                              |
| 33        | LA29   | —         | 15        | —                 | —                              |
| 34        | LA30   | 15        | —         | —                 | —                              |
| 35        | LA31   | —         | 16        | —                 | —                              |
| 36        | LA32   | 16        | —         | —                 | —                              |
| 37        | LA33   | —         | 17        | —                 | —                              |
| 38        | LA34   | 17        | —         | —                 | —                              |

## Known Issues

### 1. DDR2 Reference Voltage

There are two DDR2 devices on the board – U29 and U31. When the design is using only one DDR2 device, the DDR2\_REF signal for the unused DDR2 device will be pulled up by the unused LatticeECP3 pin. This pulls the Vref voltage away from the 0.9V generated by the LP2997 voltage regulator to around 1.6~1.7V. The DDR2 will not work with the wrong reference voltage; the DDR2 accesses will fail. The DDR2\_REF generated by LP2997 is connected to LatticeECP3 pin-V7(VREF1 of Bank 6 for the DDR2 device on U29) and pin-R9 (VREF1 of Bank 7 for the DDR2 device on U31). To avoid being pulled up to the wrong voltage, the unused VREF1 pin cannot be left unused because all unused pins will be pulled up by default. The easiest workaround is adding dummy logic with one input and one output, and then assigning this input pin to the unused VREF1 pin.

## 2. DDR2 Bandwidth

This board does not include the recommended DDR2 termination resistors. Because of this, DDR2 may not work correctly on this board at all frequencies. Performance on individual boards may vary, but testing shows the best results at 125MHz, 150 MHz and 250MHz. 200MHz operation may be compromised due to this termination issue. It has also been found that U31 tends to have such issue more likely than U29. Based on the above findings, the following is strongly recommended when using the on-board DDR2 memory:

- If only one memory device is needed, U29 is recommended over U31.
- DDR2 memory operating frequency around 200 MHz on this board should be avoided if possible.

If the operating frequency around 200 MHz cannot be avoided, the following may help work around or mitigate the issue:

- Set the DDR2 memory interface related pins on FPGA DRIVE = 8 and SLEWRATE = SLOW in Design Planner.
- Change the on-die-termination (ODT) of the DDR2 memory device. This can be done by setting the desired value for the extended mode register. ODT = 50Ω appears to be better than the others on the board tested, but this may vary from board to board. Users may wish to experiment with different ODT options to determine the best ODT value.

## Ordering Information

| Description                      | Ordering Part Number         | China RoHS Environment-Friendly Use Period (EFUP)                                    |
|----------------------------------|------------------------------|--------------------------------------------------------------------------------------|
| LatticeECP3 Video Protocol Board | LFE3-95EA-V-EVN <sup>1</sup> |  |

1. Some early revision C LatticeECP3 Video Protocol Boards have the LatticeECP3 “E” device installed (LFE3-95E-V-EVN). For these boards, see TN1180, [LatticeECP3 High-Speed I/O Interface](#), for information on the differences between the LatticeECP3 “E” and “EA” devices.

## Technical Support Assistance

Hotline: 1-800-LATTICE (North America)  
+1-503-268-8001 (Outside North America)

e-mail: [techsupport@latticesemi.com](mailto:techsupport@latticesemi.com)

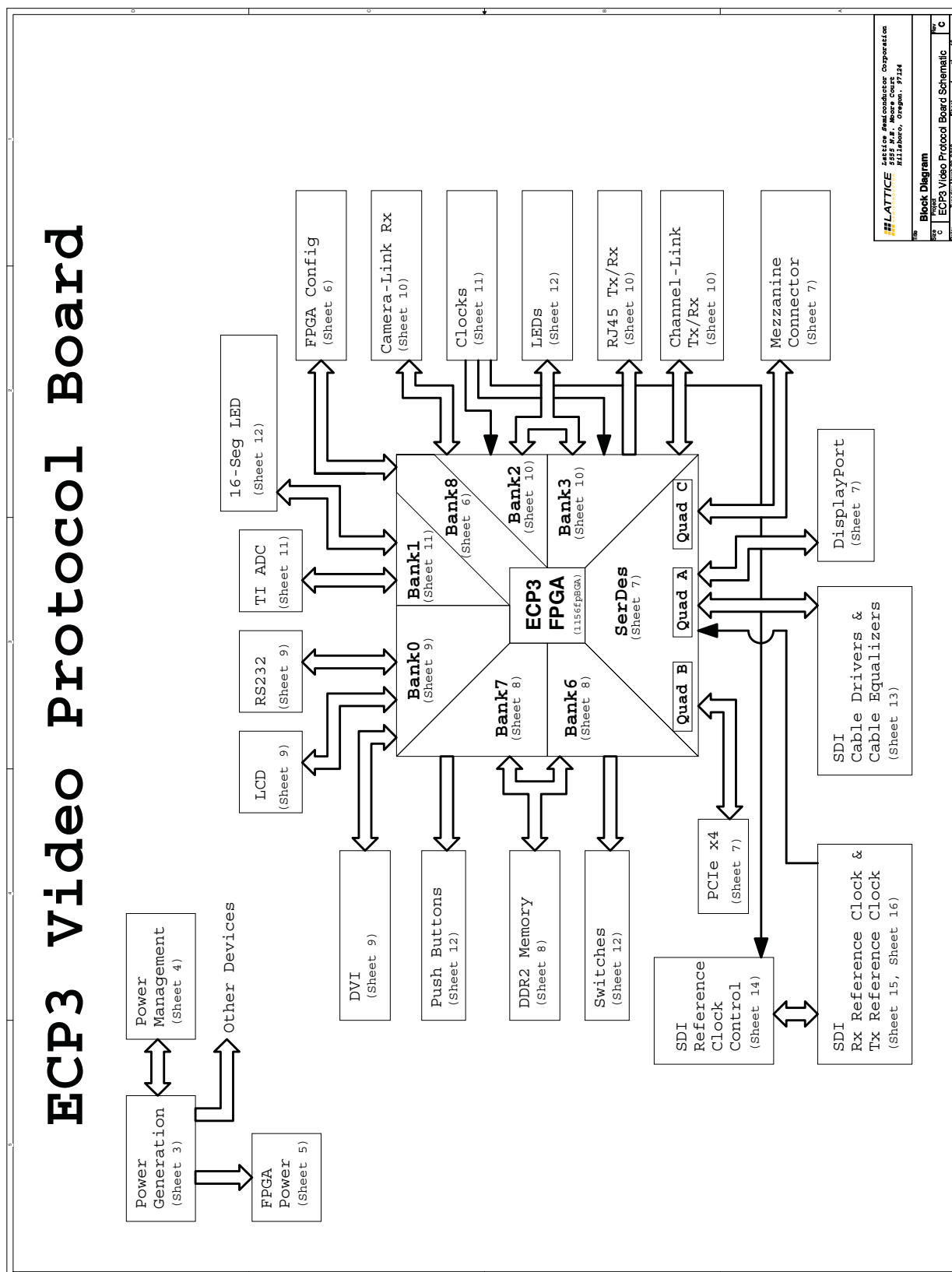
Internet: [www.latticesemi.com](http://www.latticesemi.com)

## Revision History

| Date         | Version | Change Summary                                                                              |
|--------------|---------|---------------------------------------------------------------------------------------------|
| March 2010   | 01.0    | Initial release.                                                                            |
| March 2011   | 01.1    | Added Known Issues text section.                                                            |
| May 2011     | 01.2    | Updated Ordering Information table for LFE3-95EA-V-EVN part number.                         |
| October 2012 | 01.3    | Updated document with new corporate logo.                                                   |
|              |         | Updated LatticeECP3 pin numbers in the Push-button Switch Connections table.                |
|              |         | FPGA Configuration schematic – Updated name of PR5A in the ECP3 Configuration I/Os section. |

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**Figure 10. Block Diagram**



[illegible]

**GND Vias (40-mil) for soldering pins.**  
Distributed around the board as GND reference for test equipment.

**POWER INPUT**

**1.2V Core**

**1.2V I/O Buffer**

**1.5V for SerDes I/O Buffer**

**3.3V for SD/HDP/G-SDI Cable Drivers and Equalizers**

**3.3V for SD/HDP/G-SDI Clocking Circuitry**

**5.0V**

**1.2V Video Core**

**1.2V I/O Buffer**

**1.5V for SerDes I/O Buffer**

**3.3V for SD/HDP/G-SDI Cable Drivers and Equalizers**

**3.3V for SD/HDP/G-SDI Clocking Circuitry**

**5.0V**

**1.2V Video Core**

**1.2V I/O Buffer**

**1.5V for SerDes I/O Buffer**

**3.3V for SD/HDP/G-SDI Cable Drivers and Equalizers**

**3.3V for SD/HDP/G-SDI Clocking Circuitry**

**5.0V**

The schematic diagram illustrates the power management and peripheral components of the Lattice iSPAC development board. Key features include:

- Power Management:** A 12V input is regulated to 5V by a LDO (LP3878). This 5V rail is then converted to 3.3V, 2.5V, 1.8V, and 1.2V by a series of DC-DC converters (MCP1802, MCP1801, MCP1800, MCP1803).
- Microcontroller:** The Lattice iSPAC chip is the central component, with various pins connected to the power rails and peripherals.
- Peripherals:** The board includes a USB-to-UART bridge (FT232RL), a USB-to-serial converter (MAX3232), and various LEDs and status indicators.
- Connectors:** The board has a 12V input terminal, a USB connector, and a serial connector.

The diagram is a detailed representation of the board's internal circuitry, showing the connections between the various components and the power rails.

Figure 14. FPGA Power

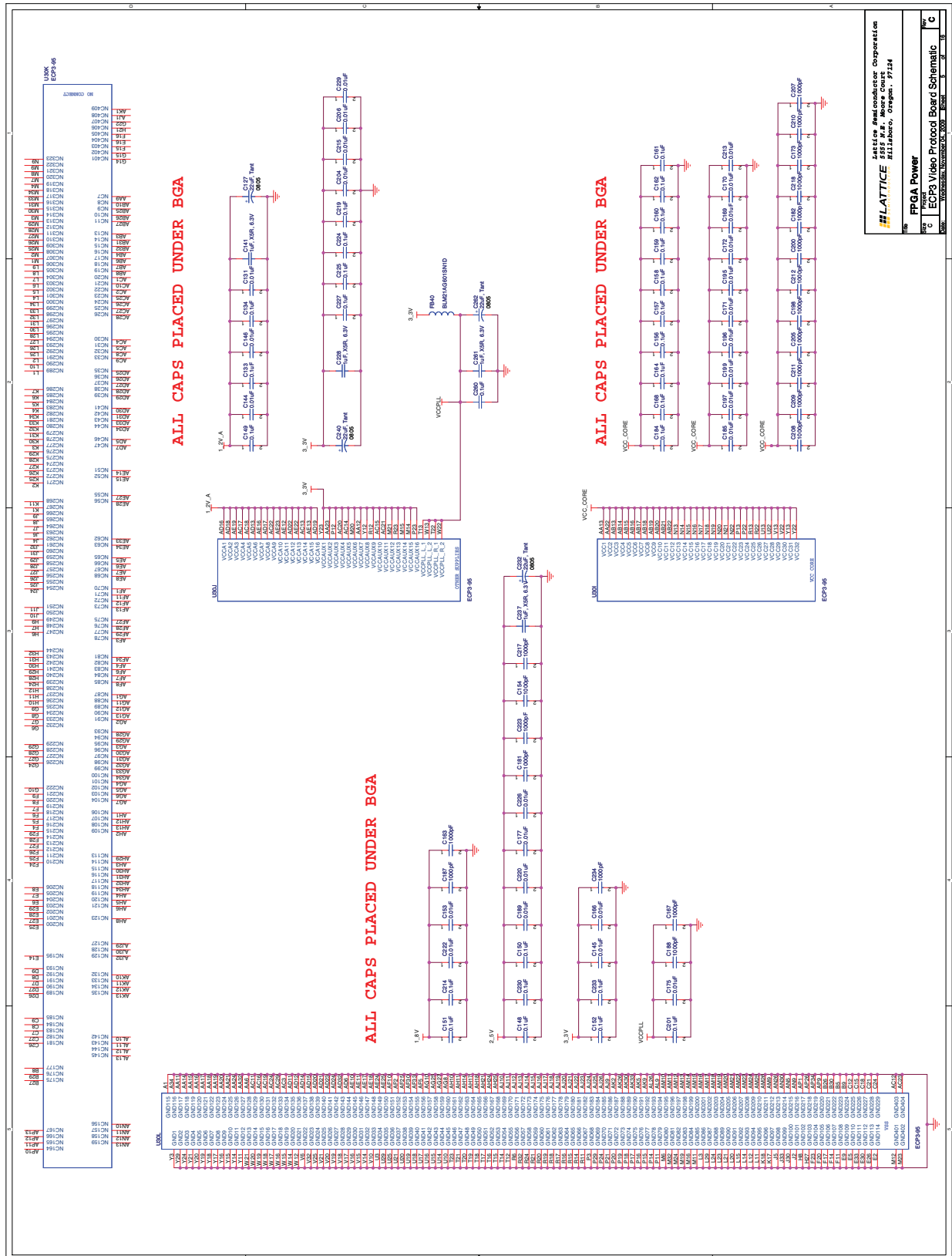


Figure 15. FPGA Configuration

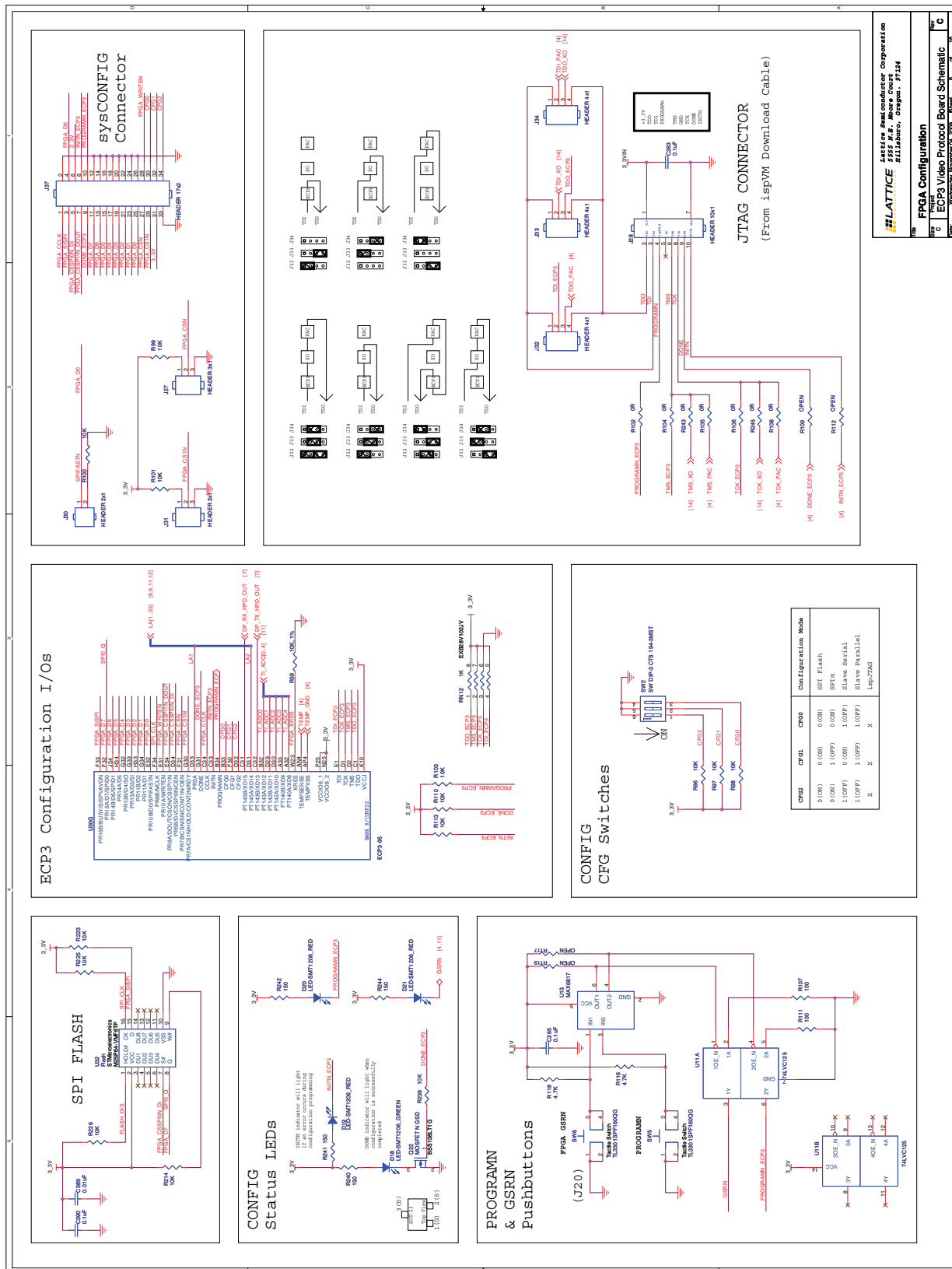


Figure 16. SERDES

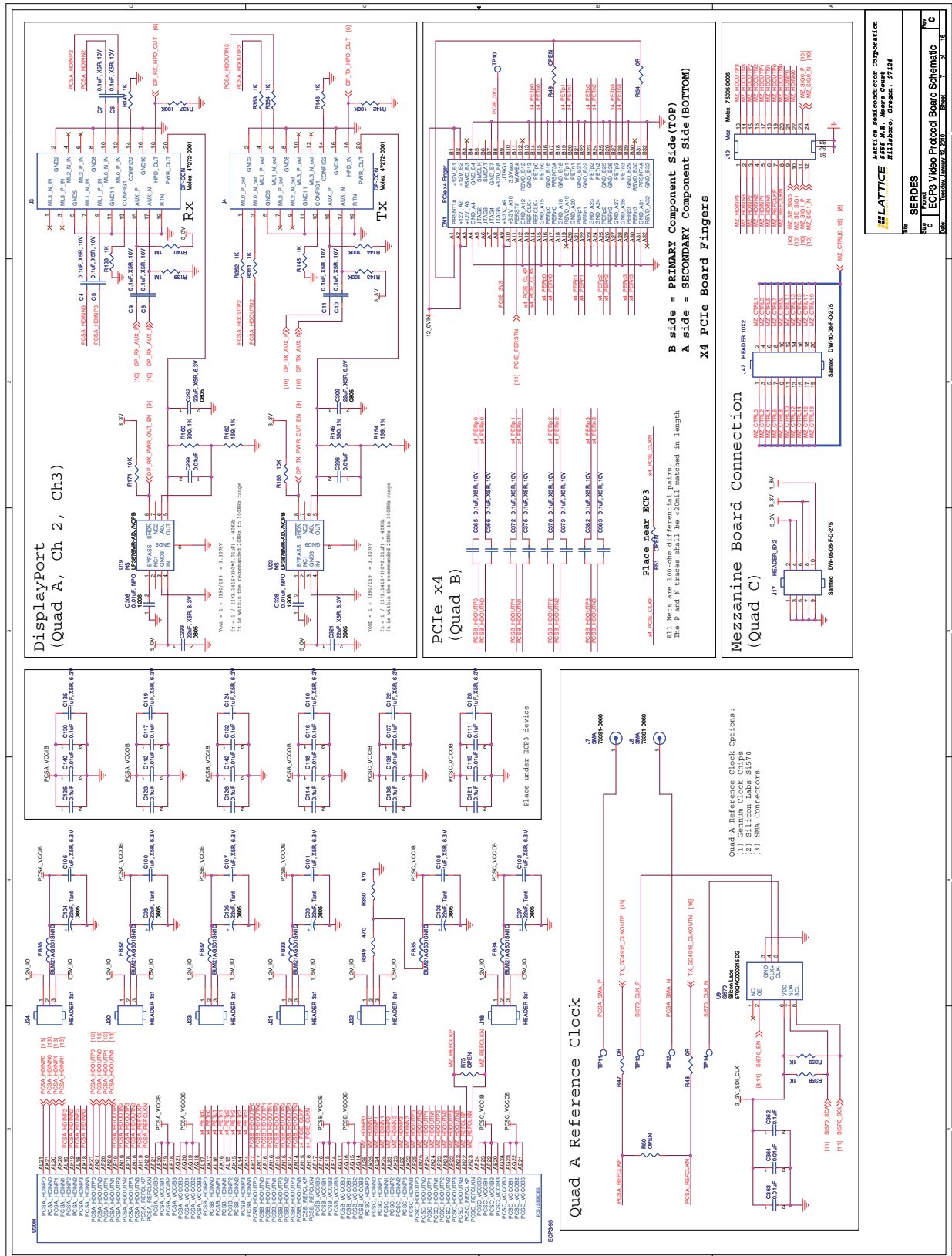
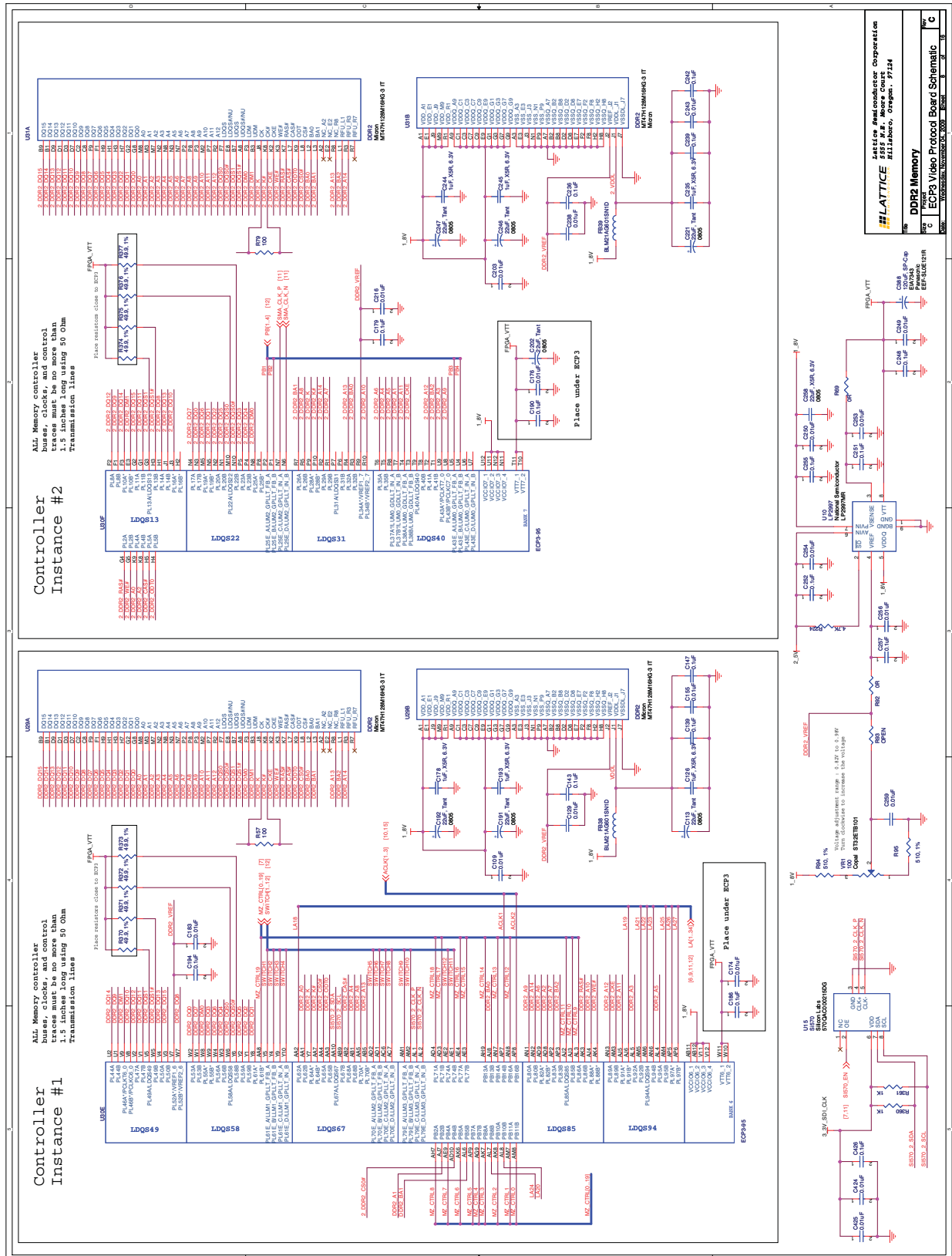


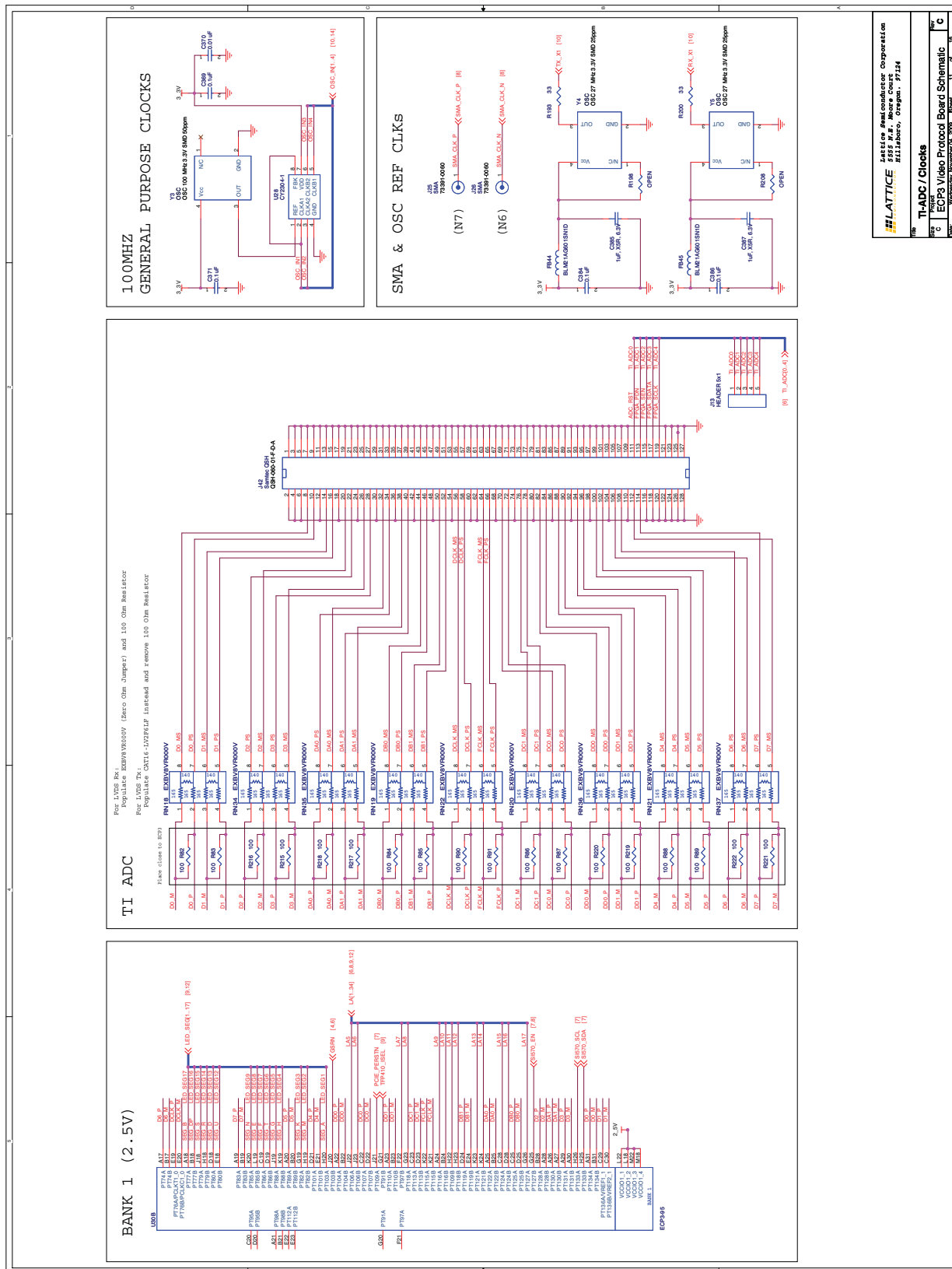
Figure 17. DDR2 Memory



The schematic diagram illustrates the internal circuitry of the ECP3 Video Protocol Board. It features a central LCD Connector (J1) with pins for data, control, and power. The board includes an RS-232 interface (J2) for communication. Power is supplied via a 3.3V regulator (U1) and a 5V regulator (U2). The diagram shows various components such as resistors (R1-R10), capacitors (C1-C10), and integrated circuits (U1-U10). The board is populated with a DVI-D connector (J1) and a DVI-I connector (J2). The schematic also shows the connection of the board to a video source (J3) and a video sink (J4). The board is designed to be compatible with the ECP3 Video Protocol and the RS-232 interface.

[illegible]

Figure 20. TI-ADC/Clocks



[illegible]

Equalizer channel 0

Equalizer channel 1

Driver channel 0

Driver channel 1

SDI Rx #0

SDI Rx #1

SDI Tx #0

SDI Tx #1

ECPS Video Protocol Board Schematic

Lattice Semiconductor Corporation

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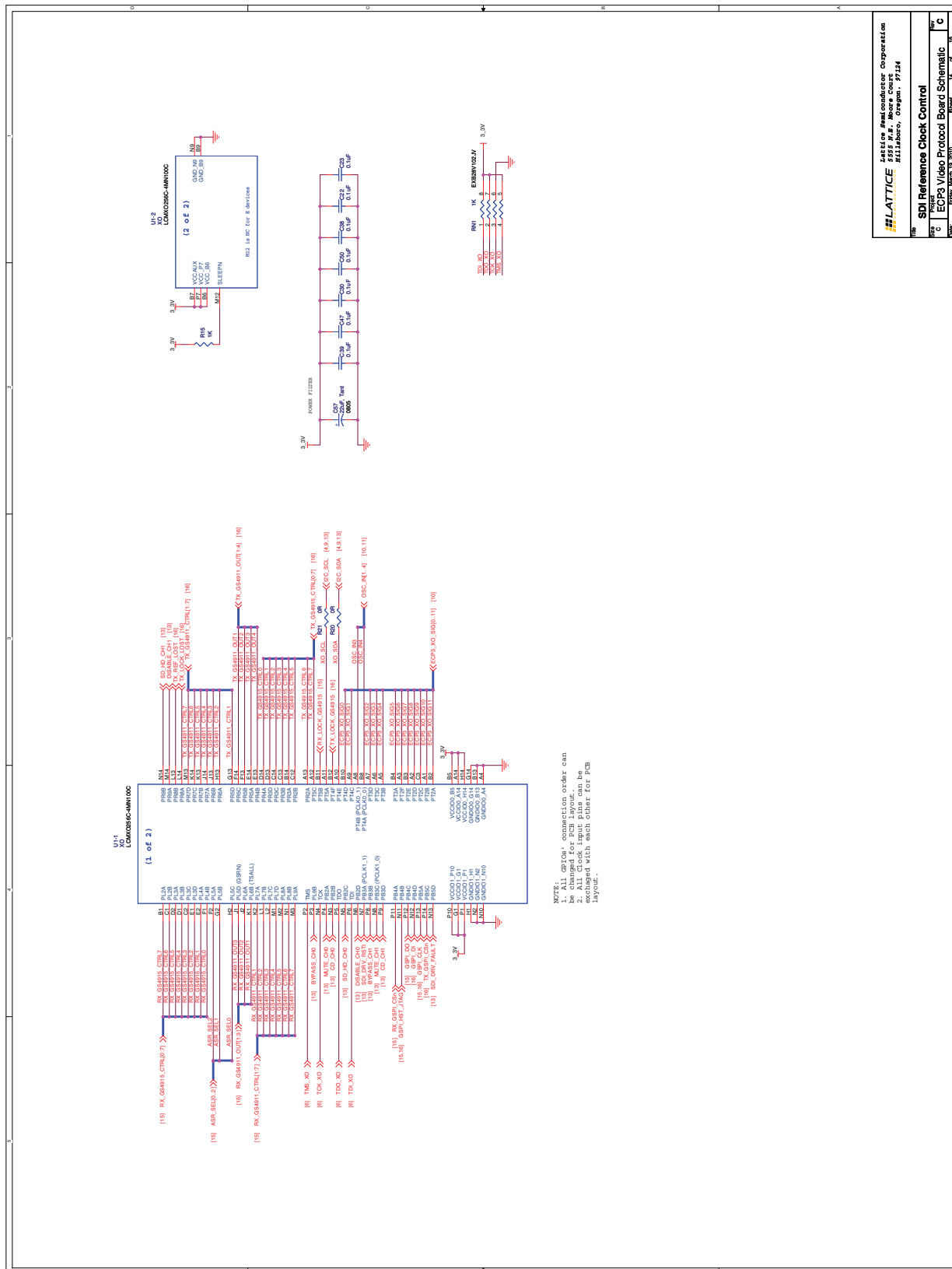
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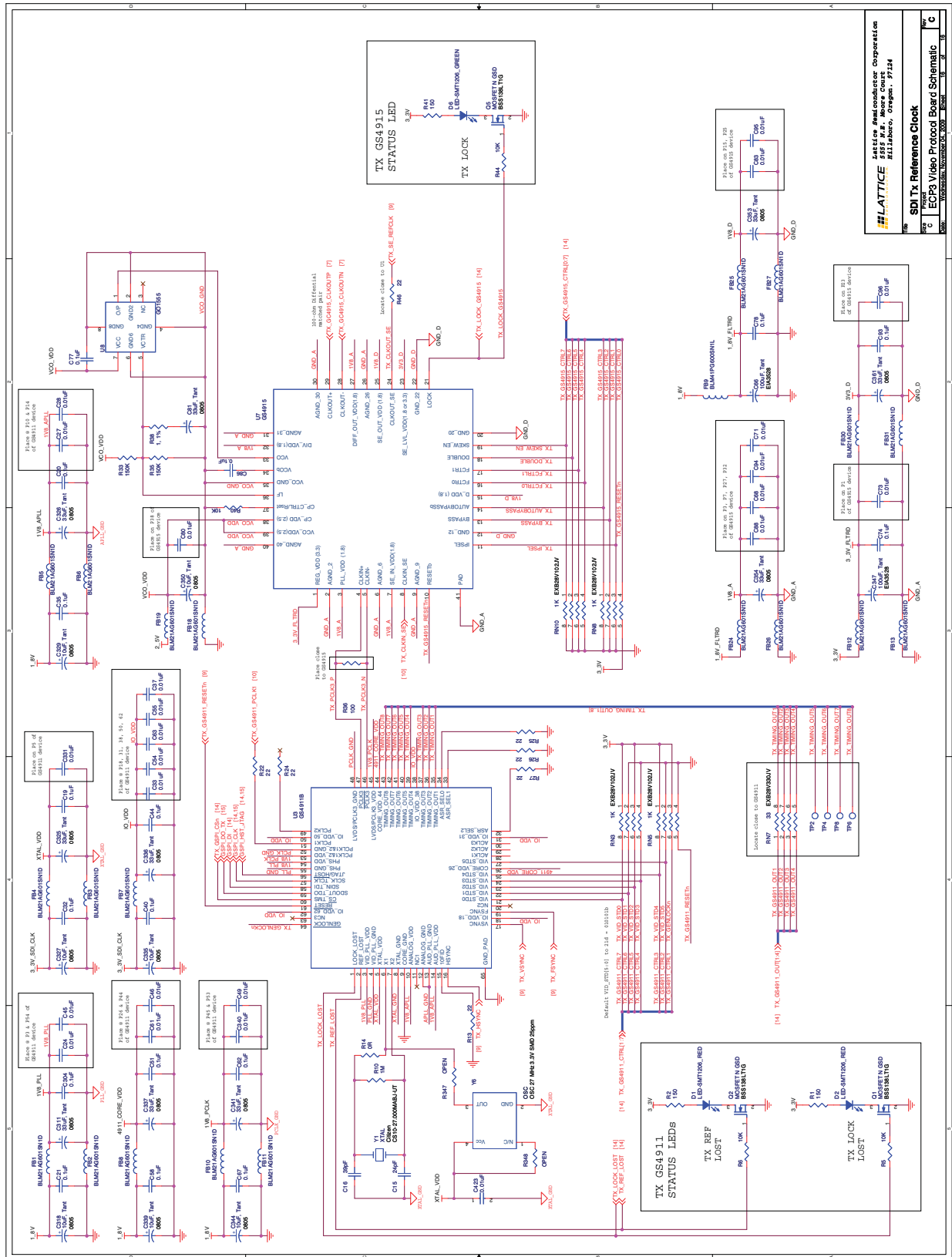
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Figure 23. SDI Reference Clock Control



[illegible]

Figure 25. SDI Tx Reference Clock



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