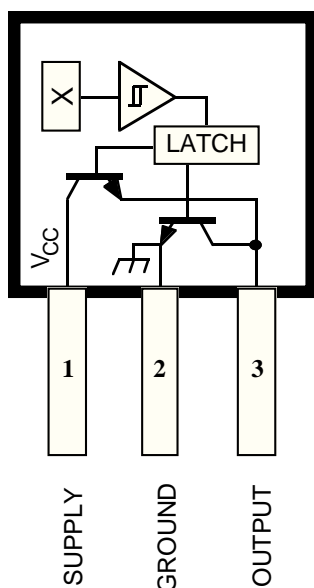


## PROTECTED, HIGH-TEMPERATURE, HALL-EFFECT LATCH WITH ACTIVE PULL-DOWN



Dwg. PH-013

Pinning is shown viewed from branded side.

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{CC}$ (100 ms) .....	115 V*
(continuous) .....	26 V
Reverse Battery Voltage, $V_{RCC}$ (100 ms) .....	-100 V
(continuous) .....	-30 V
Magnetic Flux Density, $B$ .....	Unlimited
Reverse Output Voltage, $V_{OUT}$ .....	-0.5 V
Continuous Output Current, $I_{OUT}$ .....	Internally Limited
Package Power Dissipation, $P_D$ .....	See Graph
Junction Temperature, $T_J$ .....	170°C
Operating Temperature Range, $T_A$	
Suffix "E-" .....	-40°C to +85°C
Suffix "L-" .....	-40°C to +150°C
Storage Temperature, $T_S$ .....	170°C

\*Fault condition, internal overvoltage shutdown above 28 V.

These Hall-effect latches are capable of sensing magnetic fields while using an unprotected power supply. The A3195- can provide position and speed information by providing a digital output for magnetic fields that exceed their predefined switch points. These devices operate down to zero speed and have switch points that are designed to be extremely stable over a wide operating temperature and voltage range. The latching characteristics make them ideal for use in pulse counting applications when used with a multi-pole ring magnet. A 25 mA high-side driver combined with an active pull-down is especially useful for driving capacitive loads. Output short-circuit protection allows for an increased wiring harness fault tolerance. The temperature compensated switch points, the wide operating voltage range, and the integrated protection make these devices ideal for use in automotive applications such as transmission speed sensors and integrated wheel bearing speed sensors.

Each monolithic device contains an integrated Hall-effect transducer, a temperature-compensated comparator, a voltage regulator, and a buffered high-side driver with an active pull-down. Supply protection is made possible by the integration of overvoltage shutdown circuitry that monitors supply fault conditions. Output protection circuitry includes source and sink current limiting for short circuits to supply or ground.

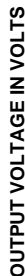
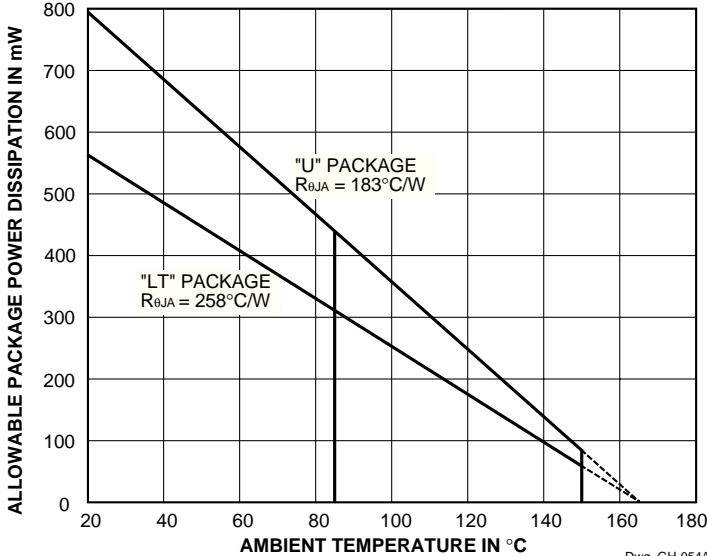
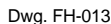
The A3195E- is rated for operation over a temperature range of -40°C to +85°C; the A3195L- is rated for operation over an extended temperature range of -40°C to +150°C. They are supplied in a three-lead SIP (suffix -U) or a surface-mount SOT-89 (suffix -LT).

### FEATURES

- Internal Protection For Automotive (ISO/DIN) Transients
- Operation From Unregulated Supply
- Reverse Battery Protection
- Undervoltage Lockout
- Supply Noise-Suppression Circuitry
- Output Short-Circuit Protection
- Output Zener Clamp
- Thermal Protection
- Symmetrical Latching Switch Points
- Operable with Multipole Ring Magnets

Always order by complete part number, e.g., **A3195LU**.

## PROTECTED, HIGH-TEMP., ACTIVE PULL-DOWN HALL-EFFECT LATCH



# 3195

## PROTECTED, HIGH-TEMP., ACTIVE PULL-DOWN HALL-EFFECT LATCH

### ELECTRICAL CHARACTERISTICS

over operating voltage and temperature range (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage	$V_{CC}$	Operating (but $V_{CC} \times I_{CC}$ vs $T_A$ limited)	3.8	12	26	V
Overvoltage Shutdown*	$V_{CC(OV)}$	$B > B_{OP}$	28	—	55	V
Output Voltage, High (Source Voltage)	$V_{OUT(H)}$	$B < B_{RP}$ , $I_{OUT} = -20$ mA	$V_{CC} - 2$	—	$V_{CC} - 0.3$	V
Output Voltage, Low (Sink Voltage)	$V_{OUT(L)}$	$B > B_{OP}$ , $I_{OUT} < 100$ $\mu$ A	—	0.1	0.2	V
		$B > B_{OP}$ , $I_{OUT} = 5$ mA	—	0.25	0.5	V
Output Clamp Voltage	$V_{OUT(CLMP)}$	$B < B_{RP}$ , $V_{CC} > 26$ V, $I_{OUT} = 0$	15	18	21	V
Output Current Limit	$I_{OUTMAX}$	$B < B_{RP}$ , $V_{CC} = 12$ V	-26	—	-70	mA
		$B > B_{OP}$ , $V_{OUT} < 14$ V	8.0	—	25	mA
Supply Current	$I_{CC}$	$B < B_{RP}$ , $V_{CC} = 18$ V, $I_{OUT} = 0$	—	6.0	9.0	mA
		$B > B_{OP}$ , $V_{CC} = 18$ V, $I_{OUT} = 0$	—	8.0	12	mA
		$V_{CC} = +115$ V*	—	8.0	17	mA
Reverse Battery Current*	$I_{RCC}$	$V_{RCC} = -35$ V*	—	-0.1	-5.0	mA
		$V_{RCC} = -100$ V*	—	-0.1	-10	mA
Output Rise Time	$t_r$	$C_L = 20$ pF, $R_L = 330$ $\Omega$	—	0.12	2.0	$\mu$ s
Output Fall Time	$t_f$	$C_L = 20$ pF, $R_L = 330$ $\Omega$	—	0.30	5.0	$\mu$ s
Package Thermal Resist.	$R_{\theta JA}$	"LT" Package	—	258	—	$^{\circ}$ C/W
		"U" Package	—	183	—	$^{\circ}$ C/W

### MAGNETIC CHARACTERISTICS

over operating voltage range (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Operate Point	$B_{OP}$	$T_A = -40^{\circ}$ C	60	125	200	G
		$T_A = +25^{\circ}$ C	50	110	160	G
		$T_A = \text{Maximum}$	40	100	150	G
Release Point	$B_{RP}$	$T_A = -40^{\circ}$ C	-200	-125	-60	G
		$T_A = +25^{\circ}$ C	-160	-110	-50	G
		$T_A = \text{Maximum}$	-150	-100	-40	G
Hysteresis ( $B_{OP} - B_{RP}$ )	$B_{hys}$	$T_A = -40^{\circ}$ C	150	250	—	G
		$T_A = +25^{\circ}$ C	130	220	—	G
		$T_A = \text{Maximum}$	110	200	—	G

NOTES: Negative current is defined as coming out of (sourcing) the output.

$B_{OP}$  = magnetic operate point (output turns ON);  $B_{RP}$  = magnetic release point (output turns OFF).

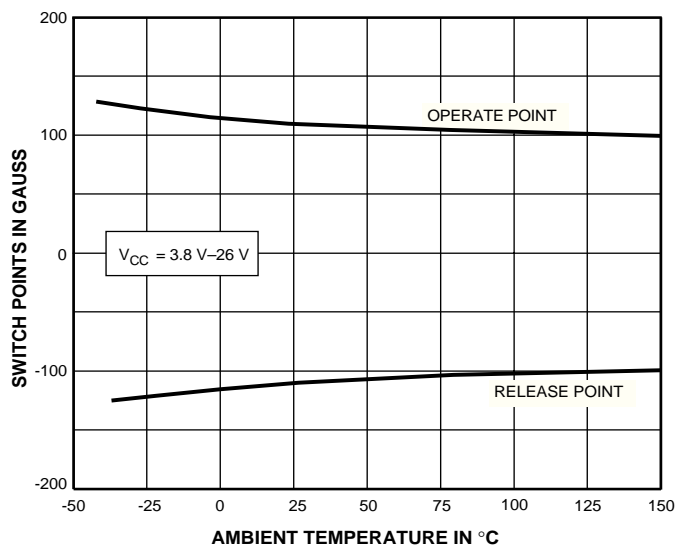
As used here, negative flux densities are defined as less than zero (algebraic convention).

Typical values are at  $T_A = +25^{\circ}$ C and  $V_{CC} = 12$  V.

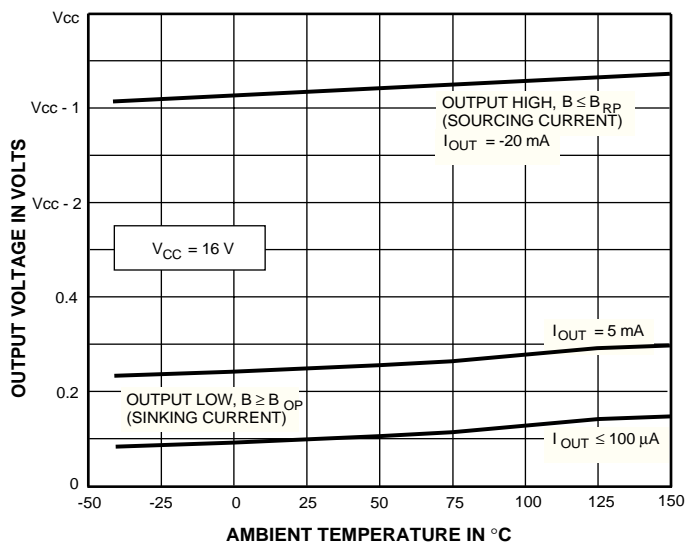
\* Fault condition. Device is shut down and operation is not possible.

# 3195 PROTECTED, HIGH-TEMP., ACTIVE PULL-DOWN HALL-EFFECT LATCH

## TYPICAL OPERATING CHARACTERISTICS



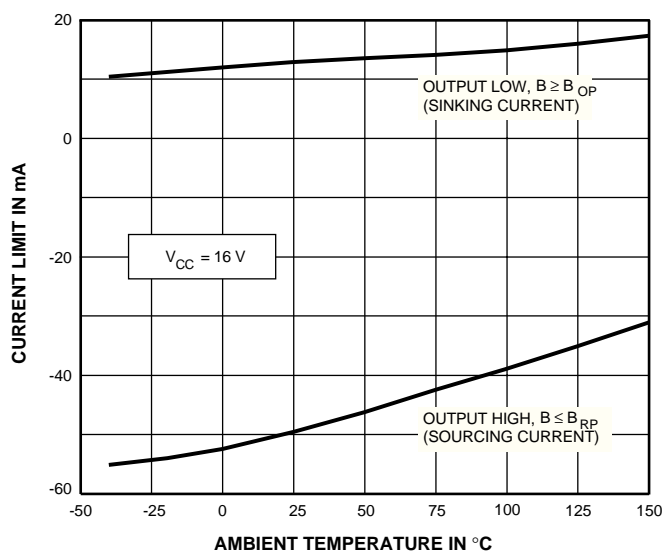
Dwg. GH-052-1



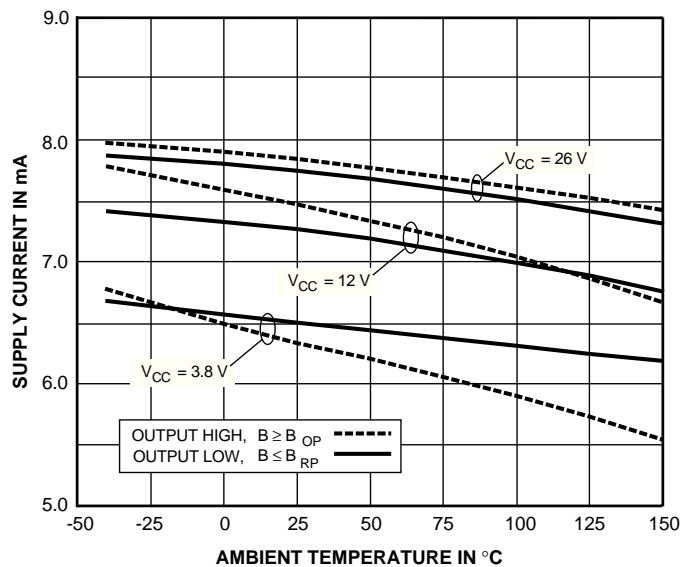
Dwg. GH-040-2

## TYPICAL OPERATING CHARACTERISTICS

### Output Current Limit



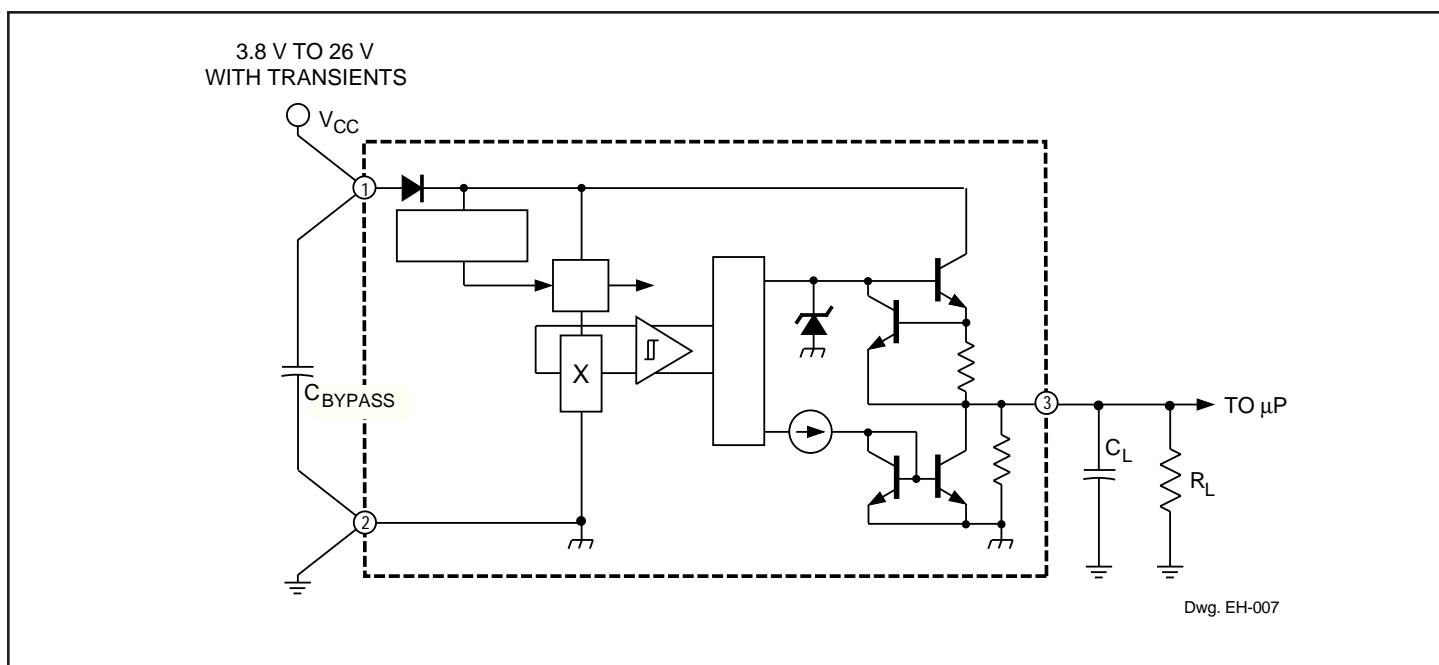
Dwg. GH-004-1



Dwg. GH-028-2

# 3195

## PROTECTED, HIGH-TEMP., ACTIVE PULL-DOWN HALL-EFFECT LATCH



### OPERATION

In operation, the output transistor is OFF until the strength of the magnetic field perpendicular to the surface of the chip exceeds the threshold or operate point ( $B_{OP}$ ). When the field strength exceeds  $B_{OP}$ , the output transistor switches ON (a logic low) and is capable of sinking 35 mA of current.

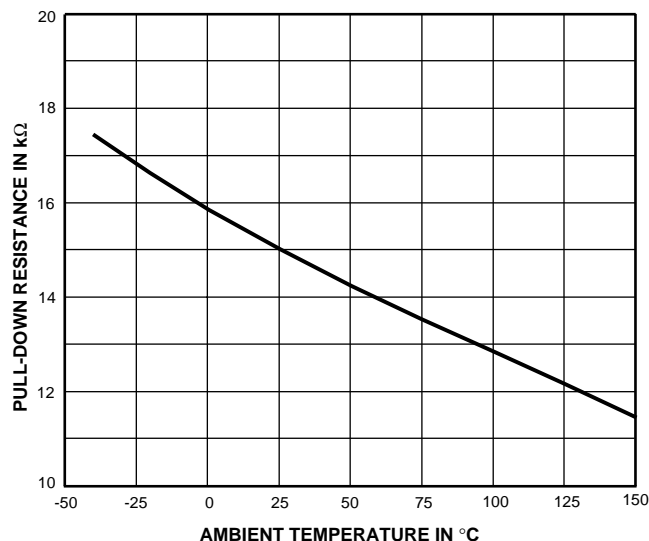
The output transistor switches OFF (a logic high) when magnetic field reversal results in a magnetic flux density below the OFF threshold ( $B_{RP}$ ). This is illustrated in the transfer characteristics graph. Note that the device latches; that is, a south pole of sufficient strength will turn the device ON. Removal of the south pole will leave the device ON. The presence of a north pole of sufficient strength is required to turn the device OFF.

The switch points increase in sensitivity with increasing temperature to compensate for the typical ferrite magnet temperature characteristic. The simplest form of magnet that will operate these devices is a ring magnet. Other methods of operation are possible.

### TEST CIRCUIT AND TYPICAL APPLICATION

An external 0.1  $\mu\text{F}$  to 0.47  $\mu\text{F}$  capacitor, with good high-frequency characteristics, should be connected between terminals 1 and 2 to bypass high-voltage noise and reduce EMI susceptibility.

**Internal Pull-Down Resistor.** An internal pull-down resistor (nominal 15 k $\Omega$ ) is provided to allow testing of the device without the need for an external load.

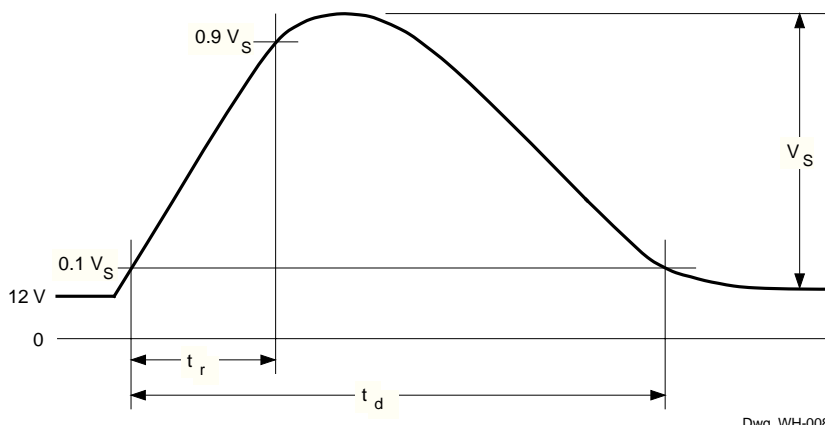


Dwg. GH-060

# 3195 PROTECTED, HIGH-TEMP., ACTIVE PULL-DOWN HALL-EFFECT LATCH

## INTERNAL PROTECTIVE FEATURES

ISO Pulse No.	Test	Test Conditions (at $T_A = +25^\circ\text{C}$ )
1	Inductive Turn Off (Negative)	$V_S = -100\text{ V}$ , $R_S = 10\ \Omega$ , $t_r = 1\ \mu\text{s}$ , $t_d = 2\text{ ms}$
2	Inductive Turn Off (Positive)	$V_S = 90\text{ V}$ , $R_S = 10\ \Omega$ , $t_r = 1\ \mu\text{s}$ , $t_d = 50\ \mu\text{s}$
3a	Capacitive/Inductive Coupling (Neg)	$V_S = -150\text{ V}$ , $R_S = 50\ \Omega$ , $t_r = 50\text{ ns}$ , $t_d = 100\text{ ns}$
3b	Capacitive/Inductive Coupling (Pos)	$V_S = 100\text{ V}$ , $R_S = 50\ \Omega$ , $t_r = 50\text{ ns}$ , $t_d = 100\text{ ns}$
4	Reverse Battery	$V_S = -14\text{ V}$ , $t_d = 20\text{ s}$
5	Load Dump (ISO) (DIN)	$V_S = 86.5\text{ V}$ , $R_S = 0.5\ \Omega$ , $t_r = 5\text{ ms}$ , $t_d = 400\text{ ms}$ $V_S = 120\text{ V}$ , $R_S = 0.5\ \Omega$ , $t_r = 100\text{ ns}$ , $t_d = 400\text{ ms}$
6	Ignition Coil Disconnect EXTERNAL PROTECTION REQ'D	$V_S = -300\text{ V}$ , $R_S = 30\ \Omega$ , $t_r = 60\ \mu\text{s}$ , $t_d = 300\ \mu\text{s}$
7	Field Decay (Negative)	$V_S = -80\text{ V}$ , $R_S = 10\ \Omega$ , $t_r = 5\text{ ms}$ , $t_d = 100\text{ ms}$



Power supply voltage transients, or device output short circuits, may be caused by faulty connectors, crimped wiring harnesses, or service errors. To prevent catastrophic failure, internal protection against overvoltage, reverse voltage, output overloads have been incorporated to meet the automotive 12 volt system protection requirements of ISO DP7637/1 and DIN 40839-1. A series-blocking diode or current-limiting resistor is required in order to survive pulse number six.

**Output Overloads.** Current through the output source transistor is sensed with a low-value on-chip aluminum resistor. The voltage drop across this resistor is fed back to control the base drive of the output stage. This feedback prevents the output transistor from exceeding its maximum current density rating by limiting the output current to between -26 mA and -70 mA. Under short-circuit conditions, the device will dissipate an increased amount of power ( $P_D = V_{OUT} \times I_{LIMIT}$ ) and the

output transistor will be thermally stressed. Current through the active pull-down is limited to between 8 mA and 25 mA.

**Overvoltage.** The device protects itself against high-voltage transients by shutting OFF the output source driver and all supply-referenced active components, reducing the supply current, and minimizing device power dissipation. Overvoltage shutdown can occur anywhere between 28 V and 55 V and device operation above 28 V cannot be recommended. The device will continue to operate, with increased power dissipation, for supply voltages above the internal clamp voltage but below the overvoltage shutdown. Under a sustained overvoltage, the device may be required to dissipate an increased amount of power ( $P_D = V_{CC} \times I_{CC}$ ) and the device may be thermally stressed (see above).

**Output Voltage.** The output is clamped with an on-chip Zener diode to prevent supply overvoltage faults from appearing at the output when the field is less than  $B_{RP}$ .

When any fault condition is removed, the device returns to normal operating mode.

**3195**  
***PROTECTED, HIGH-TEMP.,  
ACTIVE PULL-DOWN  
HALL-EFFECT LATCH***

**CRITERIA FOR DEVICE QUALIFICATION**

All Allegro sensors are subjected to stringent qualification requirements prior to being released to production. To become qualified, except for the destructive ESD tests, no failures are permitted.

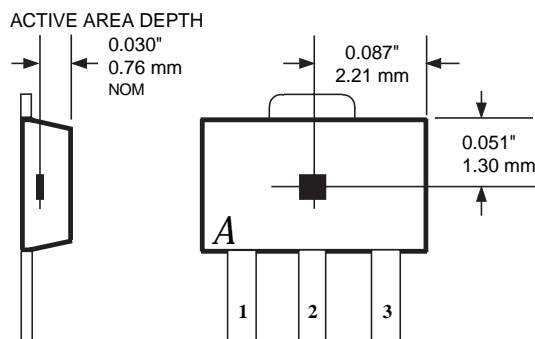
<b>Qualification Test</b>	<b>Test Method and Test Conditions</b>	<b>No. of Lots</b>	<b>Test Length</b>	<b>Samples Per Lot</b>	<b>Comments</b>
Biased Humidity	JESD22-A101 $T_A = 85^{\circ}\text{C}$ , RH = 85%	3	1200 hrs	116	Device biased for minimum power
High-Temperature Operating Life	JESD22-A108 $T_A = 150^{\circ}\text{C}$ , $T_J = 165^{\circ}\text{C}$	3	1200 hrs	116	
Surge Operating Life	JESD22-A108 $T_A = 175^{\circ}\text{C}$ , $T_J = 190^{\circ}\text{C}$	1	504 hrs	116	
Pressure Cooker, Unbiased	JESD22-A102, Method C	3	96 hrs	77	
Storage Life	MIL-STD-883, Method 1008 $T_A = 170^{\circ}\text{C}$	1	1200 hrs	77	
Temperature Cycle	MIL-STD-883, Method 1010	3	1000 cycles	153	
ESD Human Body Model	MIL-STD-883, Method 3015	1	Pre/Post Reading	3 per test	Test to failure $\text{HBM} \geq 12 \text{ kV}$
ESD Machine Model		1	Pre/Post Reading	3 per test	Test to failure $\text{MM} \geq 600 \text{ V}$

# 3195 PROTECTED, HIGH-TEMP., ACTIVE PULL-DOWN HALL-EFFECT LATCH

## SENSOR LOCATIONS

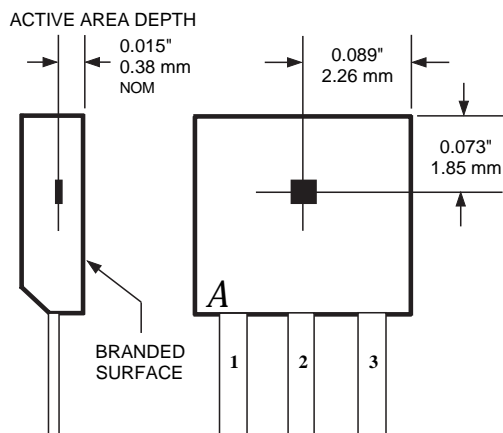
( $\pm 0.005"$  [0.13 mm]  
die placement)

### SUFFIX "LT"



Dwg. MH-008-6A

### SUFFIX "U"



Dwg. MH-002-13A

## APPLICATIONS INFORMATION

The A3195– latch has been optimized for use in automotive ring magnet sensing applications. Such applications include transmission speed sensors, motor position encoders, and wheel bearing speed sensors. Special care has been taken to optimize the operation of these devices in automotive subsystems that require ISO DP9637 protection but NOT operation. Short-circuit protection is included to prevent damage caused by pinched wiring harnesses. An on-chip pull-down resistor is provided to allow device testing without the connection of the control module.

A typical application consists of a ferrite ring magnet located on a rotating shaft. Typically, this shaft is attached to the transmission, the sensor is mounted on a board, with care being taken to keep a tight tolerance on the air gap between the package face and the magnet. The device will provide a change in digital state at the transition of every magnetic pole and, thus, give an indication of the transmission speed. The high magnetic hysteresis allows the device to be immune to vibration of the magnet shaft and relatively good duty cycles can be obtained.

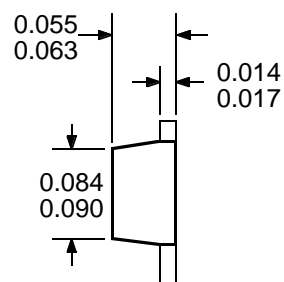
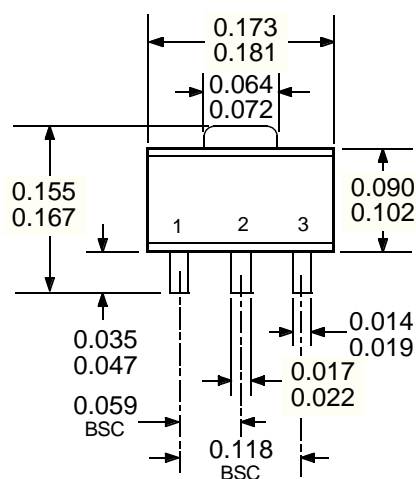
Hall effect applications information is also available in the *Allegro Integrated and Discrete Semiconductors Data Book* or *Application Note 27701*.



**3195**  
**PROTECTED, HIGH-TEMP.,**  
**ACTIVE PULL-DOWN**  
**HALL-EFFECT LATCH**

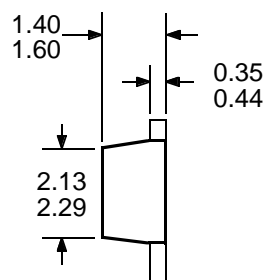
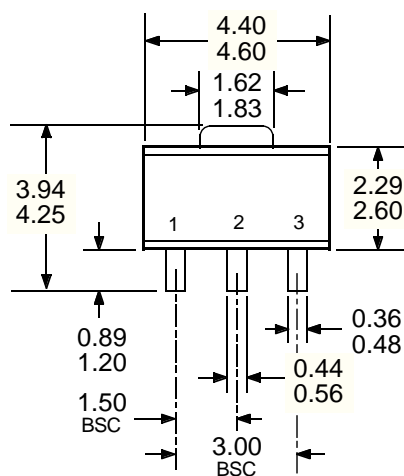
**A3195ELT AND A3195LLT**

Dimensions in Inches  
(for reference only)



Dwg. MA-009-3 in

Dimensions in Millimeters  
(controlling dimensions)

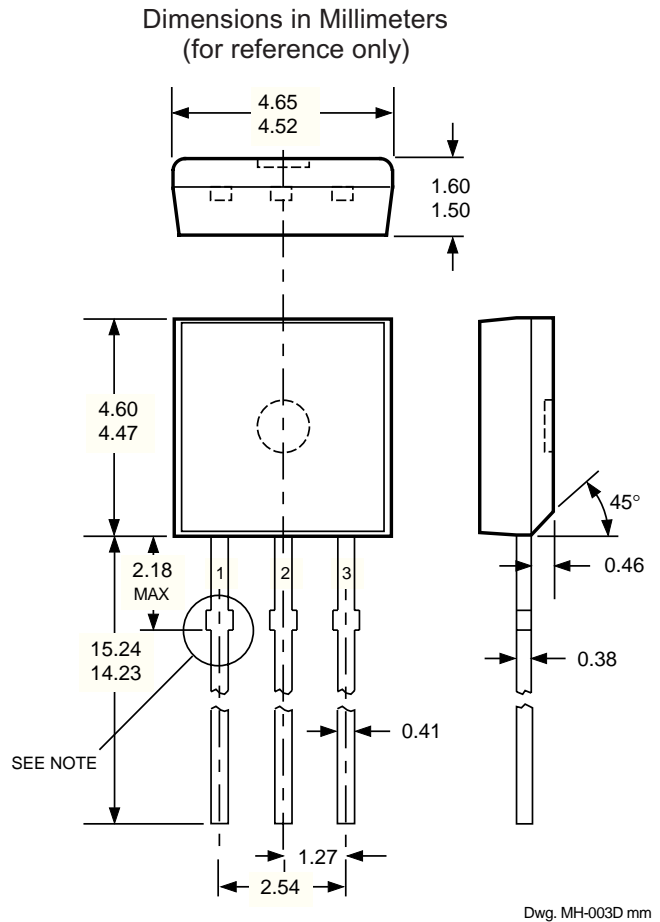
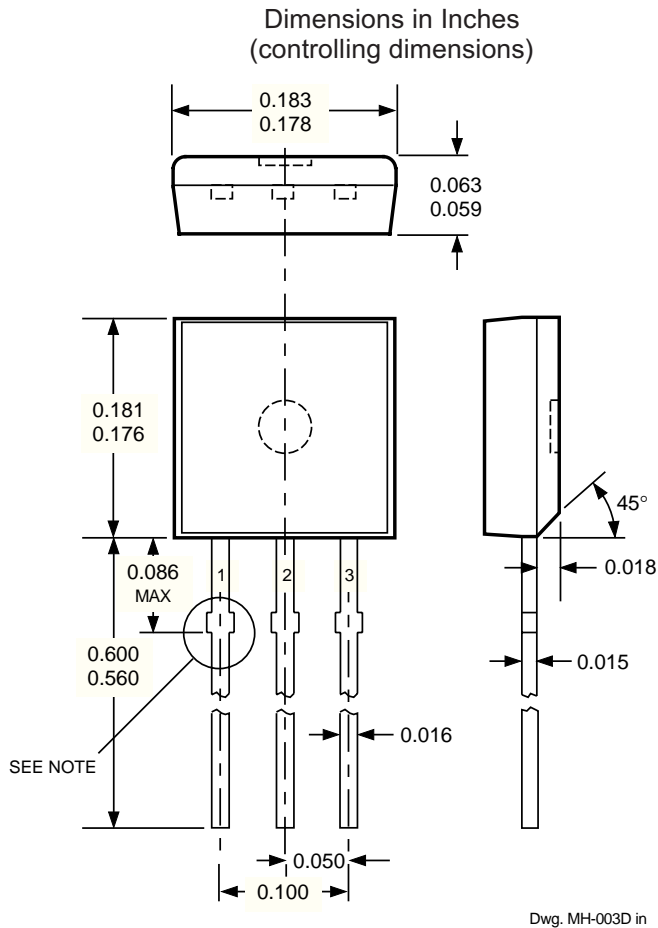


Dwg. MA-009-3 mm

NOTE — Exact body and lead configuration at vendor's option within limits shown.

# 3195 PROTECTED, HIGH-TEMP., ACTIVE PULL-DOWN HALL-EFFECT LATCH

## A3195EU AND A3195LU



- NOTES: 1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).  
2. Exact body and lead configuration at vendor's option within limits shown.  
3. Height does not include mold gate flash.  
4. Recommended minimum PWB hole diameter to clear transition area is 0.035" (0.89 mm).  
5. Where no tolerance is specified, dimension is nominal.

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*The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringements of patents or other rights of third parties which may result from its use.*