



198 Champion Court, San Jose, CA 95134-1709 (408)943-2600

## PRODUCT INFORMATION NOTIFICATION

**PCN:** PCN125151

**Date:** June 15, 2012

**Subject:** Design Marginality issue with CPLL of CY2291/CY2292 device family (Three-PLL General Purpose EPROM Programmable Clock Generator)

**To:** PCN ADMINISTRATOR  
CYPRESS PCN ADMIN  
pcn\_adm@cypress.com

**Change Type:** N/A

**Product Information:**

Cypress CY2291/CY2292 is a family of EPROM based programmable clock generators that have three Phase-Locked Loops (PLLs): a CPU PLL (CPLL), System Clock PLL (SPLL), and Utility PLL (UPLL). It supports 3.3V/5V VDD range and can operate up to a max frequency of 100MHz.

In electrical characterization testing, Cypress has identified a minor design marginality with the CY2291/CY2292 family of devices that causes the CPLL to not achieve phase lock within the datasheet specification of 50ms. This condition occurs in application environments with certain Temperature/ Vcc/noise levels during device start up. The other two PLL viz. SPLL and UPLL are not affected by this startup issue.

No field failures have been reported. As a proactive measure, we have implemented a test screen last May 30, 2012. However, this test screen may not be 100% effective in screening all devices. Hence we request that customers send us their JEDEC configuration files so that we may verify if the C-PLL is being used, and if so, we can assist in ascertaining whether the application is at risk.

**Affected Part Numbers:**

**Affected Parts:** 38. Please see attached sheet for part list.

**Customer Part Numbers Affected:**

**Affected Parts:** Not Applicable

**Qualification Status:**

Not Applicable

**Sample Status:**

Not Applicable

**Approximate Implementation Date:**

The test screen was implemented last May 30, 2012.

**Anticipated Impact:**

Based on the investigation, if the C-PLL is used in the customer's configuration, the device may be affected by this startup issue.

**Method of Identification:**

Cypress maintains traceability of product to wafer level, including wafer fabrication location, through the lot number marked on the package.

**Response Required:**

We request that customers forward their JEDEC configuration files to Prasad Tawade at [pyta@cypress.com](mailto:pyta@cypress.com), in order that we may assess whether the application is at risk.

For additional information regarding this change, contact your local sales representative or contact the PCN Administrator at [pcn\\_adm@cypress.com](mailto:pcn_adm@cypress.com).

Sincerely,

Cypress PCN Administration