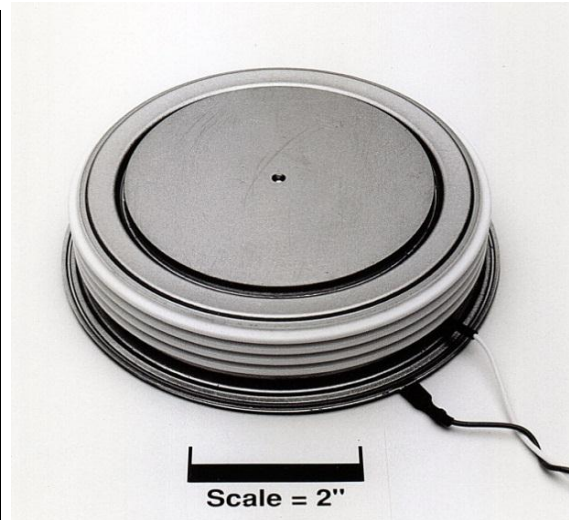
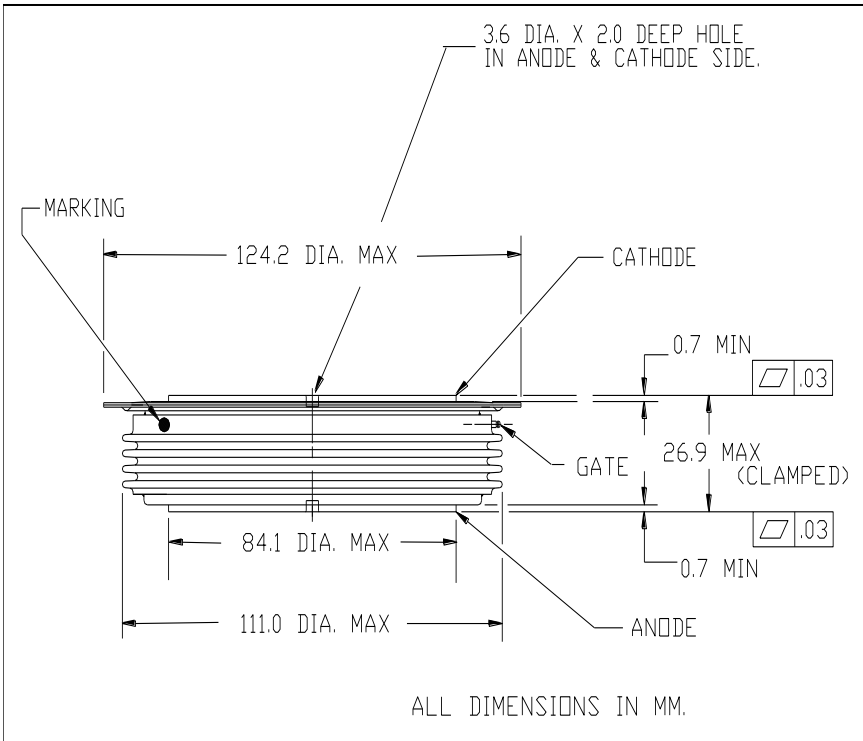




The TCS4 is a high voltage, high current disc pack SCR employing a high di/dt gate structure. This gate design allows the SCR to be reliably operated at high di/dt and dv/dt conditions in various phase control applications.

FEATURES:

- Low On-State Voltage
- High di/dt Capability
- High dv/dt Capability
- Hermetic Ceramic Package
- Excellent Surge and I^2t Ratings

APPLICATIONS:

- DC Power Supplies
- Motor Controls
- SS Contactors

ORDERING INFORMATION

Select the complete 12 digit Part Number using the table below.
 EXAMPLE: TCS444340HDH is a 4400V-3400A SCR with 250ma IGT and 12 inch gate and cathode potential leads.

PART	Voltage Rating V_{DRM} - V_{RRM}	Voltage Code	Current Rating I_{TAVG}	Current Code	Turn-Off T_q	Gate I_{GT}	Leads
TCS4	3600	36	3400	34	0	H	DH
	4000	40					
	4200	42			500us	250ma	12"
	4400	44			(typ.)	(max)	
	4500	45					

Revised: 5/1/2012

Absolute Maximum Ratings

Characteristic	Symbol	Rating	Units
Repetitive Peak Voltage	$V_{DRM}-V_{RRM}$	3600 - 4500	Volts
Average On-State Current, $T_C=70^{\circ}C$	$I_{T(Avg.)}$	3400	A
RMS On-State Current, $T_C=70^{\circ}C$	$I_{T(RMS)}$	5341	A
Average On-State Current, $T_C=50^{\circ}C$	$I_{T(Avg.)}$	4125	A
RMS On-State Current, $T_C=50^{\circ}C$	$I_{T(RMS)}$	6480	A
Peak One Cycle Surge Current, 60Hz, $V_R=0V$	I_{TSM}	43,500	A
Peak One Cycle Surge Current, 50Hz, $V_R=0V$	I_{TSM}	41,012	A
Fuse Coordination I^2t , 60Hz	I^2t	7.88E+06	A ² s
Fuse Coordination I^2t , 50Hz	I^2t	8.41E+06	A ² s
Critical Rate-of-Rise of On-State Current Repetitive	di/dt	100	A/us
Critical Rate-of-Rise of On-State Current Non-Repetitive	di/dt	300	A/us
Application Specific Repetitive di/dt Rate Linear Rate to 700A followed by 10A/us to I_{Tavg} .	di/dt	400	A/us
Peak Gate Power, 100us	P_{GM}	16	Watts
Average Gate Power	$P_{G(avg)}$	5	Watts
Operating Temperature	T_J	-40 to+125	$^{\circ}C$
Storage Temperature	$T_{Stg.}$	-50 to+150	$^{\circ}C$
Approximate Weight		3.2	lb
		1.45	Kg
Mounting Force		12,000-15,000	lbs
		53 - 67	Knewtons

Information listed is based upon Powerex testing and projected ratings and is subject to change without notice. Powerex makes no implicit or explicit claim to reliability, capability, performance or suitability of this product for a users application. Powerex makes no guarantee of future availability of this product.

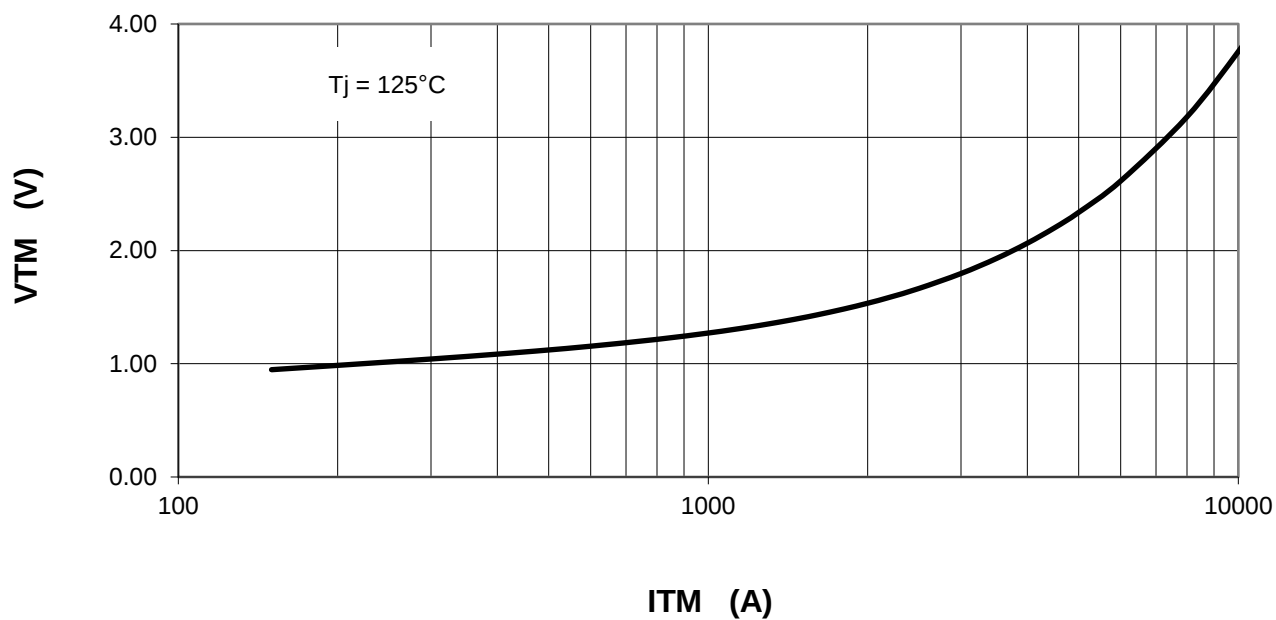
Electrical Characteristics, Tj=25°C unless otherwise specified

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Repetitive Peak Forward Leakage Current	I_{DRM}	Tj=125°C, V_{DRM} =Rated			300	ma
Repetitive Peak Reverse Leakage Current	I_{RRM}	Tj=125°C, V_{RRM} =Rated			300	ma
Peak On-State Voltage	V_{TM}	Tj=125°C, I_{TM} =3000A			1.80	V
V_{TM} Model, Low Level	V_0	Tj=125°C			0.990	V
$V_{TM} = V_0 + r \cdot I_{TM}$	r	15% $I_{TM} - I_{TSM}$			0.271	mΩ
V_{TM} Model, High Level	V_0	Tj=125°C			0.698	V
$V_{TM} = V_0 + r \cdot I_{TM}$	r	$\pi \cdot I_{TM} - I_{TSM}$			0.304	mΩ
V_{TM} Model, 4-Term	A	Tj=125°C			0.191	
$V_{TM} = A + B \cdot \ln(I_{TM}) +$	B	15% $I_{TM} - I_{TSM}$			0.181	
$C \cdot (I_{TM}) + D \cdot (I_{TM})^{1/2}$	C				3.56E-04	
	D				-0.0166	
Turn-On Delay Time	t_d	$V_D = 0.5 \cdot V_{DRM}$ Gate Drive: 40V - 20Ω		2.5		us
Turn-Off Time	t_q	Tj=125°C dv/dt = 20V/us to 80% V_{DRM}			500	us
dv/dt _(Crit)	dv/dt	Tj=125°C Exp. Waveform V_D =80% Rated	1000			V/us
Gate Trigger Current	I_{GT}	Tj=25°C $V_D = 12V$	30	100	250	ma
Gate Trigger Voltage	V_{GT}		0.8	2.0	4.5	V
Peak Reverse Gate Voltage	V_{GRM}				5	V

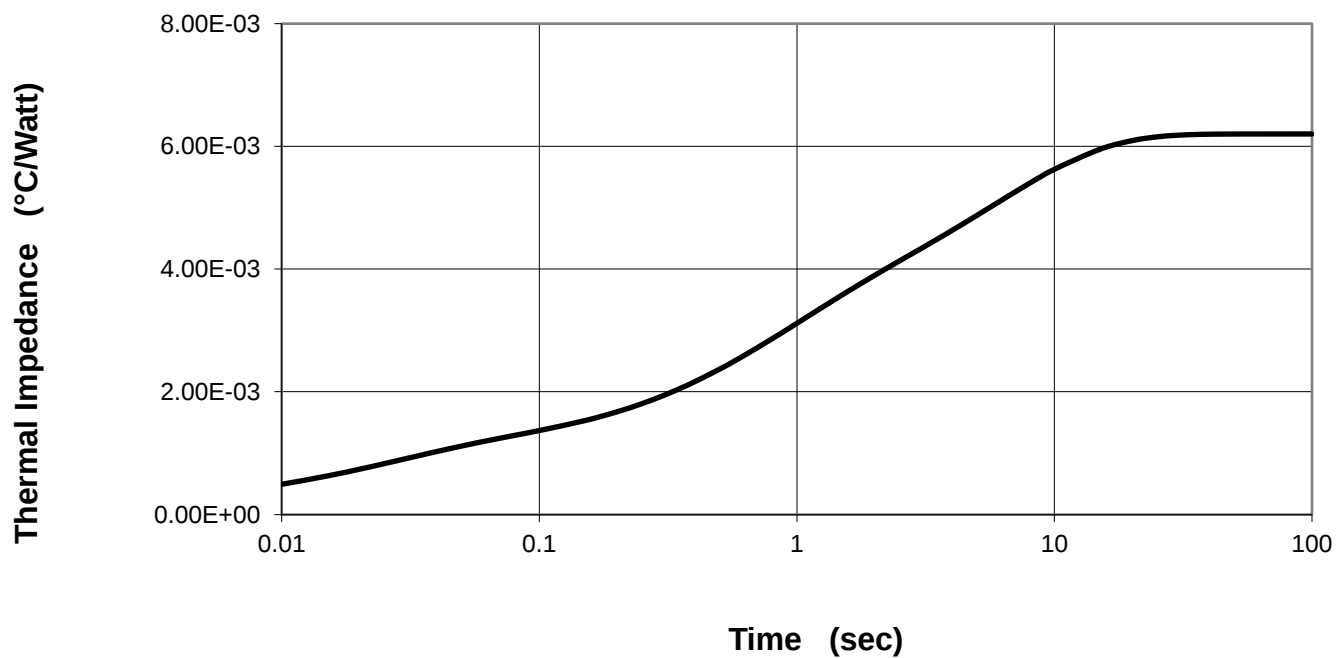
Thermal Characteristics

Characteristic	Symbol	Test Conditions	min	Rating typ	max	Units
Thermal Resistance						
Junction to Case	RΘ _{jc}	Double side cooled		0.007	0.008	°C/Watt
Case to Sink	RΘ _{cs}	Double side cooled		0.0015	0.002	°C/Watt
Thermal Impedance Model						
ZΘ _{jc} (t) = Σ(A(N)•(1-exp(-t/Tau(N))))	ZΘ _{jc}	Double side cooled				
	where:	N =	1	2	3	4
		A(N) =	1.43E-04	9.08E-04	2.37E-03	4.60E-03
		Tau(N) =	2.62E-03	2.31E-02	5.00E-01	8.00E+00

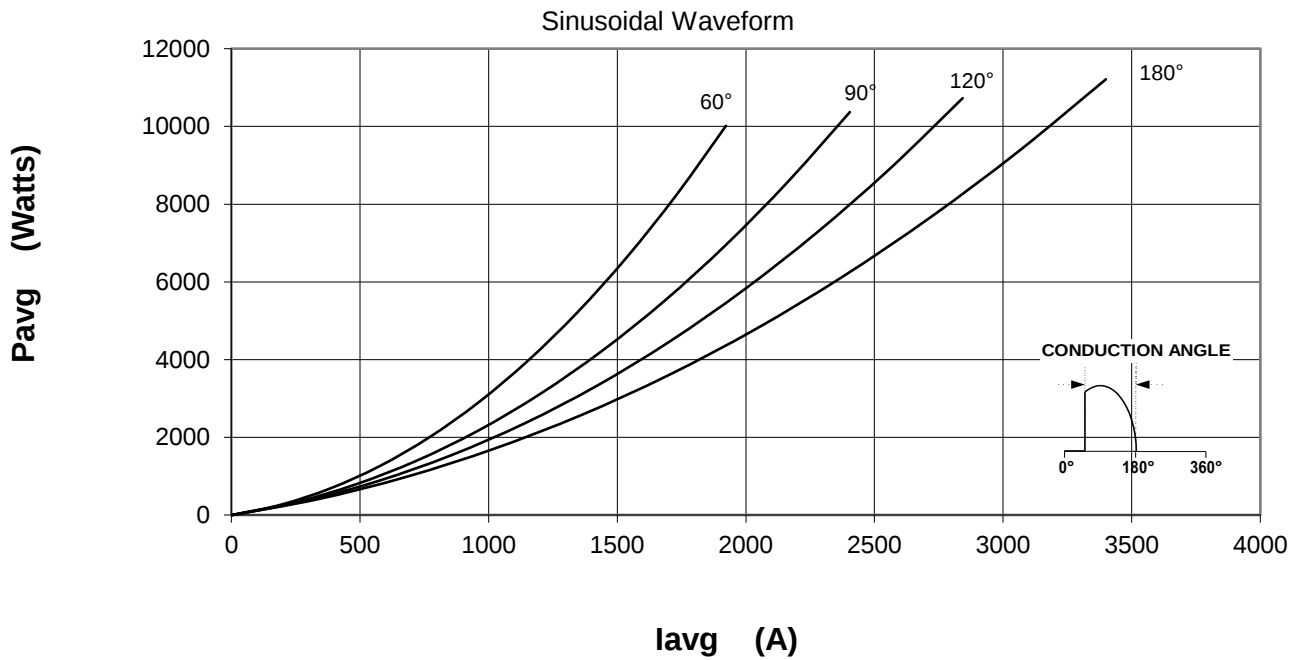
Maximum On-State Voltage Drop



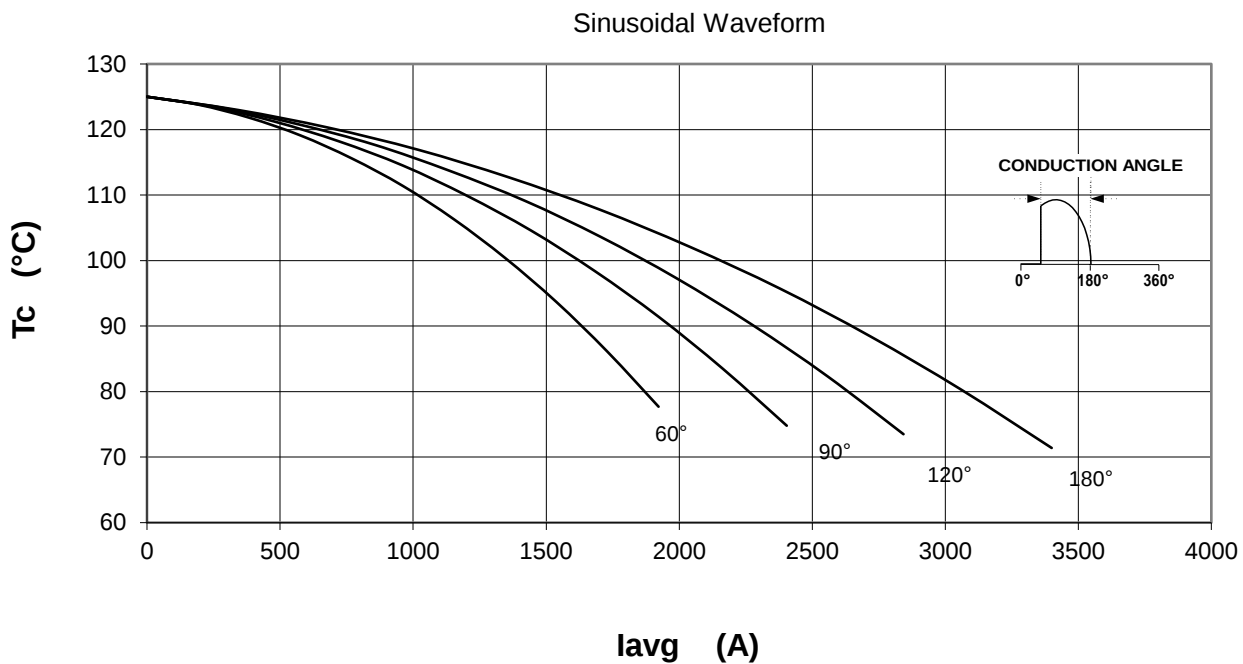
MAXIMUM TRANSIENT THERMAL IMPEDANCE



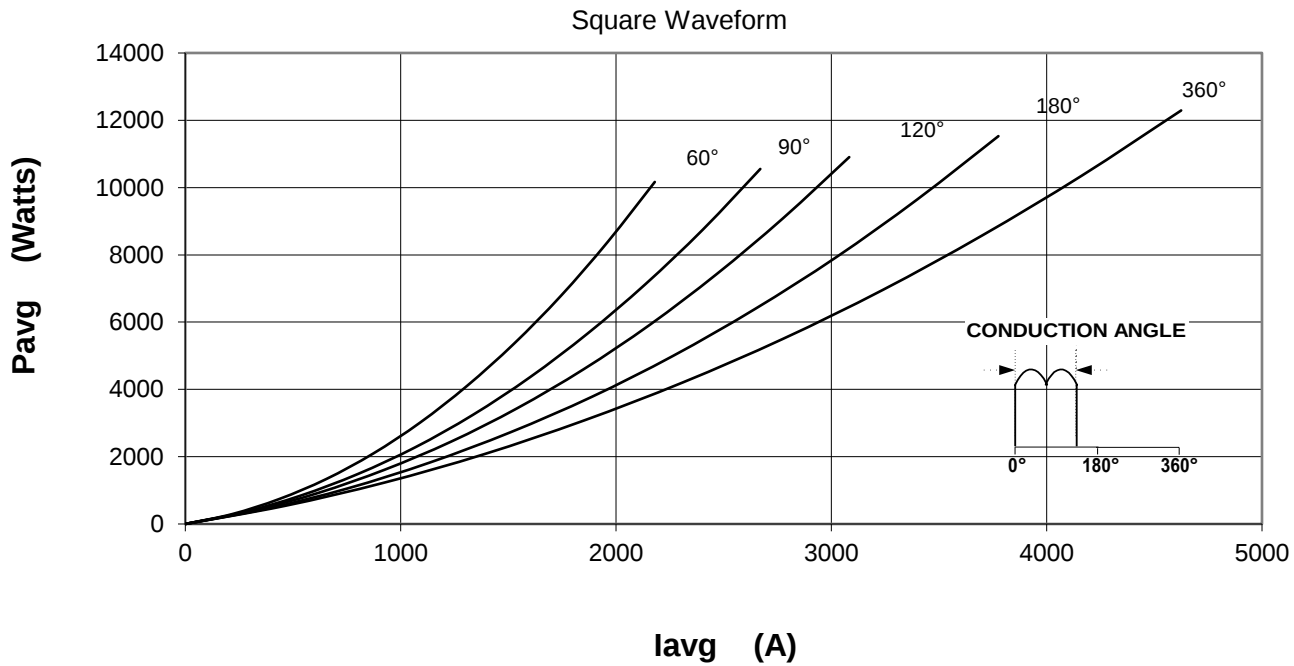
Maximum On-State Power Dissipation



Maximum Allowable Case Temperature



Maximum On-State Power Dissipation



Maximum Allowable Case Temperature

