# M74LS192P

## SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

### DESCRIPTION

The M74LS192P is a semiconductor integrated circuit containing a synchronous decade up/down counter function with direct reset and preset inputs.

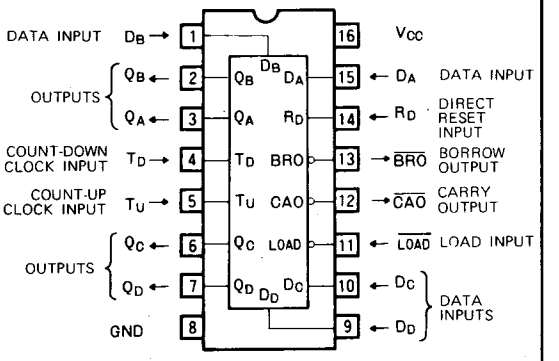
### FEATURES

- Special up count, down count clock inputs
- Asynchronous preset input provided
- Direct reset input provided
- Easy cascade connection possible
- High-speed counting ($f_{max}$= 38MHz typical)
- Wide operating temperature range ($T_a$= −20~+75°C)

### APPLICATION

General purpose, for use in industrial and consumer equipment.

### PIN CONFIGURATION (TOP VIEW)




Outline 16P4

### FUNCTIONAL DESCRIPTION

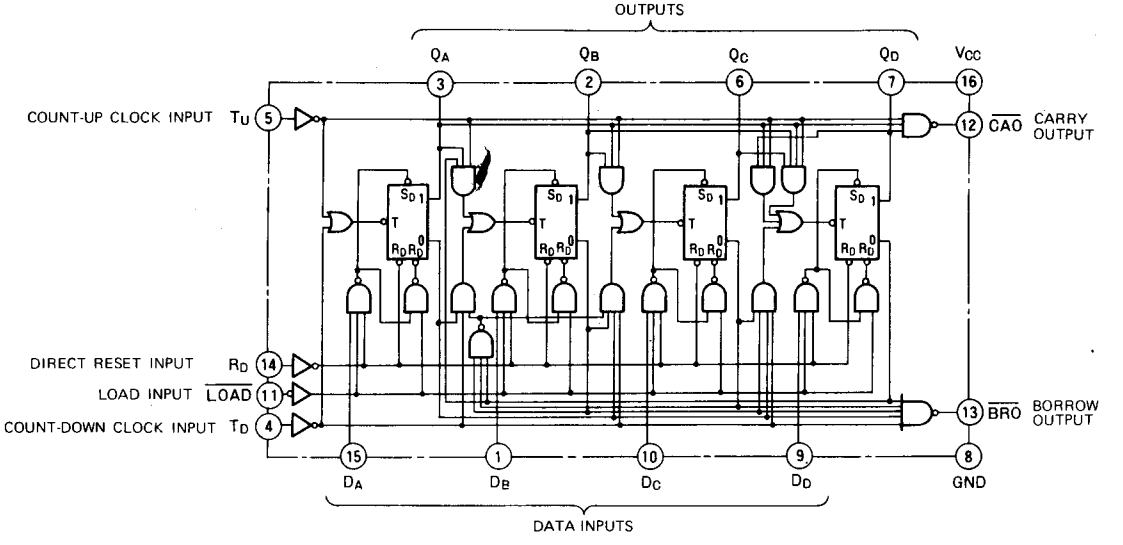
This device comes with special count-up clock input $T_U$ and count-down clock input $T_D$ used independently for count-up and count-down applications. For count-up, the number of count pulses appears as a BCD code in outputs $Q_A$, $Q_B$, $Q_C$ and $Q_D$ in synchronization with the count pulses by setting load input $\overline{LOAD}$ and $T_D$ high, applying the count pulses to $T_U$ while for count-down, $\overline{LOAD}$ and $T_U$ are set high and the count pulses are applied to $T_D$. Counting is performed when $T_U$ or $T_D$ changes from low to high.

Presetting is performed independently of the count pulse. When data are applied to data inputs $D_A$, $D_B$, $D_C$ and $D_D$ and $\overline{LOAD}$ is set low, the $D_A$, $D_B$, $D_C$ and $D_D$ signals appear in the $Q_A$, $Q_B$, $Q_C$ and $Q_D$ outputs, respectively, regardless of the status of the $T_U$ and $T_D$ signals, thereby presetting the counter. Counting proceeds as per the status transition diagram with presetting to a numerical value of 10 or more.

Reset can be performed by setting the direct reset input $R_D$ high which sets $Q_A = Q_B = Q_C = Q_D$ low irrespective of the status of the other inputs.

Low appears in the carry output $\overline{CAO}$ during count-up when 9 appears in $Q_A$, $Q_B$, $Q_C$ and $Q_D$ and when $T_U$ is low while low appears in output $\overline{BRO}$ when 0 appears in the outputs $\overline{CAO}$ and $\overline{BRO}$ should be connected to the next stage $T_U$ and $T_D$ for counter cascade connection. (Refer to the application examples.)

### BLOCK DIAGRAM





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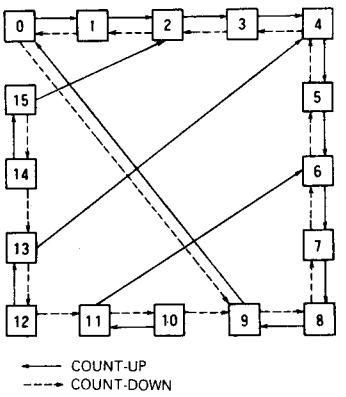
## SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

### FUNCTION TABLE (Note 1)

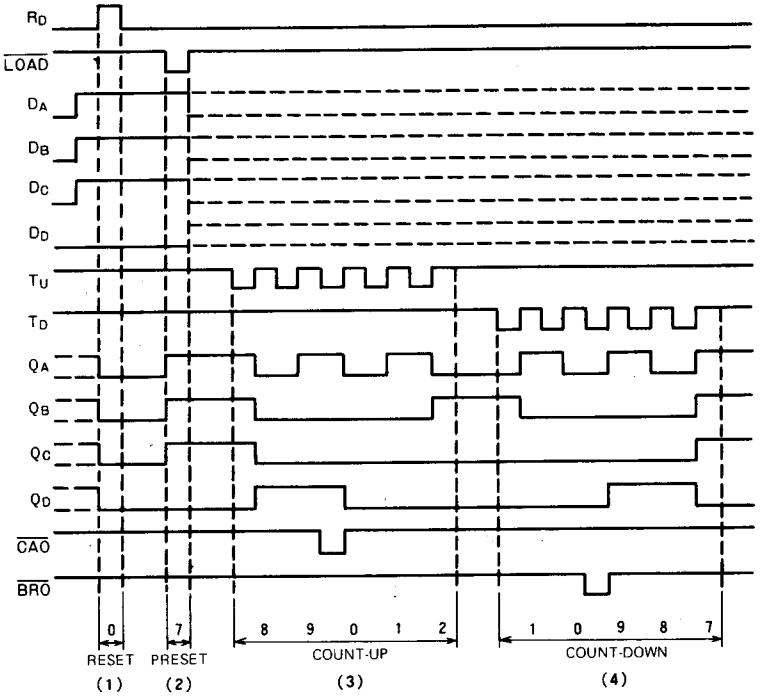
| $R_D$ | $\overline{LOAD}$ | $T_U$ | $T_D$ | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $\overline{CAO}$ | $\overline{BRO}$ |
|---|---|---|---|---|---|---|---|---|---|
| H | X | X | X | L | L | L | L | H | H* |
| L | L | X | X | $D_A$ | $D_B$ | $D_C$ | $D_D$ | H* | H* |
| L | H | H | H | Inhibit | | | | H* | H* |
| L | H | ↑ | H | Count-up | | | | H* | H* |
| L | H | H | ↑ | Count-down | | | | H* | H* |

Note 1. ↑ : Transition from low to high
* : Normally high but low appears in accordance with the following logical expressions.
$\overline{CAO} = \overline{Q_A \cdot Q_D \cdot T_U}$ ..... Count-up
$\overline{BRO} = \overline{Q_A \cdot Q_B \cdot Q_C \cdot Q_D \cdot T_D}$ ..... Count-down
X : Irrelevant

### STATE DIAGRAM




### OPERATION TIMING DIAGRAM




Details of timing diagram
(1) Reset
(2) Preset to 7
(3) Count-up 8, 9, 0, 1, 2
(4) Count-down 1, 0, 9, 8, 7

### ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 ~ +7 | V |
| $V_I$ | Input voltage | | −0.5 ~ +15 | V |
| $V_O$ | Output voltage | High-level state | −0.5 ~ $V_{CC}$ | V |
| Topr | Operating free-air ambient temperature range | | −20 ~ +75 | °C |
| Tstg | Storage temperature range | | −65 ~ +150 | °C |

## SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

### RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

| Symbol | Parameter | | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | | 4.75 | 5 | 5.25 | V |
| $I_{OH}$ | High-level output current | $V_{OH} \geqq 2.7V$ | 0 | | −400 | μA |
| $I_{OL}$ | Low-level output current | $V_{OL} \leqq 0.4V$ | 0 | | 4 | mA |
| | | $V_{OL} \leqq 0.5V$ | 0 | | 8 | mA |

### ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

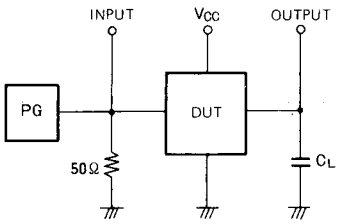
| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ * | Max | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $V_{IC}$ | Input clamp voltage | $V_{CC} = 4.75V$, $I_{IC} = -18mA$ | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC} = 4.75V$, $V_I = 0.8V$<br>$V_I = 2V$, $I_{OH} = -400\mu A$ | | 2.7 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC} = 4.75V$ | $I_{OL} = 4mA$ | | 0.25 | 0.4 | V |
| | | $V_I = 0.8V, V_I = 2V$ | $I_{OL} = 8mA$ | | 0.35 | 0.5 | V |
| $I_{IH}$ | High-level input current | $V_{CC} = 5.25V$, $V_I = 2.7V$ | | | | 20 | μA |
| | | $V_{CC} = 5.25V$, $V_I = 10V$ | | | | 0.1 | mA |
| $I_{IL}$ | Low-level input current | $V_{CC} = 5.25V$, $V_I = 0.4V$ | | | | −0.4 | mA |
| $I_{OS}$ | Short-circuit output current (Note 2) | $V_{CC} = 5.25V$, $V_O = 0V$ | | −20 | | −100 | mA |
| $I_{CC}$ | Supply current | $V_{CC} = 5.25V$ (Note 3) | | | 19 | 34 | mA |

* : All typical values are at $V_{CC} = 5V$, $Ta = 25°C$.
Note 2. All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3. $I_{CC}$ is measured with $R_D$ and $\overline{LOAD}$ at 0V and $T_U$, $T_D$, $D_A \sim D_D$ at 4.5V

### SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25°C$, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $f_{max}$ | Maximum clock frequency | $C_L = 15pF$ (Note 4) | 25 | 38 | | MHz |
| $t_{PLH}$ | Low-to-high-level, high-to-low-level output propagation time, from input $T_U$ to output $\overline{CAO}$ | | | 7 | 26 | ns |
| $t_{PHL}$ | | | | 14 | 24 | ns |
| $t_{PLH}$ | Low-to-high-level, high-to-low-level output propagation time, from input $T_D$ to output $\overline{BRO}$ | | | 7 | 24 | ns |
| $t_{PHL}$ | | | | 19 | 24 | ns |
| $t_{PLH}$ | Low-to-high-level, high-to-low-level output propagation time, from input $T_U$, $T_D$ to outputs $Q_A$, $Q_B$, $Q_C$, $Q_D$ | | | 20 | 38 | ns |
| $t_{PHL}$ | | | | 17 | 47 | ns |
| $t_{PLH}$ | Low-to-high-level, high-to-low-level output propagation time, from input $\overline{LOAD}$ to outputs $Q_A$, $Q_B$, $Q_C$, $Q_D$ | | | 24 | 40 | ns |
| $t_{PHL}$ | | | | 20 | 40 | ns |
| $t_{PHL}$ | High-to-low-level output propagation time, from input $R_D$ to outputs $Q_A$, $Q_B$, $Q_C$, $Q_D$ | | | 12 | 35 | ns |

Note 4. Measurement circuit



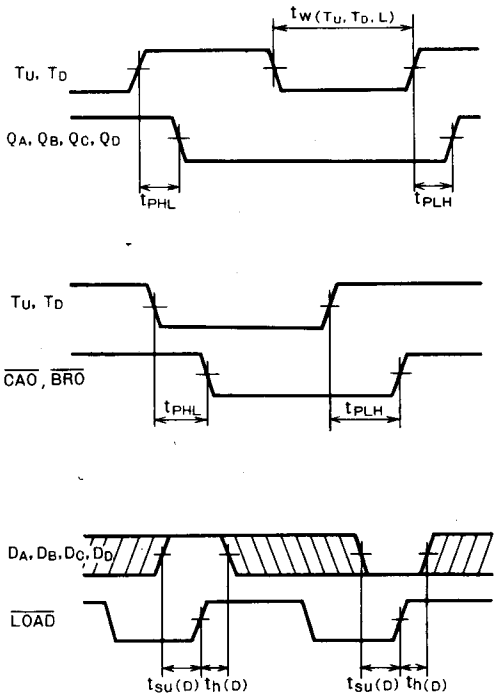

(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, $t_r$ = 6ns, $t_f$ = 6ns, $t_W$ = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
(2) $C_L$ includes probe and jig capacitance

## SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

### TIMING REQUIREMENTS ($V_{CC}$ = 5V, $T_a$ = 25°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{w(T_UL)}$ | Clock input $T_U$ low pulse width | | 20 | 14 | | ns |
| $t_{w(T_DL)}$ | Clock input $T_D$ low pulse width | | 20 | 18 | | ns |
| $t_{w(\overline{LOAD})}$ | Load $\overline{LOAD}$ pulse width | | 20 | 11 | | ns |
| $t_{w(R_D)}$ | Direct reset $R_D$ pulse width | | 20 | 4 | | ns |
| $t_{su(D)}$ | Setup time $D_A$~$D_D$ to $\overline{LOAD}$ | | 20 | 4 | | ns |
| $t_{h(D)}$ | Hold time $D_A$~$D_D$ to $\overline{LOAD}$ | | 5 | −3 | | ns |

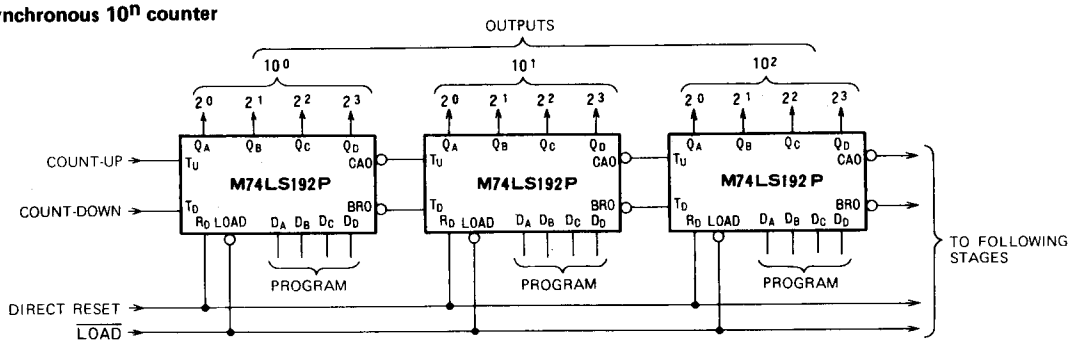
### TIMING DIAGRAM (Reference level = 1.3V)




Note 5. The shaded areas indicate when the input is permitted to change for predictable output performance.

### APPLICATION EXAMPLE

**Asynchronous $10^n$ counter**



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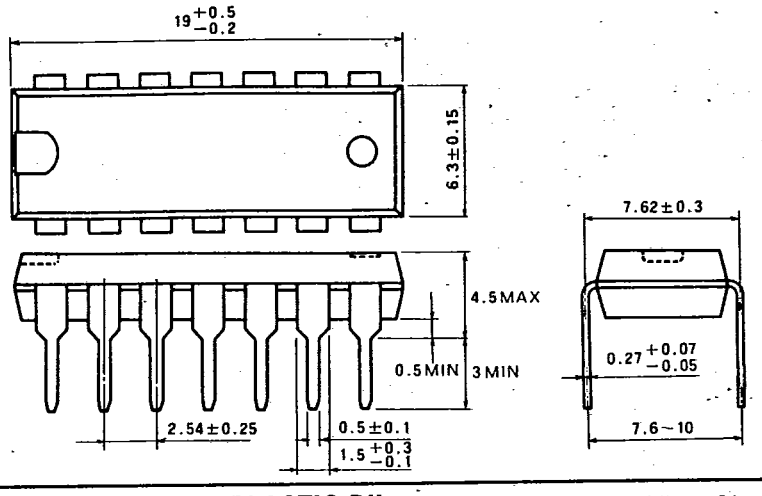
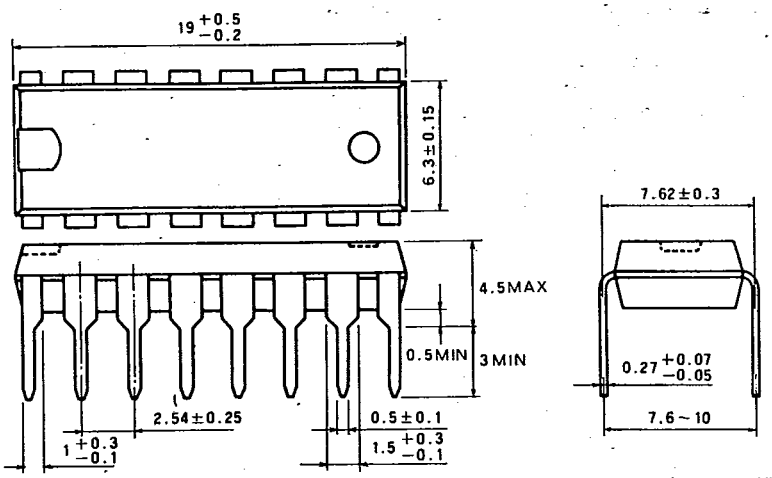
## TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm




## TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm




## TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm