FMC ADC Evaluation Board User's Guide

High-Speed ADC Evaluation Platform

- Interfaces Intersil's High-Speed ADC Evaluation PCB Family to FMC Based Evaluation Platforms
- 40MSPS to 500MSPS Operation
- SPI Access for ADC Configuration
- Compatible with all Intersil High-Speed ADC Daughter Cards

Evaluation Platform Overview

Intersil's FMC based high-speed ADC evaluation platform consists of custom designed hardware, which allows interfacing to an FMC based FPGA evaluation platform. This allows for direct FPGA processing of the ADC output data and system prototyping for a user. SPI access to the ADC is possible at the FMC connector or optionally at a separate header on the PCB (JP3).

Hardware

There are two components in the hardware portion of the evaluation platform: the daughter card and the motherboard (Figure 1). The ADC is contained on the daughter card, which routes power from the motherboard and contains the analog input circuitry, clock drive and decoupling. The daughter card interfaces to the motherboard through a mezzanine connector. The motherboard provides power to the ADCs analog and digital supply pins from separate LDOs from Intersil's High performance linear regulator family. The ADCs digital outputs are routed through the mezzanine connector to the FMC connector at the motherboard card edge.

The user must supply low-jitter RF generators for the clock and analog inputs. Recommendations of suitable generators can be found in "Appendix A: RF Generators" on page 2.

Many low-jitter RF generators exhibit high harmonic spectral content relative to the ADC performance. A band-pass filter is recommended to attenuate the harmonics. A wideband attenuator in series with the band-pass filter is also recommended for daughter cards without on-board attenuators. Current spikes from the ADCs switched capacitor sample-and-hold amplifier can create signal reflections in the coaxial cable. The attenuator reduces these reflections and improves performance.

Software

There is no software provided with the evaluation system. Data capture and ADC performance verification needs to be done at the receiving FPGA. A reset of the ADC is possible at switch S1 on the PCB.

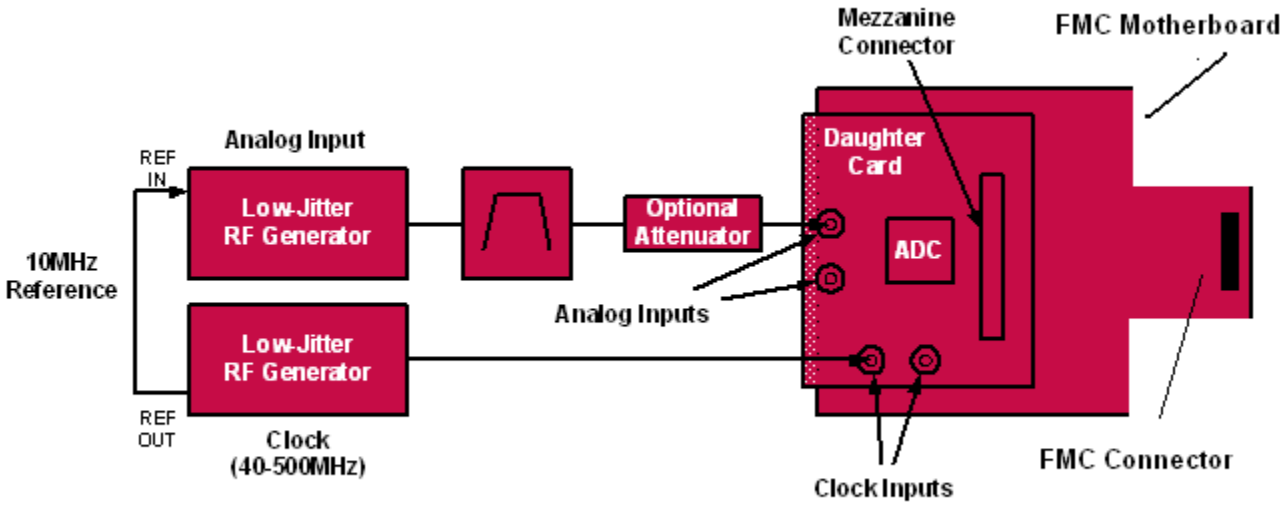

FIGURE 1. EVALUATION PLATFORM BLOCK DIAGRAM

Initial Start-Up

Referring to Figure 1, connect the daughter card to the motherboard by aligning the two mating mezzanine connectors. Four screws on the motherboard (not shown) align with mounting holes in the daughter card. The FMC connector should be aligned and connected with an appropriate mating FMC-based FPGA evaluation system. Next, connect the RF generators to the Clock and Analog input SMA connectors. Set the clock frequency as desired with the power level at +10dBm. Similarly, set the analog input frequency with a power level of approximately +7dBm (the full-scale value will vary depending on the loss of the input path and gain of the ADC). With the RF generators on, apply +5V power supply to the motherboard. The daughter card is powered by Intersil linear regulators on the motherboard.

Daughter Cards

Each daughter card is designed to produce optimal ADC performance and simplify the evaluation process. Some boards have multiple connections for the analog input and clock. For example, low-frequency and high-frequency input paths are provided on certain boards. A high-frequency input path may have a balun interface, while a low frequency path may use a transformer or buffer amplifier (for DC-coupling).

Motherboard

The only connection required for the motherboard is +5V power at J1 (5V wall supply is supplied), JP1 is an optional connection. The data outputs are LVDS and will require 100Ω differential termination resistors at the receiver/FPGA. .

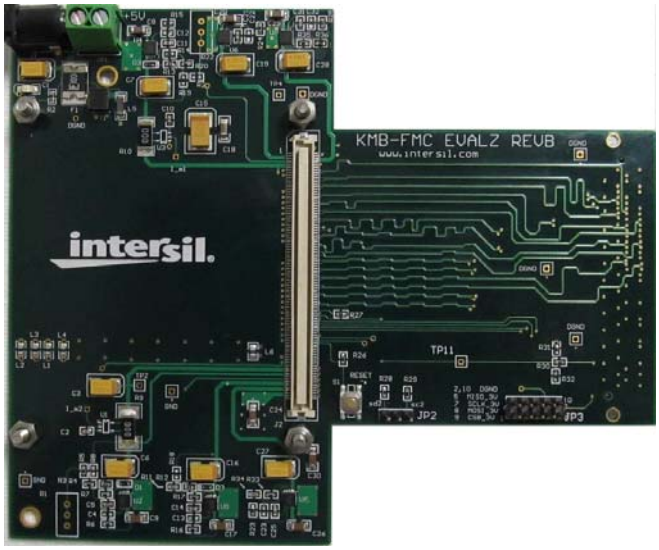

FIGURE 2. PCB TOP VIEW

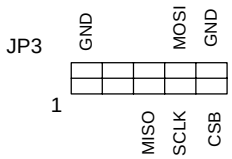

FIGURE 3. JP3 PINOUT

SPI Programming

Access to the ADC SPI port is available at both the FMC connector and header JP3. The ADCs typically support both 3-wire and 4-wire SPI communication and the default mode at power-up is 3-wire mode (consult the appropriate ADC data sheet for more information). It is recommended to use 4-wire SPI communication with the FMC based ADC motherboard, requiring that the ADC first be placed in 4-wire SPI mode by writing to the appropriate ADC register (consult data sheet). A resistor on the daughter card (R4) at the CPLD will need to be removed. Logic levels for the SPI port on card is 3.3V LVCMOS (level translation to 1.8V is done on the ADC daughter cards).

Appendix A: RF Generators

Intersil uses the following RF generators as clock and signal sources when characterizing high-speed ADCs:

- Rohde & Schwarz: SMA100A
- Agilent: 8644B (with Low-Noise option)

These generators provide very low jitter to optimize the SNR performance of the ADC under test. Other generators with similar phase noise performance can also be used. Contact Intersil Technical Support for recommendations.

Appendix B: Daughter Cards

The FMC ADC Evaluation Board (KAD-FMC-EVALZ) connects data, clock, and SPI control signals to/from an ADC to an external FPGA through an LPC FMC connector and a 180 pin Molex connector. The Molex connector interfaces with any of the KAD5XXX and ISLAXXX ADC daughtercards. The schematic for the respective Intersil ADC daughtercard can be downloaded from our website for additional information and bit-ordering. Note that the MSB bit-ordering is different for the ISLA2XXX and KAD5XXX,ISL1XXP50 families. Additional information on Intersil ADC Daughter Cards can be found at the respective ADC product pages on our website.

TABLE 1. LPC FMC CONNECTOR PINOUT

	H	G	D	C
1	NC	GND	NC	GND
2	NC	NC	GND	NC
3	GND	NC	GND	NC
4	NC	GND	NC	GND
5	NC	GND	NC	GND
6	GND	CLKOUTP (FMC LA00_P_CC)	GND	NC
7	DIG_OUT14 (FMC LA02_P)	CLKOUTN (FMC LA00_N_CC)	GND	NC
8	DIG_OUT14N (FMC LA02_N)	GND	DIG_OUT15 (FMC LA01_P)	GND
9	GND	DIG_OUT13 (FMC LA03_P)	DIG_OUT15N (FMC LA01_N)	GND
10	DIG_OUT12 (FMC LA04_P)	DIG_OUT13N (FMC LA03_N)	GND	DIG_OUT10 (FMC LA06_P)
11	DIG_OUT12N (FMC LA04_N)	GND	DIG_OUT11 (FMC LA05_P)	DIG_OUT10N (FMC LA06_N)
12	GND	DIG_OUT9 (FMC LA08_P)	DIG_OUT11N (FMC LA05_N)	GND
13	DIG_OUT8 (FMC LA07_P)	DIG_OUT9N (FMC LA08_N)	GND	GND
14	DIG_OUT8N (FMC LA07_N)	GND	DIG_OUT7 (FMC LA09_P)	DIG_OUT6 (FMC LA10_P)
15	GND	DIG_OUT5 (FMC LA12_P)	DIG_OUT7N (FMC LA09_N)	DIG_OUT6N (FMC LA10_N)
16	DIG_OUT4 (FMC LA11_P)	DIG_OUT5N (FMC LA12_N)	GND	GND
17	DIG_OUT4N (FMC LA11_N)	GND	DIG_OUT3 (FMC LA13_P)	GND
18	GND	DIG_OUT1 (FMC LA16_P)	DIG_OUT3N (FMC LA13_N)	DIG_OUT2 (FMC LA14_P)
19	DIG_OUT0 (FMC LA15_P)	DIG_OUT1N (FMC LA16_N)	GND	DIG_OUT2N (FMC LA14_N)
20	DIG_OUT0N (FMC LA15_N)	GND	NC	GND
21	GND	NC	NC	GND
22	NC	NC	GND	NC
23	NC	GND	NC	NC
24	GND	NC	NC	GND
25	SCLK (LA21_P)	NC	GND	GND
26	CSB (LA21_N	GND	NC	NC
27	GND	NC	NC	NC
28	MISO (LA24_P)	NC	GND	GND

TABLE 1. LPC FMC CONNECTOR PINOUT (Continued)

	H	G	D	C
29	MOSI (LA24_N)	GND	NC	GND
30	GND	NC	NC	NC
31	NC	NC	NC	NC
32	NC	GND	NC	GND
33	GND	NC	NC	GND
34	NC	NC	NC	NC
35	NC	GND	NC	NC
36	GND	NC	NC	GND
37	PC2 (LA32_P)	NC	GND	NC
38	NC	GND	NC	GND
39	GND	NC	GND	NC
40	NC	GND	NC	GND

TABLE 2. FMC PIN OUT DAUGHTER CARD CROSS REFERENCE

FMC PCB 180 PIN DATA CONNECTOR		ISLA2XXX DAUGHTER CARD(72pin QFN) (Note)	KAD5XXX DAUGHTER CARD (72 pin QFN) (Note)
PIN NUMBER	PIN NAME	PIN NAME	PIN NAME
14	dig_out15	lvds_0	ORP
16	dig_outn15	lvds_n0	ORN
20	dig_out14	lvds_1	D13P (MSB)
22	dig_outn14	lvds_n1	D13N (MSB)
26	dig_out13	lvds_2	D12P
28	dig_outn13	lvds_n2	D12N
32	dig_out12	lvds_3	D11P
34	dig_outn12	lvds_n3	D11N
38	dig_out11	lvds_4	D10P
40	dig_outn11	lvds_n4	D10N
44	dig_out10	lvds_5	D9P
46	dig_outn10	lvds_n5	D9N
50	dig_out9	lvds_6	D8P
52	dig_outn9	lvds_n6	D8N
62	dig_out8	lvds_7	D7P
64	dig_outn8	lvds_n7	D7N
68	dig_out7	lvds_8	D6P
70	dig_outn7	lvds_n8	D6N
74	dig_out6	lvds_9	D5P
76	dig_outn6	lvds_n9	D5N
80	dig_out5	lvds_10	D4P
82	dig_outn5	lvds_n10	D4N
86	dig_out4	lvds_11	D3P
88	dig_outn4	lvds_n11	D3N
92	dig_out3	lvds_12	D2P
94	dig_outn3	lvds_n12	D2N
98	dig_out2	lvds_13	D1P
100	dig_outn2	lvds_n13	D1N
104	dig_out1	lvds_14	D0P
106	dig_outn1	lvds_n14	D0N
110	dig_out0	lvds_15 (MSB)	NC
112	dig_outn0	lvds_n15 (MSB)	NC
56	clk_out	clk_out	clkoutp
58	clk_outn	clk_outn	clkoutn
124	sclk_3v	sclk_3v	sclk_3v
126	csb_3v	csb_3v	csb_3v
128	miso_3v	miso_3v	miso_3v

TABLE 2. FMC PIN OUT DAUGHTER CARD CROSS REFERENCE (Continued)

FMC PCB 180 PIN DATA CONNECTOR		ISLA2XXX DAUGHTER CARD(72pin QFN) (Note)	KAD5XXX DAUGHTER CARD (72 pin QFN) (Note)
PIN NUMBER	PIN NAME	PIN NAME	PIN NAME
130	mosi_3v	mosi_3v	mosi_3v
140	PORn_ExtResetn_fpga	PORn_ExtResetn_fpga	PORn_ExtResetn_fpga

NOTE: The 72 pin QFN ADC eval boards are MSB justified; J6 pins 110/112 are the MSB for 16,14,and 12-bit devices: ISLA2XXX while J6 pins 20/22 are the MSB for 14, 12, 10 and 8-bit devices: KAD5XXX, and ISL1XXP50

Schematics

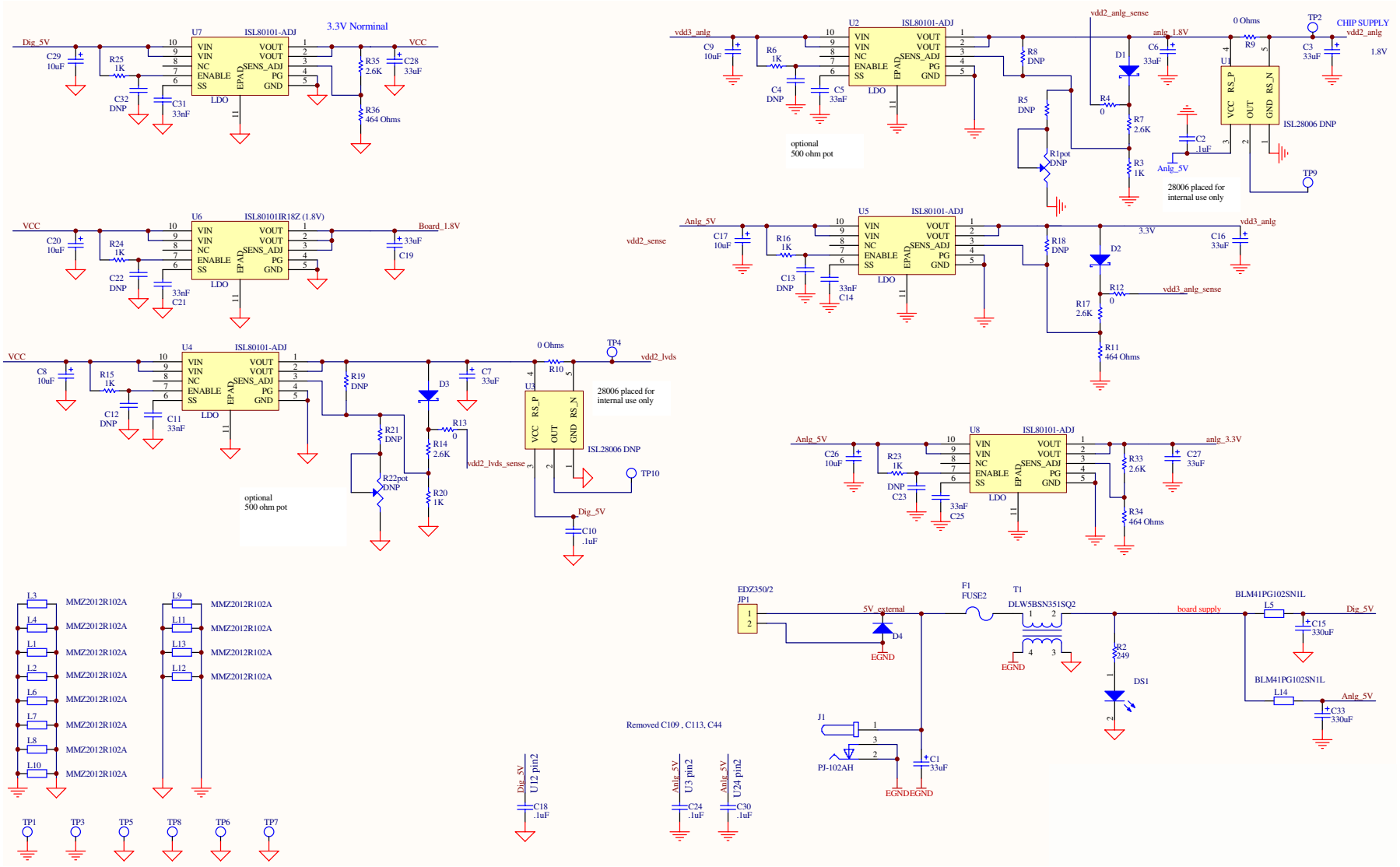

FIGURE 4.

Schematics (Continued)

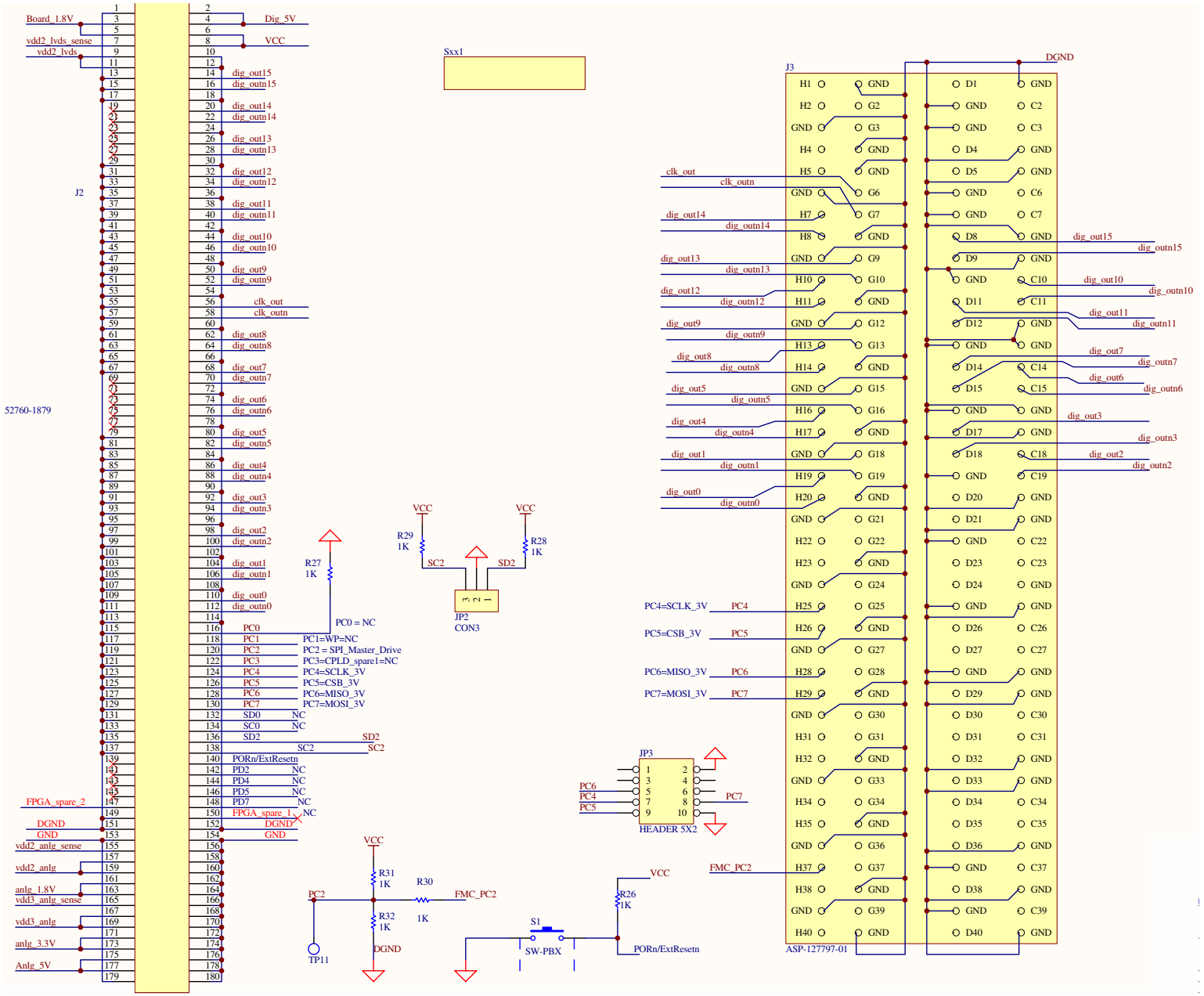

FIGURE 5.

Mouser Electronics

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Intersil:
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