



±80V Fault-Protected, Fail-Safe, 1/4-Unit Load, +3.3V RS-485 Transceiver

MAX3430

General Description

The MAX3430 fault-protected RS-485 transceiver features ±80V protection from overvoltage signal faults on communication bus lines. Each device contains one driver and one receiver, and the output pins can withstand faults, with respect to ground, of up to ±80V. Even if the faults occur when the transceiver is active, shut down, or powered off, the device will not be damaged. The MAX3430 operates from a 3.3V supply and features a slew-rate-limited driver that minimizes EMI and reduces reflections caused by improperly terminated cables, allowing error-free data transmission at data rates up to 250kbps. The MAX3430 has a 1/4-unit-load receiver input impedance allowing up to 128 transceivers on a single bus and features fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open.

Hot-swap circuitry eliminates false transitions on the data cable during circuit initialization or connection to a live backplane. Short-circuit current limiting and thermal-shutdown circuitry protect the driver against excessive power dissipation.

The MAX3430 is available in 8-pin SO and 8-pin PDIP packages, and is specified over commercial and industrial temperature ranges.

Applications

RS-422/RS-485 Communications
Lighting Systems
Industrial-Control Local Area Networks
Profibus Applications
Multimaster RS-485 Networks

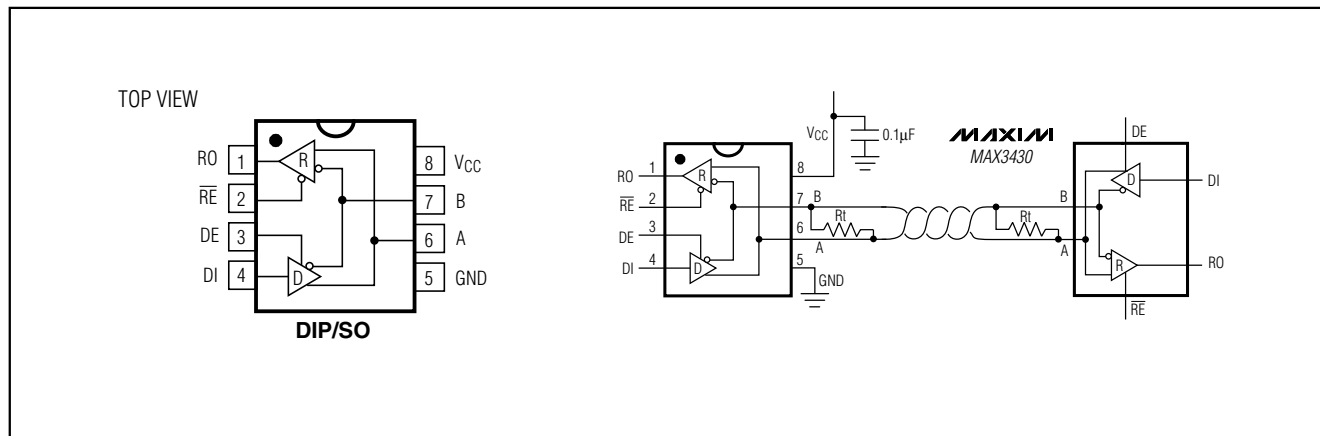
Features

- ◆ ±80V Fault Protection
- ◆ ±12kV ESD Protection
- ◆ +3.3V Operation
- ◆ Internal Slew-Rate Limiting
- ◆ 250kbps Data Rate
- ◆ Allows Up to 128 Transceivers on the Bus
- ◆ -7V to +12V Common-Mode Input Voltage Range
- ◆ True Fail-Safe Inputs
- ◆ Hot-Swap Input Structure on DE
- ◆ Available in 8-Pin SO and PDIP Packages

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3430CPA	0°C to +70°C	8 Plastic DIP
MAX3430CSA	0°C to +70°C	8 SO
MAX3430EPA	-40°C to +85°C	8 Plastic DIP
MAX3430ESA	-40°C to +85°C	8 SO

Pin Configuration and Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

(All voltages are referenced to GND.)

V _{CC}	+5V
RE, DE, DI	-0.3V to (V _{CC} + 0.3V)
Driver Output Voltage (A, B) (Note 1)	±80V
Receiver Input Voltage (A, B) (Note 1)	±80V
RO	-0.3V to (V _{CC} + 0.3V)
Continuous Power Dissipation (T _A = +70°C)	
8-Pin SO (derate 5.88mW/°C above +70°C)	471mW
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C)	727mW

Operating Temperature Ranges

MAX3430C_	0°C to +70°C
MAX3430E_	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: A, B must be terminated with 54Ω or 100Ω to guarantee ±80V fault protection.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.3V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
Differential Driver Output	V _{OD}	Figure 1, R _L = 100Ω	2.0		V _{CC}	V
		Figure 1, R _L = 54Ω	1.5		V _{CC}	
Change in Magnitude of Differential Output Voltage	ΔV _{OD}	Figure 1, R _L = 100Ω or 54Ω (Note 2)			0.2	V
Driver Common-Mode Output Voltage	V _{OC}	Figure 1, R _L = 100Ω or 54Ω		V _{CC} / 2	3	V
Change in Magnitude of Common-Mode Voltage	ΔV _{OC}	Figure 1, R _L = 100Ω or 54Ω (Note 2)			0.2	V
DRIVER LOGIC						
Driver Input High Voltage	V _{IH}	DI	2.0			V
Driver Input Low Voltage	V _{IL}	DI			0.8	V
Driver Input Current	I _{IN}	DI			±1	μA
Driver Short-Circuit Output Current	I _{OSD}	0 ≤ V _{OUT} ≤ 12V (Note 3)			+250	mA
		-7V ≤ V _{OUT} ≤ V _{CC} (Note 3)	-250			
Driver Short-Circuit Foldback Output Current	I _{OSDF}	(V _{CC} - 1V) ≤ V _{OUT} ≤ 12V (Note 3)	+10			mA
		-7V ≤ V _{OUT} ≤ 1V (Note 3)			-10	
RECEIVER						
Input Current (A, B)	I _{A, B}	DE = GND, $\overline{\text{RE}}$ = GND, V _{IN} = +12V			250	μA
		DE = GND, $\overline{\text{RE}}$ = GND, V _{IN} = -7V			-200	
		V _{IN} = -80V to +80V	-6		+6	mA
Receiver Differential Threshold Voltage	V _{TH}	-7V ≤ V _{CM} ≤ 12V	-200		-50	mV
Receiver Input Hysteresis	ΔV _{TH}	V _A + V _B = 0		25		mV

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +3.3V \pm 10\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER LOGIC						
RO Output High Voltage	V_{OH}	$I_O = -1.6mA$	$V_{CC} - 0.6$			V
RO Output Low Voltage	V_{OL}	$I_O = 1mA$			0.4	V
Three-State Output Current at Receiver	I_{OZR}	$0 \leq V_O \leq V_{CC}$			± 1	μA
Receiver Input Resistance	R_{IN}	$-7V \leq V_{CM} \leq 12V$	48			$k\Omega$
Receiver Output Short-Circuit Current	I_{OSR}	$0 \leq V_{RO} \leq V_{CC}$			± 95	mA
CONTROL						
Control Input High Voltage	V_{CIH}	DE, $\overline{RE}$	2.0			V
Control Input Low Voltage	V_{CIL}	DE, $\overline{RE}$			0.8	V
Input Current DE Current Latch During First DE Rising Edge				80		μA
Input Current $\overline{RE}$ Current Latch During First $\overline{RE}$ Rising Edge				80		μA

PROTECTION SPECIFICATIONS

($V_{CC} = +3.3V \pm 10\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ESD Protection		A, B	Human Body Model		± 12		kV
SUPPLY CURRENT							
Supply Current	I_{CC}	No load, $\overline{RE} = 0$, DE = V_{CC} , DI = 0 or V_{CC}			3.5	10	mA
		No load, $\overline{RE} = V_{CC}$, DE = V_{CC} , DI = 0 or V_{CC}			3.0	8	
Supply Current in Shutdown Mode	I_{SHDN}	$\overline{RE} = V_{CC}$, DE = 0				200	μA

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DRIVER SWITCHING CHARACTERISTICS

($V_{CC} = +3.3V \pm 10\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Propagation Delay	t_{DPLH}	Figures 2 and 3, $R_L = 54\Omega$, $C_L = 50pF$		700	1500	ns
	t_{DPLH}			700	1500	
Driver Differential Output Rise or Fall Time	t_{DR}, t_{DF}	Figures 2 and 3, $R_L = 54\Omega$, $C_L = 50pF$	250		1200	ns
Differential Driver Output Skew, $ t_{DPLH} - t_{DPLH} $	t_{DSKEW}	Figures 2 and 3, $R_L = 54\Omega$, $C_L = 50pF$		150	200	ns
Maximum Data Rate			250			kbps
Driver Enable to Output Low	t_{DZL}	Figure 4, $C_L = 50pF$			5200	ns
Driver Disable Time from Output Low	t_{DLZ}	Figure 4, $C_L = 50pF$			1000	ns
Driver Output Enable Time from Shutdown	$t_{DZL}(SHDN)$	Figure 4, $C_L = 50pF$			8000	ns
Driver Enable to Output High	t_{DZH}	Figure 5, $C_L = 50pF$			5200	ns
Driver Disable Time from Output High	t_{DZH}	Figure 5, $C_L = 50pF$			1000	ns
Driver Output Enable Time from Shutdown	$t_{DZH}(SHDN)$	Figure 5, $C_L = 50pF$			8000	ns
Driver Time to Shutdown	t_{SHDN}				1000	ns

RECEIVER SWITCHING CHARACTERISTICS

($V_{CC} = +3.3V \pm 10\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Receiver Propagation Delay	t_{RPLH}	Figure 6, $C_L = 20pF$, $V_{ID} = 2V$, $V_{CM} = 0$			120	ns
	t_{RPHL}				120	
Receiver Output Skew, $ t_{RPLH} - t_{RPHL} $	t_{SKEW}	Figure 6, $C_L = 20pF$			40	ns
Receiver Enable to Output Low	t_{RZL}	Figure 7, $R = 1k\Omega$, $C_L = 20pF$			80	ns
Receiver Enable to Output High	t_{RZH}	Figure 7, $R = 1k\Omega$, $C_L = 20pF$			80	ns
Receiver Disable Time from Low	t_{RLZ}	Figure 7, $R = 1k\Omega$, $C_L = 20pF$			80	ns
Receiver Disable Time from High	t_{RHZ}	Figure 7, $R = 1k\Omega$, $C_L = 20pF$			80	ns
Receiver Output Enable Time from Shutdown	$t_{RZH}(SHND)$, $t_{RZL}(SHND)$	Figure 7, $R = 1k\Omega$, $C_L = 20pF$			5000	ns
Receiver Time to Shutdown	t_{SHDN}				1000	ns

Note 2: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC} , respectively, when the DI input changes state.

Note 3: The short-circuit output current applies to peak current just prior to foldback current limiting; the short-circuit foldback output current applies during current limiting to allow a recovery from bus contention.

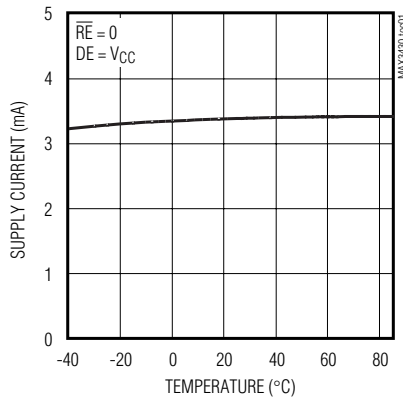
±80V Fault-Protected, Fail-Safe, 1/4-Unit Load, +3.3V RS-485 Transceiver

Typical Operating Characteristics

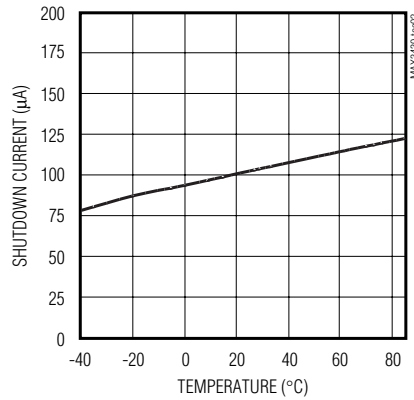
($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)

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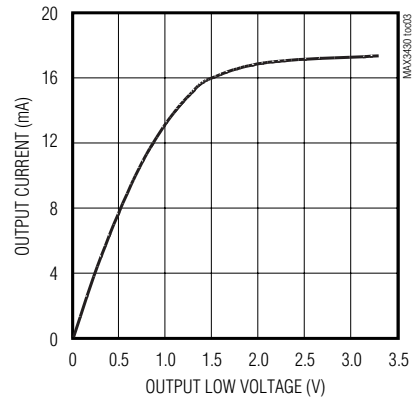
**SUPPLY CURRENT
vs. TEMPERATURE**



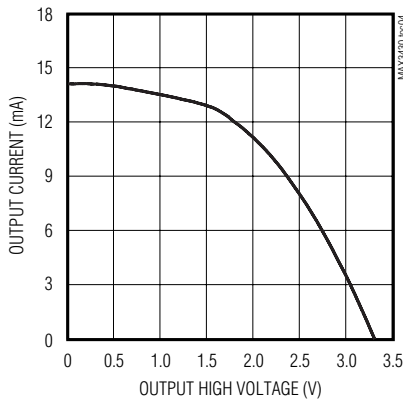
**SHUTDOWN CURRENT
vs. TEMPERATURE**



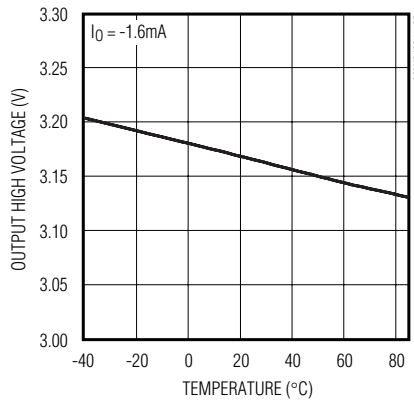
**OUTPUT CURRENT
vs. RECEIVER OUTPUT LOW VOLTAGE**



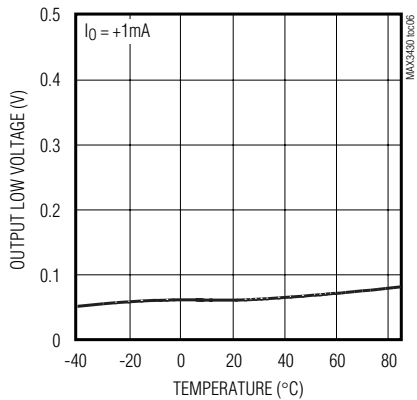
**OUTPUT CURRENT
vs. RECEIVER OUTPUT HIGH VOLTAGE**



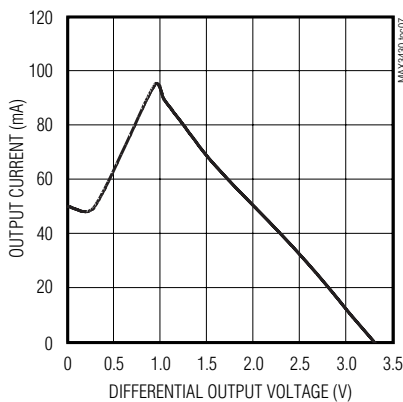
**RECEIVER OUTPUT HIGH VOLTAGE
vs. TEMPERATURE**



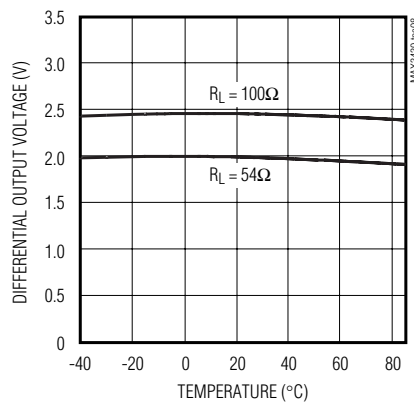
**RECEIVER OUTPUT LOW VOLTAGE
vs. TEMPERATURE**



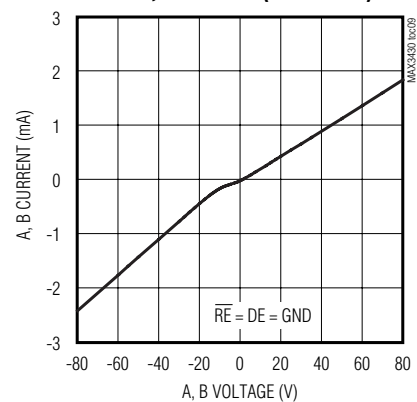
**DRIVER OUTPUT CURRENT
vs. DIFFERENTIAL OUTPUT VOLTAGE**



**DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs. TEMPERATURE**



**A, B CURRENT
vs. A, B VOLTAGE (TO GROUND)**



$\pm 80V$ Fault-Protected, Fail-Safe, 1/4-Unit Load, +3.3V RS-485 Transceiver

Test Circuits/Timing Diagrams

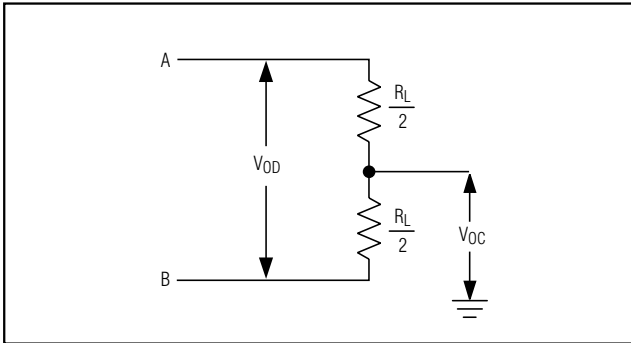


Figure 1. Driver DC Test Load

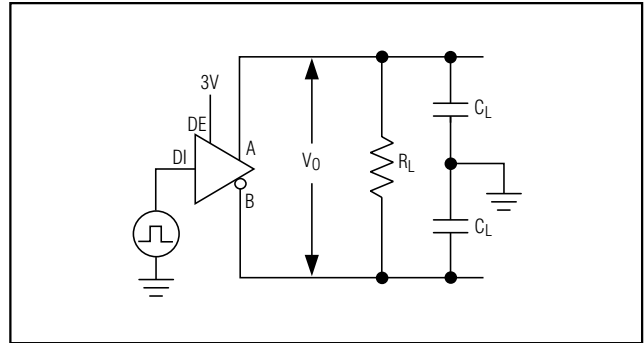


Figure 2. Driver Timing Test Circuit

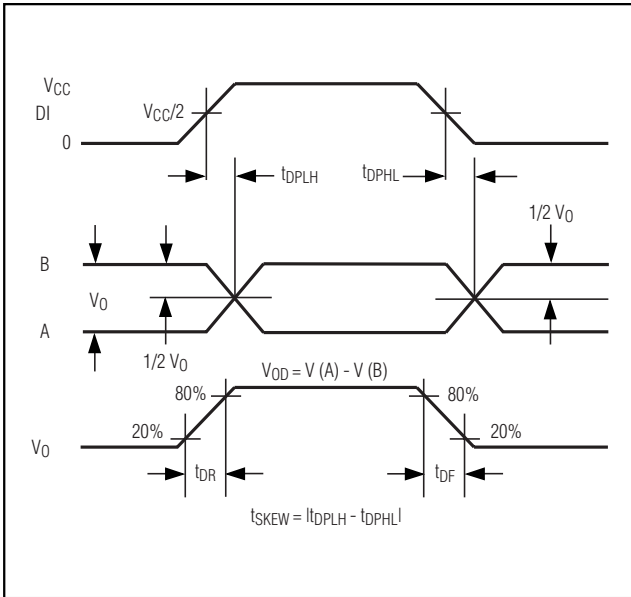


Figure 3. Driver Propagation Delays

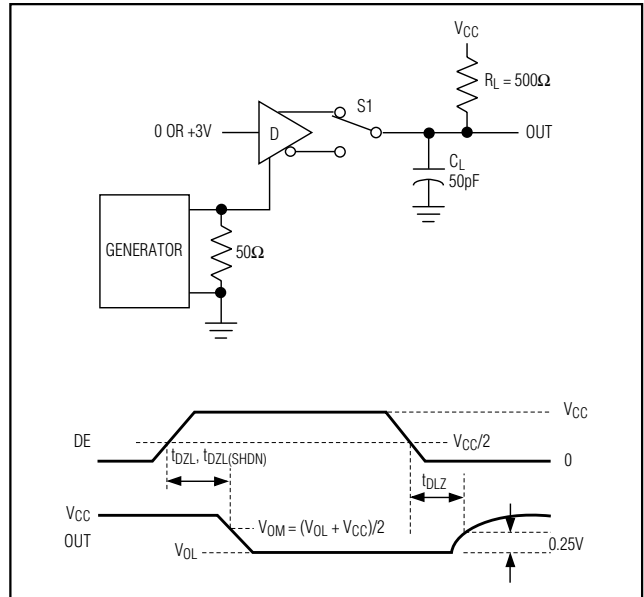


Figure 4. Driver Enable and Disable Times (t_{DZL} , t_{DLZ} , $t_{DLZ(SHDN)}$)

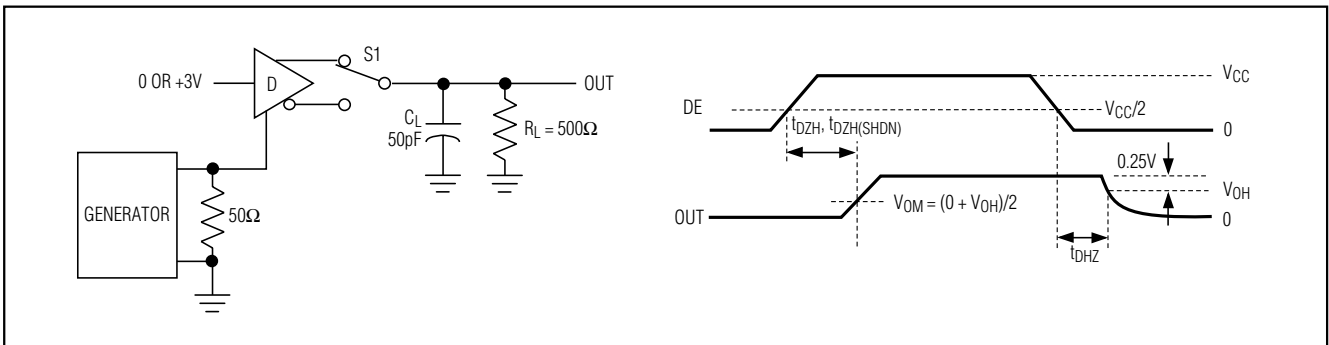


Figure 5. Driver Enable and Disable Times (t_{DZH} , $t_{DZH(SHDN)}$)

$\pm 80V$ Fault-Protected, Fail-Safe, 1/4-Unit Load, +3.3V RS-485 Transceiver

Test Circuits/Timing Diagrams (continued)

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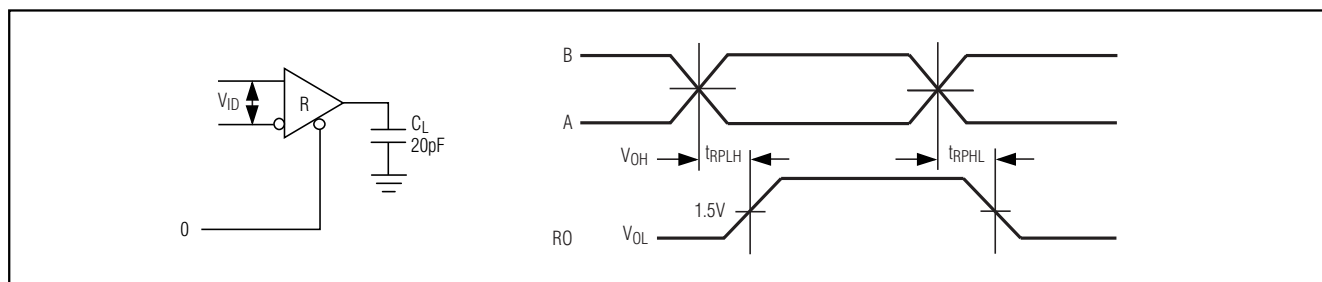


Figure 6. Receiver Propagation Delays

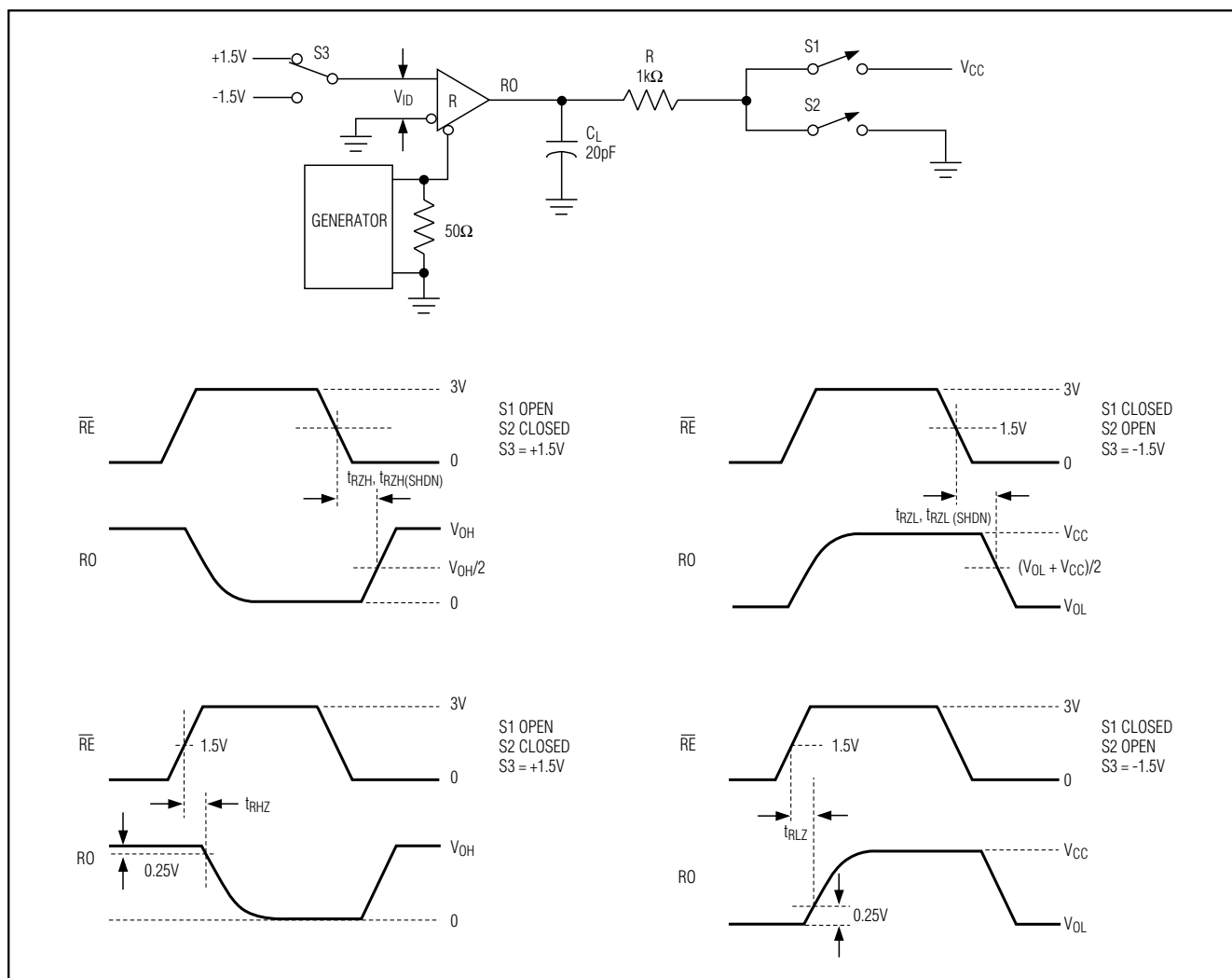


Figure 7. Receiver Enable and Disable Times

±80V Fault-Protected, Fail-Safe, 1/4-Unit Load, +3.3V RS-485 Transceiver

Pin Description

PIN	NAME	FUNCTION
1	RO	Receiver Output
2	$\overline{RE}$	Receiver Output Enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high. The device enters a low-power shutdown mode if $\overline{RE}$ is high and DE is low.
3	DE	Driver Output Enable. Driving DE high enables the driver outputs. Pulling DE low puts the driver outputs in a high-impedance state. If $\overline{RE}$ is high and DE is low, the device enters a low-power shutdown mode. If the driver outputs are enabled, the device functions as a line driver, and when they are high impedance it functions as a line receiver if $\overline{RE}$ is low.
4	DI	Driver Input. A logic low on DI forces output A low and output B high, while a logic high on DI forces output A high and output B low.
5	GND	Ground
6	A	Noninverting Receiver Input/Driver Output
7	B	Inverting Receiver Input/Driver Output
8	VCC	Positive Supply, VCC = +3.3V ±10%. Bypass VCC to GND with a 0.1µF ceramic capacitor.

Function Tables

Table 1. Transmitting

INPUTS			OUTPUTS		MODE
$\overline{RE}$	DE	DI	B	A	
X	1	1	0	1	Normal
X	1	0	1	0	Normal
0	0	X	High-Z	High-Z	Normal
1	0	X	High-Z	High-Z	Shutdown

X = Don't care.

Table 2. Receiving

INPUTS			OUTPUTS	MODE
$\overline{RE}$	DE	(A - B)	RO	
0	0	≥ -50mV	1	Normal
0	0	≤ -200mV	0	Normal
0	0	Inputs open	1	Normal
1	0	X	High-Z	Shutdown

X = Don't care.

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Detailed Description

Driver

The driver accepts a single-ended, logic-level input (DI) and transfers it to a differential, RS-485 level output (A and B). Driving DE high enables the driver, while pulling DE low places the driver outputs (A and B) into a high-impedance state.

Receiver

The receiver accepts a differential, RS-485 level input (A and B), and transfers it to a single-ended, logic-level output (RO). Pulling $\overline{RE}$ low enables the receiver, while driving $\overline{RE}$ high and DE low places the receiver inputs (A and B) into a high-impedance state.

Low-Power Shutdown

Force DE low and $\overline{RE}$ high to shut down the MAX3430. A time delay of $1\mu s$ prevents the device from accidentally entering shutdown due to logic skews when switching between transmit and receive modes. Holding DE low and $\overline{RE}$ high for at least 1ms guarantees that the MAX3430 enters shutdown. In shutdown, the device consumes $100\mu A$ supply current.

$\pm 80V$ Fault Protection

The driver outputs/receiver inputs of RS-485 devices in industrial network applications often experience voltage faults resulting from transients that exceed the $-7V$ to $+12V$ range specified in the EIA/TIA-485 standard. In these applications, ordinary RS-485 devices (typical absolute maximum ratings $-8V$ to $+12.5V$) require costly external protection devices. To reduce system complexity and the need for external protection, the driver outputs/receiver inputs of the MAX3430 withstand voltage faults of up to $\pm 80V$ with respect to ground without damage (see the *Absolute Maximum Ratings* section, Note 1). Protection is guaranteed regardless of whether the device is active, shut down, or without power.

True Fail-Safe

The MAX3430 uses a $-50mV$ to $-200mV$ differential input threshold to ensure true fail-safe receiver inputs. This threshold guarantees the receiver outputs a logic high for shorted, open, or idle data lines. The $-50mV$ to $-200mV$ threshold complies with the $\pm 200mV$ threshold EIA/TIA-485 standard.

$\pm 12kV$ ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against ESD encountered during handling and assembly. The MAX3430 receiver inputs/driver outputs (A, B) have extra protection against static electricity found in normal operation. Maxim's engineers have developed state-of-the-art structures to protect these pins against $\pm 12kV$ ESD without damage. After an ESD event, the MAX3430 continues working without latchup.

ESD protection can be tested in several ways. The receiver inputs are characterized for protection up to $\pm 12kV$ using the Human Body Model.

ESD Test Conditions

ESD performance depends on a number of conditions. Contact Maxim for a reliability report that documents test setup, methodology, and results.

Human Body Model

Figure 8a shows the Human Body Model, and Figure 8b shows the current waveform it generates when discharged into a low impedance. This model consists of a $100pF$ capacitor charged to the ESD voltage of interest, which is then discharged into the device through a $1.5k\Omega$ resistor.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or bus contention. The first, a foldback current limit on the driver output

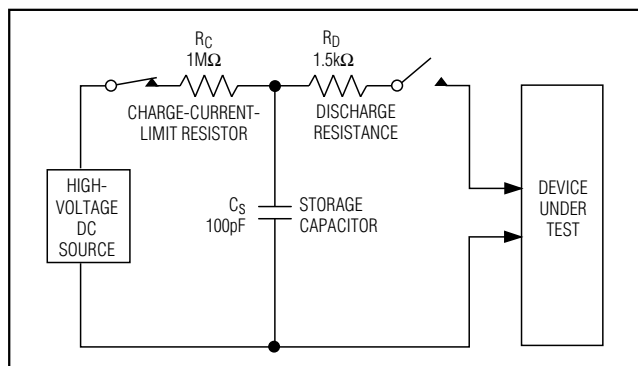


Figure 8a. Human Body ESD Test Model

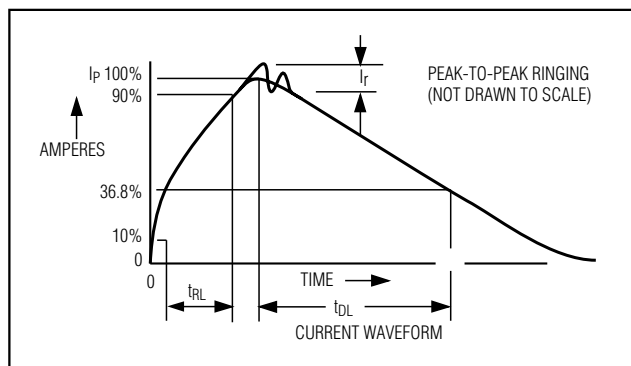


Figure 8b. Human Body Model Current Waveform

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stage, provides immediate protection against short circuits over the whole common-mode voltage range. The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds $+160^{\circ}\text{C}$. Normal operation resumes when the die temperature cools by $+140^{\circ}\text{C}$, resulting in a pulsed output during continuous short-circuit conditions.

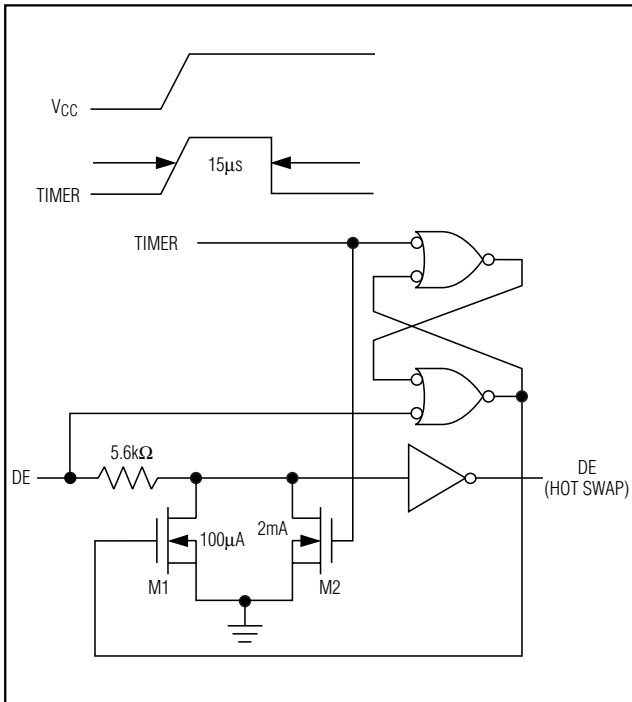


Figure 9. Simplified Structure of the Driver Enable Pin (DE)

Hot-Swap Capability

Hot-Swap Inputs

Inserting circuit boards into a hot, or powered backplane may cause voltage transients on DE, RE, and receiver inputs A and B that can lead to data errors. For example, upon initial circuit board insertion, the processor undergoes a power-up sequence. During this period, the high-impedance state of the output drivers makes them unable to drive the MAX3430 enable inputs to a defined logic level. Meanwhile, leakage currents of up to $10\mu\text{A}$ from the high-impedance output, or capacitively coupled noise from VCC or GND, could cause an input to drift to an incorrect logic state. To prevent such a condition from occurring, the MAX3430 features hot-swap input circuitry on DE to safeguard against unwanted driver activation during hot-swap situations. When VCC rises, an internal pulldown circuit holds DE low for at least $10\mu\text{s}$, and until the current into DE exceeds $200\mu\text{A}$. After the initial power-up sequence, the pulldown circuit becomes transparent, resetting the hot-swap tolerable input.

Hot-Swap Input Circuitry

At the driver enable input (DE), there are two NMOS devices, M1 and M2 (Figure 9). When VCC ramps from 0, an internal $15\mu\text{s}$ timer turns on M2 and sets the SR latch, which also turns on M1. Transistors M2, a 2mA current sink, and M1, a $100\mu\text{A}$ current sink, pull DE to GND through a $5.6\text{k}\Omega$ resistor. M2 pulls DE to the disabled state against an external parasitic capacitance up to 100pF that may drive DE high. After $15\mu\text{s}$, the timer deactivates M2 while M1 remains on, holding DE low against three-state leakage currents that may drive DE high. M1 remains on until an external current source overcomes the required input current. At this time, the SR latch resets M1 and turns off. When M1 turns off, DE reverts to a standard, high-impedance CMOS input. Whenever VCC drops below $1V$, the input is reset.

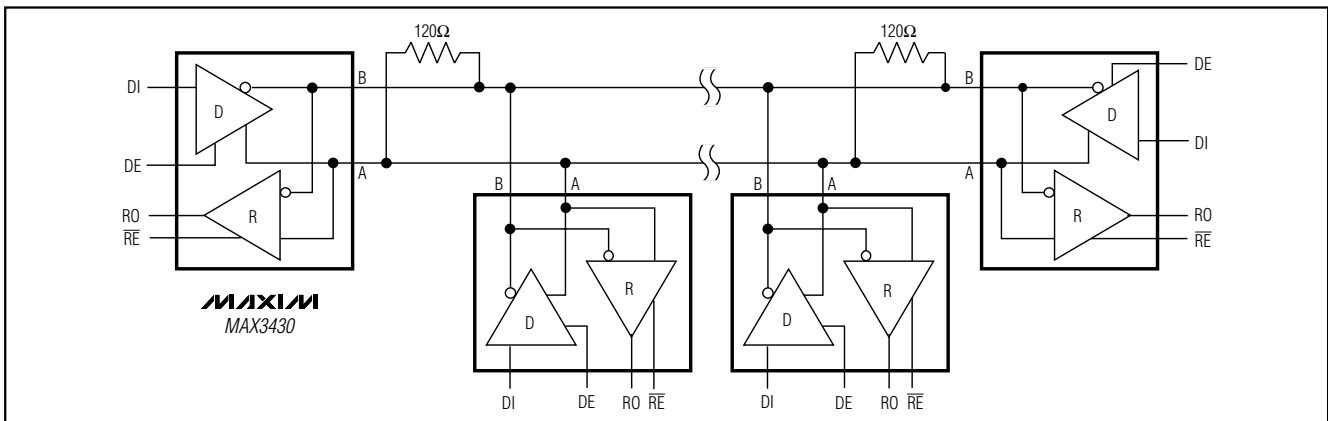


Figure 10. Typical RS-485 Network

$\pm 80V$ Fault-Protected, Fail-Safe, 1/4-Unit Load, +3.3V RS-485 Transceiver

Applications Information

128 Transceivers on the Bus

The standard RS-485 receiver input impedance is $12k\Omega$ (one-unit load), and a standard driver can drive up to 32-unit loads. The MAX3430 transceiver 1/4-unit-load receiver input impedance ($48k\Omega$) allows up to 128 transceivers connected in parallel on one communication line. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit loads to the line.

RS-485 Applications

The MAX3430 transceiver provides bidirectional data communications on multipoint bus transmission lines. Figure 10 shows a typical network applications circuit. The RS-485 standard covers line lengths up to 4000ft. The signal line must be terminated at both ends in its characteristic impedance, and stub lengths off the main line kept as short as possible.

Chip Information

TRANSISTOR COUNT: 300

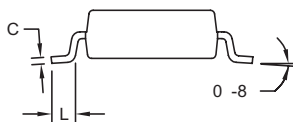
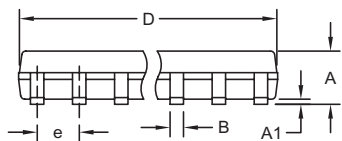
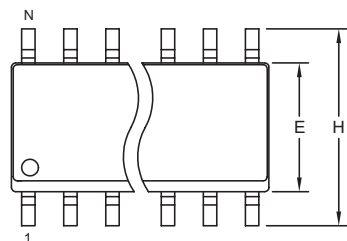
PROCESS: BiCMOS

MAX3430

±80V Fault-Protected, Fail-Safe, 1/4-Unit Load, +3.3V RS-485 Transceiver

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

DIM	INCHES		MILLIMETERS		N	MS012
	MIN	MAX	MIN	MAX		
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC

NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

 DALLAS SEMICONDUCTOR			
PROPRIETARY INFORMATION			
TITLE:			
PACKAGE OUTLINE, .150" SOIC			
APPROVAL	DOCUMENT CONTROL NO.	REV.	1/
	21-0041	B	

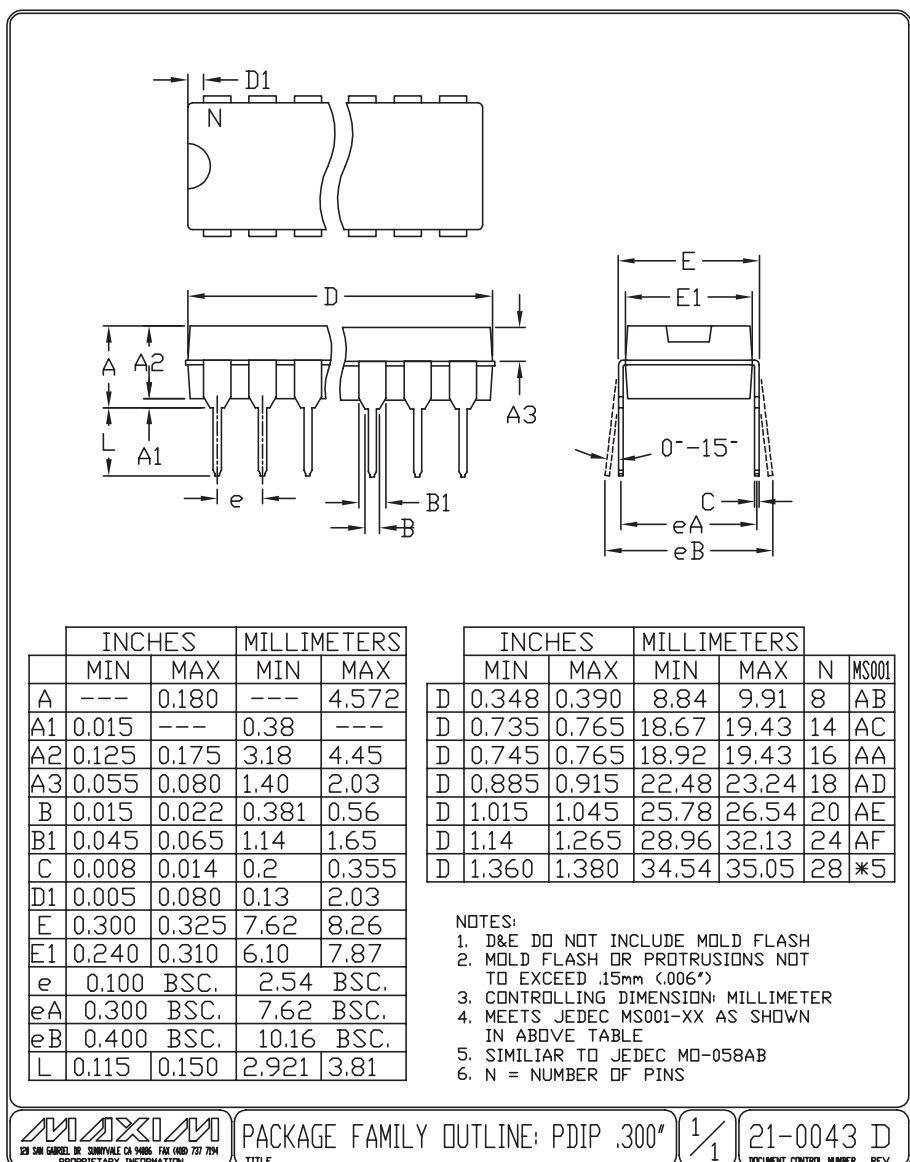
SOICN EPS

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Package Information (continued)

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MAX3430



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