

**NE5550979A-EV04-A**

**Evaluation Board**

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- Circuit Schematic and Assembly Drawing

## Circuit Description

The NE5550979A-EV04-A is an evaluation circuit board for Renesas' LDMOS power FET, NE5550979A optimized for the performance at 460MHz. The circuit board is RoHS compliant.

### Matching and Bias Circuits

Both input and output matching networks consist of shunt capacitors and sections of transmission lines (refer to the schematic and assembly drawing in the two last pages for the component designation). The electrical lengths of the transmission lines labeled on the schematic are estimated and for reference only. Some bench tuning on the actual circuit board is usually required to achieve optimal performance. For applications where there is a constraint on the board space, a serial inductor, instead of transmission lines, can be used for the matching circuits. The efficiency, PAE, will be slightly lower in that case. The resistor, R1(=1ohm) at input is used to improve the stability margin. The gain is reduced by about 1dB when R1 used.

LDMOSFETs essentially draw no gate current under normal operation conditions. Therefore a large value resistor, in the order of  $k\Omega$ , can be used for the bias at gate so that the RF path is completely isolated from the DC line. At the drain an inductor is used as the RF choke. The current rating for this inductor should be high enough to provide the required current at the operation conditions.

### Bias Conditions

This evaluation board was optimized at a specific drain voltage, 7.5V. For different supply voltages, the matching circuits should be adjusted to fully utilize the device capability. The quiescent current is 200mA for the data shown below. The gain is higher at higher quiescent currents, particularly when the device is not completely saturated. For many communication systems, where the PA is never at idle state, a high quiescent current might be used.

### PCB Material:

The PCB is Getek 28mil two layer board. The dielectric constant of Getek is 4.2.

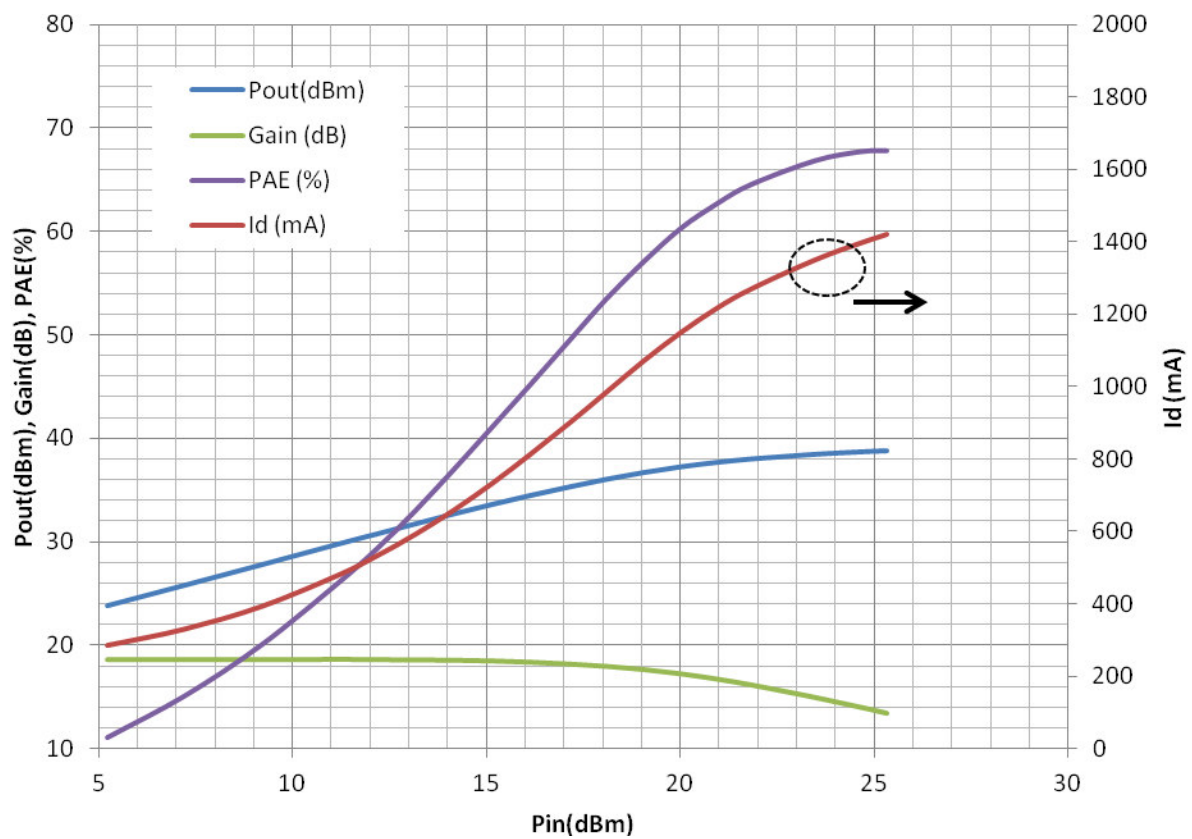
## Typical Performance Data

Test Conditions:

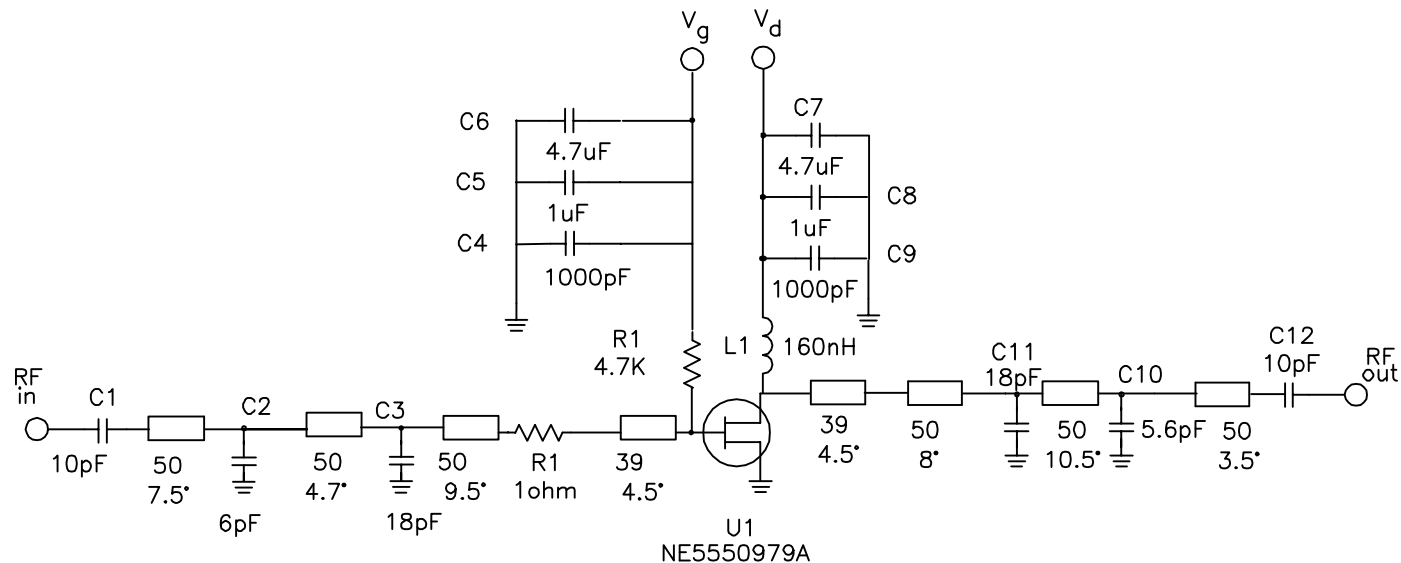
$f=460\text{MHz}$

$V_d=7.5\text{V}$ ,  $I_{dsq}=200\text{mA}$

$P_{out}$ , Gain, PAE and Current vs  $P_{in}$  are shown in the following plot.



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

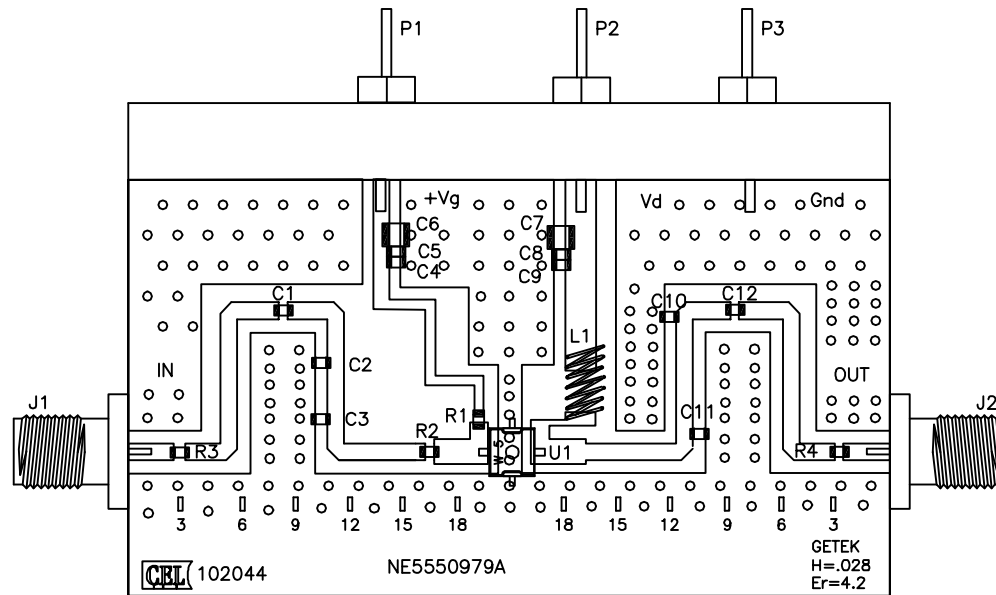


Note: All trace electrical lengths are at 460MHz

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS .01 ± ANGULAR .005 ± 1° .XXX ± DO NOT SCALE DRAWING	APPROVALS		<b>CALIFORNIA EASTERN LABS</b> 4590 PATRICK HENRY DR. SANTA CLARA CA. 95054 TITLE: NE5550979A-EV04-A SCHEMTAIC
			Drawing by:	Mouqun Dong	3/1/2012
			Designed by:	Mouqun Dong	3/1/2012
			Checked by:		
		MATERIAL	Project Engineer:		
		FINISH	Quality Control:		
NEXT ASSY	USED ON				
APPLICATION					

SIZE	FSCM NO.	DWG NO.	REV
C		AD102044	—
SCALE NONE	RELEASE DATE	PROTOTYPE	SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



1	GRM1885C1H5R6CZ01B+C01	C10	0603 5.6pF CAP MURATA	15
2	GRM185R61C105KE44D	C5,C8	0603 1uF CAP MURATA	14
2	GRM1885C1H102JA01B+A01	C4,C9	0603 1000pF CAP MURATA	13
2	GRM1885C1H180JA01B+A01	C3,C11	0603 18pF CAP MURATA	12
2	267M1002475K	C6,C7	4.7uF 10V TANT CHIP CAP B MATS	11
1	GRM1885C1H6R0DZ01B+C01	C2	0603 6.0pF CAP MURATA	10
2	GRM1885C1H100JA01B+A01	C1,C12	0603 10pF CAP MURATA	9
2	GENERIC	R3,R4	0603 0 OHM RESISTOR	8
1	GENERIC	R2	0603 1 OHM RESISTOR	7
1	GENERIC	R1	0603 4.7K OHM RESISTOR	6
1	2222SQ-161-JE	L1	160nH INDUCTOR COILCRAFT	5
3	2340-6111 TG	P1,P2,P3	PIN HEADER 3M	4
2	5308-2CC	J1,J2	SMA 4H FLANGE JACK TENSOLITE	3
1	NE5550979A-A	U1	RENESAS NE5550979A-A	2
1	CL-102044	DRAWING	COMPONENT LAYOUT DRAWING	1
QTY	PART NUMBER OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION	ITEM NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS ANGULAR .XX± .01 ± 1° .XXX± .005 DO NOT SCALE DRAWING		APPROVALS		CALIFORNIA EASTERN LABS 4590 PATRICK HENRY DR. SANTA CLARA CA. 95054 TITLE: NE5550979A-EV04-A ASSEMBLY DRAWING AND BOM						
		MATERIAL		Drawing by: M Dong	3/1/2012	SIZE C	FSCM NO. DWG NO. AD-102044	REV -		
		FINISH		Designed by: M Dong	3/1/2012					
NEXT ASSY		USED ON		Project Engineer:		SCALE	RELEASE DATE	PROTOTYPE	SHEET 1	OF 1
APPLICATION				Quality Control:						