Dual, 2-Phase Synchronous Step-Down Switching Controller

FEATURES

- **Dual, 180° Phased Controllers Reduce Required Input Capacitance and Power Supply Induced Noise**
- **High Efficiency: Up to 95%**
- **R_{SENSE} or DCR Current Sensing**
- **±1% 0.8V Output Voltage Accuracy**
- **Phase-Lockable Fixed Frequency 250kHz to 780kHz**
- Supports Pre-Biased Output
- Dual N-Channel MOSFET Synchronous Drive
- Wide V_{IN} Range: 4V to 24V (30V for LTC3850I) Operation
- Adjustable Soft-Start Current Ramping or Tracking
- Foldback Output Current Limiting
- Output Overvoltage Protection
- Power Good Output Voltage Monitor
- 28-Pin 4mm × 4mm, 4mm × 5mm QFN and Narrow SSOP Packages

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Battery-Operated Digital Devices
- DC Power Distribution Systems

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DESCRIPTION

The LTC®3850 is a high performance dual synchronous step-down switching regulator controller that drives all N-channel power MOSFET stages. A constant-frequency current mode architecture allows a phase-lockable frequency of up to 780kHz. Power loss and supply noise are minimized by operating the two controller output stages out of phase.

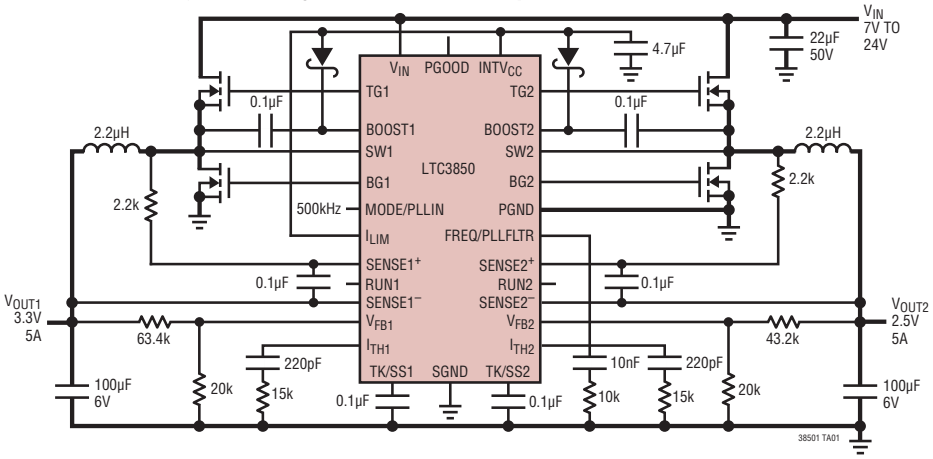
OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The LTC3850 features a precision 0.8V reference and a power good output indicator. A wide 4V to 24V (28V maximum/30V for LTC3850I) input supply range encompasses most battery chemistries and intermediate bus voltages.

Independent TK/SS pins for each controller ramp the output voltages during start-up. Current foldback limits MOSFET heat dissipation during short-circuit conditions. The MODE/PLLIN pin selects among Burst Mode® operation, pulse-skipping mode, or continuous inductor current mode and allows the IC to be synchronized to an external clock.

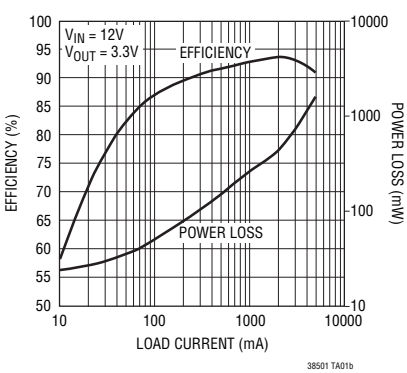
The LTC3850 is available in low profile 28-pin 4mm × 4mm, 4mm × 5mm QFN and narrow SSOP packages.

TYPICAL APPLICATION

High Efficiency Dual 3.3V/2.5V Step-Down Converter



Efficiency

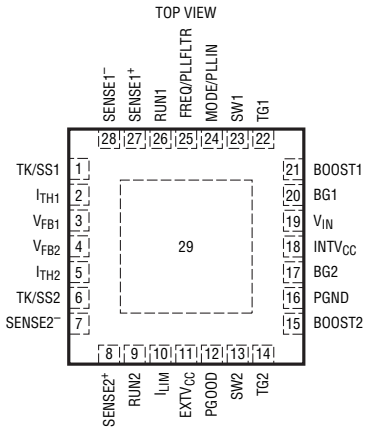


ABSOLUTE MAXIMUM RATINGS (Note 1)

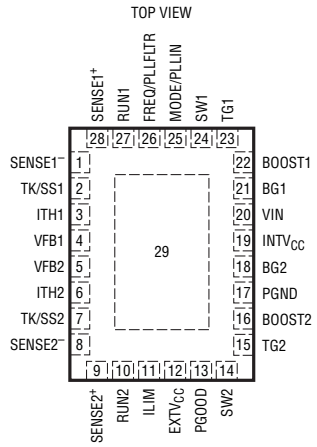
Input Supply Voltage (V_{IN}) ..... 28V to –0.3V
Input Supply Voltage (V_{IN}),
LTC3850I Only ..... 30V to –0.3V
Input Supply Transient Voltage (V_{IN}) < 500ms, with
$INTV_{CC}$ ≥ 5V, LTC3850I Only..... 34V to –0.3V
Top Side Driver Voltages
BOOST1, BOOST2..... 34V to –0.3V
Switch Voltage (SW1, SW2) ..... 28V to –5V
Switch Voltage (SW1, SW2),
LTC3850I Only ..... 30V to –5V
$INTV_{CC}$, RUN1, RUN2, PGOOD, $EXTV_{CC}$,
(BOOST1-SW1), (BOOST2-SW2)..... 6V to –0.3V
$SENSE1^+$, $SENSE2^+$, $SENSE1^–$,
$SENSE2^–$ Voltages..... 5.5V to –0.3V
MODE/PLLIN, I_{LIM},TK/SS1,TK/SS2, FREQ/PLLFLTR
Voltages ..... $INTV_{CC}$ to –0.3V
I_{TH1}, I_{TH2}, V_{FB1}, V_{FB2} Voltages..... 2.7V to –0.3V
$INTV_{CC}$ Peak Output Current 100mA
Operating Temperature Range (Note 2)....–40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range.....–65°C to 125°C
Lead Temperature (Soldering, 10 sec)
(GN Package)..... 300°C

PIN CONFIGURATION

GN PACKAGE
28-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 95°C/W
*PIN 14 = I_{LIM} FOR LTC3850GN, $EXTV_{CC}$ FOR LTC3850GN-1



UF PACKAGE
28-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W, θ_{JC} = 2.6°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W, EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3850EGN#PBF	LTC3850EGN#TRPBF	LTC3850GN	28-Lead Narrow Plastic SSOP	–40°C to 85°C
LTC3850EGN-1#PBF	LTC3850EGN-1#TRPBF	LTC3850GN-1	28-Lead Narrow Plastic SSOP	–40°C to 85°C
LTC3850IGN#PBF	LTC3850IGN#TRPBF	LTC3850GN	28-Lead Narrow Plastic SSOP	–40°C to 85°C
LTC3850IGN-1#PBF	LTC3850IGN-1#TRPBF	LTC3850GN-1	28-Lead Narrow Plastic SSOP	–40°C to 85°C
LTC3850EUF#PBF	LTC3850EUF#TRPBF	3850	28-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C
LTC3850EUFD#PBF	LTC3850EUFD#TRPBF	3850	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LTC3850IUF#PBF	LTC3850IUF#TRPBF	3850	28-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C
LTC3850IUFD#PBF	LTC3850IUFD#TRPBF	3850	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 15V, $V_{RUN1,2}$ = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops							
$V_{FB1,2}$	Regulated Feedback Voltage	$I_{TH1,2}$ Voltage = 1.2V; (Note 4)	●	0.792	0.800	0.808	V
$I_{FB1,2}$	Feedback Current	(Note 4)			–10	–50	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{IN} = 6V to 24V (Note 4)			0.002	0.02	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 0.7V Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 1.6V	 ● ●		 0.01 –0.01	 0.1 –0.1	 % %
$g_{m1,2}$	Transconductance Amplifier g_m	$I_{TH1,2}$ = 1.2V; Sink/Source 5µA; (Note 4)			2.2		mmho
I_Q	Input DC Supply Current Normal Mode Shutdown	(Note 5) V_{IN} = 15V; $EXTV_{CC}$ Tied to V_{OUT1}; V_{OUT1} = 5V $V_{RUN1,2}$ = 0V			 850 30	 50	 µA µA
UVLO	Undervoltage Lockout on $INTV_{CC}$	V_{INTVCC} Ramping Down			3		V
$UVLO_{HYS}$	UVLO Hysteresis				0.5		V
DF_{MAX}	Maximum Duty Factor	In Dropout		96	97.2		%
V_{OVL}	Feedback Overvoltage Lockout	Measured at $V_{FB1,2}$	●	0.84	0.86	0.88	V
I_{SENSE}	Sense Pin Bias Current	(Each Channel) $V_{SENSE1,2}$ = 3.3V			±1	±2	µA
$I_{TK/SS1,2}$	Soft-Start Charge Current	$V_{TK/SS1,2}$ = 0V		0.9	1.3	1.7	µA
$V_{RUN1,2}$	RUN Pin ON Threshold	V_{RUN1}, V_{RUN2} Rising	●	1.1	1.22	1.35	V
$V_{RUN1,2HYS}$	RUN Pin ON Hysteresis				80		mV
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold (Note 8)	$V_{FB1,2}$ = 0.7V, $V_{SENSE1,2}$ = 3.3V, I_{LIM} = 0V $V_{FB1,2}$ = 0.7V, $V_{SENSE1,2}$ = 3.3V, I_{LIM} = Float $V_{FB1,2}$ = 0.7V, $V_{SENSE1,2}$ = 3.3V, I_{LIM} = $INTV_{CC}$	● ● ●	20 40 60	30 50 75	40 60 90	mV mV mV
TG R_{UP}	TG Driver Pull-Up On-Resistance	TG High			2.6		Ω
TG R_{DOWN}	TG Driver Pulldown On-Resistance	TG Low			1.5		Ω
BG R_{UP}	BG Driver Pull-Up On-Resistance	BG High			2.4		Ω
BG R_{DOWN}	BG Driver Pulldown On-Resistance	BG Low			1.1		Ω
 TG1,2 t_r TG1,2 t_f	TG Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 25 25		 ns ns
 BG1,2 t_r BG1,2 t_f	BG Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 25 25		 ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			30		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			30		ns
$t_{ON(MIN)}$	Minimum On-Time	(Note 7)			90		ns
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	7V < V_{IN} < 24V		4.8	5	5.2	V
V_{LDO} INT	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA			0.5	2	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive	●	4.5	4.7		V
V_{LDO} EXT	$EXTV_{CC}$ Voltage Drop	I_{CC} = 20mA, V_{EXTVCC} = 5V			50	100	mV
V_{LDOHYS}	$EXTV_{CC}$ Hysteresis				200		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 15V, $V_{RUN1,2}$ = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	V_{FREQ} = 1.2V		450	500	550	kHz
f_{LOW}	Lowest Frequency	V_{FREQ} = 0V		210	250	290	kHz
f_{HIGH}	Highest Frequency	V_{FREQ} ≥ 2.4V		700	780	860	kHz
$R_{MODE/PLLIN}$	MODE/PLLIN Input Resistance				250		kΩ
I_{FREQ}	Phase Detector Output Current Sinking Capability Sourcing Capability	 $f_{MODE} < f_{OSC}$ $f_{MODE} > f_{OSC}$			 –13 13		 µA µA
PGOOD Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±2	µA
V_{PG}	PGOOD Trip Level	V_{FB} with Respect to Set Regulated Voltage V_{FB} Ramping Negative V_{FB} Ramping Positive		 –5 5	 –7.5 7.5	 –10 10	 % %

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3850E/LTC3850E-1 are guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3850I/LTC3850I-1 are guaranteed to meet performance specifications over the –40°C to 85°C operating temperature range.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC3850GN: $T_J = T_A + (P_D \bullet 95°C/W)$

LTC3850UF: $T_J = T_A + (P_D \bullet 37°C/W)$

LTC3850UFD: $T_J = T_A + (P_D \bullet 43°C/W)$

Note 4: The LTC3850 is tested in a feedback loop that servos $V_{ITH1,2}$ to a specified voltage and measures the resultant $V_{FB1,2}$.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

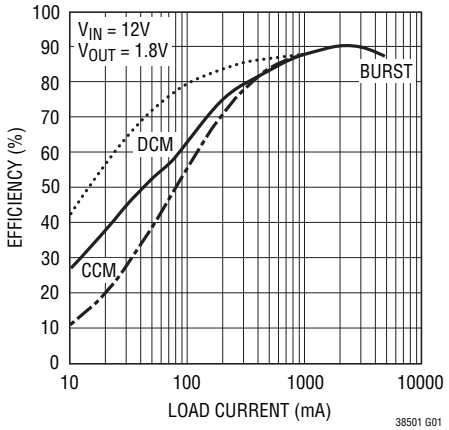
Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current ≥40% of I_{MAX} (see Minimum On-Time Considerations in the Applications Information section).

Note 8: $V_{SENSE(MAX)}$ defaults to 50mV typical for the LTC3850-1.

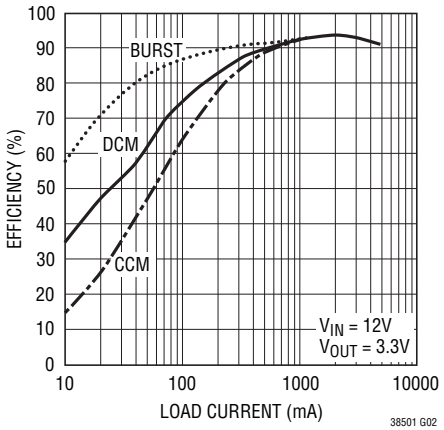
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Output Current and Mode



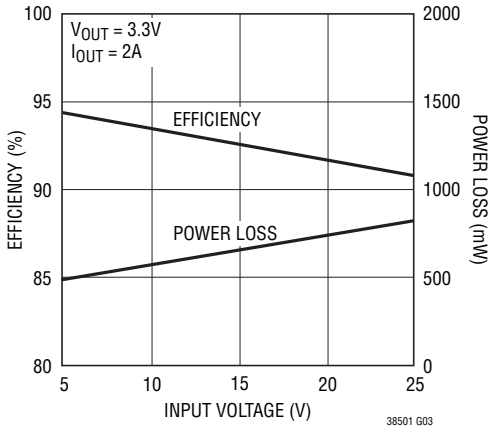
CIRCUIT OF FIGURE 14

Efficiency vs Output Current and Mode



CIRCUIT OF FIGURE 14

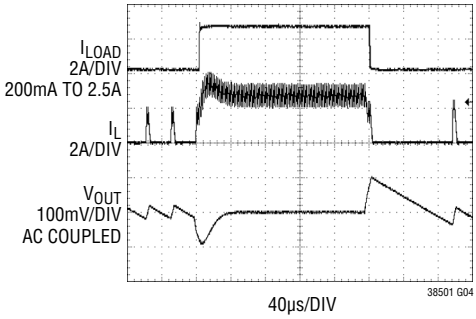
Efficiency and Power Loss vs Input Voltage



CIRCUIT OF FIGURE 14

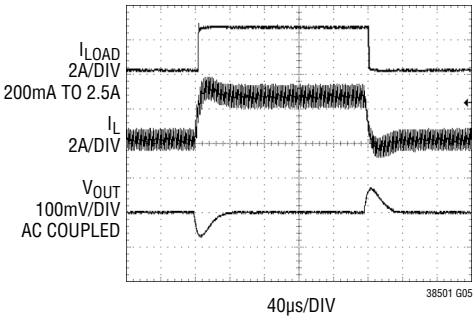
TYPICAL PERFORMANCE CHARACTERISTICS

Load Step (Burst Mode Operation)



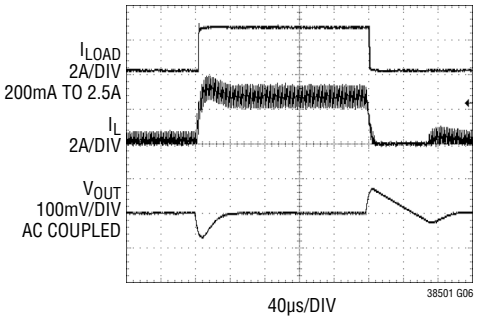
CIRCUIT OF FIGURE 14
V_{IN} = 12V, V_{OUT} = 1.8V

Load Step (Forced Continuous Mode)



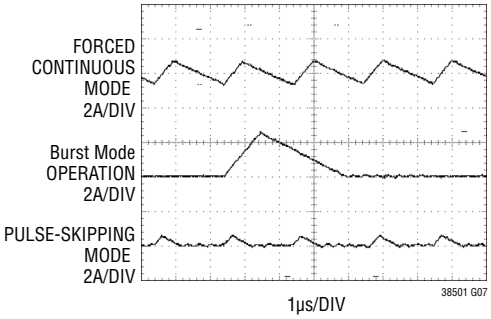
CIRCUIT OF FIGURE 14
V_{IN} = 12V, V_{OUT} = 1.8V

Load Step (Pulse-Skipping Mode)



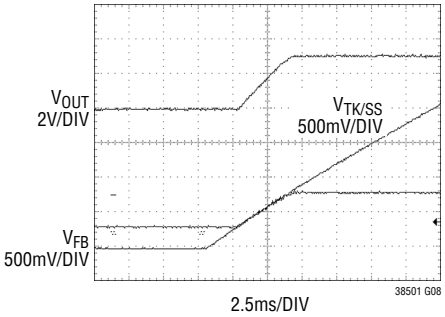
CIRCUIT OF FIGURE 14
V_{IN} = 12V, V_{OUT} = 1.8V

Inductor Current at Light Load

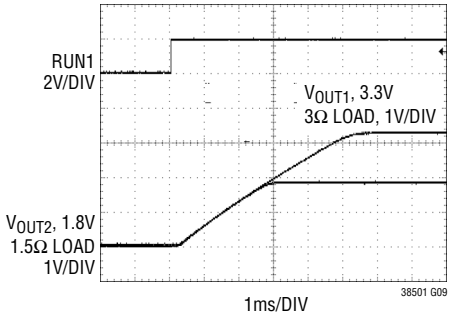


CIRCUIT OF FIGURE 14
V_{IN} = 12V, V_{OUT} = 1.8V
I_{LOAD} = 100µA

Prebiased Output at 2V

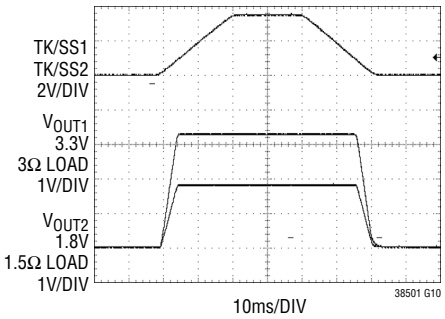


Coincident Tracking

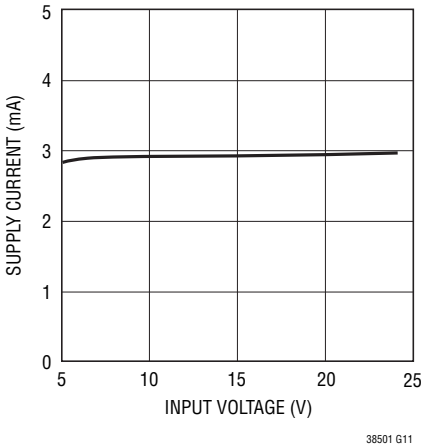


TYPICAL PERFORMANCE CHARACTERISTICS

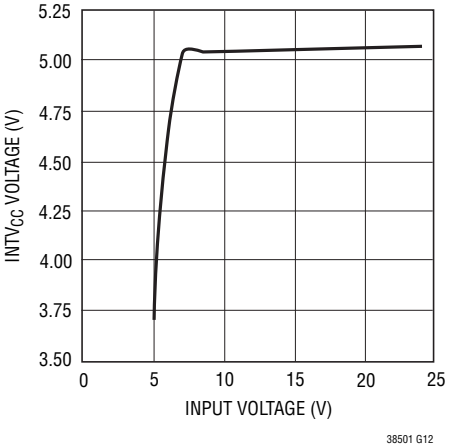
Tracking Up and Down with External Ramp



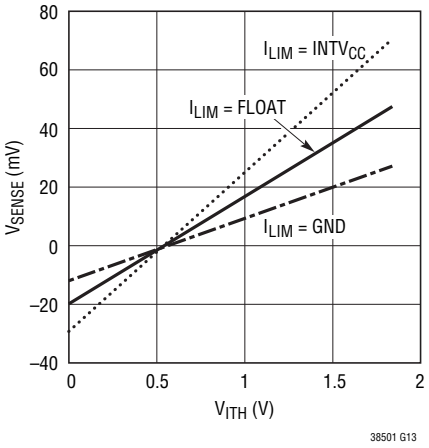
Quiescent Current vs Input Voltage without $EXTV_{CC}$



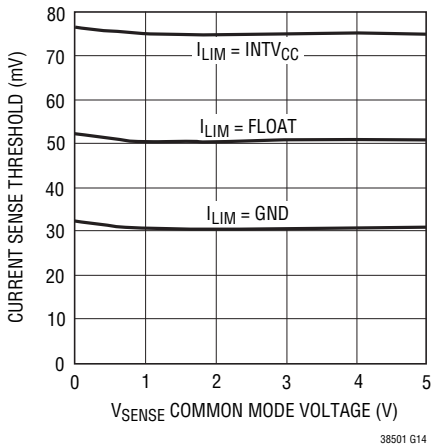
$INTV_{CC}$ Line Regulation



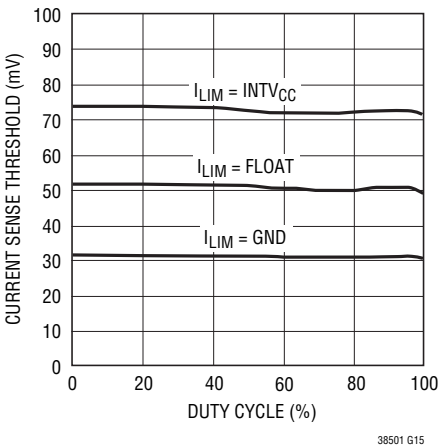
Current Sense Threshold vs I_{TH} Voltage



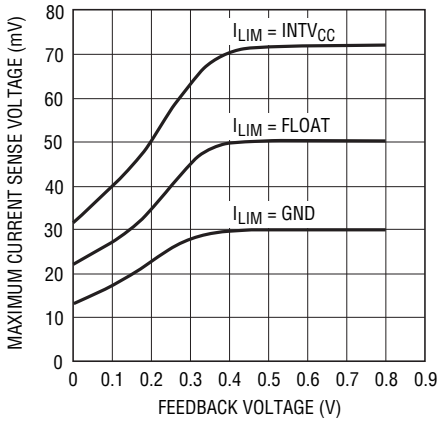
Maximum Current Sense Threshold vs Common Mode Voltage



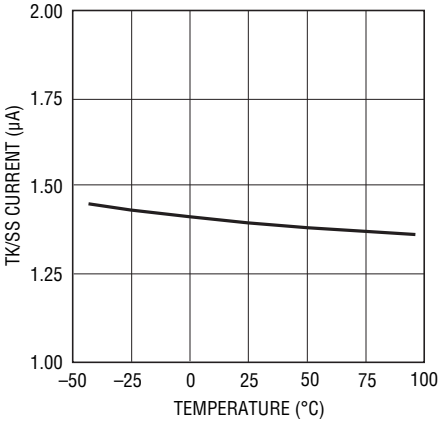
Maximum Current Sense Threshold vs Duty Cycle



Maximum Current Sense Voltage vs Feedback Voltage (Current Foldback)

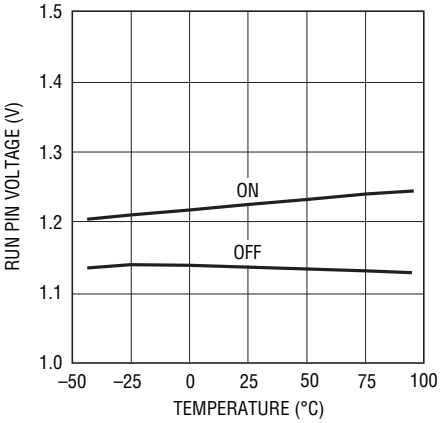


TK/SS Pull-Up Current vs Temperature

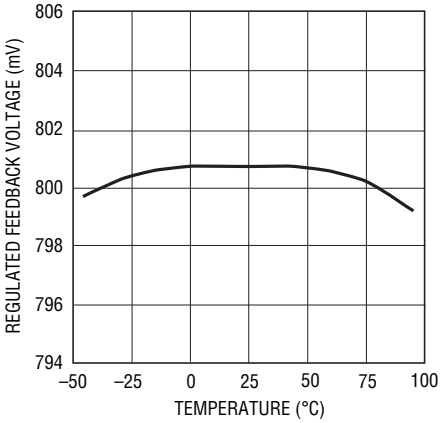


TYPICAL PERFORMANCE CHARACTERISTICS

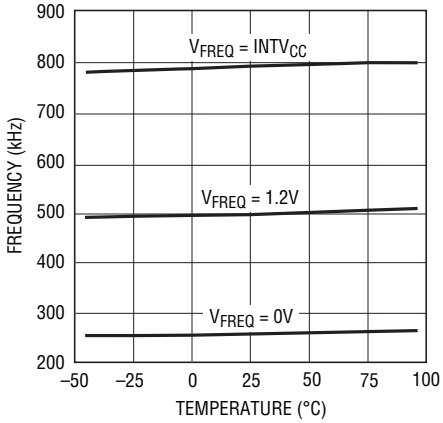
Shutdown (RUN) Threshold vs Temperature



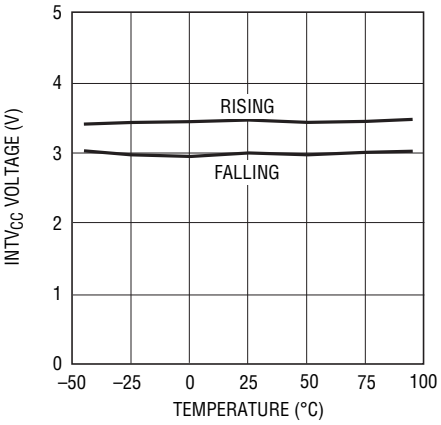
Regulated Feedback Voltage vs Temperature



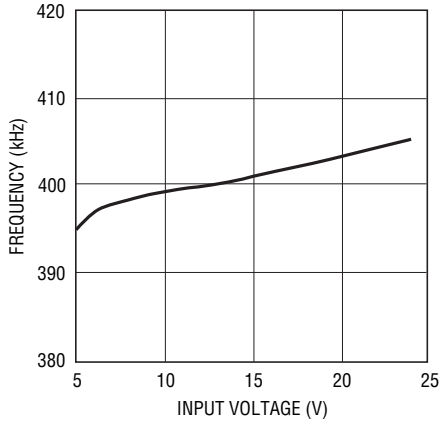
Oscillator Frequency vs Temperature



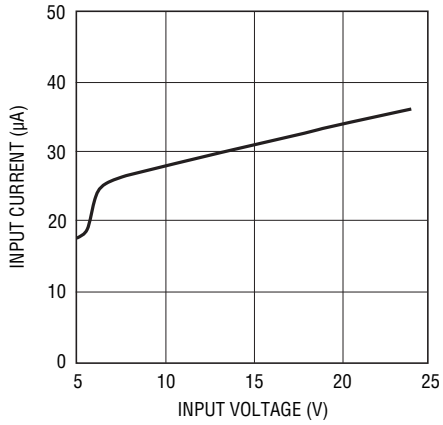
Undervoltage Lockout Threshold ($INTV_{CC}$) vs Temperature



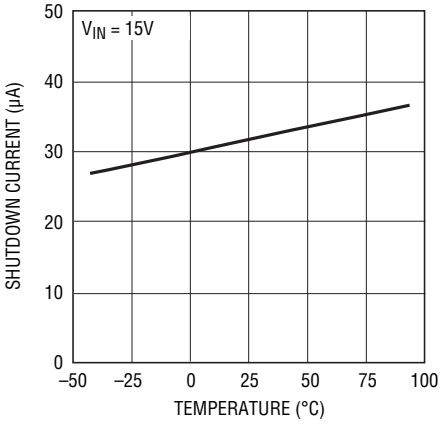
Oscillator Frequency vs Input Voltage



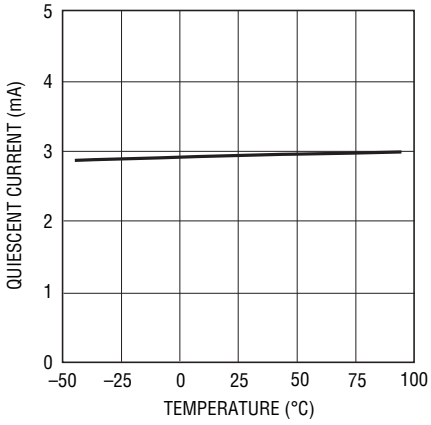
Shutdown Current vs Input Voltage



Shutdown Current vs Temperature



Quiescent Current vs Temperature without $EXTV_{CC}$



PIN FUNCTIONS (GN/UF/UFD)

RUN1, RUN2 (Pins 1, 13/Pins 26, 9/Pins 27, 10): Run Control Inputs. A voltage above 1.2V on either pin turns on the IC. However, forcing either of these pins below 1.2V causes the IC to shut down that particular channel. There are 0.5µA pull-up currents for these pins. Once the RUN pin rises above 1.2V, an additional 4.5µA pull-up current is added to the pin.

SENSE1$^+$, SENSE2$^+$ (Pins 2, 12/Pins 27, 8/Pins 28, 9): Current Sense Comparator Inputs. The (+) inputs to the current comparators are normally connected to DCR sensing networks or current sensing resistors.

SENSE1$^-$, SENSE2$^-$ (Pins 3, 11/Pins 28, 7/Pins 1, 8): Current Sense Comparator Inputs. The (–) inputs to the current comparators are connected to the outputs.

TK/SS1, TK/SS2 (Pins 4, 10/Pins 1, 6/Pins 2, 7): Output Voltage Tracking and Soft-Start Inputs. When one channel is configured to be master of the two channels, a capacitor to ground at this pin sets the ramp rate for the master channel's output voltage. When the channel is configured to be the slave of two channels, the V_{FB} voltage of the master channel is reproduced by a resistor divider and applied to this pin. Internal soft-start currents of 1.3µA charge the soft-start capacitors.

I_{TH1}, I_{TH2} (Pins 5, 9/Pins 2, 5/Pins 3, 6): Current Control Thresholds and Error Amplifier Compensation Points. Each associated channels' current comparator tripping threshold increases with its I_{TH} control voltage.

V_{FB1}, V_{FB2} (Pins 6, 8/Pins 3, 4/Pins 4, 5): Error Amplifier Feedback Inputs. These pins receive the remotely sensed feedback voltages for each channel from external resistive dividers across the outputs.

SGND (Pin 7/Pin 29/Pin 29): Signal Ground. All small-signal components and compensation components should connect to this ground, which in turn connects to PGND at one point. Pin 29 is the Exposed Pad, only available on the UF package.

$EXTV_{CC}$ (Pin 14, LTC3850-1 Only/Pin 11/Pin 12): External Power Input to an Internal Switch Connected to $INTV_{CC}$. This switch closes and supplies the IC power, bypassing the internal low dropout regulator, whenever $EXTV_{CC}$ is higher than 4.7V. Do not exceed 6V on this pin and ensure $V_{IN} > V_{EXTVCC}$ at all times. On the GN package, $EXTV_{CC}$ is the optional bonding in place of I_{LIM} for LTC3850-1. In the LTC3850-1, I_{LIM} will default to 50mV.

I_{LIM} (Pin 14, LTC3850 Only/Pin 10/Pin 11): Current Comparator Sense Voltage Range Inputs. Tying this pin to SGND, FLOAT or $INTV_{CC}$ sets the maximum current sense threshold to three different levels for each comparator.

PGOOD (Pin 15/Pin 12/Pin 13): Power Good Indicator Output. Open-drain logic out that is pulled to ground when either channel output exceeds the ±7.5% regulation window, after the internal 17µs power bad mask timer expires.

PGND (Pin 19/Pin 16/Pin 17): Power Ground Pin. Connect this pin closely to the sources of the bottom N-channel MOSFETs, the (–) terminal of CV_{CC} and the (–) terminal of C_{IN}.

$INTV_{CC}$ (Pin 21/Pin 18/Pin 19): Internal 5V Regulator Output. The control circuits are powered from this voltage. Decouple this pin to PGND with a 4.7µF low ESR tantalum or ceramic capacitor.

V_{IN} (Pin 22/Pin 19/Pin 20): Main Input Supply. Decouple this pin to PGND with a capacitor (0.1µF to 1µF). For applications where the main input power is 5V, tie the V_{IN} and $INTV_{CC}$ pins together.

BG1, BG2 (Pins 23, 20/Pins 20, 17/Pins 21, 18): Bottom Gate Driver Outputs. These pins drive the gates of the bottom N-Channel MOSFETs and swings between PGND and $INTV_{CC}$.

BOOST1, BOOST2 (Pins 24, 18/Pins 21, 15/Pins 22, 16): Boosted Floating Driver Supplies. The (+) terminal of the boost-strap capacitors connect to these pins. These pins swing from a diode voltage drop below $INTV_{CC}$ up to V_{IN} + $INTV_{CC}$.

TG1, TG2 (Pins 25, 17/Pins 22, 14/Pins 23, 15): Top Gate Driver Outputs. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ superimposed on the switch nodes voltages.

SW1, SW2 (Pins 26, 16/Pins 23, 13/Pins 24, 14): Switch Node Connections to Inductors. Voltage swing at these pins are from a body diode voltage drop below ground to V_{IN}.

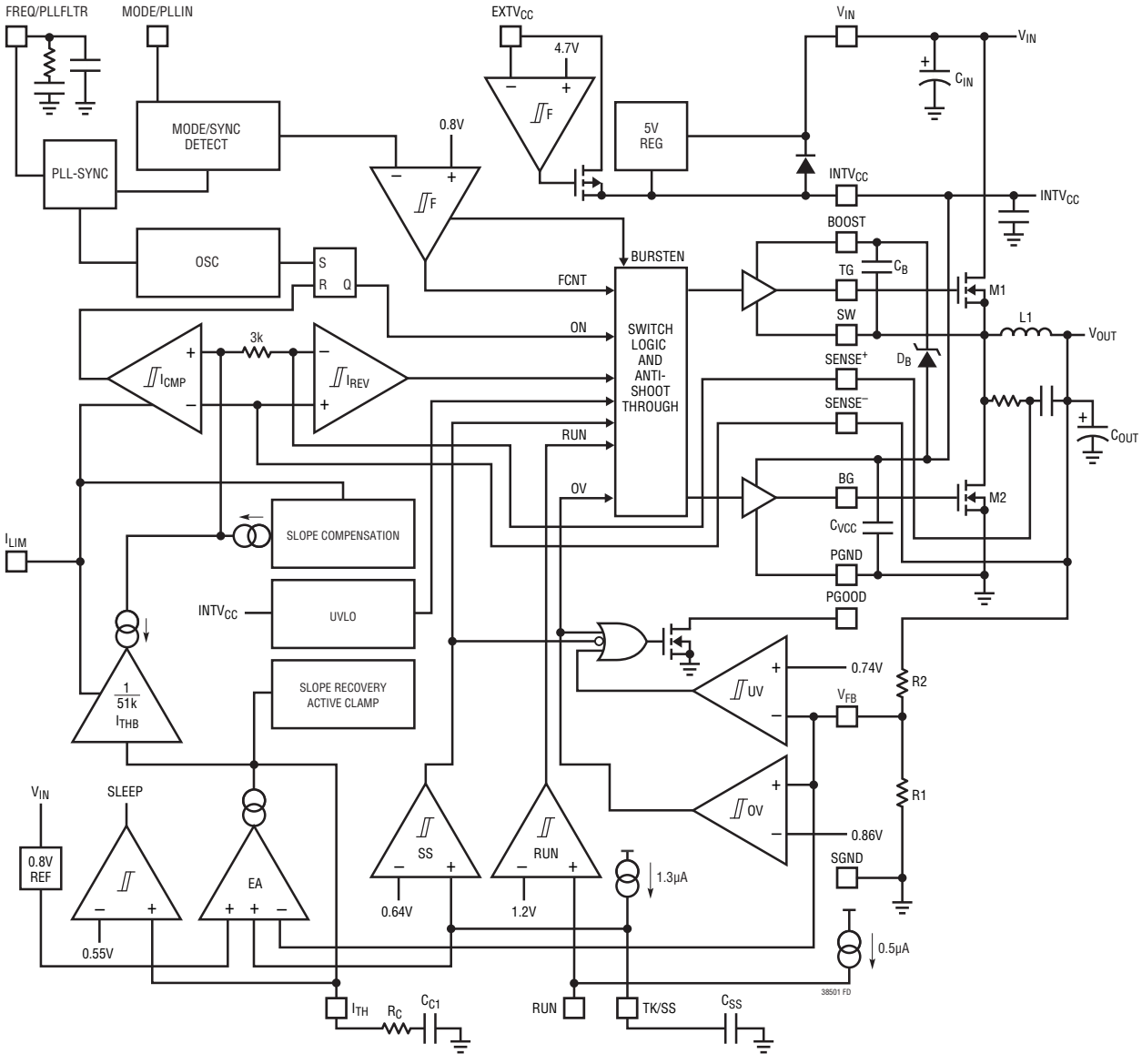
PIN FUNCTIONS

MODE/PLLIN (Pin 27/Pin 24/Pin 25): Force Continuous Mode, Burst Mode, or Pulse-Skipping Mode Selection Pin and External Synchronization Input to Phase Detector Pin. Connect this pin to SGND to force both channels into the continuous mode of operation. Connect to $INTV_{CC}$ to enable pulse-skipping mode of operation. Leaving the pin floating will enable Burst Mode operation. A clock on the pin will force the controller into continuous mode of operation and synchronize the internal oscillator.

FREQ/PLLFLTR (Pin 28/Pin 25/Pin 26): The Phase-Locked Loop's Low-Pass Filter is Tied to This Pin. Alternatively, this pin can be driven with a DC voltage to vary the frequency of the internal oscillator.

Exposed Pad (Pin 29, UF/UFD Packages Only): Signal Ground. Must be soldered to PCB, providing a local ground for the control components of the IC, and be tied to the PGND pin under the IC.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC3850 is a constant-frequency, current mode step-down controller with two channels operating 180 degrees out-of-phase. During normal operation, each top MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the main current comparator, I_{CMP}, resets the RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of each error amplifier EA. The V_{FB} pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EA. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.8V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the reverse current comparator I_{REV}, or the beginning of the next cycle.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is left open or tied to a voltage less than 4.7V, an internal 5V linear regulator supplies $INTV_{CC}$ power from V_{IN}. If $EXTV_{CC}$ is taken above 4.7V, the 5V regulator is turned off and an internal switch is turned on connecting $EXTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as one of the LTC3850 switching regulator outputs.

Each top MOSFET driver is biased from the floating bootstrap capacitor C_B, which normally recharges during each off cycle through an external diode when the top MOSFET turns off. If the input voltage V_{IN} decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one-twelfth of the clock period every third cycle to allow C_B to recharge. However, it is recommended that a load be present during the drop-out transition to ensure C_B is recharged.

Shutdown and Start-Up (RUN1, RUN2 and TK/SS1, TK/SS2 Pins)

The two channels of the LTC3850 can be independently shut down using the RUN1 and RUN2 pins. Pulling either of these pins below 1.2V shuts down the main control loop for that controller. Pulling both pins low disables both controllers and most internal circuits, including the $INTV_{CC}$ regulator. Releasing either RUN pin allows an internal 0.5µA current to pull up the pin and enable that controller. Alternatively, the RUN pin may be externally pulled up or driven directly by logic. Be careful not to exceed the Absolute Maximum Rating of 6V on this pin.

The start-up of each controller's output voltage V_{OUT} is controlled by the voltage on the TK/SS1 and TK/SS2 pins. When the voltage on the TK/SS pin is less than the 0.8V internal reference, the LTC3850 regulates the V_{FB} voltage to the TK/SS pin voltage instead of the 0.8V reference. This allows the TK/SS pin to be used to program a soft-start by connecting an external capacitor from the TK/SS pin to SGND. An internal 1.3µA pull-up current charges this capacitor, creating a voltage ramp on the TK/SS pin. As the TK/SS voltage rises linearly from 0V to 0.8V (and beyond), the output voltage V_{OUT} rises smoothly from zero to its final value. Alternatively the TK/SS pin can be used to cause the start-up of V_{OUT} to "track" that of another supply. Typically, this requires connecting to the TK/SS pin an external resistor divider from the other supply to ground (see the Applications Information section). When the corresponding RUN pin is pulled low to disable a controller, or when $INTV_{CC}$ drops below its undervoltage lockout threshold of 3V, the TK/SS pin is pulled low by an internal MOSFET. When in undervoltage lockout, both controllers are disabled and the external MOSFETs are held off.

Light Load Current Operation (Burst Mode Operation, Pulse-Skipping, or Continuous Conduction)

The LTC3850 can be enabled to enter high efficiency Burst Mode operation, constant-frequency pulse-skipping mode, or forced continuous conduction mode. To select forced continuous operation, tie the MODE/PLLIN pin to a DC voltage below 0.8V (e.g., SGND). To select pulse-skipping mode of operation, tie the MODE/PLLIN pin to $INTV_{CC}$. To select Burst Mode operation, float the MODE/PLLIN pin.

OPERATION

When a controller is enabled for Burst Mode operation, the peak current in the inductor is set to approximately one-third of the maximum sense voltage even though the voltage on the I_{TH} pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier EA will decrease the voltage on the I_{TH} pin. When the I_{TH} voltage drops below 0.5V, the internal sleep signal goes high (enabling "sleep" mode) and both external MOSFETs are turned off.

In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator. When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (I_{REV}) turns off the bottom external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation. In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous mode has the advantages of lower output ripple and less interference with audio circuitry.

When the MODE/PLLIN pin is connected to $INTV_{CC}$, the LTC3850 operates in PWM pulse-skipping mode at light loads. At very light loads, the current comparator I_{CMP} may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Frequency Selection and Phase-Locked Loop (FREQ/PLLFLTR and MODE/PLLIN Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. The switching frequency of the LTC3850's controllers can be selected using the FREQ/PLLFLTR pin. If the MODE/PLLIN pin is not being driven by an external clock source, the FREQ/PLLFLTR pin can be used to program the controller's operating frequency from 250kHz to 780kHz.

A phase-locked loop (PLL) is available on the LTC3850 to synchronize the internal oscillator to an external clock source that is connected to the MODE/PLLIN pin. The controller is operating in forced continuous mode when it is synchronized. A series R-C should be connected between the FREQ/PLLFLTR pin and SGND to serve as the PLL's loop filter.

Power Good (PGOOD Pin)

The PGOOD pin is connected to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when either V_{FB} pin voltage is not within ±7.5% of the 0.8V reference voltage. The PGOOD pin is also pulled low when either RUN pin is below 1.2V or when the LTC3850 is in the soft-start or tracking phase. When the V_{FB} pin voltage is within the ±7.5% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source of up to 6V. The PGOOD pin will flag power good immediately when both V_{FB} pins are within the ±7.5% window. However, there is an internal 17µs power bad mask when either V_{FB} goes out of the ±7.5% window.

Output Overvoltage Protection

An overvoltage comparator, OV, guards against transient overshoots (> 7.5%) as well as other more serious conditions that may overvoltage the output. In such cases, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC3850 application circuit. LTC3850 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption, and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs are selected. Finally, input and output capacitors are selected.

Current Limit Programming

The I_{LIM} pin is a tri-level logic input which sets the maximum current limit of the controller. When I_{LIM} is either grounded, floated or tied to $INTV_{CC}$, the typical value for the maximum current sense threshold will be 30mV, 50mV or 75mV, respectively.

Which setting should be used? For the best current limit accuracy, use the 75mV setting. The 30mV setting will allow for the use of very low DCR inductors or sense resistors, but at the expense of current limit accuracy. The 50mV setting is a good balance between the two. For single output dual phase applications (see Figure 21), use the 50mV or 75mV setting for optimal current sharing.

SENSE+ and SENSE– Pins

The SENSE+ and SENSE– pins are the inputs to the current comparators. The common mode input voltage range of the current comparators is 0V to 5V. Both SENSE pins are high impedance inputs with small base currents of less than 1µA. When the SENSE pins ramp up from 0V to 1.4V, the small base currents flow out of the SENSE pins. When the SENSE pins ramp down from 5V to 1.1V, the small base currents flow into the SENSE pins. The high impedance inputs to the current comparators allow accurate DCR sensing. However, care must be taken not to float these pins during normal operation.

Filter components mutual to the sense lines should be placed close to the LTC3850, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 1). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 2b), sense resistor R1 should be placed

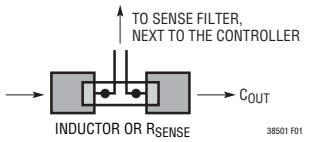
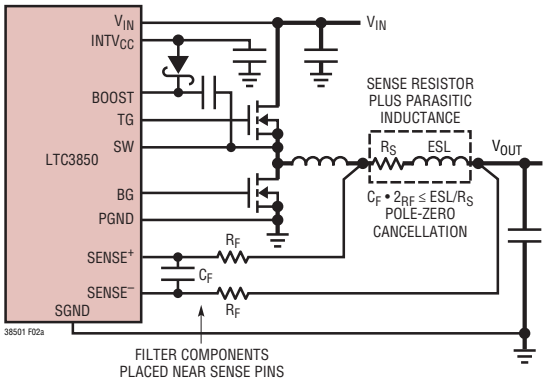
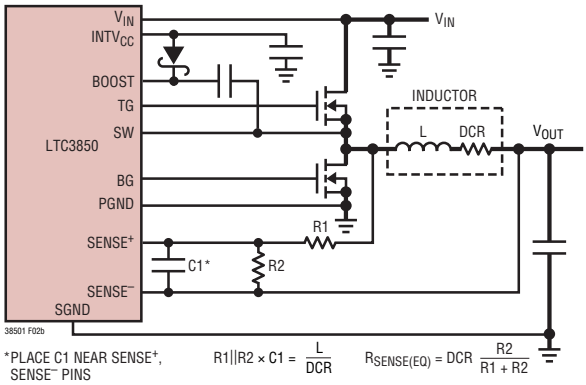


Figure 1. Sense Lines Placement with Inductor or Sense Resistor



(2a) Using a Resistor to Sense Current



(2b) Using the Inductor DCR to Sense Current

Figure 2. Two Different Methods of Sensing Current

APPLICATIONS INFORMATION

close to the switching node, to prevent noise from coupling into sensitive small-signal nodes. The capacitor C1 should be placed close to the IC pins.

Low Value Resistors Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 2a. R_{SENSE} is chosen based on the required output current.

The current comparator has a maximum threshold $V_{SENSE(MAX)}$ determined by the I_{LIM} setting. The input common mode range of the current comparator is 0V to 5V. The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{(MAX)} + \frac{\Delta I_L}{2}}$$

Because of possible PCB noise in the current sensing loop, the AC current sensing ripple of $\Delta V_{SENSE} = \Delta I_L \bullet R_{SENSE}$ also needs to be checked in the design to get a good signal-to-noise ratio. In general, for a reasonably good PCB layout, a 15mV ΔV_{SENSE} voltage is recommended as a conservative number to start with, either for R_{SENSE} or DCR sensing applications.

For previous generation current mode controllers, the maximum sense voltage was high enough (e.g., 75mV for the LTC1628/LTC3728 family) that the voltage drop across the parasitic inductance of the sense resistor represented a relatively small error. For today's highest current density solutions, however, the value of the sense resistor can be less than 1mΩ and the peak sense voltage can be as low as 20mV. In addition, inductor ripple currents greater than 50% with operation up to 1MHz are becoming more common. Under these conditions the voltage drop across the sense resistor's parasitic inductance is no longer negligible. A typical sensing circuit using a discrete resistor is shown in Figure 2a. In previous generations of controllers, a small RC filter placed near the IC was commonly used to reduce the effects of capacitive and inductive noise coupled inthe sense traces on the PCB. A typical filter consists of two series 10Ω resistors connected to a parallel 1000pF capacitor, resulting in a time constant of 20ns.

This same RC filter, with minor modifications, can be used to extract the resistive component of the current sense signal in the presence of parasitic inductance. For example, Figure 3 illustrates the voltage waveform across a 2mΩ sense resistor with a 2010 footprint for the 1.2V/15A converter shown in Figure 18 operating at 100% load. The waveform is the superposition of a purely resistive component and a purely inductive component. It was measured using two scope probes and waveform math to obtain a differential measurement. Based on additional measurements of the inductor ripple current and the on-time and off-time of the top switch, the value of the parasitic inductance was determined to be 0.5nH using the equation:

$$ESL = \frac{V_{ESL(STEP)}}{\Delta I_L} \frac{t_{ON} \bullet t_{OFF}}{t_{ON} + t_{OFF}}$$

If the RC time constant is chosen to be close to the parasitic inductance divided by the sense resistor (L/R), the resulting waveform looks resistive again, as shown in Figure 4. For applications using low maximum sense voltages, check the sense resistor manufacturer's data sheet for information about parasitic inductance. In the absence of data, measure the voltage drop directly across the sense resistor to extract the magnitude of the ESL step and use the equation above to determine the ESL. However, do not over-filter. Keep the RC time constant less than or equal to the inductor time constant to maintain a high enough ripple voltage on V_{RSENSE}.

The above generally applies to high density / high current applications where $I_{(MAX)}$ > 10A and low values of inductors are used. For applications where $I_{(MAX)}$ < 10A, set R_F to 10 Ohms and C_F to 1000pF. This will provide a good starting point.

The filter components need to be placed close to the IC. The positive and negative sense traces need to be routed as a differential pair and Kelvin connected to the sense resistor.

APPLICATIONS INFORMATION

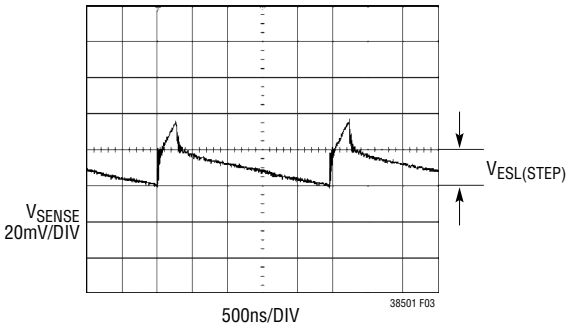


Figure 3. Voltage Waveform Measured Directly Across the Sense Resistor.

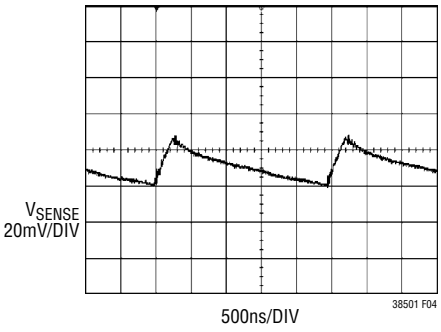


Figure 4. Voltage Waveform Measured After the Sense Resistor Filter. C_F = 1000pF, R_F = 100Ω.

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC3850 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 2b. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, conduction loss through a sense resistor would cost several points of efficiency compared to DCR sensing.

If the external R1 || R2 • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' datasheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{(MAX)} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for the Maximum Current Sense Threshold ($V_{SENSE(MAX)}$) in the Electrical Characteristics table (20mV, 40mV, or 60mV, depending on the state of the I_{LIM} pin).

Next, determine the DCR of the inductor. Where provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C.

To scale the maximum inductor DCR to the desired sense resistor value, use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{(MAX)} \text{ at } T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.047µF to 0.47µF. This forces R1 || R2 to around 2kΩ, reducing error that might have been caused by the SENSE pins' ±1µA current.

The equivalent resistance R1 || R2 is scaled to the room temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR \text{ at } 20°C) \bullet C1}$$

The sense resistor values are:

$$R1 = \frac{R1||R2}{R_D}; \quad R2 = \frac{R1 \bullet R_D}{1 - R_D}$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}\ R1 = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \bullet V_{OUT}}{R1}$$

APPLICATIONS INFORMATION

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

To maintain a good signal to noise ratio for the current sense signal, use a minimum ΔV_{SENSE} of 10mV to 15mV. For a DCR sensing application, the actual ripple voltage will be determined by the equation:

$$\Delta V_{SENSE} = \frac{V_{IN} - V_{OUT}}{R1 \bullet C1} \frac{V_{OUT}}{V_{IN} \bullet f_{OSC}}$$

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant-frequency architectures by preventing subharmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, this results in a reduction of maximum inductor peak current for duty cycles >40%. However, the LTC3850 uses a patented scheme that counteracts this compensating ramp, which allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

Inductor Value Calculation

Given the desired input and output voltages, the inductor value and operating frequency f_{OSC} directly determine the inductor's peak-to-peak ripple current:

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN}} \left(\frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet L} \right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet I_{RIPPLE}} \bullet \frac{V_{OUT}}{V_{IN}}$$

Inductor Core Selection

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET and Schottky Diode (Optional) Selection

Two external power MOSFETs must be selected for each controller in the LTC3850: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5V during start-up (see $EXTV_{CC}$ Pin Connection). Consequently, logic-level threshold MOSFETs must be used in most applications. The only exception is if low input voltage is expected (V_{IN} < 5V); then, sub-logic level threshold MOSFETs ($V_{GS(TH)}$ < 3V) should be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; most of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, Miller capacitance C_{MILLER}, input

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voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet \left[\frac{1}{V_{INTVCC} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right]\bullet f_{OSC}$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. $V_{TH(MIN)}$ is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

The optional Schottky diodes conduct during the dead time between the conduction of the two power MOSFETs. These prevent the body diodes of the bottom MOSFETs from turning on, storing charge during the dead time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high V_{IN}. A 1A to 3A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

Soft-Start and Tracking

The LTC3850 has the ability to either soft-start by itself with a capacitor or track the output of another channel or external supply. When one particular channel is configured to soft-start by itself, a capacitor should be connected to its TK/SS pin. This channel is in the shutdown state if its RUN pin voltage is below 1.2V. Its TK/SS pin is actively pulled to ground in this shutdown state.

Once the RUN pin voltage is above 1.2V, the channel powers up. A soft-start current of 1.3µA then starts to charge its soft-start capacitor. Note that soft-start or tracking is achieved not by limiting the maximum output current of the controller but by controlling the output ramp voltage according to the ramp rate on the TK/SS pin. Current foldback is disabled during this phase to ensure smooth soft-start or tracking. The soft-start or tracking range is defined to be the voltage range from 0V to 0.8V on the TK/SS pin. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = 0.8 \bullet \frac{C_{SS}}{1.3\mu A}$$

Regardless of the mode selected by the MODE/PLLIN pin, the regulator will always start in pulse-skipping mode up to TK/SS = 0.64V. Between TK/SS = 0.64V and 0.74V, it will operate in forced continuous mode and revert to the

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selected mode once TK/SS > 0.74V. The output ripple is minimized during the 100mV forced continuous mode window ensuring a clean PGOOD signal.

When the channel is configured to track another supply, the feedback voltage of the other supply is duplicated by a resistor divider and applied to the TK/SS pin. Therefore, the voltage ramp rate on this pin is determined by the ramp rate of the other supply's voltage. Note that the small soft-start capacitor charging current is always flowing, producing a small offset error. To minimize this error, select the tracking resistive divider value to be small enough to make this error negligible.

In order to track down another channel or supply after the soft-start phase expires, the LTC3850 is forced into continuous mode of operation as soon as V_{FB} is below the undervoltage threshold of 0.74V regardless of the setting on the MODE/PLLIN pin. However, the LTC3850 should always be set in force continuous mode tracking down when there is no load. After TK/SS drops below 0.1V, its channel will operate in discontinuous mode.

Output Voltage Tracking

The LTC3850 allows the user to program how its output ramps up and down by means of the TK/SS pins. Through these pins, the output can be set up to either coincidentally or ratiometrically track another supply's output, as shown in Figure 5. In the following discussions, V_{OUT1} refers to the LTC3850's output 1 as a master channel and V_{OUT2} refers to the LTC3850's output 2 as a slave channel. In practice, though, either phase can be used as the master. To implement the coincident tracking in Figure 5a, connect an additional resistive divider to V_{OUT1} and connect its midpoint to the TK/SS pin of the slave channel. The ratio of this divider should be the same as that of the slave channel's feedback divider shown in Figure 6a. In this tracking mode, V_{OUT1} must be set higher than V_{OUT2}. To implement the ratiometric tracking, the ratio of the V_{OUT2} divider should be exactly the same as the master channel's feedback divider. By selecting different resistors, the LTC3850 can achieve different modes of tracking including the two in Figure 5.

So which mode should be programmed? While either mode in Figure 5 satisfies most practical applications, some tradeoffs exist. The ratiometric mode saves a pair of resistors, but the coincident mode offers better output regulation. This can be better understood with the help of Figure 7. At the input stage of the slave channel's error amplifier, two common anode diodes are used to clamp the equivalent reference voltage and an additional diode is used to match the shifted common mode voltage. The top two current sources are of the same amplitude. In the coincident mode, the TK/SS voltage is substantially higher than 0.8V at steady state and effectively turns off D1. D2 and D3 will therefore conduct the same current and offer tight matching between V_{FB2} and the internal precision 0.8V reference. In the ratiometric mode, however, TK/SS equals 0.8V at steady state. D1 will divert part of the bias current to make V_{FB2} slightly lower than 0.8V.

Although this error is minimized by the exponential I-V characteristic of the diode, it does impose a finite amount of output voltage deviation. Furthermore, when the master channel's output experiences dynamic excursion (under load transient, for example), the slave channel output will be affected as well. For better output regulation, use the coincident tracking mode instead of ratiometric.

$INTV_{CC}$ Regulators and $EXTV_{CC}$

The LTC3850 features an NPN linear regulator that supplies power to $INTV_{CC}$ from the V_{IN} supply. $INTV_{CC}$ powers the gate drivers and much of the LTC3850's internal circuitry. The linear regulator regulates the voltage at the $INTV_{CC}$ pin to 5V when V_{IN} is greater than 6.5V. $EXTV_{CC}$ connects to $INTV_{CC}$ through a P-channel MOSFET and can supply the needed power when its voltage is higher than 4.7V. Each of these can supply a peak current of 100mA and must be bypassed to ground with a minimum of 1µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and PGND pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3850 to be

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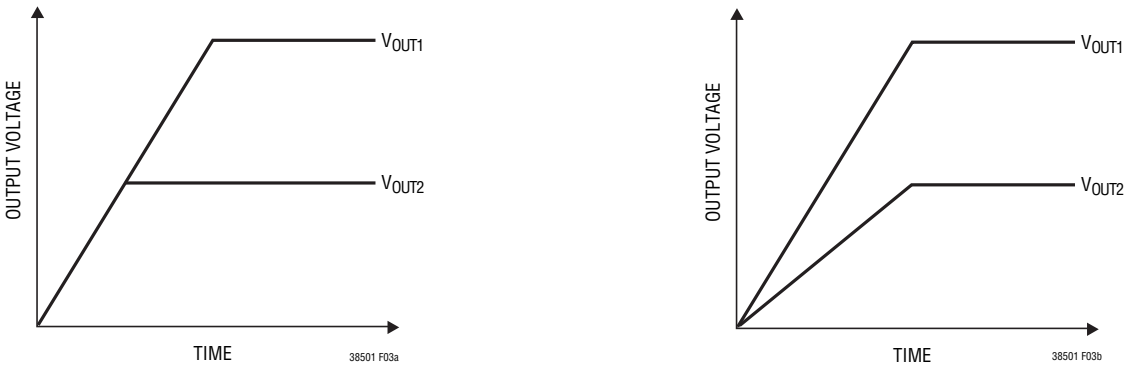
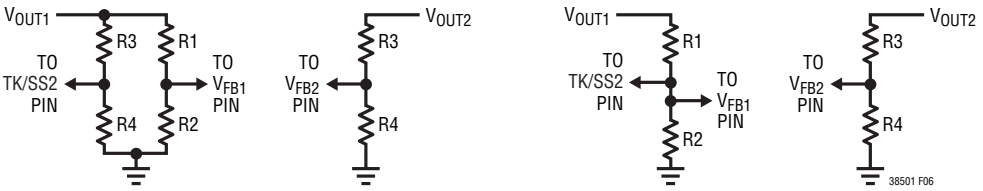


(5a) Coincident Tracking

(5b) Ratiometric Tracking

Figure 5. Two Different Modes of Output Voltage Tracking



(6a) Coincident Tracking Setup

(6b) Ratiometric Tracking Setup

Figure 6. Setup for Coincident and Ratiometric Tracking

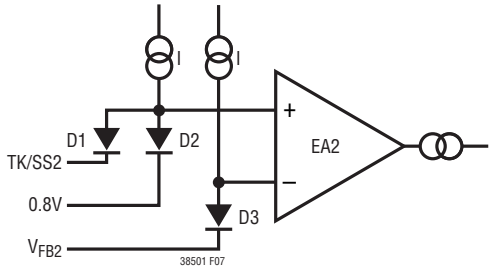


Figure 7. Equivalent Input Circuit of Error Amplifier

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exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, may be supplied by either the 5V linear regulator or $EXTV_{CC}$. When the voltage on the $EXTV_{CC}$ pin is less than 4.7V, the linear regulator is enabled. Power dissipation for the IC in this case is highest and is equal to $V_{IN} \bullet I_{INTVCC}$. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 3 of the Electrical Characteristics. For example, the LTC3850 $INTV_{CC}$ current is limited to less than 24mA from a 24V supply in the GN package and not using the $EXTV_{CC}$ supply:

$T_J = 70°C + (24mA)(24V)(95°C/W) = 125°C$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode (MODE/PLLIN = SGND) at maximum V_{IN}. When the voltage applied to $EXTV_{CC}$ rises above 4.7V, the $INTV_{CC}$ linear regulator is turned off and the $EXTV_{CC}$ is connected to the $INTV_{CC}$. The $EXTV_{CC}$ remains on as long as the voltage applied to $EXTV_{CC}$ remains above 4.5V. Using the $EXTV_{CC}$ allows the MOSFET driver and control power to be derived from one of the LTC3850's switching regulator outputs during normal operation and from the $INTV_{CC}$ when the output is out of regulation (e.g., start-up, short-circuit). If more current is required through the $EXTV_{CC}$ than is specified, an external Schottky diode can be added between the $EXTV_{CC}$ and $INTV_{CC}$ pins. Do not apply more than 6V to the $EXTV_{CC}$ pin and make sure that $EXTV_{CC} < V_{IN}$.

Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Switcher Efficiency).

Tying the $EXTV_{CC}$ pin to a 5V supply reduces the junction temperature in the previous example from 125°C to:

$T_J = 70°C + (24mA)(5V)(95°C/W) = 81°C$

However, for 3.3V and other low voltage outputs, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from the internal 5V regulator resulting in an efficiency penalty of up to 10% at high input voltages.
2. $EXTV_{CC}$ connected directly to V_{OUT}. This is the normal connection for a 5V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If a 5V external supply is available, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements.
4. $EXTV_{CC}$ connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 4.7V.

For applications where the main input power is 5V, tie the V_{IN} and $INTV_{CC}$ pins together and tie the combined pins to the 5V input with a 1Ω or 2.2Ω resistor as shown in Figure 8 to minimize the voltage drop caused by the gate charge current. This will override the $INTV_{CC}$ linear regulator and will prevent $INTV_{CC}$ from dropping too low due to the dropout voltage. Make sure the $INTV_{CC}$ voltage is at or exceeds the $R_{DS(ON)}$ test voltage for the MOSFET which is typically 4.5V for logic level devices.

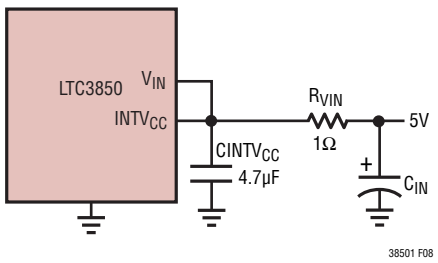

Figure 8. Setup for a 5V Input

Topside MOSFET Driver Supply (C_B, DB)

External bootstrap capacitors C_B connected to the BOOST pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged though external diode DB from $INTV_{CC}$ when the SW pin is low. When one of the topside MOSFETs is to be turned on, the driver places the C_B voltage across the gate source of the desired MOSFET. This enhances the MOSFET and

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turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Undervoltage Lockout

The LTC3850 has two functions that help protect the controller in case of undervoltage conditions. A precision UVLO comparator constantly monitors the $INTV_{CC}$ voltage to ensure that an adequate gate-drive voltage is present. It locks out the switching action when $INTV_{CC}$ is below 3V. To prevent oscillation when there is a disturbance on the $INTV_{CC}$, the UVLO comparator has 500mV of precision hysteresis.

Another way to detect an undervoltage condition is to monitor the V_{IN} supply. Because the RUN pins have a precision turn-on reference of 1.2V, one can use a resistor divider to V_{IN} to turn on the IC when V_{IN} is high enough. An extra 4.5µA of current flows out of the RUN pin once the RUN pin voltage passes 1.2V. One can program the hysteresis of the run comparator by adjusting the values of the resistive divider. For accurate V_{IN} undervoltage detection, V_{IN} needs to be higher than 4V.

C_{IN} and C_{OUT} Selection

The selection of C_{IN} is simplified by the 2-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case capacitor RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula below to determine the maximum RMS capacitor current requirement. Increasing the output current drawn from the other controller will actually decrease the input RMS ripple current from its maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[\left(V_{OUT}\right)\left(V_{IN} - V_{OUT}\right)\right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3850, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The benefit of the LTC3850 2-phase operation can be calculated by using the equation above for the higher power controller and then calculating the loss that would have resulted if both controller channels switched on at the same time. The total RMS power lost is lower when both controllers are operating due to the reduced overlap of current pulses required through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Also, the input protection fuse resistance, battery resistance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a 2-phase system. The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing. The sources of the top MOSFETs should be placed within 1cm of each other and share a common C_{IN}(s). Separating the sources and C_{IN} may produce undesirable voltage and current resonances at V_{IN}.

A small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC3850, is also

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suggested. A 2.2Ω – 10Ω resistor placed between C_{IN} (C1) and the V_{IN} pin provides further isolation between the two channels.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE}\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since I_{RIPPLE} increases with input voltage.

Setting Output Voltage

The LTC3850 output voltages are each set by an external feedback resistive divider carefully placed across the output, as shown in Figure 9. The regulated output voltage is determined by:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R_B}{R_A}\right)$$

To improve the frequency response, a feed-forward capacitor, C_{FF}, may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

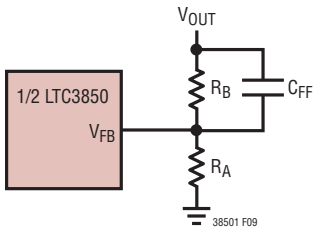

Figure 9. Setting Output Voltage

Fault Conditions: Current Limit and Current Foldback

The LTC3850 includes current foldback to help limit load current when the output is shorted to ground. If the output falls below 50% of its nominal output level, then the maximum sense voltage is progressively lowered from its maximum programmed value to one-third of the maximum value. Foldback current limiting is disabled during the soft-start or tracking up. Under short-circuit conditions with very low duty cycles, the LTC3850 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short-circuit ripple current is determined by the minimum on-time $t_{ON(MIN)}$ of the LTC3850 (≈ 90ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \bullet \frac{V_{IN}}{L}$$

The resulting short-circuit current is:

$$I_{SC} = \frac{1/3\ V_{SENSE(MAX)}}{R_{SENSE}} - \frac{1}{2}\Delta I_{L(SC)}$$

Phase-Locked Loop and Frequency Synchronization

The LTC3850 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (V_{CO}) and a phase detector. This allows the turn-on of the top MOSFET of controller 1 to be locked to the rising edge of an external clock signal applied to the MODE/PLLIN pin. The turn-on of controller 2's top MOSFET is thus 180 degrees out-of-phase with the external clock. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the external filter network connected to the FREQ/PLLFLTR pin. The relationship between the voltage on the FREQ/PLLFLTR pin and operating frequency is shown in Figure 10 and specified in the Electrical Characteristics table. Note that the LTC3850 can only be synchronized to an external clock whose frequency is within range of the LTC3850's internal V_{CO}. This is guaranteed to be between 250kHz and 780kHz. A simplified block diagram is shown in Figure 11.

If no clock is applied to MODE/PLLIN pin, the FREQ/PLLFLTR pin will be high impedance.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced con-

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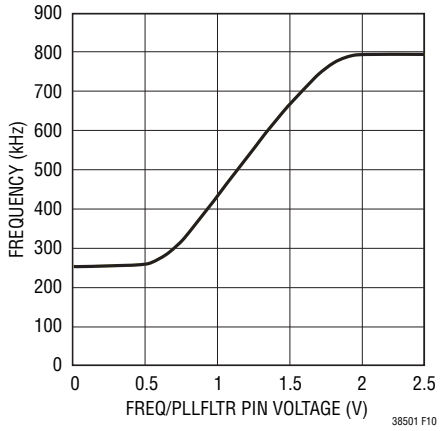

Figure 10. Relationship Between Oscillator Frequency and Voltage at the FREQ/PLLFLTR Pin

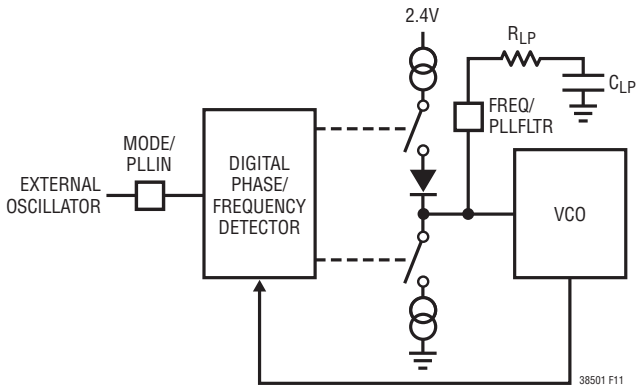

Figure 11. Phase-Locked Loop Block Diagram

tinuously from the phase detector output, pulling up the FREQ/PLLFLTR pin. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the FREQ/PLLFLTR pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the FREQ/PLLFLTR pin is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor C_{LP} holds the voltage.

The loop filter components, C_{LP} and R_{LP}, smooth out the current pulses from the phase detector and provide a stable input to the voltage-controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} = 10k and C_{LP} is 2200pF to 0.01µF.

Typically, the external clock (on MODE/PLLIN pin) input high threshold is 1.6V, while the input low threshold is 1V.

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest time duration that the LTC3850 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTC3850 is approximately 90ns, with reasonably good PCB layout, minimum 30% inductor current ripple and at least 10mV – 15mV ripple on the current sense signal. The minimum on-time can be affected by PCB switching noise in the voltage and current loop. As the peak sense voltage decreases the minimum on-time gradually increases to 130ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

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Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3850 circuits: 1) IC V_{IN} current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) Topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. V_{IN} current typically results in a small (<0.1%) loss.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

   Supplying $INTV_{CC}$ power through $EXTV_{CC}$ from an output-derived source will scale the V_{IN} current required for the driver and control circuits by a factor of (Duty Cycle)/(Efficiency). For example, in a 20V to 5V application, 10mA of $INTV_{CC}$ current results in approximately 2.5mA of V_{IN} current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor. In continuous mode, the average output current flows through L and R_{SENSE}, but is "chopped" between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 10mΩ, R_L = 10mΩ, R_{SENSE} = 5mΩ, then the total resistance is 25mΩ. This results in losses ranging from 2% to 8% as the output current increases from 3A to 15A for a 5V output, or a 3% to 12% loss for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the topside MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

   $$\text{Transition Loss} = (1.7)\ V_{IN}^2\ I_{O(MAX)}\ C_{RSS}\ f$$

Other "hidden" losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these "system" level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. The LTC3850 2-phase architecture typically halves this input capacitance requirement over competing solutions. Other losses including Schottky conduction losses during dead time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the I_{TH} pin not only allows optimization of control loop behavior but also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time and settling at this test point truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this

APPLICATIONS INFORMATION

pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in the Typical Application circuit will provide an adequate starting point for most applications.

The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the I_{TH} pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 12. Figure 13 illustrates the current waveforms present in the various branches of the 2-phase synchronous regulators operating in the continuous mode. Check the following in your layout:

1. Are the top N-channel MOSFETs M1 and M3 located within 1 cm of each other with a common drain connection at C_{IN}? Do not attempt to split the input decoupling for the two channels as it can cause a large resonant loop.
2. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The V_{FB} and I_{TH} traces should be as short as possible. The path formed by the top N-channel MOSFET, Schottky diode and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.
3. Do the LTC3850 V_{FB} pins' resistive dividers connect to the (+) terminals of C_{OUT}? The resistive divider must be connected between the (+) terminal of C_{OUT} and signal ground. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).
4. Are the $SENSE^+$ and $SENSE^-$ leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor or inductor, whichever is used for current sensing.

APPLICATIONS INFORMATION

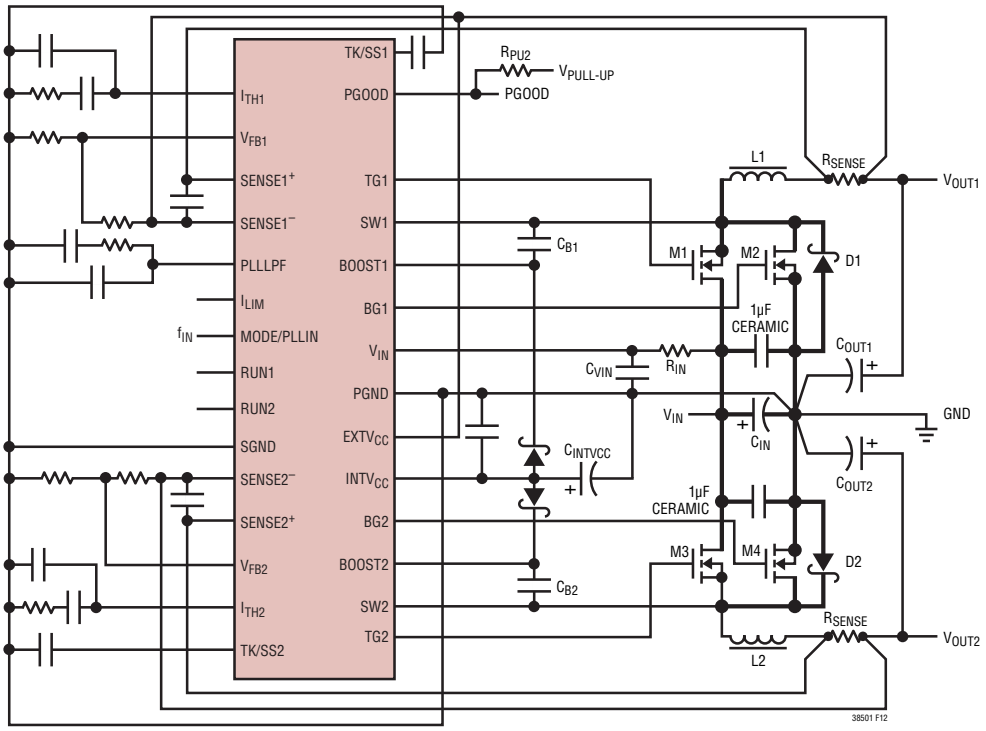


Figure 12. Recommended Printed Circuit Layout Diagram

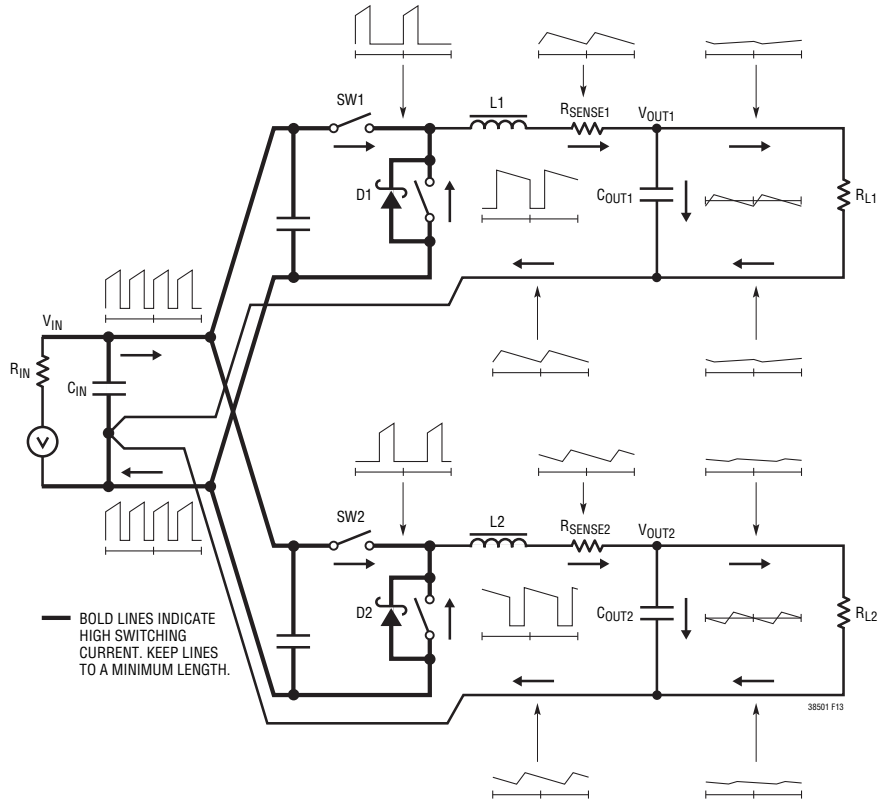


Figure 13. Branch Current Waveforms

APPLICATIONS INFORMATION

5. Is the $INTV_{CC}$ decoupling capacitor connected close to the IC, between the $INTV_{CC}$ and the power ground pins? This capacitor carries the MOSFET drivers current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and PGND pins can help improve noise performance substantially.
6. Keep the switching nodes (SW1, SW2), top gate nodes (TG1, TG2), and boost nodes (BOOST1, BOOST2) away from sensitive small-signal nodes, especially from the opposite channel's voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the "output side" of the LTC3850 and occupy minimum PC trace area. If DCR sensing is used, place the top resistor (Figure 2b, R1) close to the switching node.
7. Use a modified "star ground" technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the SGND pin of the IC.

PC Board Layout Debugging

Start with one controller at a time. It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 10% of the maximum designed current level in Burst Mode operation.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required. Only after each controller is checked for its individual performance should both controllers be turned on at the same time. A particularly difficult region of operation is when one controller channel is nearing its current comparator trip point when the other channel is turning on its top MOSFET. This occurs around 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty cycle jitter.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, Schottky and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the SGND pin of the IC.

Design Example

As a design example for a two channel medium current regulator, assume V_{IN} = 12V(nominal), V_{IN} = 20V(maximum), V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, $I_{MAX1,2}$ = 5A, and f = 500kHz (see Figure 14).

The regulated output voltages are determined by:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R_B}{R_A}\right)$$

Using 20k 1% resistors from both V_{FB} nodes to ground, the top feedback resistors are (to the nearest 1% standard value) 63.4k and 25.5k.

The frequency is set by biasing the FREQ/PLLFLTR pin to 1.2V (see Figure 10), using a divider from $INTV_{CC}$. This

APPLICATIONS INFORMATION

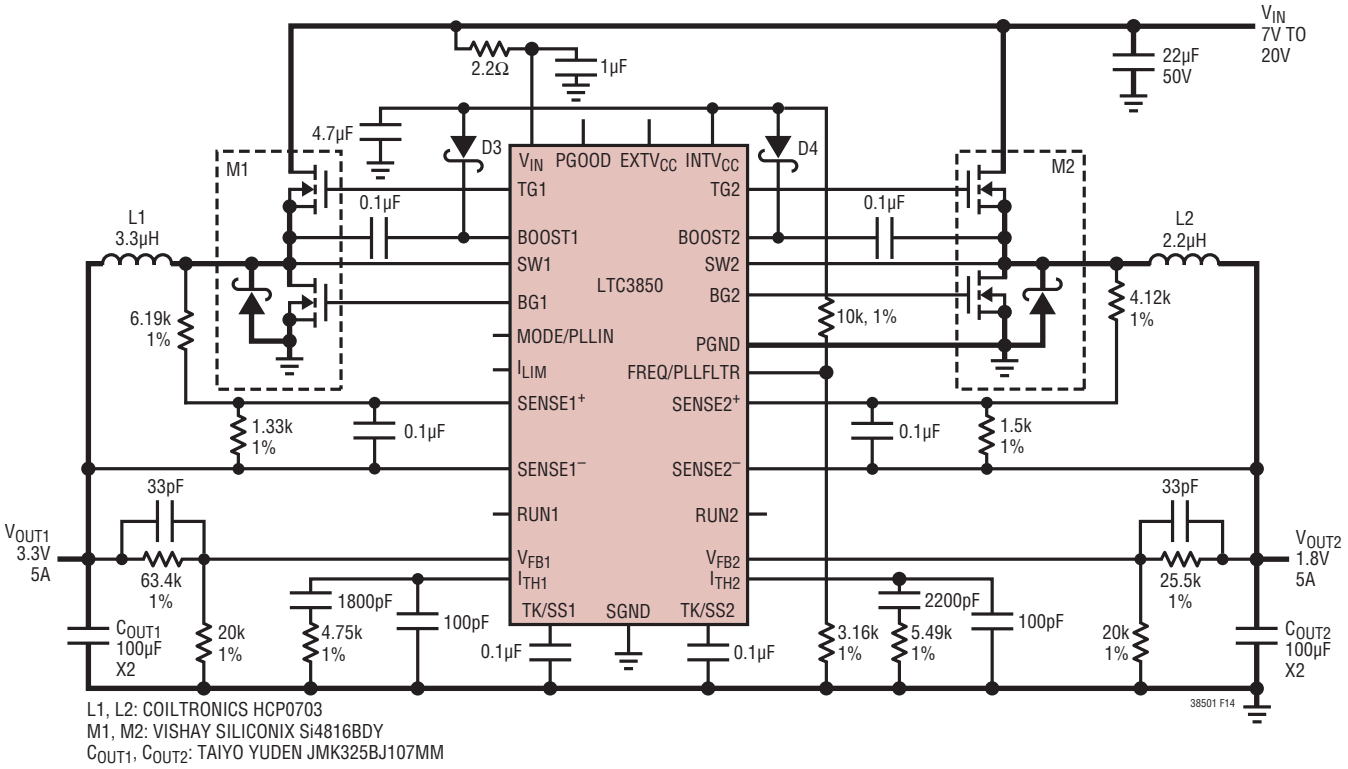


Figure 14. High Efficiency Dual 500kHz 3.3V/1.8V Step-Down Converter

voltage will decrease as V_{IN} approaches 5V, lowering the switching frequency. If a separate 5V supply is connected to $EXTV_{CC}$, $INTV_{CC}$ will remain at 5V even if V_{IN} decreases.

The inductance values are based on a 35% maximum ripple current assumption (1.75A for each channel). The highest value of ripple current occurs at the maximum input voltage:

$$L = \frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}} \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Channel 1 will require 3.2µH, and Channel 2 will require 1.9µH. The next highest standard values are 3.3µH and 2.2µH. At the nominal input voltage (12V), the ripple will be:

$$\Delta I_{L(NOM)} = \frac{V_{OUT}}{f \bullet L} \left(1 - \frac{V_{OUT}}{V_{IN(NOM)}}\right)$$

Channel 1 will have 1.45A (29%) ripple, and Channel 2 will have 1.4A (28%) ripple. The peak inductor current will be the maximum DC value plus one-half the ripple current, or 5.725A for Channel 1 and 5.7A for Channel 2.

The minimum on-time occurs on Channel 1 at the maximum V_{IN}, and should not be less than 90ns:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)} f} = \frac{1.8V}{20V(500kHz)} = 180ns$$

With I_{LIM} floating, the equivalent R_{SENSE} resistor value can be calculated by using the minimum value for the maximum current sense threshold (40mV).

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MIN)}}{I_{LOAD(MAX)} + \frac{\Delta I_{L(NOM)}}{2}} =$$

$$\frac{40mV}{5A + \frac{1.5A}{2}} \cong 7m\Omega$$

The equivalent R_{SENSE} is the same for Channel 2.

APPLICATIONS INFORMATION

The Coiltronics (Cooper) HCP0703-2R2 (20mΩ DCR_{MAX} at 20°C) and HCP0703-3R3 (30mΩ DCR_{MAX} at 20°C) are chosen. At 100°C, the estimated maximum DCR values are 26.4mΩ and 39.6mΩ. The divider ratios are:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX}\ \text{at}\ T_{L(MAX)}} = \frac{7m\Omega}{26.4m\Omega} = 0.26;$$

$$\text{and}\quad \frac{7m\Omega}{39.6m\Omega} \cong 0.18$$

For each channel, 0.1µF is selected for C1.

$$R1||R2 = \frac{L}{(DCR_{MAX}\ \text{at}\ 20°C)\bullet C1} = \frac{2.2\mu H}{20m\Omega\bullet 0.1\mu F}$$

$$= 1.1k;\quad \text{and}\quad \frac{3.3\mu H}{30m\Omega\bullet 0.1\mu F} = 1.1k$$

For channel 1, the DCR_{SENSE} filter/divider values are:

$$R1 = \frac{R1||R2}{R_D} = \frac{1.1k}{0.18} \cong 6.19k;$$

$$R2 = \frac{R1\bullet R_D}{1-R_D} = \frac{6.19k\bullet 0.18}{1-0.18} \cong 1.33k$$

The power loss in R1 at the maximum input voltage is:

$$P_{LOSS}R1 = \frac{(V_{IN(MAX)} - V_{OUT})\bullet V_{OUT}}{R1} =$$

$$\frac{(20V-3.3V)\bullet 3.3V}{6.19k} = 9mW$$

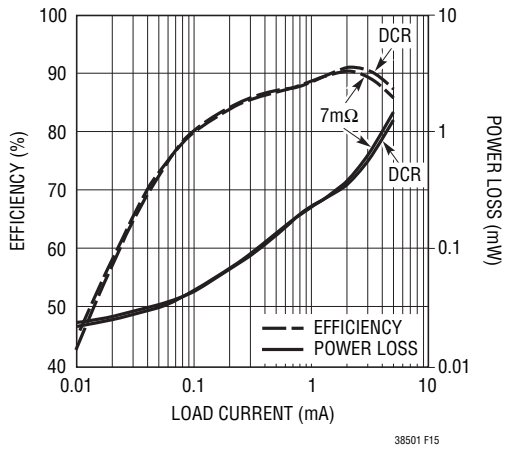


Figure 15. Design Example Efficiency vs Load

The respective values for Channel 2 are R1 = 4.12k, R2 = 1.5k; and P_{LOSS} R1 = 8mW.

Burst Mode operation is chosen for high light load efficiency (Figure 15) by floating the MODE/PLLIN pin. Power loss due to the DCR sensing network is slightly higher at light loads than would have been the case with a suitable sense resistor (7mΩ). At heavier loads, DCR sensing provides higher efficiency.

The power dissipation on the topside MOSFET can be easily estimated. Choosing a Siliconix Si4816BDY dual MOSFET results in: $R_{DS(ON)}$ = 0.023Ω/0.016Ω, C_{MILLER} ≅ 100pF. At maximum input voltage with T(estimated) = 50°C:

$$P_{MAIN} = \frac{3.3V}{20V}(5)^2\left[1+(0.005)(50°C-25°C)\right]\bullet$$

$$(0.023\Omega)+(20V)^2\left(\frac{5A}{2}\right)(2\Omega)(100pF)\bullet$$

$$\left[\frac{1}{5-2.3}+\frac{1}{2.3}\right](500kHz) = 186mW$$

A short-circuit to ground will result in a folded back current of:

$$I_{SC} = \frac{(1/3)50mV}{0.007\Omega} - \frac{1}{2}\left(\frac{90ns(20V)}{3.3\mu H}\right) = 2.1A$$

with a typical value of $R_{DS(ON)}$ and δ = (0.005/°C)(20) = 0.1. The resulting power dissipated in the bottom MOSFET is:

$$P_{SYNC} = \frac{20V-3.3V}{20V}(2.1A)^2(1.125)(0.016\Omega)$$

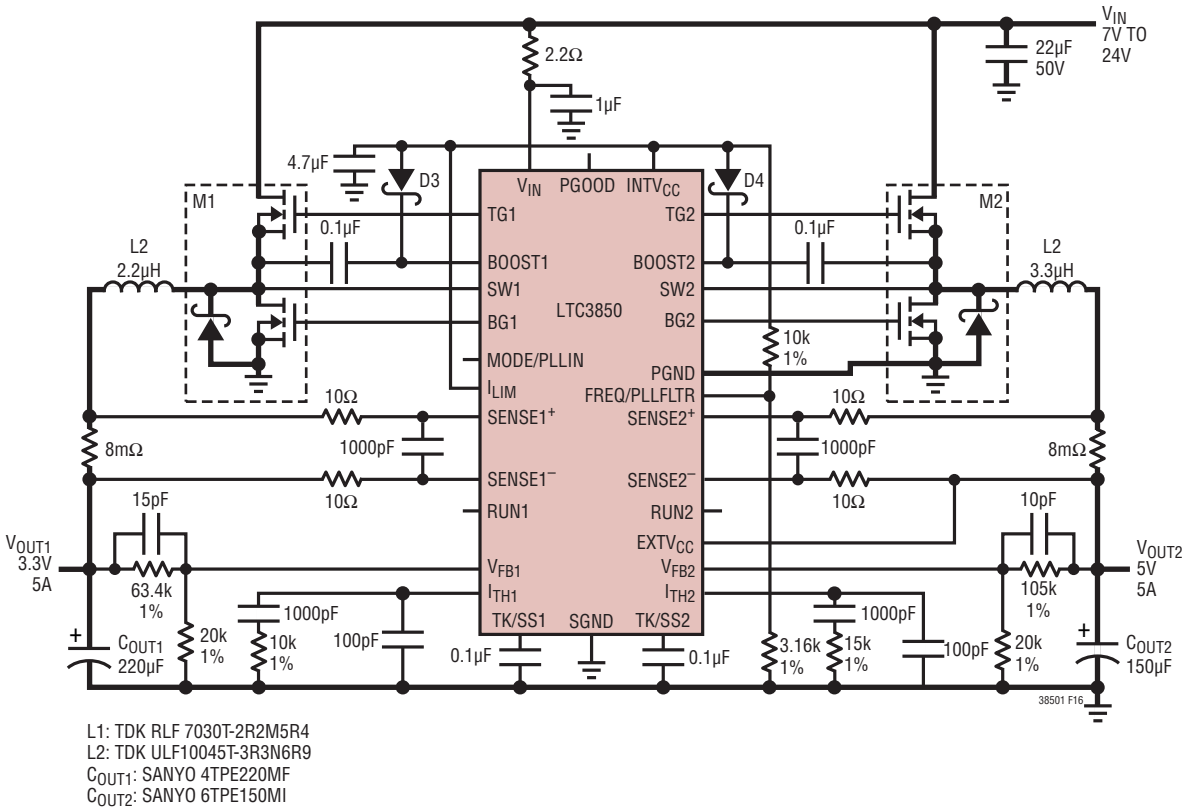
$$= 66mW$$

which is less than under full-load conditions.

C_{IN} is chosen for an RMS current rating of at least 2A at temperature assuming only channel 1 or 2 is on. C_{OUT} is chosen with an ESR of 0.02Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$$V_{ORIPPLE} = R_{ESR}\ (\Delta I_L) = 0.02\Omega(1.5A) = 30mV_{P-P}$$

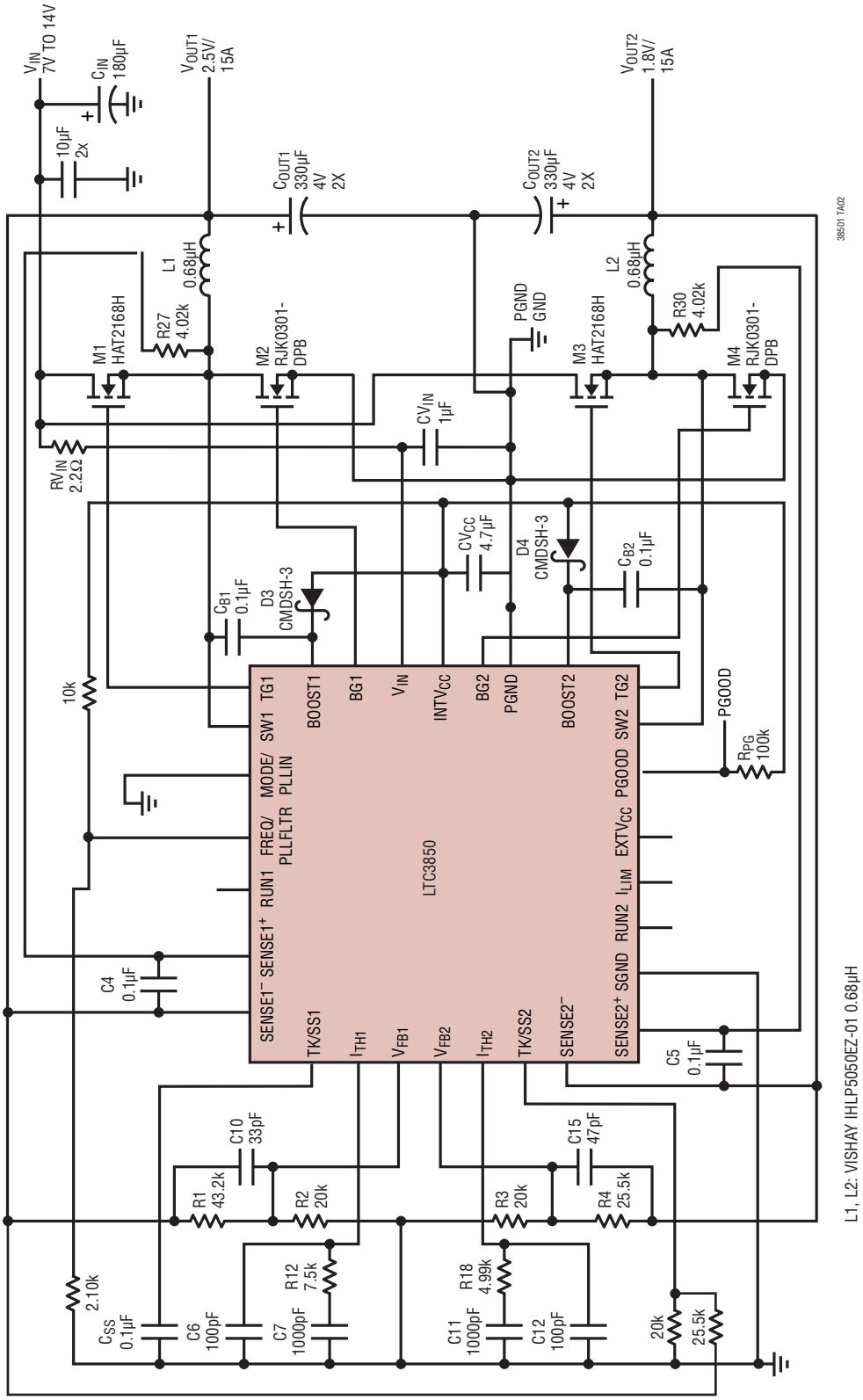
TYPICAL APPLICATIONS



L1: TDK RLF 7030T-2R2M5R4
L2: TDK ULF10045T-3R3N6R9
C_{OUT1}: SANYO 4TPE220MF
C_{OUT2}: SANYO 6TPE150MI

Figure 16. 3.3V/5A, 5V/5A Converter Using Sense Resistors

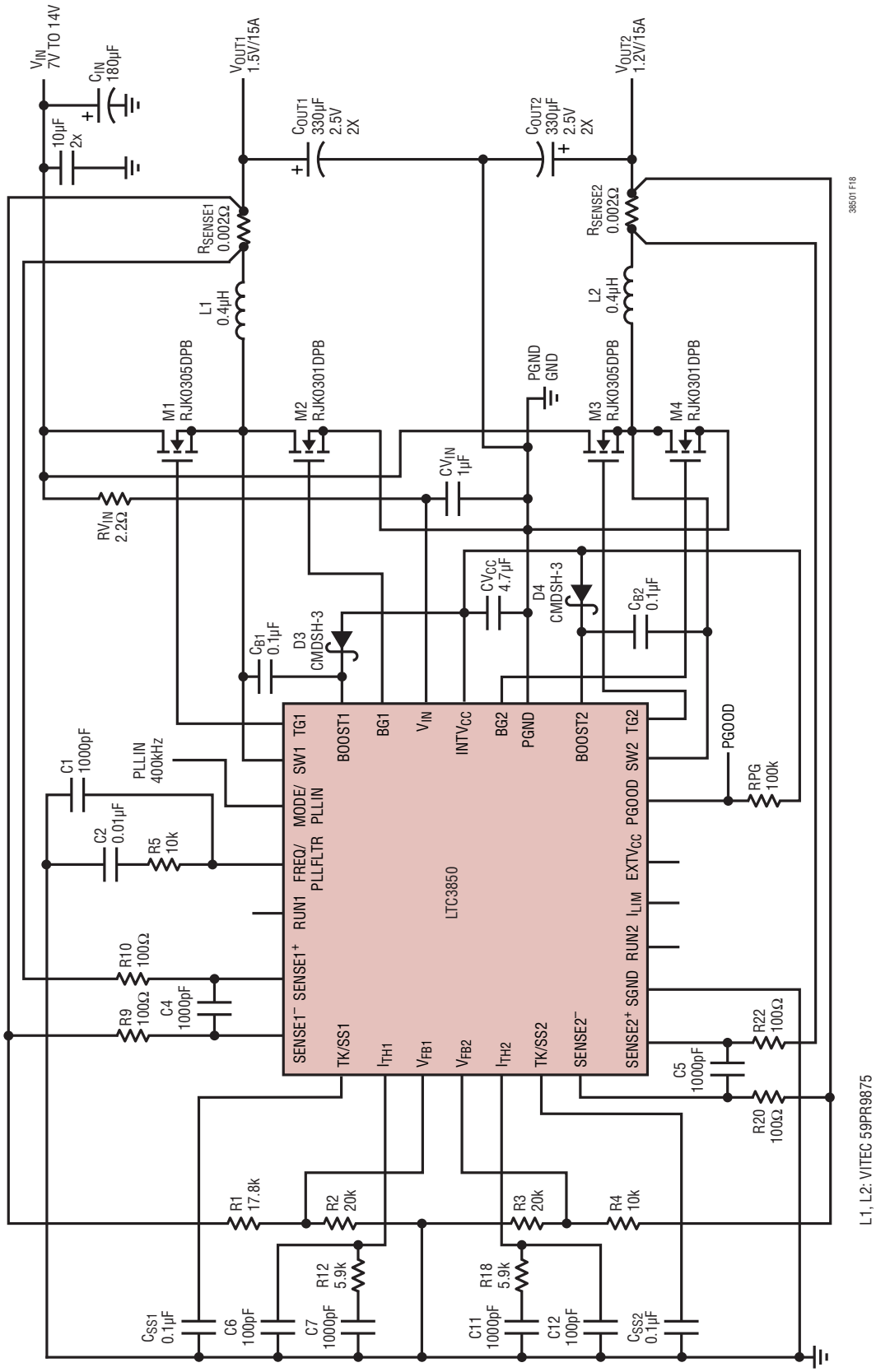
TYPICAL APPLICATIONS



L1, L2: VISHAY IHLP5050EZ-01 0.68µH
COUT1, COUT2: SANYO 4TPD330M

Figure 17. 2.5V/15A, 1.8V/15A Converter with DCR Sensing and Coincident Rail Tracking F_{SW} = 350kHz

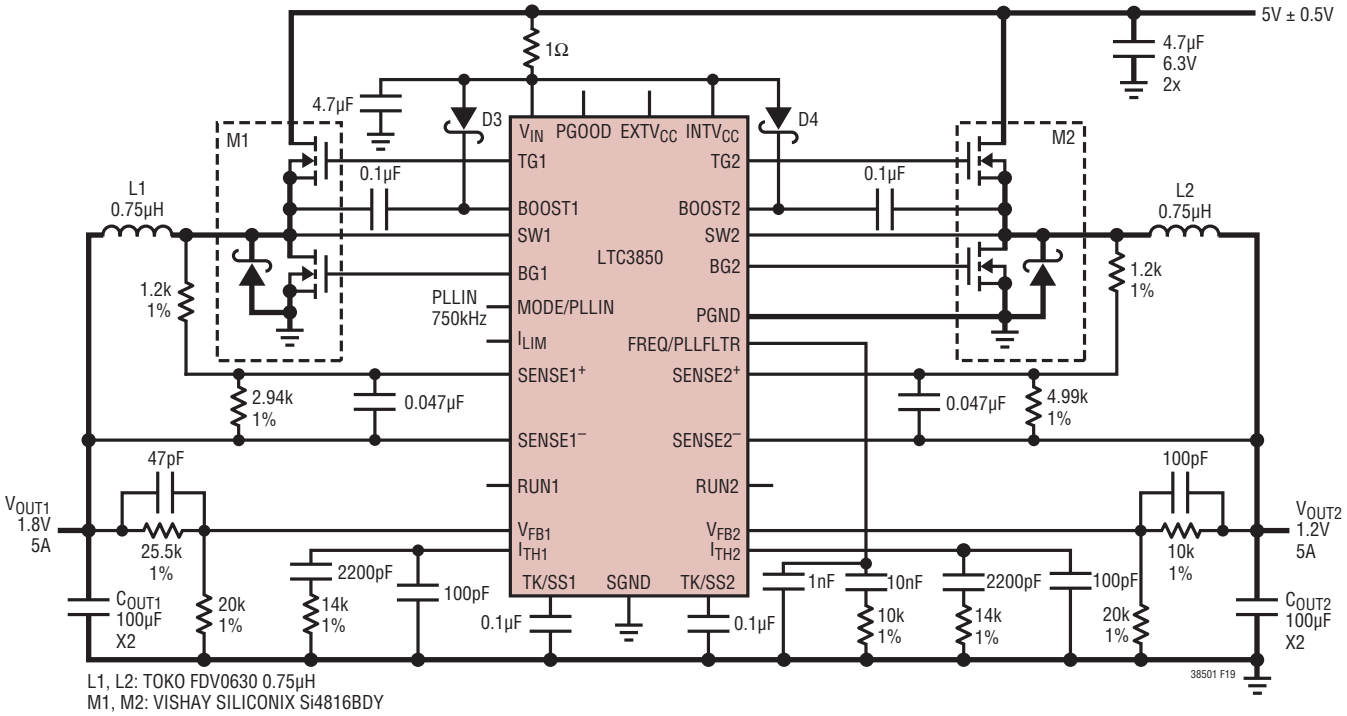
TYPICAL APPLICATIONS



L1, L2: VITEC 59PR9875
COUT1, COUT2: 2R5TPE330M9

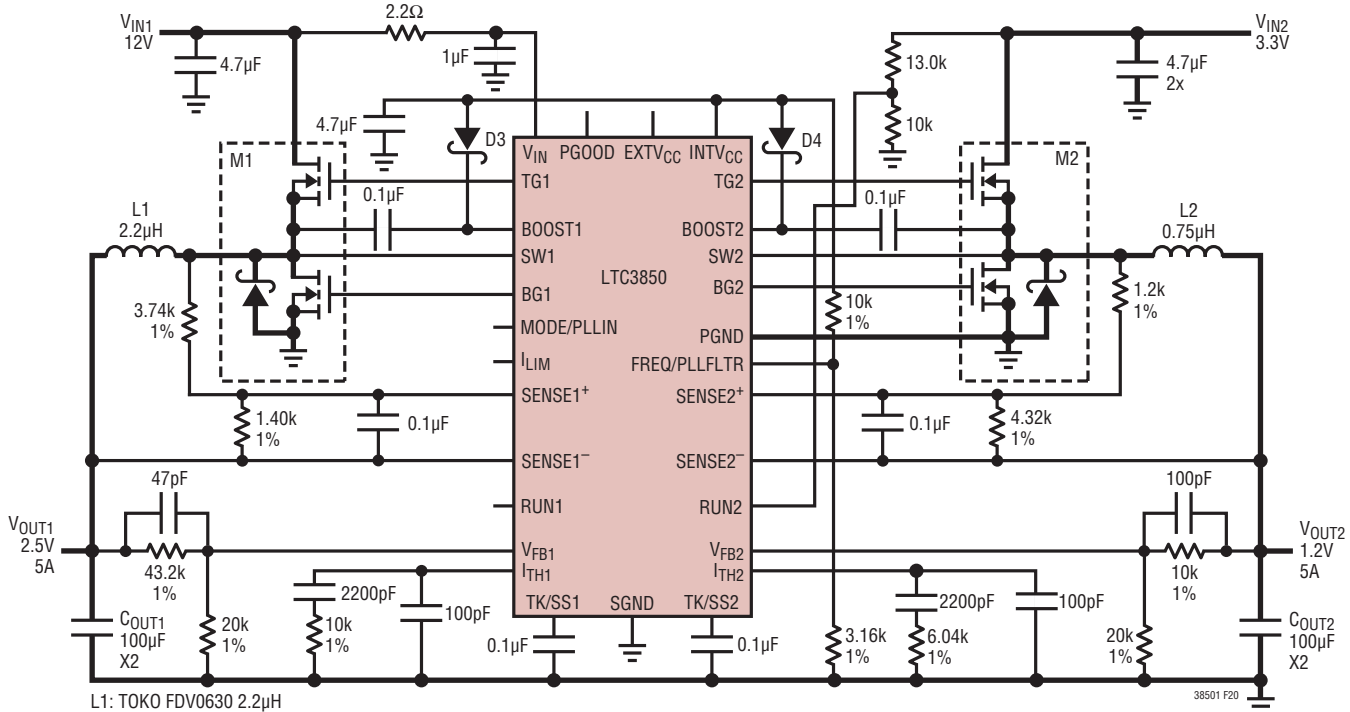
Figure 18. 1.5V/15A, 1.2V/15A Core-I/O Converter with Sense Resistor Synchronized at 400kHz

TYPICAL APPLICATIONS



L1, L2: TOKO FDV0630 0.75µH
M1, M2: VISHAY SILICONIX Si4816BDY
C_{OUT1}, C_{OUT2}: TAIYO YUDEN JMK325BJ107MM

Figure 19. 1.8V/5A, 1.2V/5A Core-I/O Converter with a 5V Input Synchronized at 750kHz

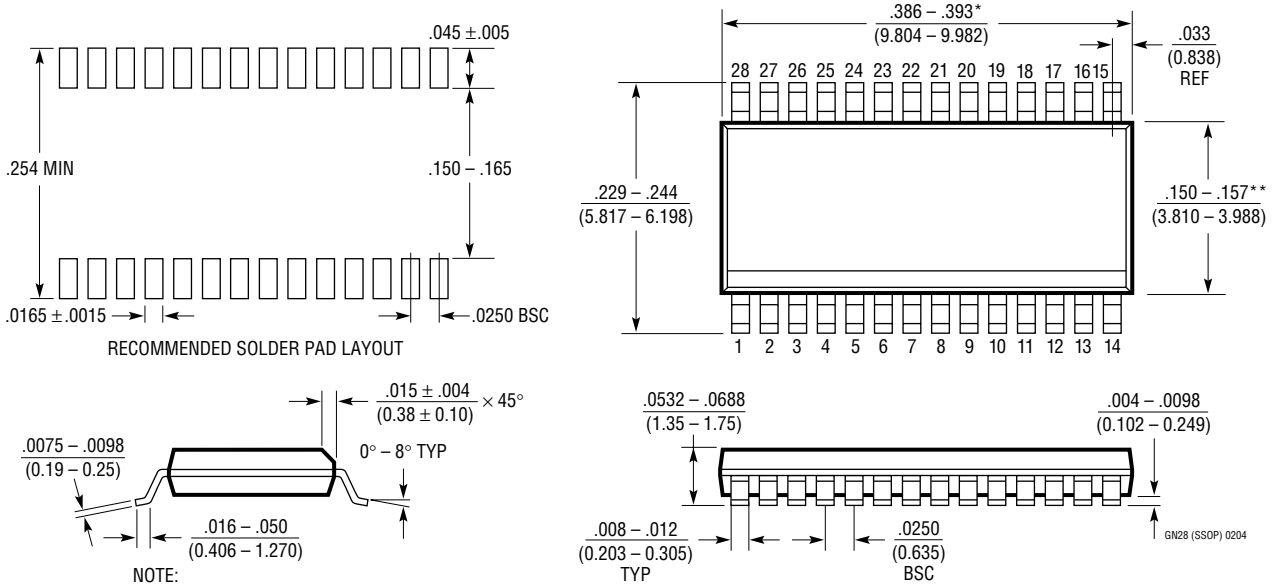


L1: TOKO FDV0630 2.2µH
L2: TOKO FDV0630 0.75µH
M1, M2: VISHAY SILICONIX Si4816BDY
C_{OUT1}, C_{OUT2}: TAIYO YUDEN JMK325BJ107MM

Figure 20. 2.5V/5A, 1.2V/5A Core-I/O Converter with Dual Inputs

PACKAGE DESCRIPTION

GN Package
28-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)

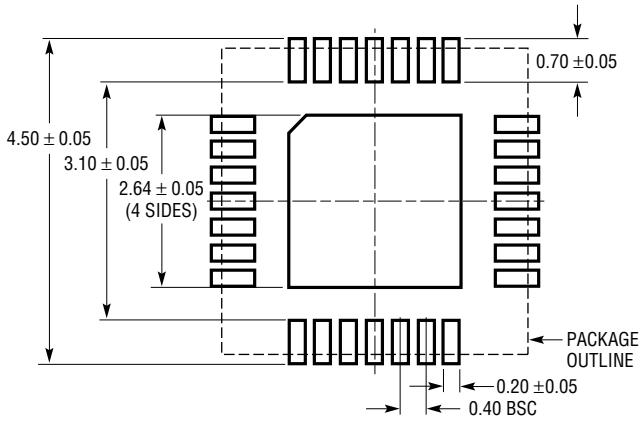


NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

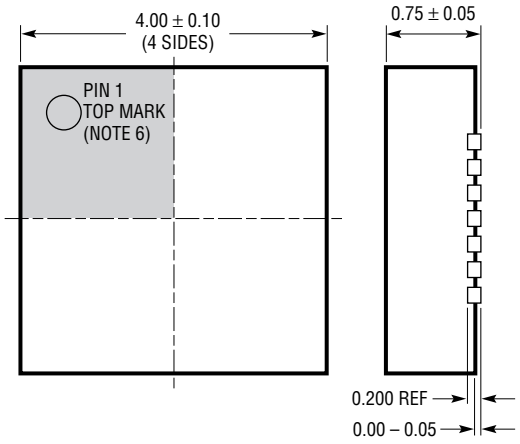
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

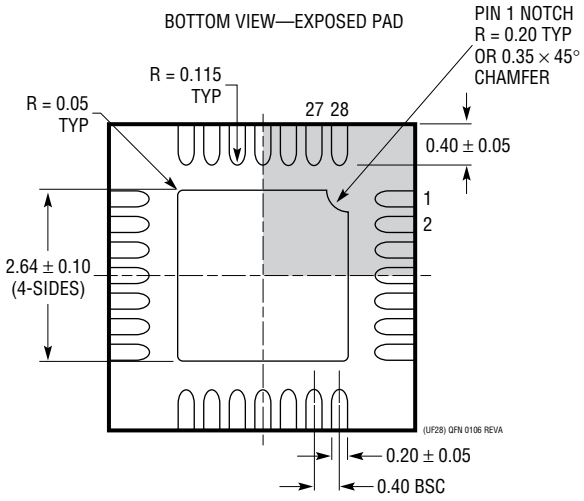
UF Package
28-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1721 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



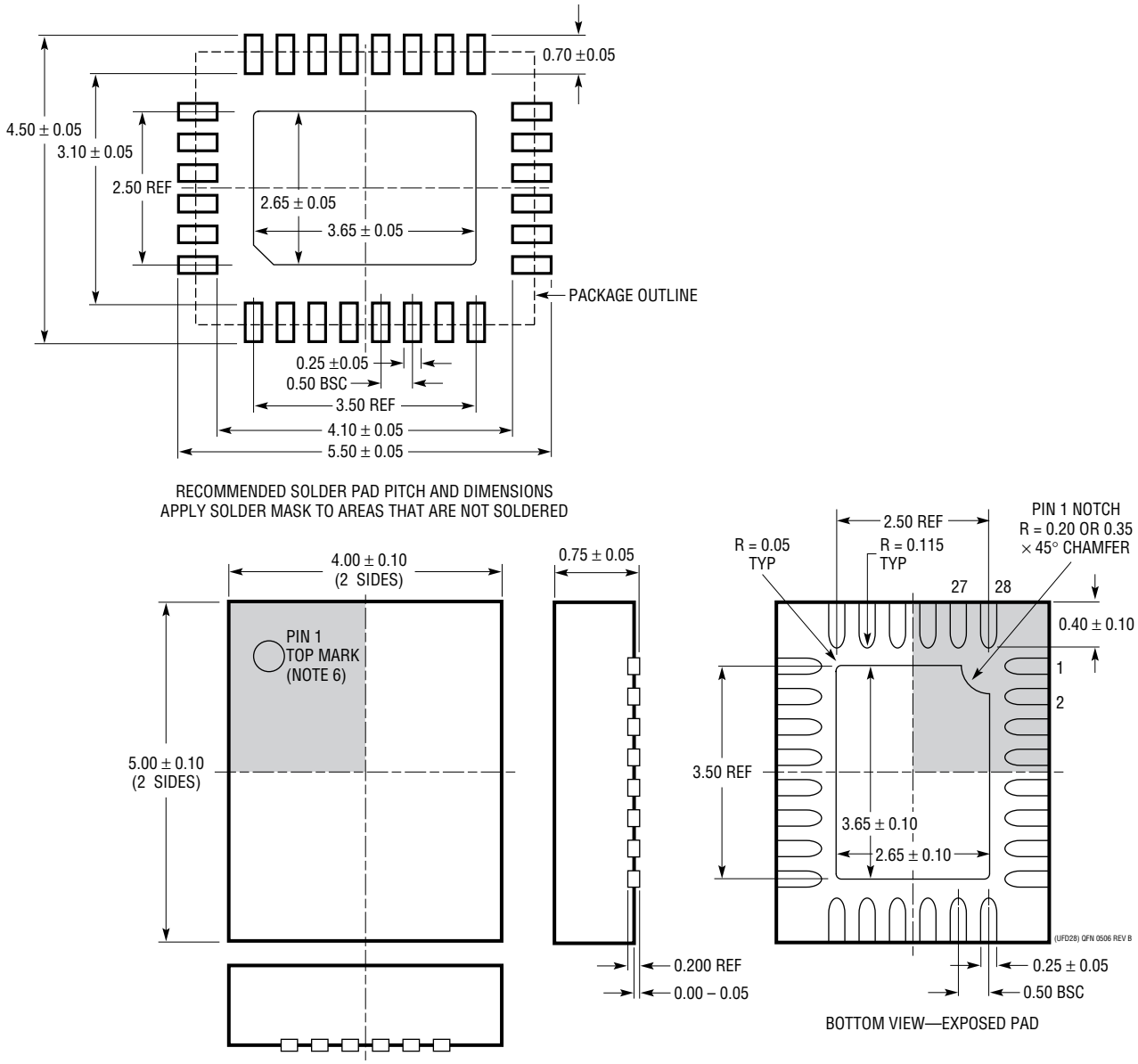
BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

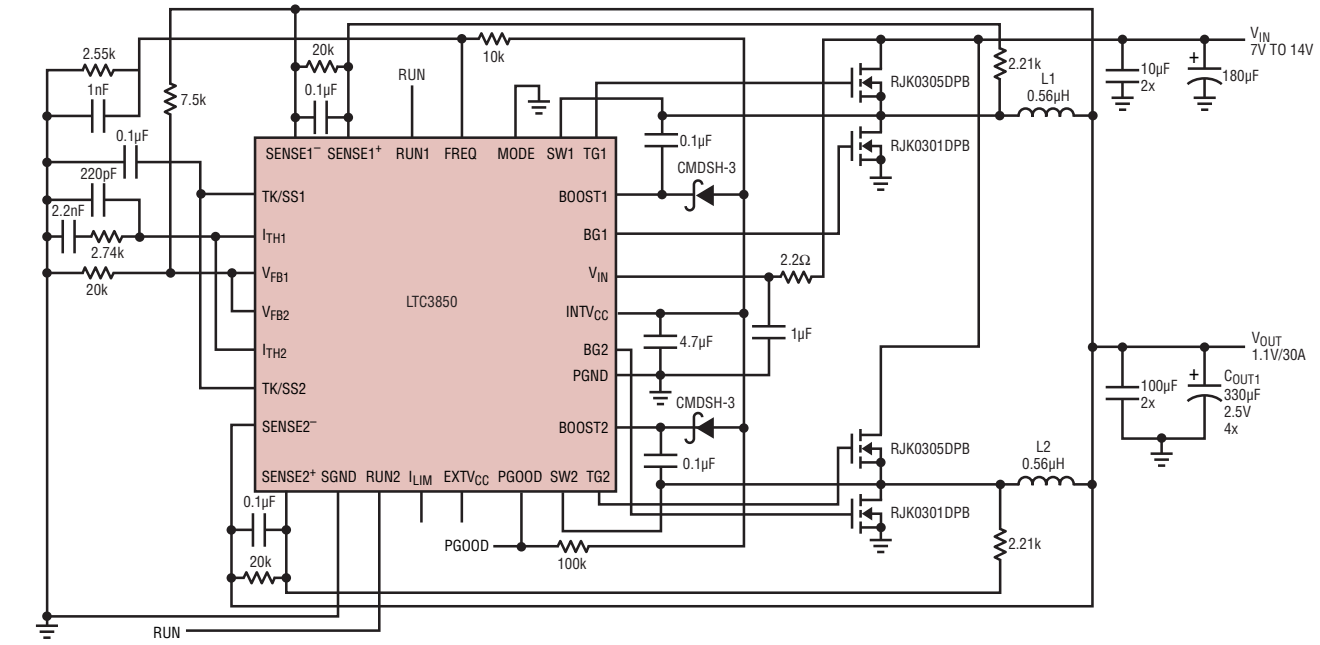
REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	3/11	Updated Switch Voltage (SW1, SW2) LTC3850I only from 30V to –0.3V to 30V to –5V	2

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION



L1, L2: VISHAY IHLP4040DZ-01 0.56µH
C_{OUT}: SANYO 2R5TPE330M9

FOR SINGLE OUTPUT, DUAL PHASE OPERATION, TIE THE FOLLOWING PINS TOGETHER:
V_{FB1} TO V_{FB1} TK/SS1 TO TK/SS2
ITH1 TO ITH2 RUN1 TO RUN2

Figure 21. 1.1V/30A Dual Phase Core Converter, F_{SW} = 400kHz

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1625/ LTC1775	No R_{SENSE}™ Current Mode Synchronous Step-Down Controllers	97% Efficiency, No Sense Resistor, 16-Pin SSOP
LTC1735	High Efficiency Synchronous Step-Down Switching Regulator	Programmable Fixed Frequency from 200kHz to 550kHz
LTC1778	No R_{SENSE} Wide Input Range Synchronous Step-Down Controller	Up to 97% Efficiency, 4V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ (0.9)(V_{IN}), I_{OUT} Up to 20A
LTC3727A-1	Dual, 2-Phase Synchronous Controller	Very Low Dropout; V_{OUT} ≤ 14V, 4V ≤ V_{IN} ≤ 36V
LTC3728	2-Phase 550kHz, Dual Synchronous Step-Down Controller	QFN and SSOP Packages, High Frequency for Smaller L and C
LTC3729	20A to 200A PolyPhase® Synchronous Controllers	Expandable from 2-Phase to 12-Phase, Uses All Surface Mount Components
LTC3731	3-Phase, Single Output From 250kHz to 600kHz Synchronous Step-Down Controller	0.6V ≤ V_{OUT} ≤ 6V, 4.5V ≤ V_{IN} ≤ 32V, I_{OUT} ≤ 60A, Integrated MOSFET Drivers
LTC3773	Triple Output DC/DC Synchronous Controller	3-Phase Step-Down DC/DC Controller, 3.3V ≤ V_{IN} ≤ 36V, Fixed Frequency 160kHz to 700kHz
LTC3810	100V Current Mode Synchronous Step-Down Switching Controller	0.8V ≤ V_{OUT} ≤ 0.93V_{IN}, 6.2V ≤ V_{IN} ≤ 100V, No R_{SENSE}
LTC3826	Low I_Q, Dual, 2-Phase Synchronous Step-Down Controller	30µA I_Q, 0.8V ≤ V_{OUT} ≤ 10V, 4V ≤ V_{IN} ≤ 36V
LTC3828	Dual, 2-Phase Synchronous Step-Down Controller with Tracking	Up to Six Phases, 0.8V ≤ V_{OUT} ≤ 7V, 4.5V ≤ V_{IN} ≤ 28V
LTC3834/ LTC3834-1	Low I_Q, Synchronous Step-Down Controller	30µA I_Q, 0.8V ≤ V_{OUT} ≤ 10V, 4V ≤ V_{IN} ≤ 36V
LT3845	Low I_Q, High Voltage Single Output Synchronous Step-Down DC/DC Controller	1.23V ≤ V_{OUT} ≤ 36V, 4V ≤ V_{IN} ≤ 60V, 120µA I_Q

PolyPhase is a registered trademark of Linear Technology Corporation. No R_{SENSE} is a trademark of Linear Technology Corporation.

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