

# TLE42994

Low Dropout Fixed Voltage Regulator

TLE42994G  
TLE42994GM  
TLE42994E

## Data Sheet

Rev. 1.2, 2014-07-03

Automotive Power



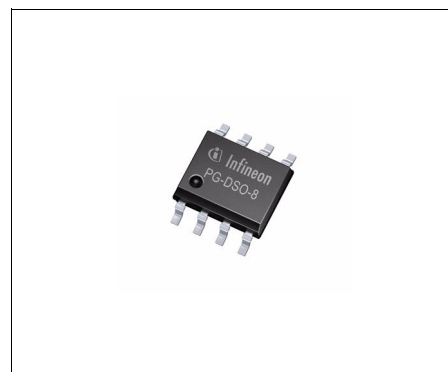
## 1 Overview

### Features

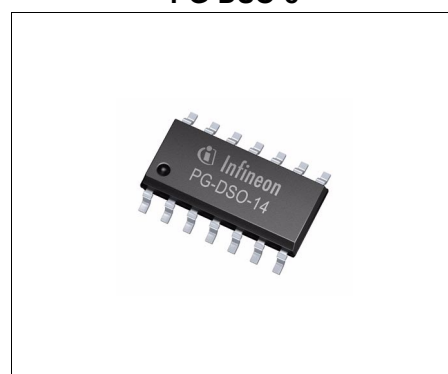
- Output Voltage 5 V  $\pm$  2%
- Output Current up to 150 mA
- Extreme Low Current Consumption In ON State
- Enable Function: Below 1  $\mu$ A Current Consumption In OFF State
- Early Warning
- Power-on and Undervoltage Reset with Programmable Delay Time
- Reset Low Down to  $V_Q = 1$  V
- Adjustable Reset Threshold
- Very Low Dropout Voltage
- Output Current Limitation
- Reverse Polarity Protection
- Overtemperature Protection
- Suitable for Use in Automotive Electronics
- Wide Temperature Range from -40 °C up to 150 °C
- Input Voltage Range from -42 V to 45 V
- Green Product (RoHS compliant)
- AEC Qualified

### Description

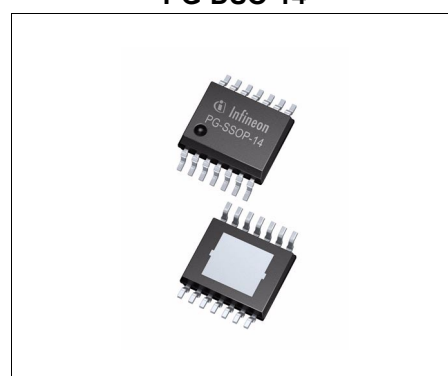
The TLE42994 is a monolithic integrated low dropout voltage regulator, especially designed for automotive applications that need to be in ON state during the car's engine is turned off. An input voltage up to 45 V is regulated to an output voltage of 5.0 V. The component is able to drive loads up to 150 mA. It is short-circuit protected by the implemented current limitation and has an integrated overtemperature shutdown. A reset signal is generated for an output voltage  $V_{Q,rt}$  of typically 4.65 V. This threshold can be decreased by an external



**PG-DSO-8**



**PG-DSO-14**



**PG-SSOP-14 exposed pad**

Type	Package	Marking
TLE42994G	PG-DSO-8	42994G
TLE42994GM	PG-DSO-14	42994GM
TLE42994E	PG-SSOP-14 exposed pad	42994E

resistor divider. The power-on reset delay time can be programmed by the external delay capacitor. The additional sense comparator provides an early warning function: Any voltage (e.g. the input voltage) can be monitored, an under-voltage condition is indicated by setting the comparator's output to low. The TLE42994GM (PG-DSO-14 package) and TLE42994E (PG-SSOP-14 exposed pad package) include additionally an Enable function permitting enabling/disabling the regulator. In case the regulator is disabled it consumes less current than 1  $\mu\text{A}$ .

### Dimensioning Information on External Components

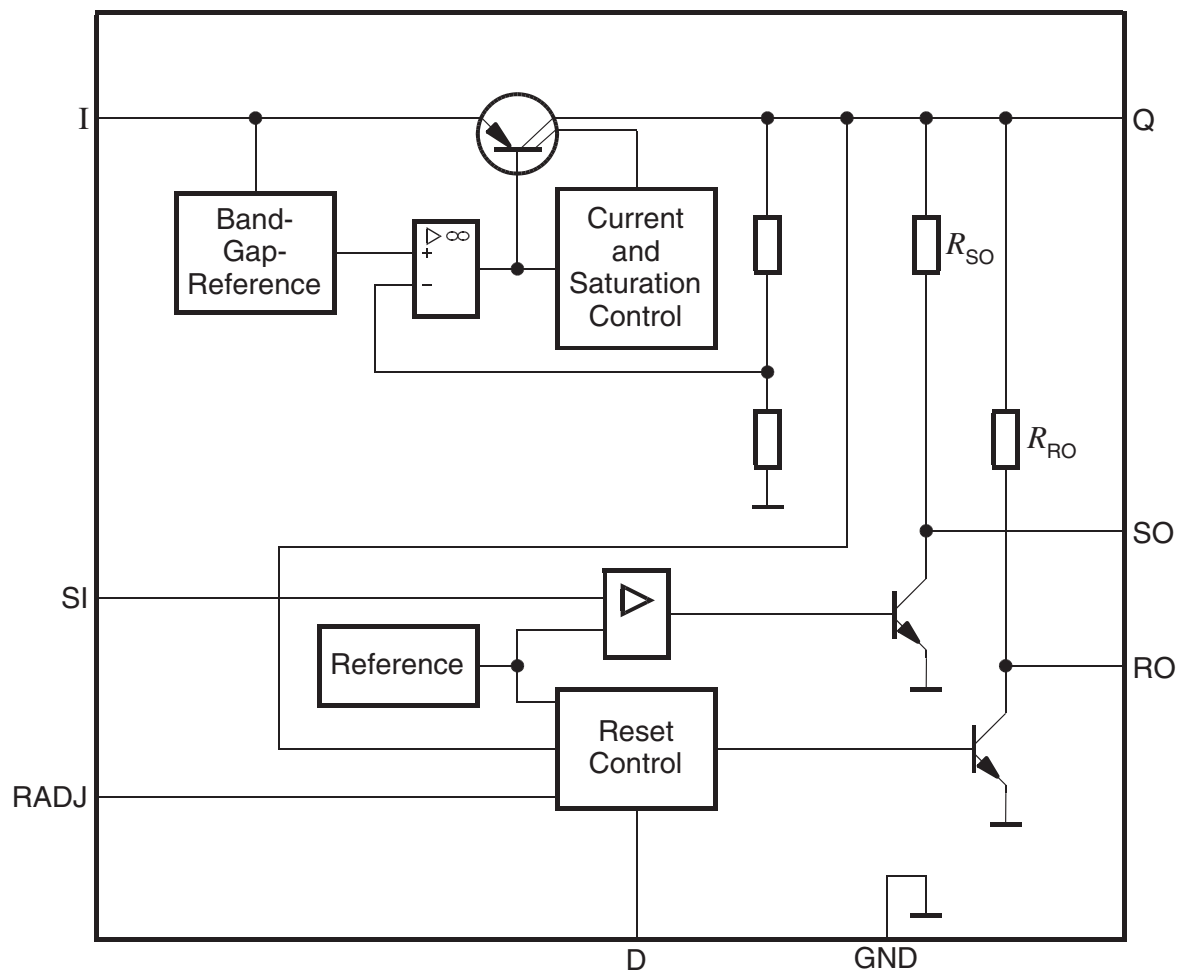
The input capacitor  $C_I$  is recommended for compensation of line influences. The output capacitor  $C_Q$  is necessary for the stability of the control loop.

### Circuit Description

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The component also has a number of internal circuits for protection against:

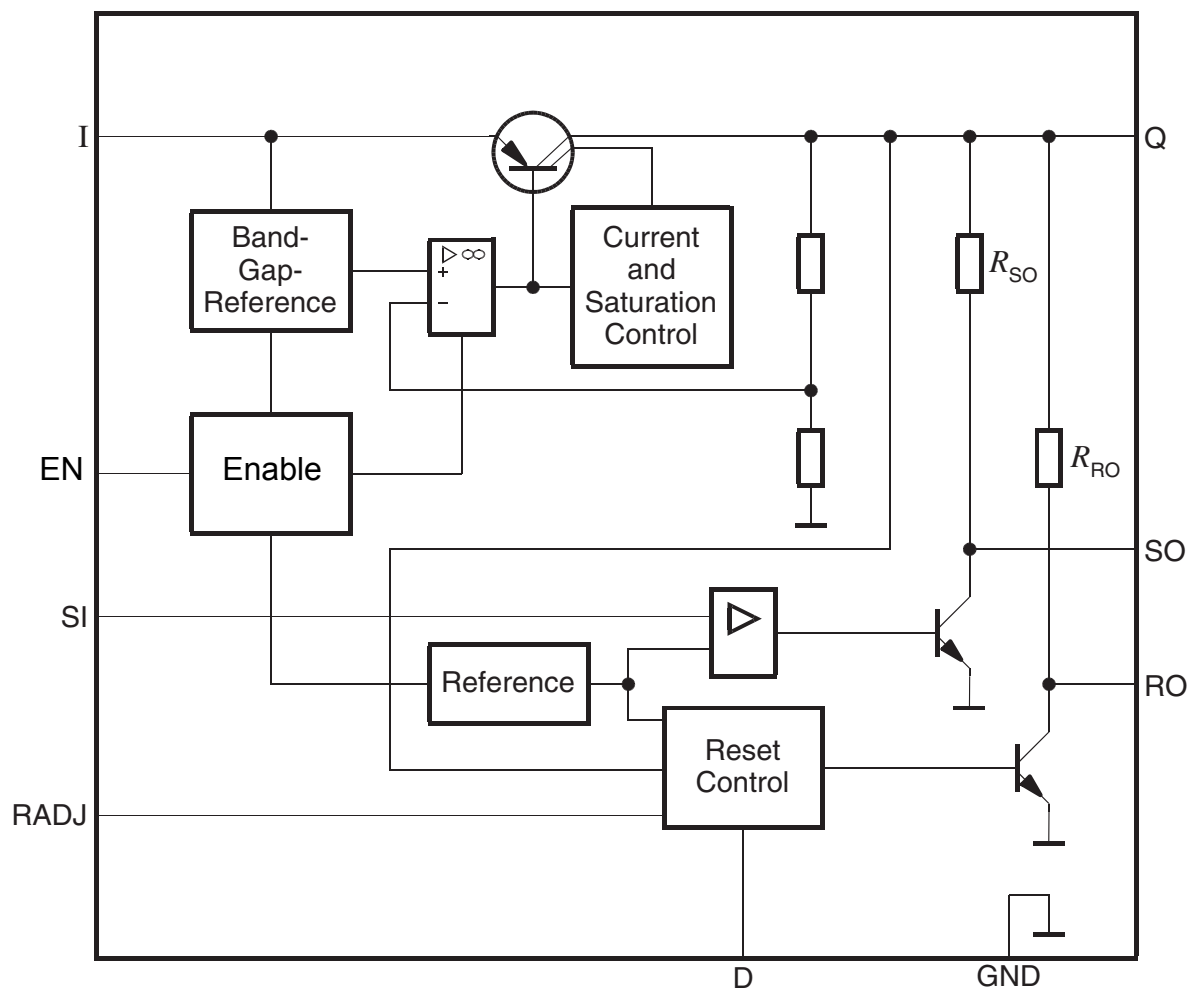
- Overload
- Overtemperature
- Reverse polarity

## 2 Block Diagram



AEB03103

Figure 1 Block Diagram TLE42994G (package PG-DSO-8)



AEB03104

Figure 2 Block Diagram TLE42994GM, TLE42994E (packages PG-DSO-14, PG-SSOP-14 exposed pad)

## 3 Pin Configuration

### 3.1 Pin Assignment TLE42994G (PG-DSO-8)

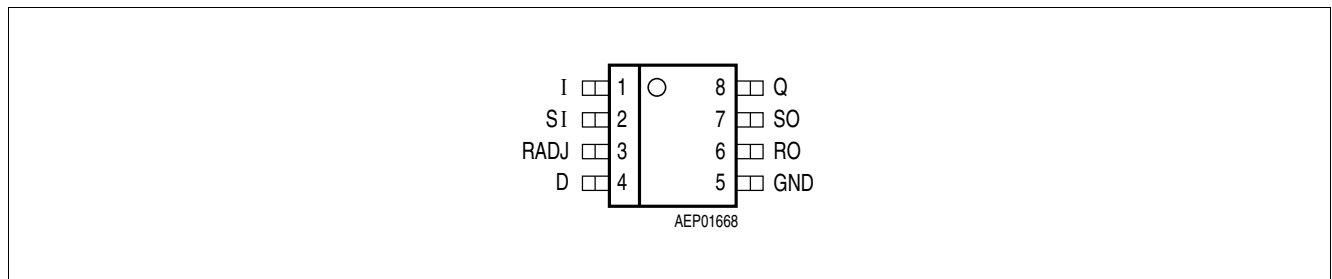


Figure 3 Pin Configuration (top view)

### 3.2 Pin Definitions and Functions TLE42994G (PG-DSO-8)

Pin	Symbol	Function
1	I	<b>Input</b> for compensating line influences, a capacitor to GND close to the IC terminals is recommended
2	SI	<b>Sense Input</b> connect the voltage to be monitored; connect to Q if the sense comparator is not needed
3	RADJ	<b>Reset Threshold Adjust</b> connect an external voltage divider to adjust reset threshold; connect to GND for using internal threshold
4	D	<b>Reset Delay Timing</b> connect a ceramic capacitor to GND for adjusting the reset delay time; leave open if the reset function is not needed
5	GND	<b>Ground</b>
6	RO	<b>Reset Output</b> open collector output; internally linked to the output via a 20 kΩ pull-up resistor; leave open if the reset function is not needed
7	SO	<b>Sense Output</b> open collector output; internally linked to the output via a 20 kΩ pull-up resistor; leave open if the sense comparator is not needed
8	Q	<b>Output</b> block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance $C_Q$ and ESR in <a href="#">“Functional Range” on Page 12</a>

### 3.3 Pin Assignment TLE42994GM (PG-DSO-14)

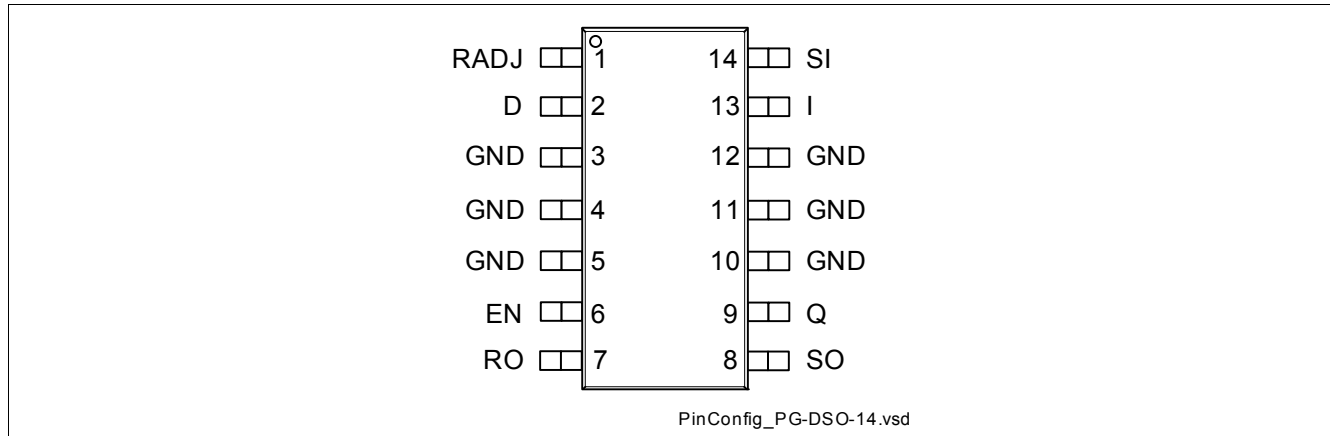


Figure 4 Pin Configuration (top view)

### 3.4 Pin Definitions and Functions TLE42994GM (PG-DSO-14)

Pin	Symbol	Function
1	RADI	<b>Reset Threshold Adjust</b> connect an external voltage divider to adjust reset threshold; connect to GND for using internal threshold
2	D	<b>Reset Delay Timing</b> connect a ceramic capacitor to GND for adjusting the reset delay time; leave open if the reset function is not needed
3, 4, 5	GND	<b>Ground</b> connect all pins to PCB and heatsink area
6	EN	<b>Enable</b> high signal enables the regulator; low signal disables the regulator; connect to I if the Enable function is not needed
7	RO	<b>Reset Output</b> open collector output; internally linked to the output via a 20kΩ pull-up resistor; leave open if the reset function is not needed
8	SO	<b>Sense Output</b> open collector output; internally linked to the output via a 20kΩ pull-up resistor; leave open if the sense comparator is not needed
9	Q	<b>Output</b> block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance $C_Q$ and ESR in the table <a href="#">“Functional Range” on Page 12</a>
10, 11, 12	GND	<b>Ground</b> connect all pins to PCB and heatsink area

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**Pin Configuration**

Pin	Symbol	Function
13	I	<b>Input</b> for compensating line influences, a capacitor to GND close to the IC terminals is recommended
14	SI	<b>Sense Input</b> connect the voltage to be monitored; connect to Q if the sense comparator is not needed



### 3.5 Pin Assignment TLE42994E (PG-SSOP-14 exposed pad)

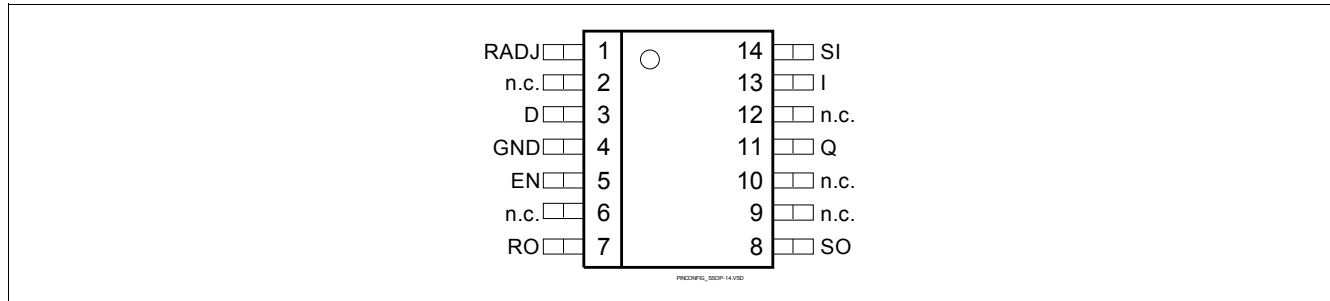


Figure 5 Pin Configuration (top view)

### 3.6 Pin Definitions and Functions TLE42994E (PG-SSOP-14 exposed pad)

Pin	Symbol	Function
1	RADJ	<b>Reset Threshold Adjust</b> connect an external voltage divider to adjust reset threshold; connect to GND for using internal threshold
2, 6	n.c.	<b>not connected</b> leave open or connect to GND
3	D	<b>Reset Delay Timing</b> connect a ceramic capacitor to GND for adjusting the reset delay time; leave open if the reset function is not needed
4	GND	<b>Ground</b> connect all pins to PCB and heatsink area
5	EN	<b>Enable</b> high signal enables the regulator; low signal disables the regulator; connect to I if the Enable function is not needed
7	RO	<b>Reset Output</b> open collector output; internally linked to the output via a 20kΩ pull-up resistor; leave open if the reset function is not needed
8	SO	<b>Sense Output</b> open collector output; internally linked to the output via a 20kΩ pull-up resistor; leave open if the sense comparator is not needed
9, 10, 12	n.c.	<b>not connected</b> leave open or connect to GND
11	Q	<b>Output</b> block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance $C_Q$ and ESR in the table <a href="#">“Functional Range” on Page 12</a>
13	I	<b>Input</b> for compensating line influences, a capacitor to GND close to the IC terminals is recommended

## Pin Configuration

Pin	Symbol	Function
14	SI	<b>Sense Input</b> connect the voltage to be monitored; connect to Q if the sense comparator is not needed
PAD	–	<b>Exposed Pad</b> attach the exposed pad on package bottom to the heatsink area on circuit board; connect to GND

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

**Table 1 Absolute Maximum Ratings<sup>1)</sup>**

-40 °C ≤  $T_j$  ≤ 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input I, Enable Input EN, Sense Input SI							
Voltage	$V_I, V_{EN}, V_{SI}$	-40	–	45	V	–	P_4.1.1
Output Q, Reset Output RO, Sense Output SO							
Voltage	$V_Q, V_{RO}, V_{SO}$	-0.3	–	7	V	–	P_4.1.2
Reset Delay D, Reset Threshold RADJ							
Voltage	$V_D, V_{RADJ}$	-0.3	–	7	V	–	P_4.1.3
Temperature							
Junction Temperature	$T_j$	-40	–	150	°C	–	P_4.1.4
Storage Temperature	$T_{stg}$	-50	–	150	°C	–	P_4.1.5
ESD Absorption							
ESD Absorption	$V_{ESD,HBM}$	-2	–	2	kV	Human Body Model (HBM) <sup>2)</sup>	P_4.1.6
ESD Absorption	$V_{ESD,CDM}$	-500	–	500	V	Charge Device Model (CDM) <sup>3)</sup>	P_4.1.7
ESD Absorption	$V_{ESD,CDM}$	-750	–	750	V	Charge Device Model (CDM) <sup>3)</sup> at corner pins	P_4.1.8

1) not subject to production test, specified by design

2) ESD susceptibility Human Body Model "HBM" according to AEC-Q100-002 - JESD22-A114

3) ESD susceptibility Charged Device Model "CDM" according to ESDA STM5.3.1

#### Notes

- Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

## 4.2 Functional Range

**Table 2 Functional Range**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Voltage	$V_I$	5.5	–	45	V	–	P_4.2.1
Output Capacitor's Requirements for Stability	$C_Q$	22	–	–	$\mu\text{F}$	– <sup>1)</sup>	P_4.2.2
Output Capacitor's Requirements for Stability	$ESR(C_Q)$	–	–	3	$\Omega$	– <sup>2)</sup>	P_4.2.3
Junction Temperature	$T_j$	–40	–	150	$^{\circ}\text{C}$	–	P_4.2.4

1) the minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

2) relevant ESR value at  $f = 10 \text{ kHz}$

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

### 4.3 Thermal Resistance

**Table 3 Thermal Resistance**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
TLE42994G (PG-DSO-8)							
Junction to Soldering Point <sup>1)</sup>	$R_{thJSP}$	—	—	60	K/W	measured to pin 5	P_4.3.1
Junction to Ambient <sup>1)</sup>	$R_{thJA}$	—	113	—	K/W	FR4 2s2p board <sup>2)</sup>	P_4.3.2
Junction to Ambient <sup>1)</sup>	$R_{thJA}$	—	185	—	K/W	FR4 1s0p board, footprint only <sup>3)</sup>	P_4.3.3
Junction to Ambient <sup>1)</sup>	$R_{thJA}$	—	142	—	K/W	FR4 1s0p board, 300mm <sup>2</sup> heatsink area on PCB <sup>3)</sup>	P_4.3.4
Junction to Ambient <sup>1)</sup>	$R_{thJA}$	—	136	—	K/W	FR4 1s0p board, 600mm <sup>2</sup> heatsink area on PCB <sup>3)</sup>	P_4.3.5
TLE42994GM (PG-DSO-14)							
Junction to Soldering Point <sup>1)</sup>	$R_{thJSP}$	—	—	30	K/W	measured to all GND pins	P_4.3.6
Junction to Ambient <sup>1)</sup>	$R_{thJA}$	—	63	—	K/W	FR4 2s2p board <sup>2)</sup>	P_4.3.7
Junction to Ambient <sup>1)</sup>	$R_{thJA}$	—	112	—	K/W	FR4 1s0p board, footprint only <sup>3)</sup>	P_4.3.8
Junction to Ambient <sup>1)</sup>	$R_{thJA}$	—	73	—	K/W	FR4 1s0p board, 300mm <sup>2</sup> heatsink area on PCB <sup>3)</sup>	P_4.3.9
Junction to Ambient <sup>1)</sup>	$R_{thJA}$	—	65	—	K/W	FR4 1s0p board, 600mm <sup>2</sup> heatsink area on PCB <sup>3)</sup>	P_4.3.10
TLE42994E (PG-SSOP-14 exposed pad)							
Junction to Case <sup>1)</sup>	$R_{thJC}$	—	10	—	K/W	—	P_4.3.11
Junction to Ambient <sup>1)</sup>	$R_{thJA}$	—	47	—	K/W	FR4 2s2p board <sup>2)</sup>	P_4.3.12
Junction to Ambient <sup>1)</sup>	$R_{thJA}$	—	140	—	K/W	FR4 1s0p board, footprint only <sup>3)</sup>	P_4.3.13
Junction to Ambient <sup>1)</sup>	$R_{thJA}$	—	63	—	K/W	FR4 1s0p board, 300mm <sup>2</sup> heatsink area on PCB <sup>3)</sup>	P_4.3.14
Junction to Ambient <sup>1)</sup>	$R_{thJA}$	—	53	—	K/W	FR4 1s0p board, 600mm <sup>2</sup> heatsink area on PCB <sup>3)</sup>	P_4.3.15

1) not subject to production test, specified by design

2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified  $R_{thJA}$  value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 1 copper layer (1 x 70µm Cu).

## 5 Block Description and Electrical Characteristics

### 5.1 Voltage Regulator

The output voltage  $V_Q$  is controlled by comparing a portion of it to an internal reference and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor  $C_Q$ , the load current, the chip temperature and the poles/zeros introduced by the integrated circuit. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the table **"Functional Range" on Page 12** have to be maintained. For details see also the typical performance graph **"Output Capacitor Series Resistor ESR( $C_Q$ ) versus Output Current  $I_Q$ " on Page 17**. As the output capacitor also has to buffer load steps it should be sized according to the application's needs.

An input capacitor  $C_I$  is strongly recommended to compensate line influences. Connect the capacitors close to the component's terminals.

A protection circuitry prevents the IC as well as the application from destruction in case of catastrophic events. These safeguards contain an output current limitation, a reverse polarity protection as well as a thermal shutdown in case of overtemperature.

To avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at input voltages above  $V_I = 22\text{ V}$ .

The overtemperature shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behaviour of the output voltage until the fault is removed. However, junction temperatures above  $150\text{ °C}$  are outside the maximum ratings and therefore significantly reduce the IC's lifetime.

The TLE42994 allows a negative supply voltage. In this fault condition, small currents are flowing into the IC, increasing its junction temperature. This has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity conditions.

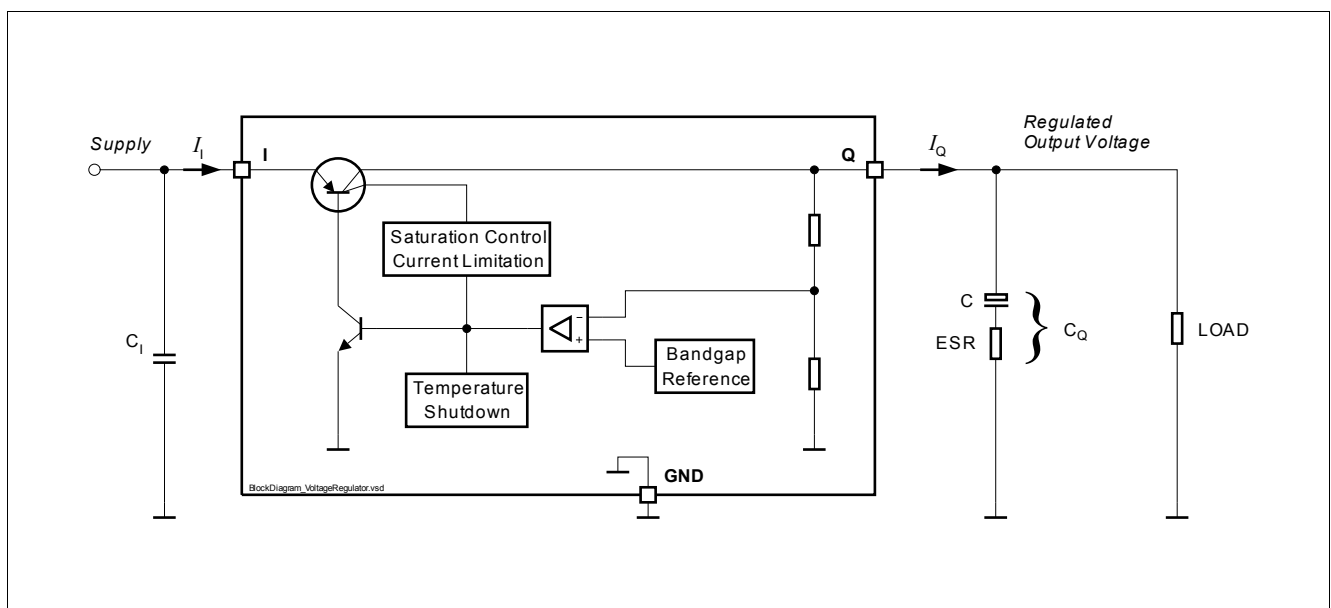


Figure 6 Voltage Regulator

## Block Description and Electrical Characteristics

**Table 4 Electrical Characteristics Voltage Regulator**

$V_I = 13.5 \text{ V}$ ,  $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Voltage	$V_Q$	4.9	5.0	5.1	V	$100 \mu\text{A} < I_Q < 100 \text{ mA}$ $6 \text{ V} < V_I < 18 \text{ V}$	P_5.1.1
Output Voltage	$V_Q$	4.85	5.0	5.15		$100 \mu\text{A} < I_Q < 150 \text{ mA}$ $6 \text{ V} < V_I < 18 \text{ V}$	P_5.1.2
Output Current Limitation	$I_{Q,\text{max}}$	150	400	500	mA	$V_Q = 4.8 \text{ V}$	P_5.1.3
Load Regulation steady-state	$\Delta V_{Q,\text{load}}$	-30	-5	—	mV	$I_Q = 1 \text{ mA to } 100 \text{ mA}$ $V_I = 6 \text{ V}$	P_5.1.4
Line Regulation steady-state	$\Delta V_{Q,\text{line}}$	—	10	25	mV	$V_I = 6 \text{ V to } 32 \text{ V}$ $I_Q = 1 \text{ mA}$	P_5.1.5
Dropout Voltage <sup>1)</sup> $V_{\text{dr}} = V_I - V_Q$	$V_{\text{dr}}$	—	220	500	mV	$I_Q = 100 \text{ mA}$	P_5.1.6
Overtemperature Shutdown Threshold	$T_{j,\text{sd}}$	151	—	200	°C	$T_j$ increasing <sup>2)</sup>	P_5.1.7
Overtemperature Shutdown Threshold Hysteresis	$T_{j,\text{sdh}}$	—	15	—	°C	$T_j$ decreasing <sup>2)</sup>	P_5.1.8
Power Supply Ripple Rejection <sup>3)</sup>	$PSRR$	—	66	—	dB	$f_{\text{ripple}} = 100 \text{ Hz}$ $V_{\text{ripple}} = 1 \text{ Vpp}$ $I_Q = 100 \text{ mA}$	P_5.1.9

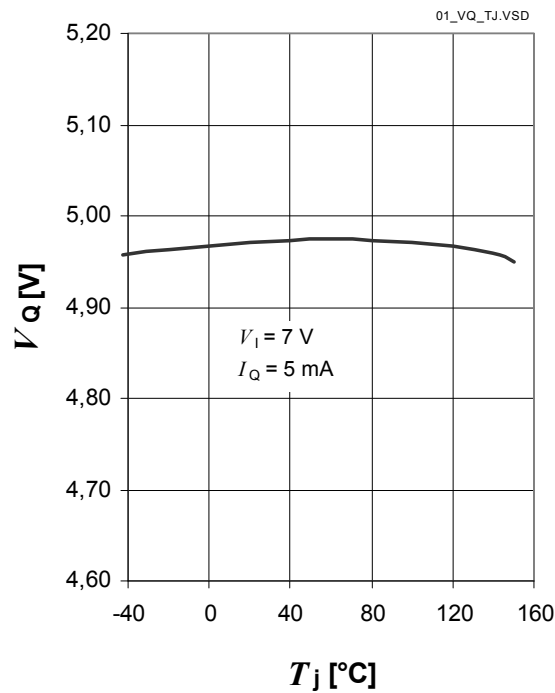
1) measured when the output voltage  $V_Q$  has dropped 100 mV from the nominal value obtained at  $V_I = 13.5 \text{ V}$

2) not subject to production test, specified by design

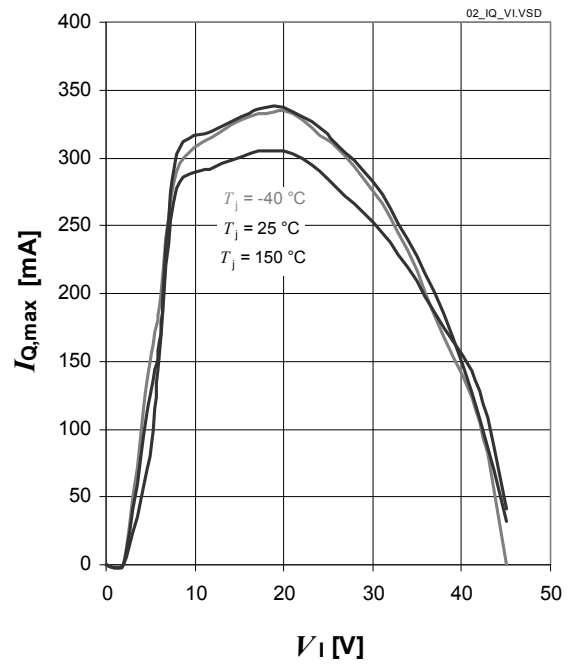
3) not subject to production test, specified by design

## 5.2 Typical Performance Characteristics Voltage Regulator

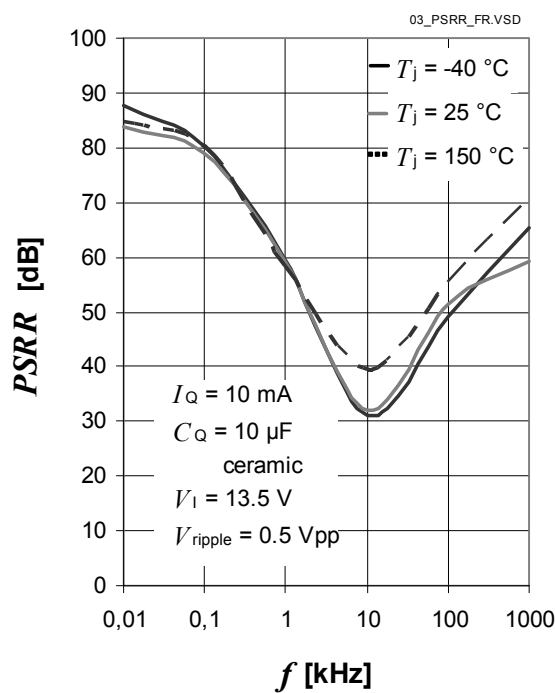
Output Voltage  $V_Q$  versus  
Junction Temperature  $T_J$



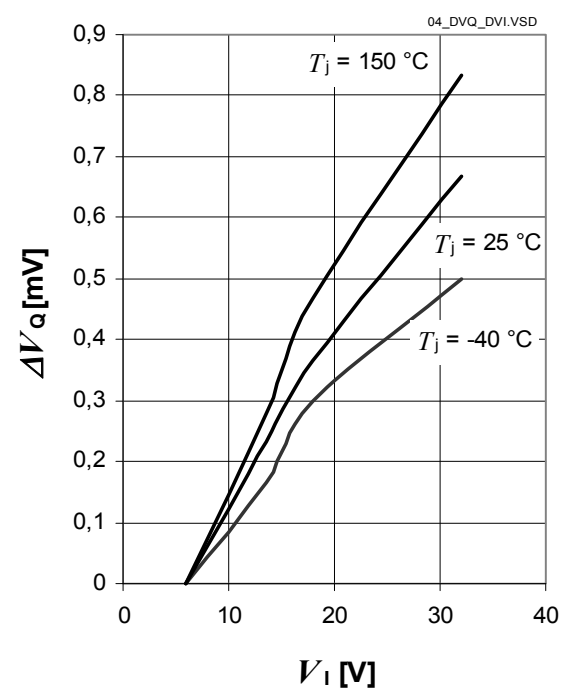
Output Current  $I_Q$  versus  
Input Voltage  $V_I$



Power Supply Ripple Rejection  $PSRR$  versus  
ripple frequency  $f_r$



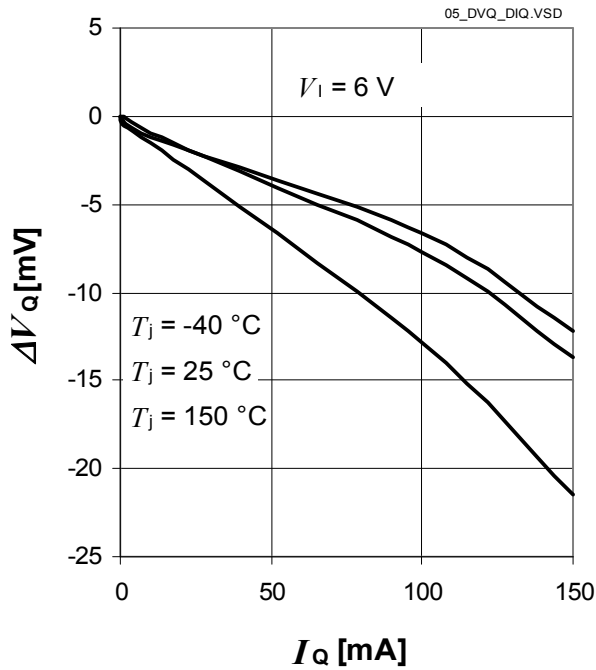
Line Regulation  $\Delta V_{Q,\text{line}}$  versus  
Input Voltage Change  $\Delta V_I$



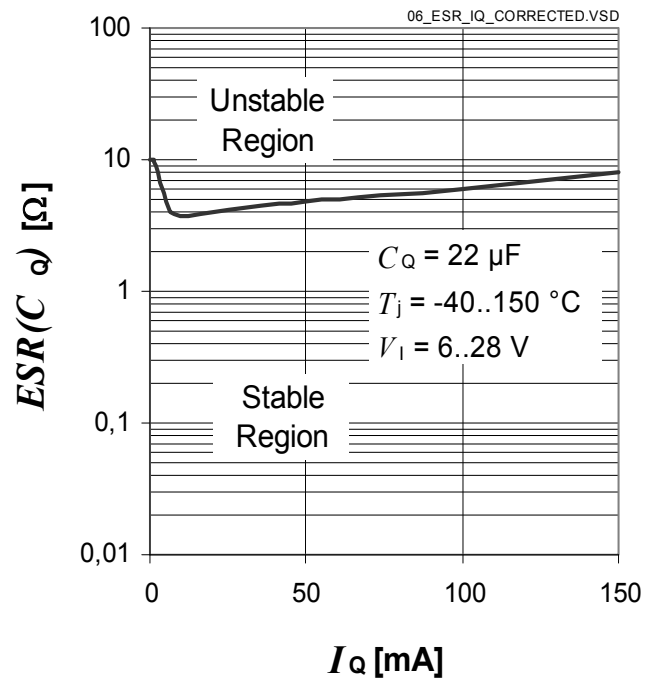


# Block Description and Electrical Characteristics

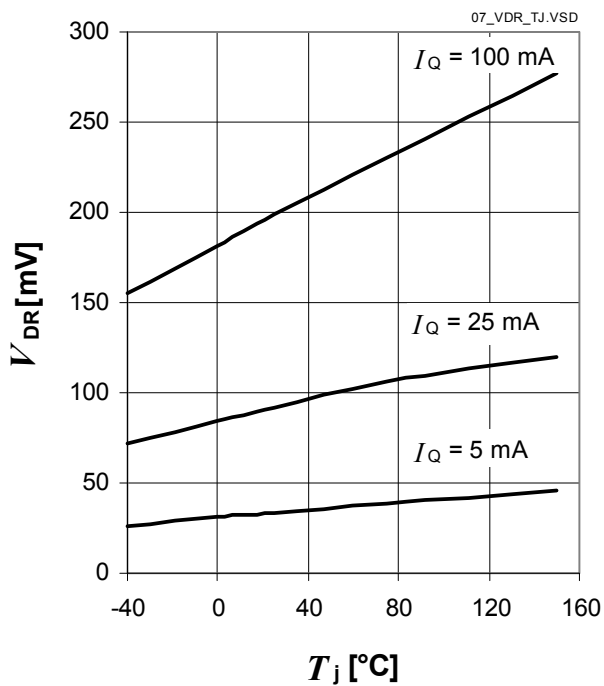
**Load Regulation  $\Delta V_{Q,load}$  versus Output Current Change  $\Delta I_Q$**



**Output Capacitor Series Resistor  $ESR(C_Q)$  versus Output Current  $I_Q$**



**Dropout Voltage  $V_{dr}$  versus Junction Temperature  $T_j$**



### 5.3 Current Consumption

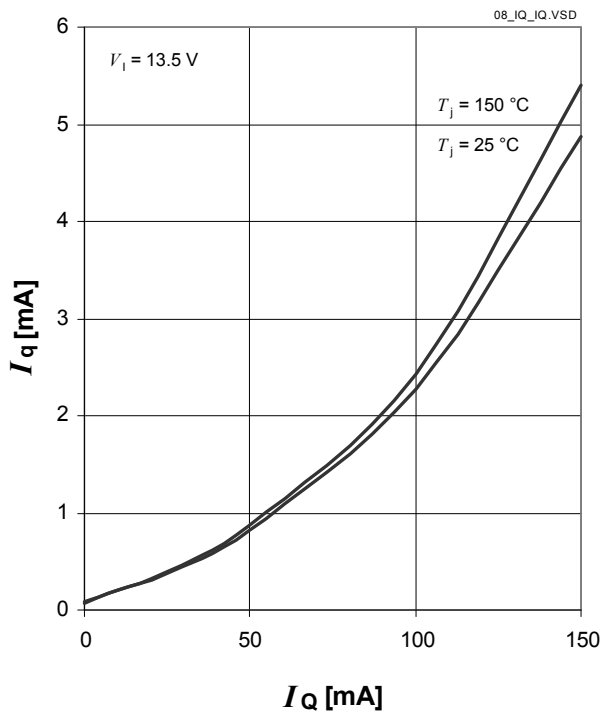
**Table 5 Electrical Characteristics Voltage Regulator**

$V_I = 13.5 \text{ V}$ ,  $-40 \text{ }^\circ\text{C} \leq T_j \leq 150 \text{ }^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

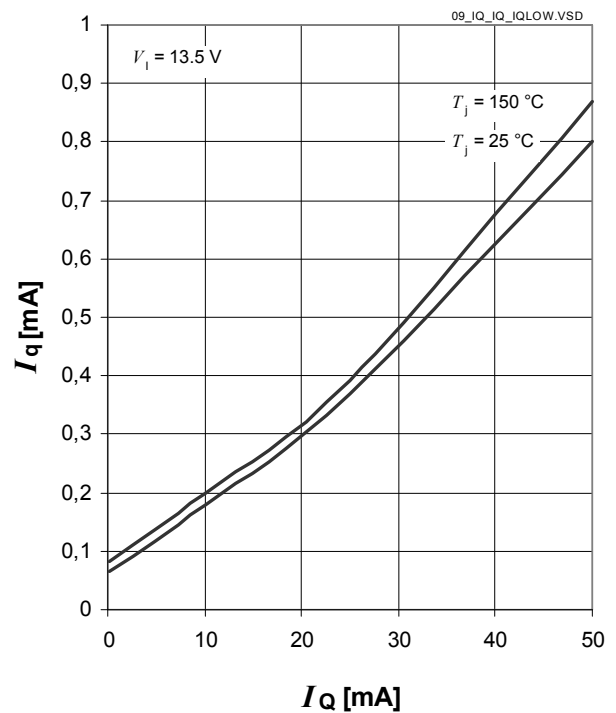
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption $I_q = I_I - I_Q$	$I_q$	–	–	1	$\mu\text{A}$	$V_{\text{EN}} = 0 \text{ V}$ TLE42994GM and TLE42994E only $T_j = 25 \text{ }^\circ\text{C}$	P_5.4.1
Current Consumption $I_q = I_I - I_Q$	$I_q$	–	65	100	$\mu\text{A}$	Enable HIGH $I_Q = 100 \text{ } \mu\text{A}$ , $T_j = 25 \text{ }^\circ\text{C}$	P_5.4.2
Current Consumption $I_q = I_I - I_Q$	$I_q$	–	65	105	$\mu\text{A}$	Enable HIGH $I_Q = 100 \text{ } \mu\text{A}$ , $T_j \leq 85 \text{ }^\circ\text{C}$	P_5.4.3
Current Consumption $I_q = I_I - I_Q$	$I_q$	–	0.17	0.5	$\text{mA}$	Enable HIGH $I_Q = 10 \text{ mA}$	P_5.4.4
Current Consumption $I_q = I_I - I_Q$	$I_q$	–	0.7	2	$\text{mA}$	Enable HIGH $I_Q = 50 \text{ mA}$	P_5.4.5

## 5.4 Typical Performance Characteristics Current Consumption

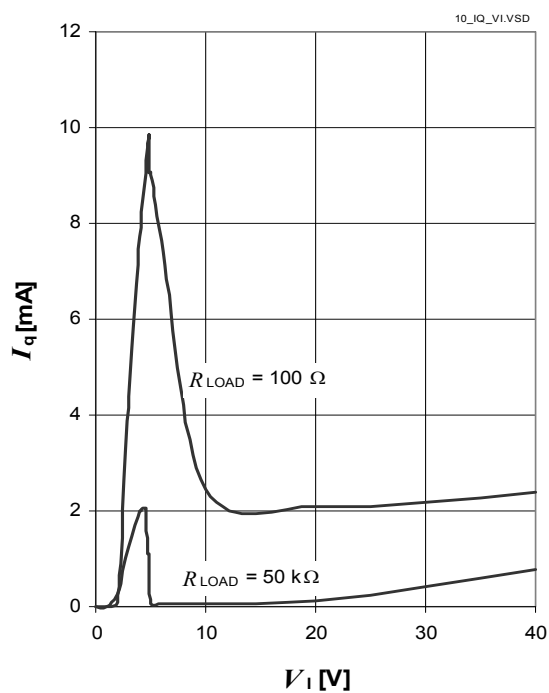
Current Consumption  $I_q$  versus Output Current  $I_Q$



Current Consumption  $I_q$  versus Output Current  $I_Q$  ( $I_Q$  low)



Current Consumption  $I_q$  versus Input Voltage  $V_I$



## 5.5 Enable Function (only TLE42994GM and TLE42994E)

**Table 6 Electrical Characteristics Voltage Regulator**

$V_I = 13.5 \text{ V}$ ,  $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Enable OFF Voltage Range	$V_{\text{EN,OFF}}$	–	–	0.8	V	–	P_5.6.1
Enable ON Voltage Range	$V_{\text{EN,ON}}$	3.5	–	–	V	–	P_5.6.2
Enable OFF Input Current	$I_{\text{EN,OFF}}$	–	0.5	2	$\mu\text{A}$	$V_{\text{EN}} = 0 \text{ V}$	P_5.6.3
Enable ON Input Current	$I_{\text{EN,ON}}$	–	3	5	$\mu\text{A}$	$V_{\text{EN}} = 5 \text{ V}$	P_5.6.4

## 5.6 Reset Function

The reset function provides several features:

### Output Undervoltage Reset:

An output undervoltage condition is indicated by setting the Reset Output RO to “low”. This signal might be used to reset a microcontroller during low supply voltage.

### Power-On Reset Delay Time:

The power-on reset delay time  $t_{rd}$  allows a microcontroller and oscillator to start up. This delay time is the time frame from exceeding the reset switching threshold  $V_{RT}$  until the reset is released by switching the reset output “RO” from “low” to “high”. The power-on reset delay time  $t_{rd}$  is defined by an external delay capacitor  $C_D$  connected to pin D charged by the delay capacitor charge current  $I_{D,ch}$  starting from  $V_D = 0$  V.

If the application needs a power-on reset delay time  $t_{rd}$  different from the value given in [Power On Reset Delay Time](#), the delay capacitor’s value can be derived from the specified values in [Power On Reset Delay Time](#) and the desired power-on delay time:

(1)

$$C_D = \frac{t_{rd,new}}{t_{rd}} \times 100nF$$

with

- $C_D$ : capacitance of the delay capacitor to be chosen
- $t_{rd,new}$ : desired power-on reset delay time
- $t_{rd}$ : power-on reset delay time specified in this datasheet

For a precise calculation also take the delay capacitor’s tolerance into consideration.

### Reset Reaction Time:

The reset reaction time avoids that short undervoltage spikes trigger an unwanted reset “low” signal. The reset reaction time  $t_{rr}$  considers the internal reaction time  $t_{rr,int}$  and the discharge time  $t_{rr,d}$  defined by the external delay capacitor  $C_D$  (see typical performance graph for details). Hence, the total reset reaction time becomes:

(2)

$$t_{rr} = t_{rd,int} + t_{rr,d}$$

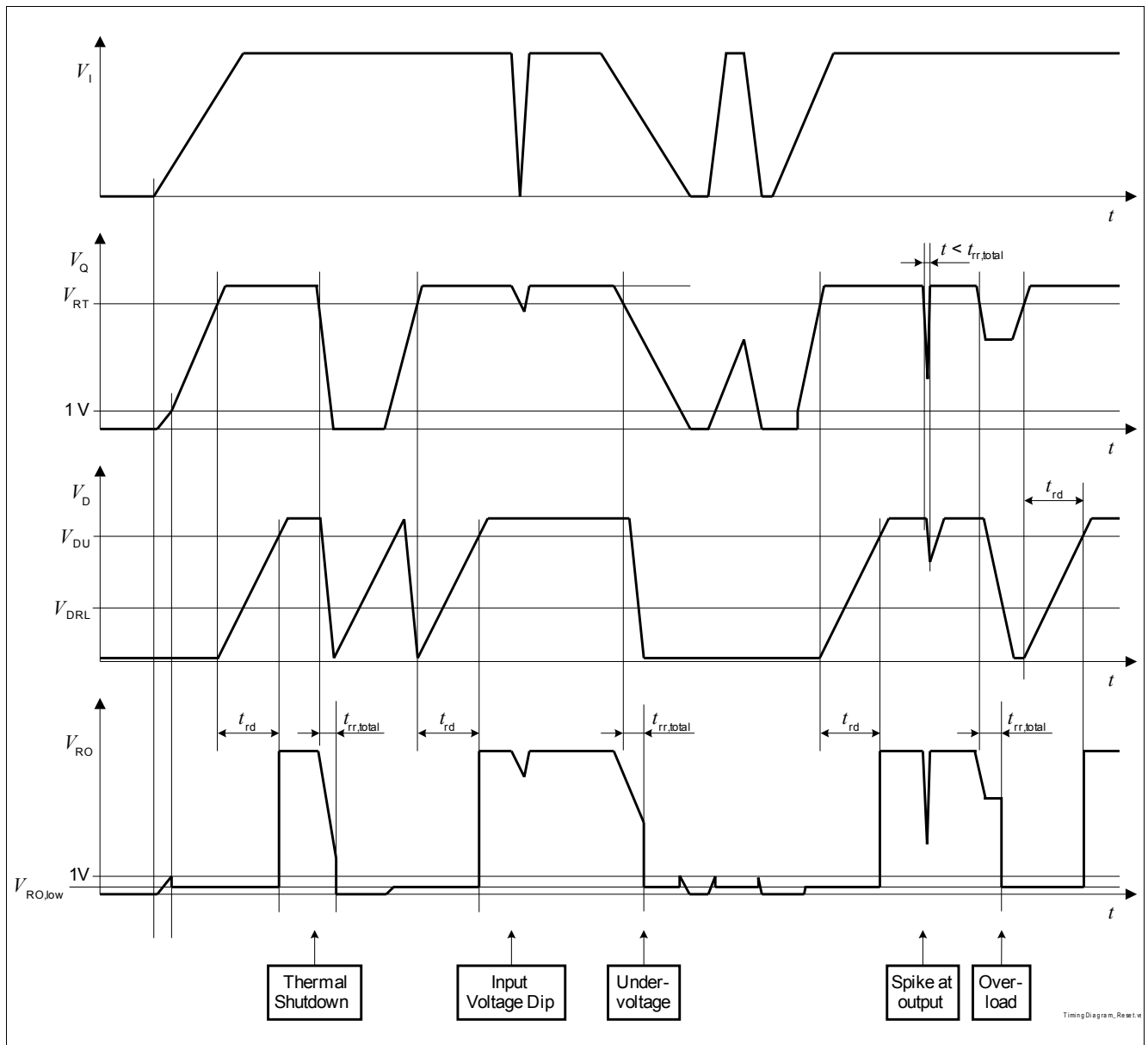
with

- $t_{rr}$ : reset reaction time
- $t_{rr,int}$ : internal reset reaction time
- $t_{rr,d}$ : reset discharge

### Optional Reset Output Pull-Up Resistor $R_{RO,ext}$ :

The Reset Output RO is an open collector output with an integrated pull-up resistor. If needed, an external pull-up resistor to the output Q can be added. In [Table 7 “Electrical Characteristics Reset Function” on Page 24](#) a minimum value for the external resistor  $R_{RO,ext}$  is given.





### Figure 8 Timing Diagram Reset

# Block Description and Electrical Characteristics

**Table 7 Electrical Characteristics Reset Function**

$V_I = 13.5 \text{ V}$ ,  $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Undervoltage Reset							
Default Output Undervoltage Reset Switching Thresholds	$V_{\text{RT}}$	4.5	4.65	4.8	V	$V_{\text{Q}}$ decreasing	P_5.7.1
Output Undervoltage Reset Threshold Adjustment							
Reset Adjust Switching Threshold	$V_{\text{RADJ,th}}$	1.26	1.36	1.44	V	$3.5\text{ V} \leq V_{\text{Q}} < 5\text{ V}$	P_5.7.2
Reset Adjustment Range <sup>1)</sup>	$V_{\text{RT,range}}$	3.50	–	4.65	V	–	P_5.7.3
Reset Output RO							
Reset Output Low Voltage	$V_{\text{RO,low}}$	–	0.1	0.4	V	$1\text{ V} \leq V_{\text{Q}} \leq V_{\text{RT}}$ no external $R_{\text{RO,ext}}$	P_5.7.4
Reset Output Internal Pull-up Resistor to $V_{\text{Q}}$	$R_{\text{RO}}$	10	20	40	kΩ	–	P_5.7.5
Optional Reset Output External Pull-up Resistor to $V_{\text{Q}}$	$R_{\text{RO,ext}}$	5.6	–	–	kΩ	$1\text{ V} \leq V_{\text{Q}} \leq V_{\text{RT}}$ ; $V_{\text{RO}} \leq 0.4\text{ V}$	P_5.7.6
Reset Delay Timing							
Delay Pin Output Voltage	$V_{\text{D}}$	–	–	5	V	–	P_5.7.7
Power On Reset Delay Time	$t_{\text{rd}}$	17	28	35	ms	$C_{\text{D}} = 100\text{ nF}$ Calculated Value: $t_{\text{rd}} = C_{\text{D}} * V_{\text{DU}} / I_{\text{D,ch}}$	P_5.7.8
Upper Delay Switching Threshold	$V_{\text{DU}}$	–	1.85	–	V	–	P_5.7.9
Lower Delay Switching Threshold	$V_{\text{DL}}$	–	0.50	–	V	–	P_5.7.10
Delay Capacitor Charge Current	$I_{\text{D,ch}}$	–	8.0	–	μA	$V_{\text{D}} = 1\text{ V}$	P_5.7.11
Delay Capacitor Reset Discharge Current	$I_{\text{D,dch}}$	–	70	–	mA	$V_{\text{D}} = 1\text{ V}$	P_5.7.12
Delay Capacitor Discharge Time	$t_{\text{rr, d}}$	–	1.9	3	μs	Calculated Value: $t_{\text{rr, d}} = C_{\text{D}} * (V_{\text{DU}} - V_{\text{DL}}) / I_{\text{D,dch}}$ $C_{\text{D}} = 100\text{ nF}$	P_5.7.13
Internal Reset Reaction Time	$t_{\text{rr, int}}$	–	14	20	μs	$C_{\text{D}} = 0\text{ nF}$ <sup>2)</sup>	P_5.7.14
Reset Reaction Time	$t_{\text{rr, total}}$	–	15.9	23	μs	Calculated Value: $t_{\text{rr, total}} = t_{\text{rr, int}} + t_{\text{rr,d}}$ $C_{\text{D}} = 100\text{ nF}$	P_5.7.15

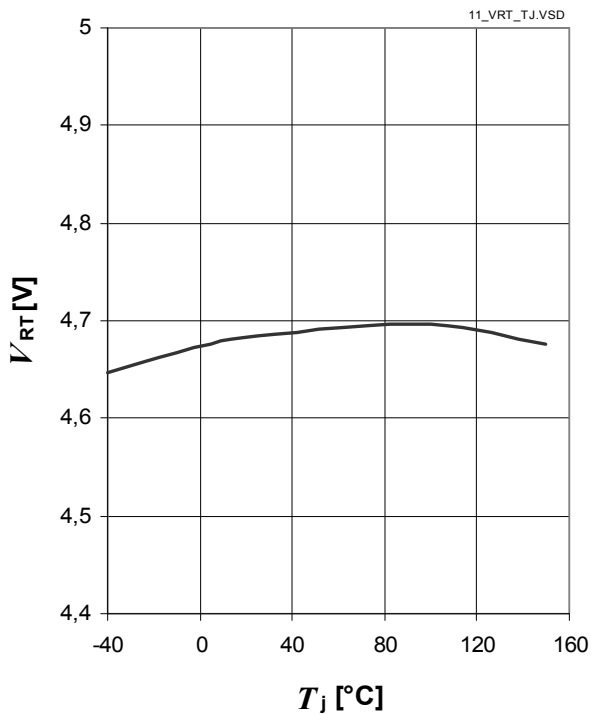
1)  $V_{RT}$  is scaled linearly, in case the Reset Switching Threshold is modified

2) parameter not subject to production test; specified by design

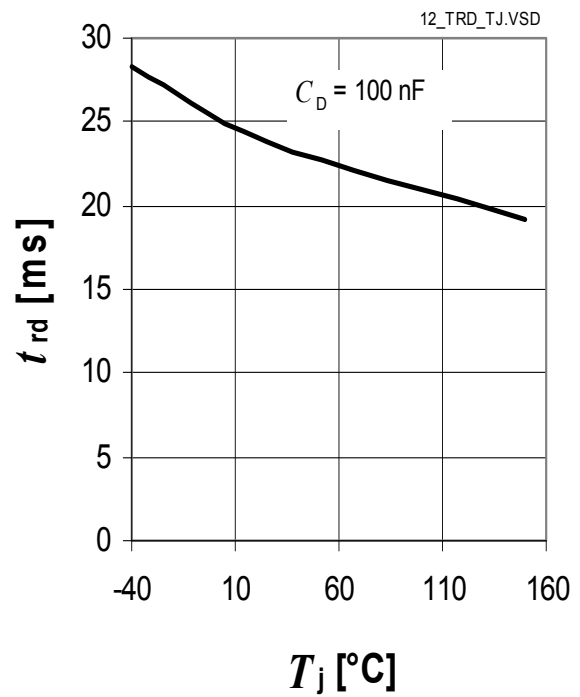


## 5.7 Typical Performance Characteristics Reset

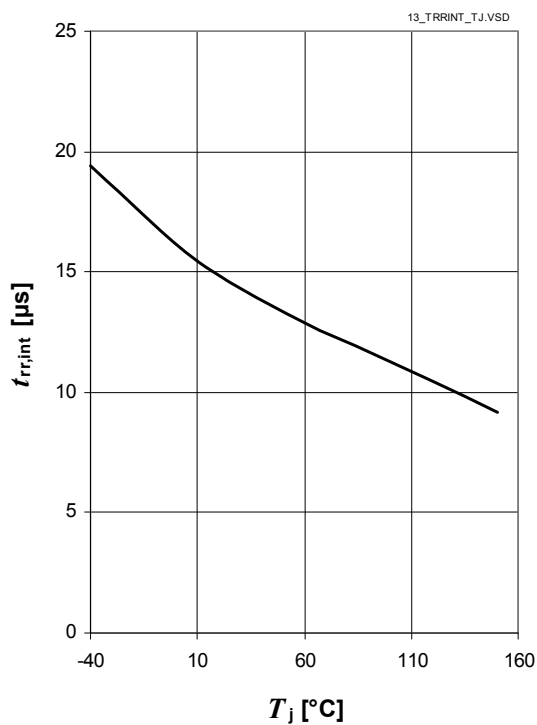
Undervoltage Reset Switching Threshold  $V_{RT}$  versus Junction Temperature  $T_j$



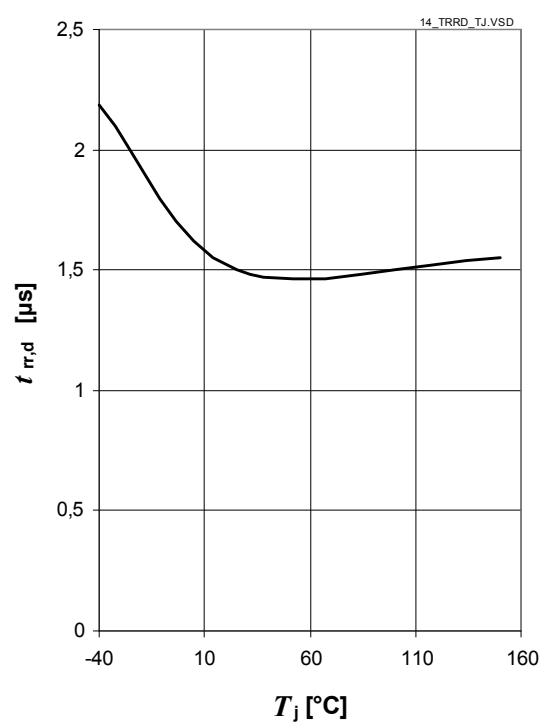
Power On Reset Delay Time  $t_{rd}$  versus Junction Temperature  $T_j$



Internal Reset Reaction Time  $t_{rr,int}$  versus Junction Temperature  $T_j$

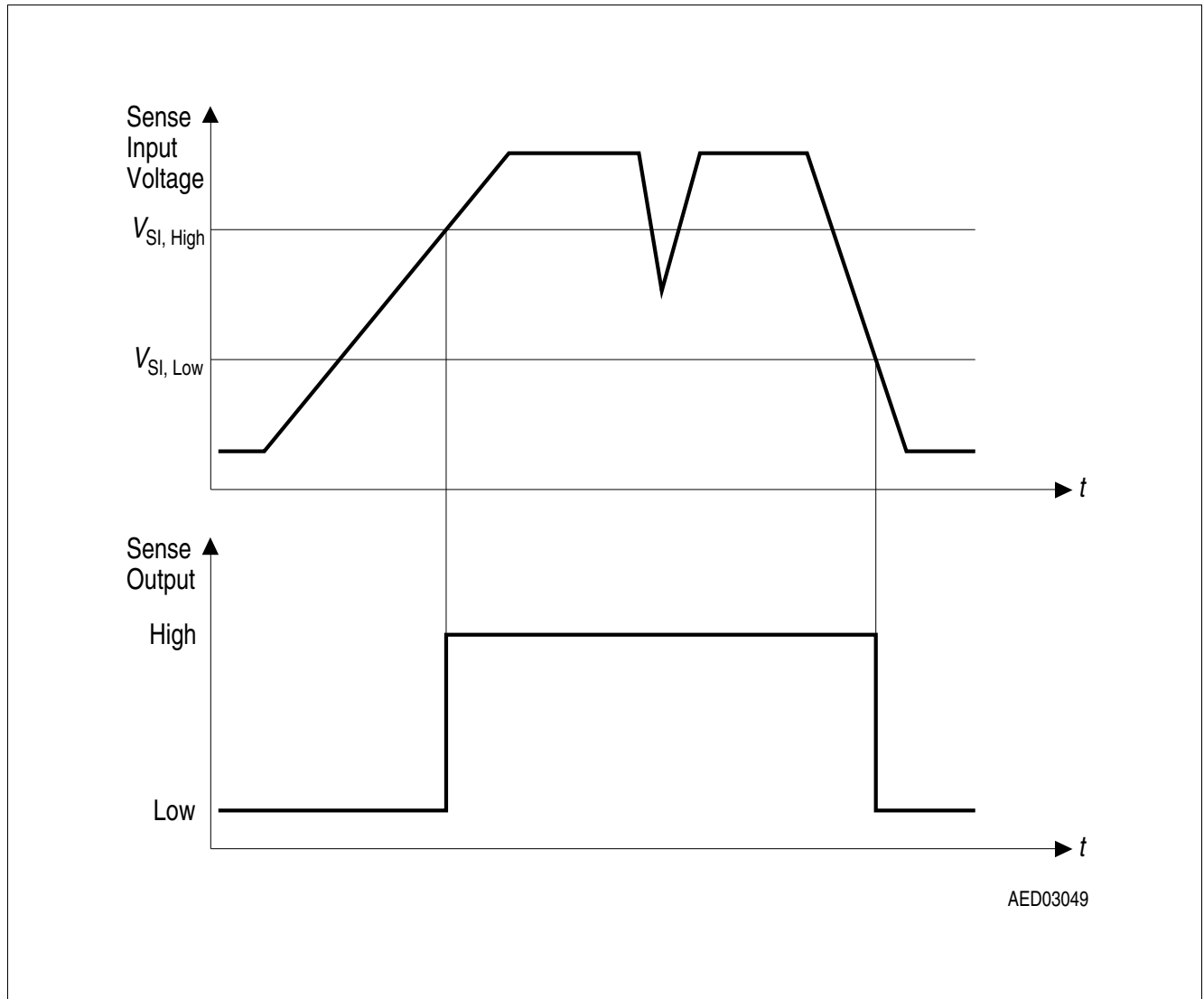


Delay Capacitor Discharge Time  $t_{rr,d}$  versus Junction Temperature  $T_j$



## 5.8 Early Warning Function

The additional sense comparator provides an early warning function: Any voltage (e.g. the input voltage) can be monitored, an undervoltage condition is indicated by setting the comparator's output to low.



**Figure 9 Sense Timing Diagram**

**Table 8 Electrical Characteristics Early Warning Function**

$V_I = 13.5 \text{ V}$ ,  $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Sense Comparator Input							
Sense Threshold High	$V_{SI,high}$	1.34	1.45	1.54	V	–	P_5.9.1
Sense Threshold Low	$V_{SI,low}$	1.26	1.36	1.44	V	–	P_5.9.2
Sense Switching Hysteresis	$V_{SI,hy}$	50	90	130	mV	$V_{SI,hy} = V_{SI,high} - V_{SI,low}$	P_5.9.3
Sense Input Current	$I_{SI}$	-1	-0.1	1	μA	–	P_5.9.4

## Block Description and Electrical Characteristics

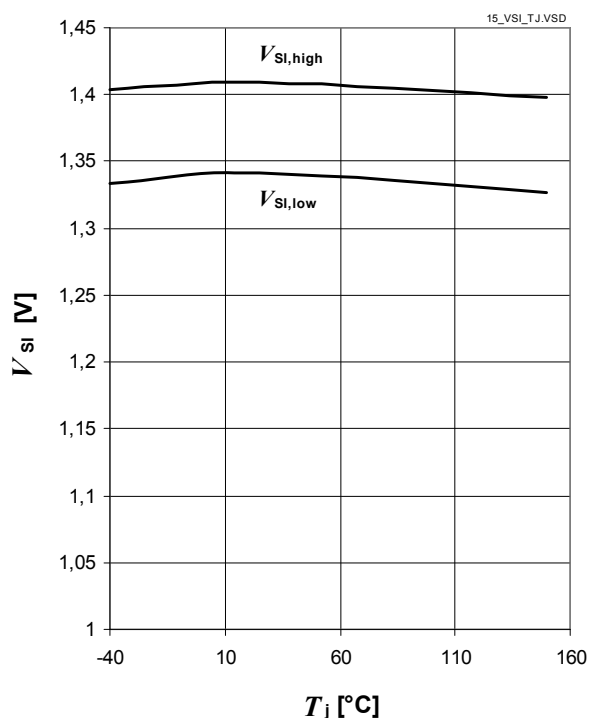
**Table 8 Electrical Characteristics Early Warning Function** (cont'd)

$V_I = 13.5 \text{ V}$ ,  $-40 \text{ }^\circ\text{C} \leq T_j \leq 150 \text{ }^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Sense Comparator Output							
Sense Output Low Voltage	$V_{SO,low}$	–	0.1	0.4	V	$V_{SI} < V_{SI,low}$ $V_I > 5.5\text{ V}$ no external $R_{SO,ext}$	P_5.9.5
Sense Output Internal Pull-up Resistor to $V_Q$	$R_{SO}$	10	20	40	k $\Omega$	–	P_5.9.6
Optional Sense Output External Pull-up Resistor to $V_Q$	$R_{SO,ext}$	5.6	–	–	k $\Omega$	$V_I > 5.5\text{ V}$ $V_{SO} \leq 0.4\text{ V}$	P_5.9.7

## 5.9 Typical Performance Characteristics Early Warning

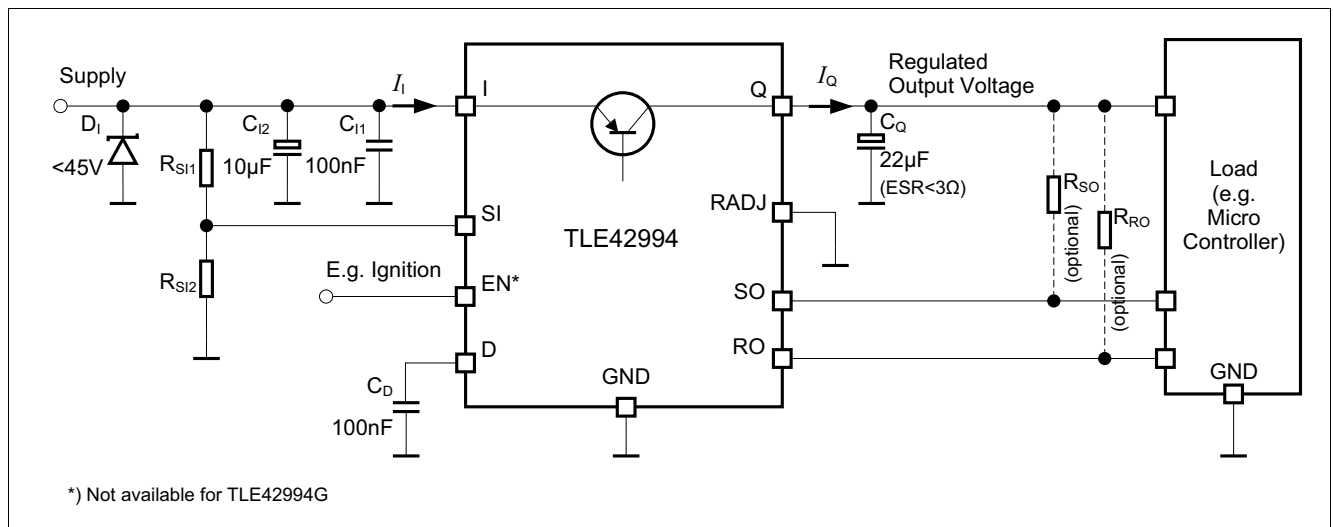
**Sense Thresholds  $V_{SI,high}$ ,  $V_{SI,low}$  versus Junction Temperature  $T_j$**



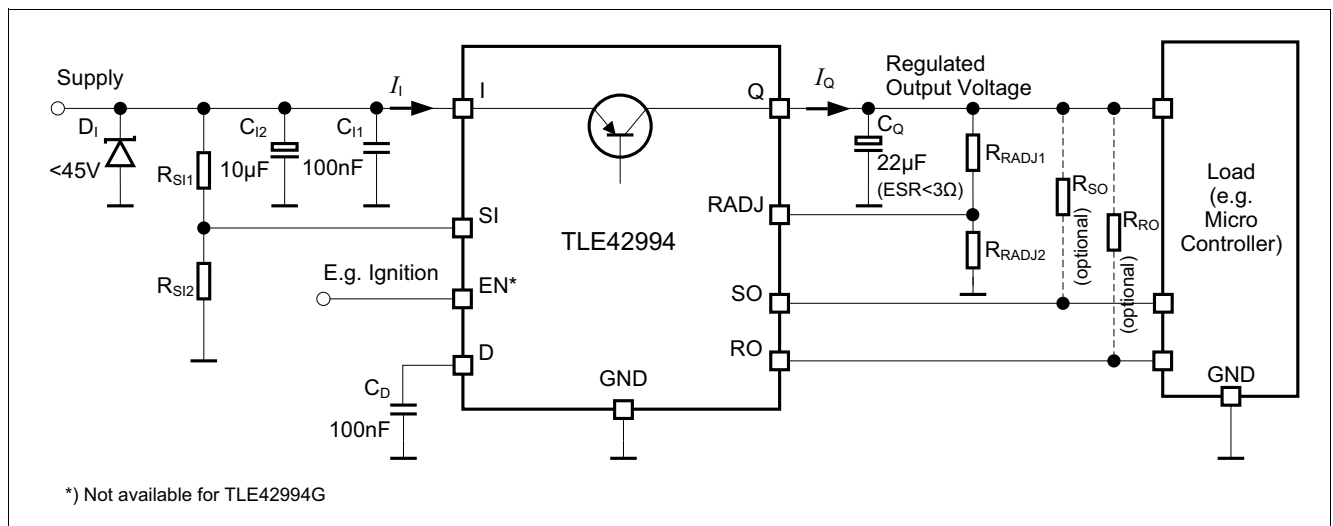
## 6 Application Information

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

### 6.1 Application Diagram



**Figure 10 Application Diagram with Selecting Default Reset Thresholds**



**Figure 11 Application Diagram with Reset Thresholds Adjustment**

## 6.2 Selection of External Components

### 6.2.1 Input Pin

The typical input circuitry for a linear voltage regulator is shown in the application diagram above.

A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line e.g. ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10  $\mu$ F to 470  $\mu$ F is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to over-voltage.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in case of possible external disturbances.

### 6.2.2 Output Pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in **“Functional Range” on Page 12**. The graph **“Output Capacitor Series Resistor ESR( $C_O$ ) versus Output Current  $I_O$ ” on Page 17** shows the stable operation range of the device.

TLE42994 is designed to be stable with extremely low ESR capacitors. According to the automotive environment, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator's output and GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

### 6.3 Thermal Considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (4)$$

with

- $P_D$ : continuous power dissipation
- $V_I$ : input voltage
- $V_Q$ : output voltage
- $I_Q$ : output current
- $I_q$ : quiescent current

The maximum acceptable thermal resistance  $R_{thJA}$  can then be calculated:

$$R_{thJA, max} = \frac{T_{j, max} - T_a}{P_D} \quad (5)$$

with

- $T_{j, max}$ : maximum allowed junction temperature
- $T_a$ : ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in [“Thermal Resistance” on Page 13](#).

#### Example

Application conditions:

$$V_I = 13.5 \text{ V}$$

$$V_Q = 5 \text{ V}$$

$$I_Q = 50 \text{ mA}$$

$$T_a = 125 \text{ °C}$$

Calculation of  $R_{thJA, max}$ :

$$\begin{aligned} P_D &= (V_I - V_Q) \cdot I_Q + V_I \cdot I_q \\ &= (13.5 \text{ V} - 5 \text{ V}) \cdot 50 \text{ mA} + 13.5 \text{ V} \cdot 2 \text{ mA} \\ &= 0.425 \text{ W} + 0.027 \text{ W} \\ &= 0.452 \text{ W} \end{aligned}$$

$$\begin{aligned} R_{thJA, max} &= (T_{j, max} - T_a) / P_D \\ &= (150 \text{ °C} - 125 \text{ °C}) / 0.452 \text{ W} \\ &= 55.3 \text{ K/W} \end{aligned}$$

As a result, the PCB design must ensure a thermal resistance  $R_{thJA}$  lower than 55.3 K/W. By considering TLE42994E (PG-SSOP-14 EP package) and according to [“Thermal Resistance” on Page 13](#), at least 600 mm<sup>2</sup> heatsink area is needed on the FR4 1s0p PCB, or the FR4 2s2p board can be used.

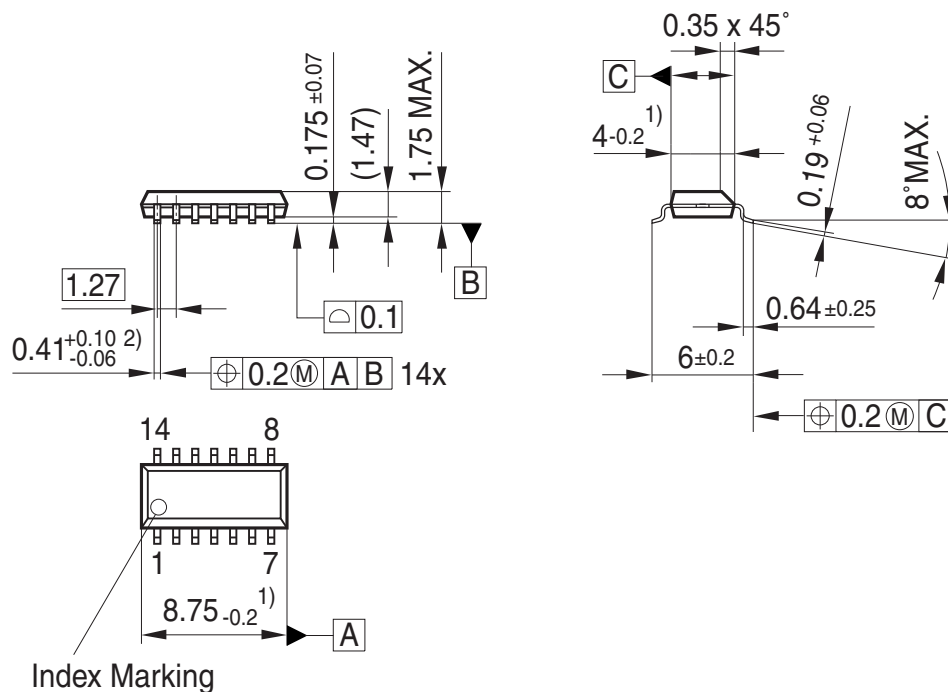
## 6.4 Reverse Polarity Protection

TLE42994 is self protected against reverse polarity faults and allows negative supply voltage. External reverse polarity diode is not needed. However, the absolute maximum ratings of the device as specified in **“Absolute Maximum Ratings” on Page 11** must be kept.

The reverse voltage causes several small currents to flow into the IC hence increasing its junction temperature. As the thermal shut down circuitry does not work in the reverse polarity condition, designers have to consider this in their thermal design.







GPS01230

Figure 13 PG-DSO-14



## 8 Revision History

Revision	Date	Changes
1.2	2014-07-03	Application information added. PG-SSOP-14 EP package outline updated.
1.1	2009-05-19	Updated version Data Sheet: Typing error corrected in <a href="#">Chapter 5.2</a> in conditions for graph “ <a href="#">Output Capacitor Series Resistor ESR(C<sub>O</sub>) versus Output Current I<sub>O</sub></a> ” on <a href="#">Page 17</a> : “10μF” corrected to “22μF”, no change done in specification of electrical parameters
1.0	2008-12-04	initial version Data Sheet

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