## Features

- Speech circuit with anti-clipping
- Tone-ringer interface with DC/DC converter
- Speaker amplifier with anti-distortion
- Power-supply management (regulated and unregulated) and a special supply for electret microphone
- Voice switch
- Interface for answering machine and cordless phone

## Applications

- Feature phone
- Answering machine
- Fax machine
- Speaker phone
- Cordless phone

## Benefits

- No piezoelectric transducer necessary for tone ringing
- Complete system integration of analog signal processing on one chip
- Very few external components

# 1. Description

The programmable telephone audio processor Atmel® U4091BM-R is a linear integrated circuit for use in feature phones, answering machines and fax machines. It contains the speech circuit, tone-ringer interface with DC/DC converter, sidetone equivalent and ear-protection rectifiers. The circuit is line-powered and contains all components necessary for signal amplification and adaptation to the line. The Atmel U4091BM-R can also be supplied via an external power supply. An integrated voice switch with loudspeaker amplifier enables hands-free or open-listening operation. With an anti-feedback function, acoustic feedback during open listening can be reduced significantly. The generated supply voltage is suitable for a wide range of peripheral circuits.
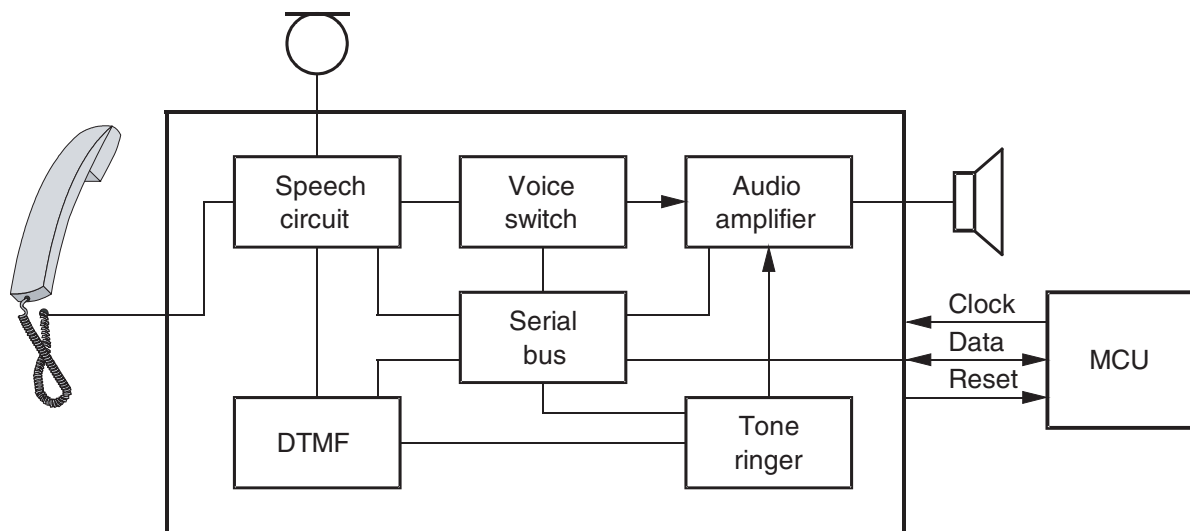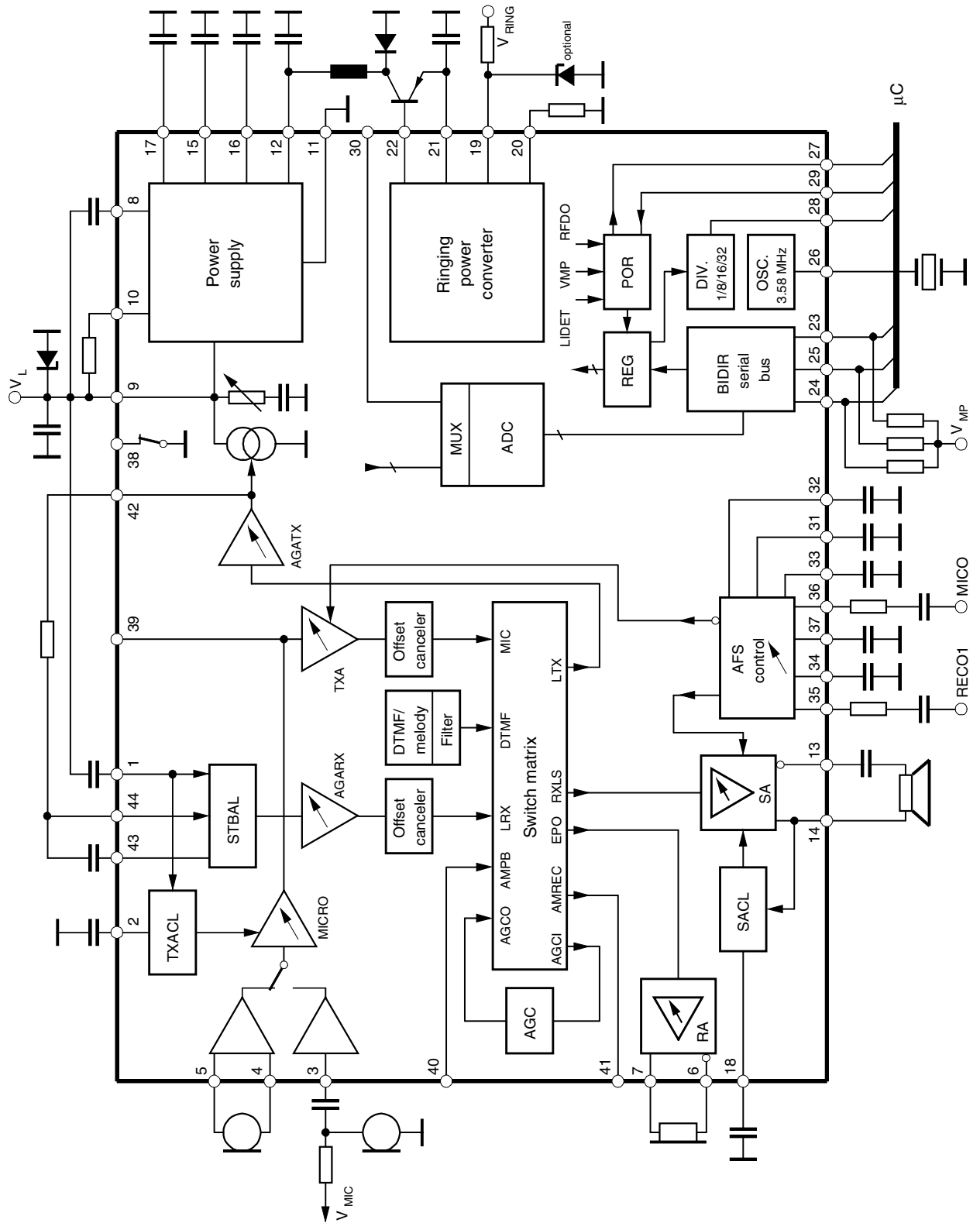
**Figure 1-1.   Block Diagram**

**Figure 1-2. Detailed Block Diagram**
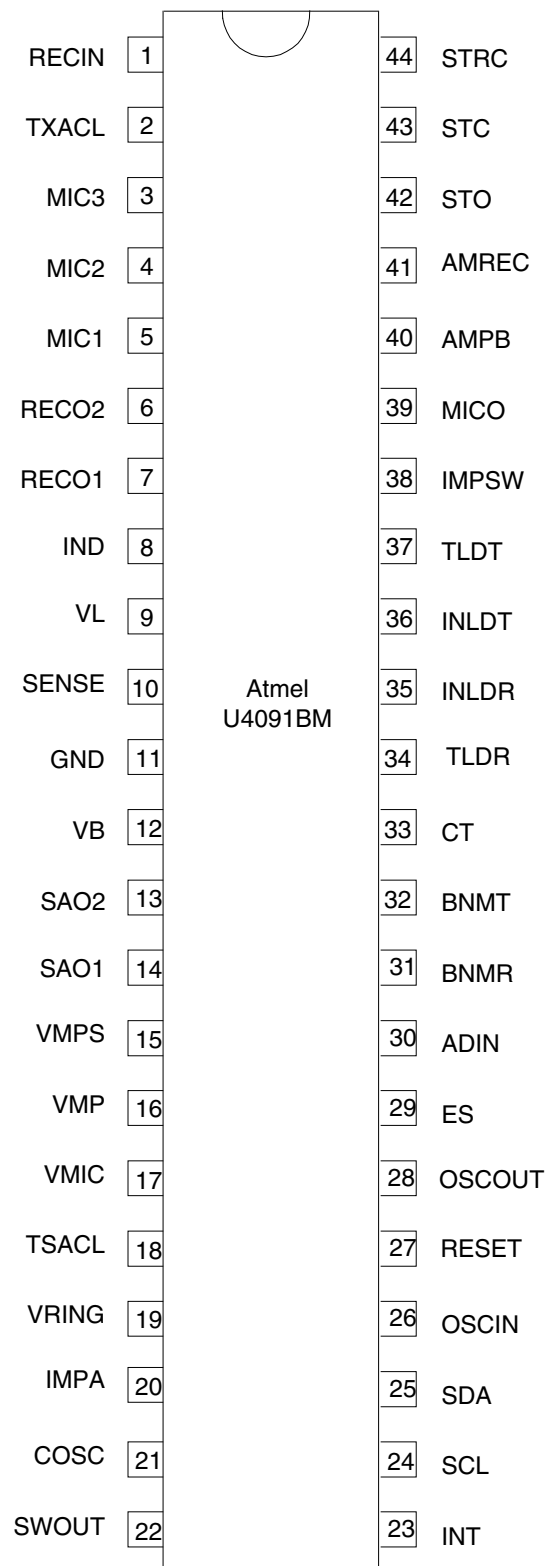
## 2. Pin Configuration

**Figure 2-1. Pinning SSO44**

| | | |
|---|---|---|
| RECIN | 1 | 44 | STRC |
| TXACL | 2 | 43 | STC |
| MIC3 | 3 | 42 | STO |
| MIC2 | 4 | 41 | AMREC |
| MIC1 | 5 | 40 | AMPB |
| RECO2 | 6 | 39 | MICO |
| RECO1 | 7 | 38 | IMPSW |
| IND | 8 | 37 | TLDT |
| VL | 9 | 36 | INLDT |
| SENSE | 10 | 35 | INLDR |
| GND | 11 | 34 | TLDR |
| VB | 12 | 33 | CT |
| SAO2 | 13 | 32 | BNMT |
| SAO1 | 14 | 31 | BNMR |
| VMPS | 15 | 30 | ADIN |
| VMP | 16 | 29 | ES |
| VMIC | 17 | 28 | OSCOUT |
| TSACL | 18 | 27 | RESET |
| VRING | 19 | 26 | OSCIN |
| IMPA | 20 | 25 | SDA |
| COSC | 21 | 24 | SCL |
| SWOUT | 22 | 23 | INT |

Atmel
U4091BM

**Table 2-1.    Pin Description**

| Pin | Symbol | Function |
|-----|--------|----------|
| 1 | RECIN | Receive amplifier input[1] |
| 2 | TXACL | Time constant adjustment for transmit anti-clipping |
| 3 | MIC3 | Microphone input for hands-free operation |
| 4 | MIC2 | Input of symmetrical microphone amplifier with high common-mode rejection ratio |
| 5 | MIC1 | Input of symmetrical microphone amplifier with high common-mode rejection ratio |
| 6 | RECO2 | Output of the receive amplifier |
| 7 | RECO1 | Output of the receive amplifier, also used for sidetone network |
| 8 | IND | The internal equivalent inductance of the circuit is proportional to the value of the capacitor at this pin. A resistor connected to ground may be used to adjust the DC mask |
| 9 | VL | Positive supply-voltage input to the device in speech mode |
| 10 | SENSE | Input for sensing the available line current |
| 11 | GND | Ground, reference point for DC and AC signals |
| 12 | VB | Unstabilized supply voltage for speech network |
| 13 | SAO2 | Negative output of speaker amplifier (push-pull only) |
| 14 | SAO1 | Positive output of speaker amplifier (single-ended and push-pull operation) |
| 15 | VMPS | Unregulated supply voltage for the microcontroller (via series regulator to VMP) |
| 16 | VMP | Regulated output voltage for supplying the microcontroller (typically 3.3V/6mA in speech mode) |
| 17 | VMIC | Reference node for microphone amplifier, supply for electret microphones |
| 18 | TSACL | Time constant for speaker amplifier anti-clipping |
| 19 | VRING | Input for ringer supply |
| 20 | IMPA | Input for adjusting the ringer input impedance |
| 21 | COSC | 70-kHz oscillator for ringing power converter |
| 22 | SWOUT | Output for driving the external switch resistor |
| 23 | INT | Interrupt line for serial bus |
| 24 | SCL | Clock input for serial bus |
| 25 | SDA | Data line for serial bus |
| 26 | OSCIN | Input for 3.58-MHz oscillator |
| 27 | RESET | Reset output for the microcontroller |
| 28 | OSCOUT | Clock output for the microcontroller |
| 29 | ES | Input for external supply indication |
| 30 | ADIN | Input of A/D converter |
| 31 | BNMR | Output of background-noise monitor receive |
| 32 | BNMT | Output of background-noise monitor transmit |
| 33 | CT | Time constant for mode switching of voice switch |
| 34 | TLDR | Time constant of receive-level detector |
| 35 | INLDR | Input of receive-level detector |
| 36 | INLDT | Input of transmit-level detector |
| 37 | TLDT | Time constant of transmit-level detector |
| 38 | IMPSW | Switch for additional line impedance |
| 39 | MICO | Microphone preamplifier output |
| 40 | AMPB | Input for playback signal of answering machine |

Note:    1.  The protection device at pin RECIN is disconnected.

**Table 2-1.    Pin Description (Continued)**

| Pin | Symbol | Function |
|-----|--------|----------|
| 41 | AMREC | Output for recording signal of answering machine |
| 42 | STO | Output for connecting the sidetone network |
| 43 | STC | Input for sidetone network |
| 44 | STRC | Input for sidetone network |

Note:    1.  The protection device at pin RECIN is disconnected.

# 3.    DC Line Interface and Supply-voltage Generation

The DC line interface consists of an electronic inductance and a dual-port output stage which charges the capacitors at VMPS and VB. The value of the equivalent inductance is given by:

$$L = \frac{2 \times R_{SENSE} \times C_{IND} \times (R_{DC} \times R_{30})}{(R_{DC} + R_{30})}$$

The U4091BM-R contains two identical series regulators which provide a supply voltage VMP of 3.3V suitable for a microprocessor. In speech mode, both regulators are active because VMPS and VB are charged simultaneously by the DC line interface. The output current is 6mA. The capacitor at VMPS is used to provide the microcomputer with sufficient power during long line interruptions. Thus, long flash pulses can be bridged or an LCD display can be turned on for more than 2 seconds after going on-hook. When the system is in ringing mode, VB is charged by the on-chip ringing power converter. In this mode, only one regulator is used to supply VMP with maximum 3mA.

# 4.  Supply Structure of the Chip

A main benefit of the Atmel® U4091BM is the easy implementation of various applications due to the flexible system structure of the chip.

Possible applications:

- Group listening phone
- Hands-free phone
- Phones which feature ringing with the built-in speaker amplifier
- Answering machine with external supply

The special supply topology for the various functional blocks is shown in .

There are four major supply states:

1. Speech condition
   In speech condition, the system is supplied by the line current. If the LIDET block detects a line voltage above approximately 2V, the internal signal VLON is activated. This is detected via the serial bus, all the blocks which are needed have to be switched on via the serial bus.
   For line voltages below 2V, the switches remain in quiescent state as shown in the diagram.

2. Power down (pulse dialing)
   When the chip is in power-down mode (bit LOMAKE), for example, during pulse dialing, all internal blocks are disabled via the serial bus. In this condition, the voltage regulators and their internal band gap are the only active blocks.

3. Ringing
   During ringing, the supply for the system is fed into VB via the Ringing Power Converter (RPC). Normally, the speaker amplifier in single-ended mode is used for ringing. The frequency for the melody is generated by the DTMF/Melody generator.

4. External supply
   In an answering machine, the chip is powered by an external supply via pin VB. The answering machine connections can be directly made to Atmel U4091BM-R. The answering machine is connected to the pin AMREC. For the output AMREC, an AGC function is selectable via the serial bus. The output of the answering machine will be connected to the pin AMPB, which is directly connected to the switching matrix. This enables the signal to be switched to every desired output.

**Figure 4-1.   Supply Generator**
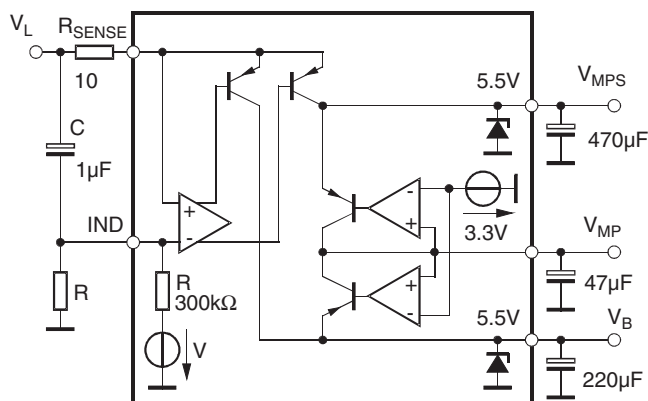
## 5. Ringing Power Converter (RPC)

The RPC transforms the input power at VRING (high voltage/low current) into an equivalent output power at VB (low voltage/high current) which is capable of driving the low-ohmic loudspeaker. The input impedance at VRING is adjustable from 3k$\Omega$ to 12k$\Omega$ by $R_{IMPA}$ ($Z_{RING}$ = $R_{IMPA}$ / 100) and the efficiency of the step-down converter is approximately 65%.

## 6. Ringing Frequency Detector (RFD)

The Atmel[®] U4091BM-R provides an output signal for the microcontroller. This output signal is always double the value of the input signal (ringing frequency). It is generated by a current comparator with hysteresis. The levels for the on-threshold are programmable in 16 steps, the off-level is fixed. Every change of the comparator output generates a high level at the interrupt output INT. The information can then be read out by means of a serial bus with either normal or fast read mode. The block RFD is always enabled.

**Table 6-1.    Threshold Level**

| RINGTH[0:3] | $V_{RING}$ |
|---|---|
| 0 | 7V |
| 15 | 22V |
| Step | 1V |

## 7. Clock Output Divider Adjustment

The pin OSCOUT is a clock output which is derived from the crystal oscillator. It can be used to drive a microcontroller or another remote component and thereby reduces the number of crystals required. The oscillator frequency can be divided by 1, 8, 16, or 32. During power-on reset, the divider will be reset to 1 until it is changed by setting the serial bus.

**Table 7-1.    Clock Output**

| CLK[0:1] | Divider | Frequency |
|---|---|---|
| 0 | 1 | 3.58MHz |
| 1 | 8 | 447kHz |
| 2 | 16 | 224kHz |
| 3 | 32 | 112kHz |

# 8. Serial Bus Interface

The circuit is controlled by an external microcontroller through the serial bus.

The serial bus is a bi-directional system consisting of a single-directional clock line (SCL) which is always driven by the microcontroller, and a bi-directional data-signal line. It is driven by the microcontroller as well as by the Atmel® U4091BM-R (see Figure 20-1 on page 37).

The serial bus requires external pull-up resistors as only pull-down transistors (pin SDA) are integrated.

## 8.1 WRITE

The data is a 12-bit word:

A0-A3: address of the destination register (0 to 15)
D0-D7: content of the register

The data line must be stable when the clock is high. Data must be shifted serially. After 12 clock periods, the write indication is sent. Then, the transfer to the destination register is (internally) generated by a strobe signal transition of the data line when the clock is high.

## 8.2 READ

There is a normal and a fast-read cycle.

In the normal read cycle, the microcontroller sends a 4-bit address followed by the read indicator, then an 8-bit word is read out. The Atmel U4091BM-R drives the data line.

The fast read cycle is indicated by a strobe signal. With the following two clocks the Atmel U4091BM-R reads out the status bits RFDO and LIDET which indicate that a ringing signal or a line signal is present (see Figure 10-1 on page 12, Figure 10-2 on page 12 and Figure 10-3 on page 12).

# 9. DTMF Dialing

The DTMF generator sends a multi-frequency signal through the matrix to the line. The signal is the result of the sum of two frequencies and is internally filtered. The frequencies are chosen from a low and a high frequency group. The circuit conforms to the CEPT recommendation concerning DTMF option. Three different levels for the low level group and two different pre-emphasis (2.5dB and 3.5dB) can be chosen by means of the serial bus (rec. T/CF 46-03).

**Attention:** In high gain mode, distortion can occur if AGATX is high and DC mask is low.

# 10. Melody and Confidence Tone Generation

Melody and confidence tone frequencies are given in Table 10-1.

The frequencies are provided at the DTMF input of the switch matrix. A sinusoidal wave, a square wave or a pulsed wave can be selected by the serial bus. A square signal means the output is high for half of the frequency cycle, and low for the other half. A pulsed signal means high impedance phases of 1/6 of the period occur between the high and low phases.

**Table 10-1.  Status of Melody Generating**

| Decimal | DTMFM[0:2] | Status |
|---------|------------|--------|
| 0 | 000 | DTMF generator OFF |
| 1 | 001 | Confidence tone melody on (sine) |
| 2 | 010 | Ringer melody (pulse) |
| 3 | 011 | Ringer melody (square signal) |
| 4 | 100 | DTMF (mid level) |
| 5 | 101 | DTMF (low level) |
| 6 | 110 | DTMF (high level) |
| 7 | 111 | – |

**Table 10-2.  DTMF Frequencies**

| Decimal | DTMFF[0:1] in DTMF Mode | Frequency | Error (%) |
|---------|-------------------------|-----------|-----------|
| 0 | 00 | 697 | –0.007 |
| 1 | 01 | 770 | –0.156 |
| 2 | 10 | 852 | 0.032 |
| 3 | 11 | 941 | 0.316 |

**Table 10-3.  DTMF Frequencies**

| Decimal | DTMFF[2:3] in DTMF Mode | Frequency | Error (%) |
|---------|-------------------------|-----------|-----------|
| 0 | 00 | 1209 | –0.110 |
| 1 | 01 | 1336 | 0.123 |
| 2 | 10 | 1477 | –0.020 |
| 3 | 11 | 1633 | –0.182 |

**Table 10-4.  DTMFF4 in DTMF Mode**

| Pre-emphasis Selection | Level |
|------------------------|-------|
| 0 | 2.5dB |
| 1 | 3.5dB |

**Table 10-5. DTMF and Melody Frequencies**

| Decimal | DTMFF [0:4] | f (Hz) | Tone/ Name | Error (%) | DTMF Freq. | DTMP Freq. | Key |
|---|---|---|---|---|---|---|---|
| 0 | 00000 | 440.0 | $A^4$ | –0.008 | 697 | 1209 | 1 |
| 1 | 00001 | 466.2 | $A\#^4$ | –0.016 | 770 | 1209 | 4 |
| 2 | 00010 | 493.9 | $B^4$ | –0.003 | 852 | 1209 | 7 |
| 3 | 00011 | 523.2 | $C^4$ | 0.014 | 941 | 1209 | * |
| 4 | 00100 | 554.4 | $C\#^4$ | 0.018 | 697 | 1336 | 2 |
| 5 | 00101 | 587.3 | $D^4$ | –0.023 | 770 | 1336 | 5 |
| 6 | 00110 | 622.3 | $D\#^4$ | –0.129 | 852 | 1336 | 8 |
| 7 | 00111 | 659.3 | $E^4$ | 0.106 | 941 | 1336 | 0 |
| 8 | 01000 | 698.5 | $F^4$ | –0.216 | 697 | 1477 | 3 |
| 9 | 01001 | 740.0 | $F\#^4$ | –0.222 | 770 | 1477 | 6 |
| 10 | 01010 | 784.0 | $G^4$ | 0.126 | 852 | 1477 | 9 |
| 11 | 01011 | 830.0 | $G\#^4$ | –0.169 | 941 | 1477 | # |
| 12 | 01100 | 880.0 | $A^5$ | 0.288 | 697 | 1633 | A |
| 13 | 01101 | 932.3 | $A\#^5$ | –0.014 | 770 | 1633 | B |
| 14 | 01110 | 987.8 | $B^5$ | –0.004 | 852 | 1633 | C |
| 15 | 01111 | 1046.5 | $C^5$ | –0.335 | 941 | 1633 | D |
| 16 | 10000 | 1108.7 | $C\#^5$ | –0.355 | 697 | 1209 | 1 |
| 17 | 10001 | 1174.7 | $D^5$ | –0.023 | 770 | 1209 | 4 |
| 18 | 10010 | 1244.5 | $D\#^5$ | –0.129 | 852 | 1209 | 7 |
| 19 | 10011 | 1318.5 | $E^5$ | 0.106 | 941 | 1209 | * |
| 20 | 10100 | 1396.9 | $F^5$ | –0.214 | 697 | 1336 | 2 |
| 21 | 10101 | 1480.0 | $F\#^5$ | –0.222 | 770 | 1336 | 5 |
| 22 | 10110 | 1568.0 | $G^5$ | 0.126 | 852 | 1336 | 8 |
| 23 | 10111 | 1661.2 | $G\#^5$ | –0.241 | 941 | 1336 | 0 |
| 24 | 11000 | 1760.0 | $A^6$ | –0.302 | 697 | 1477 | 3 |
| 25 | 11001 | 1864.6 | $A\#^6$ | –0.014 | 770 | 1477 | 6 |
| 26 | 11010 | 1975.5 | $B^6$ | 0.665 | 852 | 1477 | 9 |
| 27 | 11011 | 2093.0 | $C^6$ | 0.367 | 941 | 1477 | # |
| 28 | 11100 | 2217.5 | $C\#^6$ | 0.387 | 697 | 1633 | A |
| 29 | 11101 | 2349.3 | $D^6$ | 0.771 | 770 | 1633 | B |
| 30 | 11110 | 2663.3 | | --- | 852 | 1633 | C |
| 31 | 11111 | 2983.0 | | --- | 941 | 1633 | D |

**Figure 10-1. Write Cycle**



Write cycle

CLOCK

DATA | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A3 | A2 | A1 | A0 | R/W=0

Data from µP

Strobe
from µP
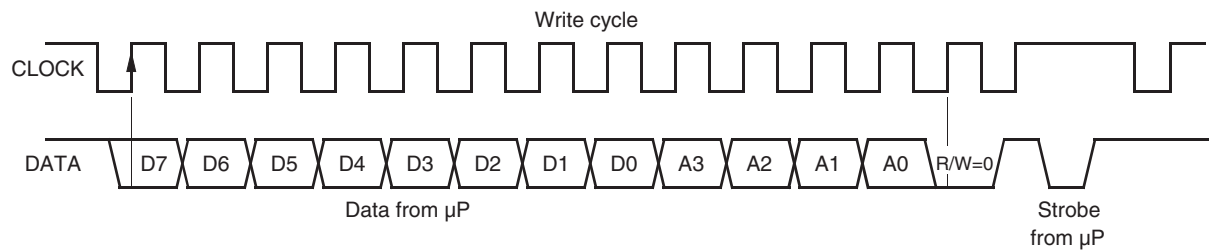
**Figure 10-2. Normal Read Cycle**



Normal read cycle

CLOCK

DATA | A3 | A2 | A1 | A0 | R/W = 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0

Data from µP

Strobe
from µP

Data from U4091BM
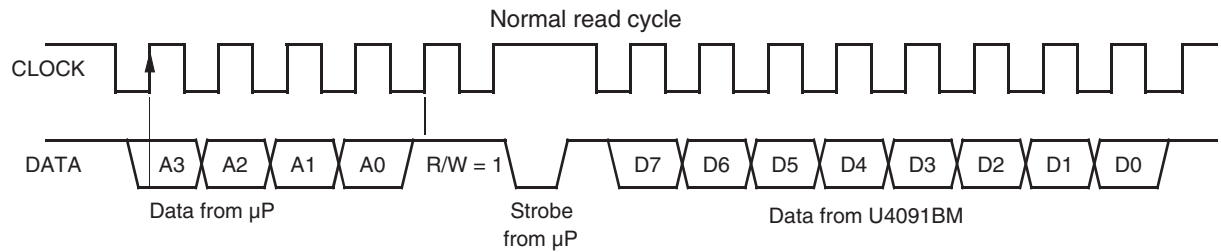
**Figure 10-3. Fast Read Cycle**



Fast read cycle

CLOCK

DATA

D7=IZC | D6=IVE

Strobe
from µP

Data from Atmel U4091BM
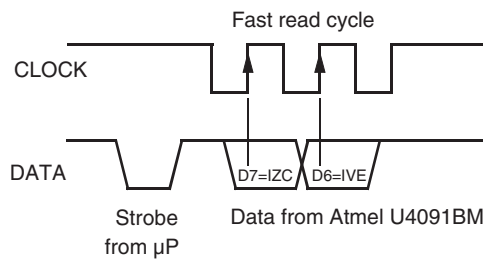
**Table 10-6.   Names and Functions of the Serial Registers**

| Register | Group | No. | Name | Description | Status | |
|----------|-------|-----|------|-------------|--------|---|
| R0 | Enables | R0B0 | ENRING | Enable ringer | | 1 |
| | | R0B1 | ERX | Enable receive part | 0 | |
| | | R0B2 | ETX | Enable transmit part | 0 | |
| | | R0B3 | ENVM | Enable VM generator | | 1 |
| | | R0B4 | ENMIC | Enable microphone | 0 | |
| | | R0B5 | ENSTBAL | Enable sidetone | 0 | |
| | | R0B6 | MUTE | Muting earpiece amplifier | 0 | |
| | | R0B7 | ENRLT | Enable POR low threshold | | 1 |
| R1 | Enables | R1B0 | ENSACL | Enable anti-clipping for speaker amplifier | 0 | |
| | | R1B1 | ENSA | Enable speaker amplifier and AFS | 0 | |
| | | R1B2 | ENSAO | Enable output stage speaker amplifier | 0 | |
| | | R1B3 | ENAM | Enable answering machine connections | 0 | |
| | | R1B4 | ENAGC | Enable AGC for answering machine | 0 | |
| | | R1B5 | Reserved | - | 0 | |
| | | R1B6 | Reserved | - | 0 | |
| | | R1B7 | FOFFC | Speed up offset canceller | 0 | |
| R2 | Matrix | R2B0 | I1O1 | Switch on MIC/LTX | 0 | |
| | | R2B1 | I1O2 | Switch on MIC/SA | 0 | |
| | | R2B2 | I1O3 | Switch on MIC/EPO | 0 | |
| | | R2B3 | I1O4 | Switch on MIC/AMREC | 0 | |
| | | R2B4 | I1O5 | Switch on MIC/AGCI | 0 | |
| | | R2B5 | I2O1 | Switch on DTMF/LTX | 0 | |
| | | R2B6 | I2O2 | Switch on DTMF/SA | 0 | |
| | | R2B7 | I2O3 | Switch on DTMF/EPO | 0 | |
| R3 | Matrix | R3B0 | I2O4 | Switch on DTMF/AMREC | 0 | |
| | | R3B1 | I2O5 | Switch on DTMF/AGCI | 0 | |
| | | R3B2 | I3O1 | Switch on LRX/LTX | 0 | |
| | | R3B3 | I3O2 | Switch on LRX/SA | 0 | |
| | | R3B4 | I3O3 | Switch on LRX/EPO | 0 | |
| | | R3B5 | I3O4 | Switch on LRX/AMREC | 0 | |
| | | R3B6 | I3O5 | Switch on LRX/AGCI | 0 | |
| | | R3B7 | I4O1 | Switch on AMPB/LTX | 0 | |

**Table 10-6. Names and Functions of the Serial Registers  (Continued)**

| Register | Group | No. | Name | Description | Status |
|---|---|---|---|---|---|
| R4 | Matrix | R4B0 | I4O2 | Switch on AMPB/SA | 0 |
| | | R4B1 | I4O3 | Switch on AMPB/EPO | 0 |
| | | R4B2 | I4O4 | Switch on AMPB/AMREC | 0 |
| R5 | AGATX MICLIM | R4B3 | I4O5 | Switch on AMPB/AGCI | 0 |
| | | R4B4 | I5O1 | Switch on AGCO/LTX | 0 |
| | | R4B5 | I5O2 | Switch on AGCO/SA | 0 |
| | | R4B6 | I5O3 | Switch on AGCO/EPO | 0 |
| | | R4B7 | I5O4 | Switch on AGCO/AMREC | 0 |
| | | R5B0 | EAFS | Enable AFS block | 0 |
| | | R5B1 | AGATX0 | Gain transmit AGA LSB | 0 |
| | | R5B2 | AGATX1 | Gain transmit AGA | 0 |
| | | R5B3 | AGATX2 | Gain transmit AGA MSB | 0 |
| | | R5B4 | MICHF | Select RF-microphone input | 0 |
| | | R5B5 | DBM5 | Maximum transmit level for anti-clipping | 0 |
| | | R5B6 | MIC0 | Gain microphone amplifier LSB | 0 |
| | | R5B7 | MIC1 | Gain microphone amplifier MSB | 0 |
| R6 | Shut down Sidetone | R6B0 | SD | Shut down | 0 |
| | | R6B1 | Reserved | - | 0 |
| | | R6B2 | SL0 | Slope adjustment for sidetone LSB | 0 |
| | | R6B3 | SL1 | Slope adjustment for sidetone MSB | 0 |
| | | R6B4 | LF0 | Low frequency adjustment for sidetone LSB | 0 |
| | | R6B5 | LF1 | Low frequency adjustment for sidetone | 0 |
| | | R6B6 | LF2 | Low frequency adjustment for sidetone | 0 |
| | | R6B7 | LF3 | Low frequency adjustment for sidetone MSB | 0 |
| R7 | Sidetone AGARX | R7B0 | P0 | Pole adjustment for sidetone LSB | 0 |
| | | R7B1 | P1 | Pole adjustment for sidetone | 0 |
| | | R7B2 | P2 | Pole adjustment for sidetone | 0 |
| | | R7B3 | P3 | Pole adjustment for sidetone | 0 |
| | | R7B4 | P4 | Pole adjustment for sidetone MSB | 0 |
| | | R7B5 | AGARX0 | Gain receive AGC LSB | 0 |
| | | R7B6 | AGARX1 | Gain receive AGC | 0 |
| | | R7B7 | AGARX2 | Gain receive AGC MSB | 0 |
| R8 | EARA Line impedance | R8B0 | EA0 | Gain earpiece amplifier LSB | 0 |
| | | R8B1 | EA1 | Gain earpiece amplifier | 0 |
| | | R8B2 | EA2 | Gain earpiece amplifier | 0 |
| | | R8B3 | EA3 | Gain earpiece amplifier | 0 |
| | | R8B4 | EA4 | Gain earpiece amplifier MSB | 0 |
| | | R8B5 | IMPH | Line impedance selection (1 = 1kΩ) | 0 |
| | | R8B6 | LOMAKE | Short circuit during pulse dialing | 0 |
| | | R8B7 | AIMP | Switch for additional external line impedance | 0 |

**Table 10-6. Names and Functions of the Serial Registers (Continued)**

| Register | Group | No. | Name | Description | Status | |
|----------|-------|-----|------|-------------|--------|---|
| R9 | AFS | R9B0 | AFS0 | AFS gain adjustment LSB | 0 | |
| | | R9B1 | AFS1 | AFS gain adjustment | 0 | |
| | | R9B2 | AFS2 | AFS gain adjustment | 0 | |
| | | R9B3 | AFS3 | AFS gain adjustment | 0 | |
| | | R9B4 | AFS4 | AFS gain adjustment | 0 | |
| | | R9B5 | AFS5 | AFS gain adjustment MSB | 0 | |
| | | R9B6 | AFS4PS | Enable 4-point sensing | 0 | |
| | | R9B7 | Reserved | - | 0 | |
| R10 | SA | R10B0 | SA0 | Gain speaker amplifier LSB | 0 | |
| | | R10B1 | SA1 | Gain speaker amplifier | 0 | |
| | | R10B2 | SA2 | Gain speaker amplifier | 0 | |
| | | R10B3 | SA3 | Gain speaker amplifier | 0 | |
| | | R10B4 | SA4 | Gain speaker amplifier MSB | 0 | |
| | | R10B5 | SE | Speaker amplifier single-ended mode | 0 | |
| | | R10B6 | LSCUR0 | Speaker amplifier charge-current adjustment LSB | 0 | |
| | | R10B7 | LSCUR1 | Speaker amplifier charge-current adjustment MSB | 0 | |
| R11 | ADC | R11B0 | ADC0 | Input selection ADC | 0 | |
| | | R11B1 | ADC1 | Input selection ADC | 0 | |
| | | R11B2 | ADC2 | Input selection ADC | 0 | |
| | | R11B3 | ADC3 | Input selection ADC | 0 | |
| | | R11B4 | NWT | Network tuning | 0 | |
| | | R11B5 | SOC | Start of ADC conversion | 0 | |
| | | R11B6 | ADCR | Selection of ADC range | 0 | |
| | | R11B7 | MSKIT | Mask for interrupt bits | 0 | |
| R12 | DTMF | R12B0 | DTMFF0 | DTMF frequency selection | 0 | |
| | | R12B1 | DTMFF1 | DTMF frequency selection | 0 | |
| | | R12B2 | DTMFF2 | DTMF frequency selection | 0 | |
| | | R12B3 | DTMFF3 | DTMF frequency selection | 0 | |
| | | R12B4 | DTMFF4 | DTMF frequency selection | 0 | |
| | | R12B5 | DTMFM0 | Generator mode selection | 0 | |
| | | R12B6 | DTMFM1 | Generator mode selection | 0 | |
| | | R12B7 | DTMFM2 | Generator mode selection | 0 | |
| R13 | CLK RTH TM | R13B0 | CLK0 | Selection clock frequency for microcontroller | 0 | |
| | | R13B1 | CLK1 | Selection clock frequency for microcontroller | 0 | |
| | | R13B2 | RTH0 | Ringer threshold adjustment LSB | 0 | |
| | | R13B3 | RTH1 | Ringer threshold adjustment | 0 | |
| | | R13B4 | RTH2 | Ringer threshold adjustment | 0 | |
| | | R13B5 | RTH3 | Ringer threshold adjustment MSB | 0 | |
| | | R13B6 | TME0 | Test mode enable (low active) | 0 | |
| | | R13B7 | TME1 | Test mode enable (high active) | 0 | |

**Table 10-6.** Names and Functions of the Serial Registers (Continued)

| Register | Group | No. | Name | Description | Status | |
|---|---|---|---|---|---|---|
| R14 | TM CLOR | R14B0 | TME2 | Test mode enable (high active) | 0 | |
| | | R14B1 | TME3 | Test mode enable (low active) | 0 | |
| | | R14B2 | Reserved | - | 0 | |
| | | R14B3 | CLOR0 | Adjustment for calculated receive log amp LSB | 0 | |
| | | R14B4 | CLOR1 | Adjustment for calculated receive log amp | 0 | |
| | | R14B5 | CLOR2 | Adjustment for calculated receive log amp | 0 | |
| | | R14B6 | CLOR3 | Adjustment for calculated receive log amp | 0 | |
| | | R14B7 | CLOR4 | Adjustment for calculated receive log amp MSB | 0 | |
| R15 | CLOT | R15B0 | Reserved | - | 0 | |
| | | R15B1 | Reserved | - | 0 | |
| | | R15B2 | Reserved | - | 0 | |
| | | R15B3 | CLOT0 | Adjustment for calculated transmit log amp LSB | 0 | |
| | | R15B4 | CLOT1 | Adjustment for calculated transmit log amp | 0 | |
| | | R15B5 | CLOT2 | Adjustment for calculated transmit log amp | 0 | |
| | | R15B6 | CLOT3 | Adjustment for calculated transmit log amp | 0 | |
| | | R15B7 | CLOT4 | Adjustment for calculated transmit log amp MSB | 0 | |

## 10.1 Power-on Reset

To avoid undefined states of the system when it is powered on, an internal reset clears the internal registers.

The system (Atmel® U4091BM-R + microcontroller) is woken up by any of the following conditions:

- VMP > 2.75V and VB > 2.95V
- and line voltage (VL)
- or ringer (VRING)
- or external supply (ES)

The power-down of the circuit is caused by a shut-down sent by the serial bus (SD = 1), low-voltage reset, or by the watchdog function (see ).

## 11. Watchdog Function

To avoid the system operating the microcontroller in a fault state, the circuit provides a watchdog function. The watchdog has to be retriggered every second by triggering the serial bus (sending information to the IC or other remote components at the serial bus). If there has been no bus transmission for more than one second, the watchdog initiates a reset.

The watchdog provides a reset for the external microcontroller, but does not change the Atmel U4091BM-R's registers.

## 12. Acoustic Feedback Suppression

Acoustical feedback from the loudspeaker to the hands-free microphone may cause instability of the system. The Atmel®
U4091BM-R has a very efficient feedback-suppression circuit which offers a 4-point or (alternatively) a 2-point signal-sensing topology (see Figure 12-1).

Two attenuators (TXA and SAI) reduce the critical loop gain via the serial bus either in the transmit or in the receive path. The overall loop gain remains constant under all operating conditions.

The LOGs produce a logarithmically-compressed signal of the TX- and RX-envelope curve. The AFSCON block determines whether the TX or the RX signal has to be attenuated.

The voice-switch topology can be selected by the serial bus. In 2-point-sensing mode, AFSCON is controlled directly by the LOG outputs.

**Figure 12-1. Basic System Configurations**
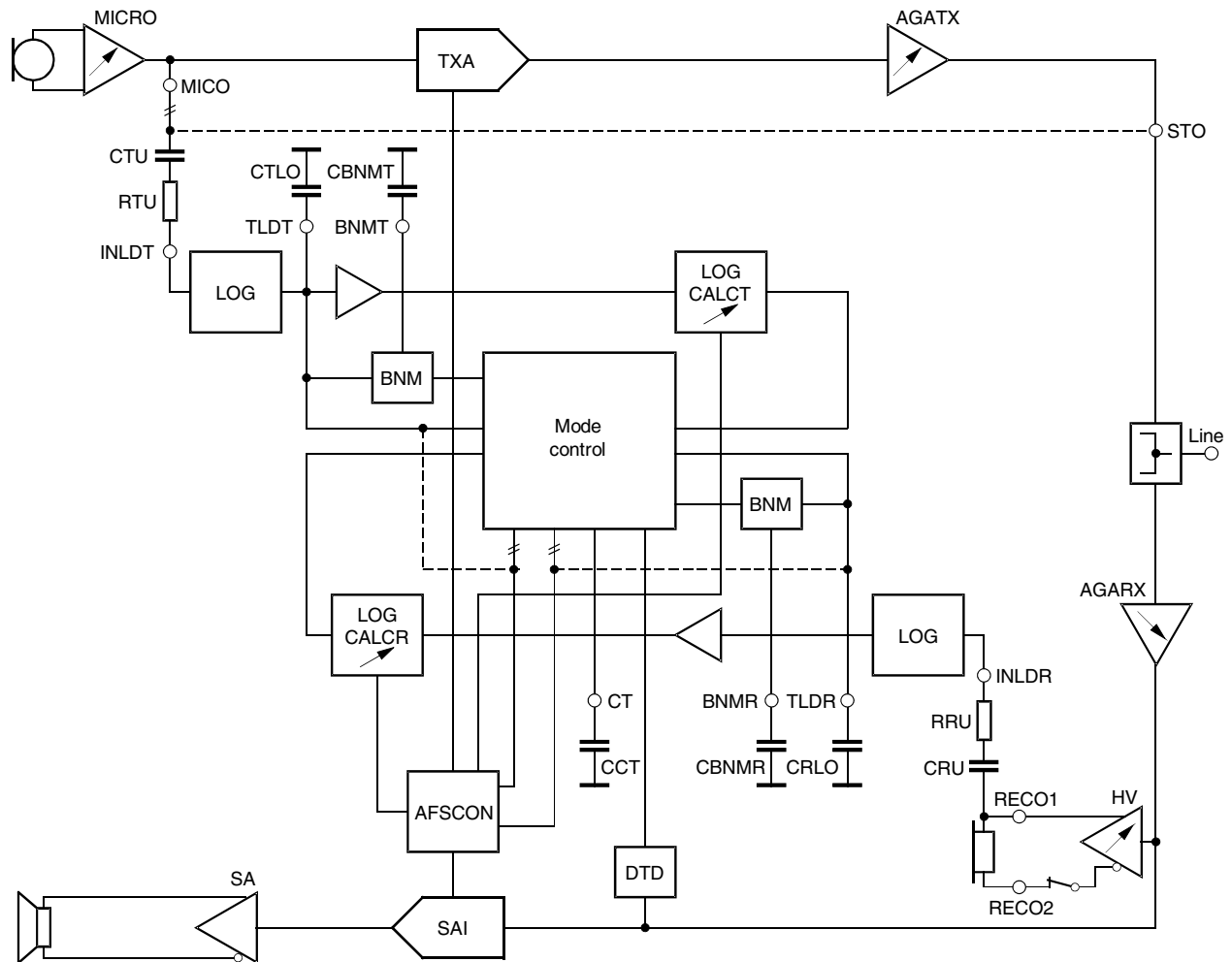
**Figure 12-2. Power-on Reset (Line)**

Line

LID

IVDD

OSCOUT — $t_{on}$

VMP

Reset — $t_{rt}$

$t_{rt} - t_{on} = 4.5$ ms
$t_{on}$ = start-up oscillator
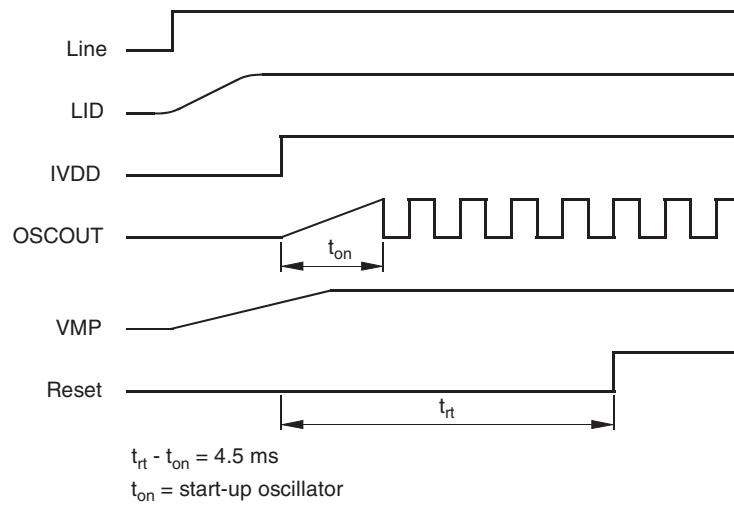
**Figure 12-3. Power-on Reset (Ringing)**

VRING

VB

IVDD

VMP

OSCOUT — $t_{on}$

Reset — $t_{rt}$
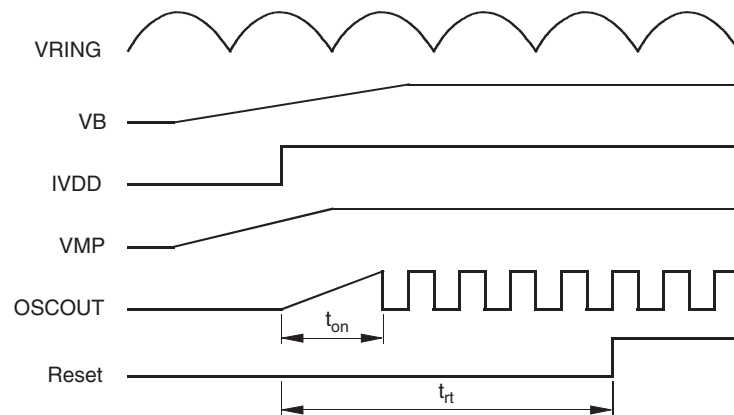
**Figure 12-4. Power-on Reset (Low Voltage Reset)**

Line

LID

VMP — LVI — LVR

LVI

Reset

OSCOUT
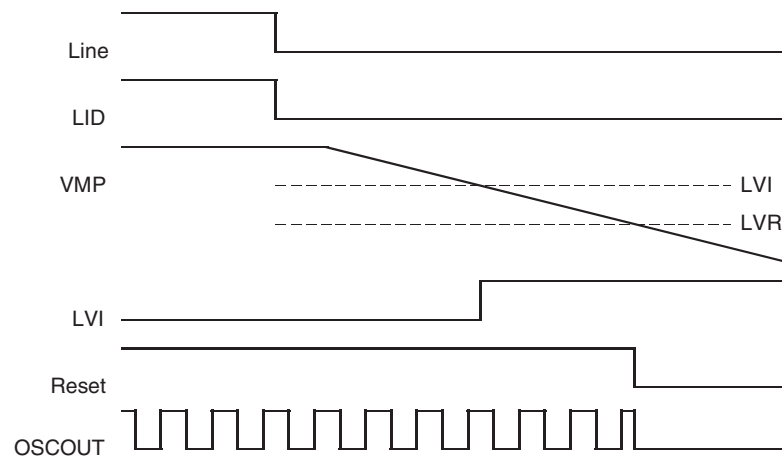
## 12.1 Dial-tone Detector

The dial-tone detector is a comparator with one side connected to the speaker amplifier input and the other to VM with a 35-mV offset (see Figure 12-5 on page 21). If the circuit is in idle mode, and the incoming signal is greater than 35mV ($25mV_{rms}$), the comparator's output will change thus disabling the receive idle mode. This circuit prevents the dial tone (which would be considered as continuous noise) from fading away as the circuit would have the tendency to switch to idle mode. By disabling the receive idle mode, the dial tone remains at the normally expected full level.

## 12.2 Background Noise Monitors

This circuit distinguishes speech (which consists of bursts) from background noise (a relatively constant signal level). There are two background-noise monitors, one for the receive path and the other for the transmit path. The receive background-noise monitor is operated on by the receive level detector, while the transmit background noise monitor is operated on by the transmit level detector (see Figure 12-6 on page 21). They monitor the background noise by storing a DC voltage representative of the respective noise levels in capacitors at CBNMR and CBNMT. The voltages at these pins have slow rise times (determined by the internal current source and an external capacitor), but fast decay times. If the signal at TLDR (or TLDT) changes slowly, the voltage at BNMR (or BNMT) will remain more positive than the voltage at the non-inverting input of the monitor's output comparator. When speech is present, the voltage at the non-inverting input of the comparator will rise more quickly than the voltage at the inverting input (due to the burst characteristic of speech), causing its output to change. This output is sensed by the mode-control block.

## 12.3 4-point Sensing

In 4-point-sensing mode, the receive- and the transmit-sensing paths include additional CLOGs (calculated logarithmic amplifiers). The block MODECON compares the detector output signals and decides whether receive, transmit or idle mode has to be activated. Depending on the mode decision, MODECON generates a differential voltage to control AFSCON.

The MODECON block has seven inputs:

- The output of the transmit log (LOGT) – the comparison of LOGT, CLOGR
- The output of the receive clog (CLOGR) – designated I1
- The output of the transmit clog (CLOGT) – the comparison of CLOGT, LOGR
- The output of the receive log (LOGR) – designated I2
- The output of the transmit background-noise monitor (BNMT) – designated I3
- The output of the receive background-noise monitor (BNMR) – designated I4
- The output of the dial-tone detector

The differential output (AFST, AFSR) of the block MODECON controls AFSCON. The effect of I1-I4 in Table 12-1 on page 19.

**Table 12-1. Mode Decision for Signal Sensing**

| Input | | | | Output |
|---|---|---|---|---|
| I1 | I2 | I3 | I4 | Mode |
| T | T | S | X | Transmit |
| T | R | Y | Y | Change mode |
| R | T | Y | Y | Change mode |
| R | R | X | S | Receive |
| T | T | N | X | Idle |
| T | R | N | N | Idle |
| R | T | N | N | Idle |
| R | R | X | N | Idle |

Note: X = don't care; Y = I3 and I4 are not both noise.

LOGT > CLOGR          I1 = T
LOGT < CLOGR          I1 = R
LOGR < CLOGT          I2 = T
LOGR > CLOGT          I2 = R
BNMT detects speech      I3 = S
BNMT detects noise       I3 = N
BNMR detects speech     I4 = S
BNMR detects noise      I4 = N

## 12.4 Term Definitions

1. Transmit means the transmit attenuator is fully on, and the receive attenuator is at maximum attenuation.

2. Receive means the receive attenuator is fully on, and the transmit attenuator is at maximum attenuation.

3. In idle mode, the transmit and receive attenuator are at half of their maximum attenuation.
   - Change mode means both the transmit and receive speech are present in approximately equal levels. The attenuators are quickly switched (30ms) to the opposite mode until one speech level dominates the other.
   - Idle means speech has ceased in both transmit and receive paths. The attenuators are then slowly switched (1.5s) to idle mode.

4. Switching to full transmit or receive modes from the idle mode is done at a fast rate (30ms).

## 12.5 Summary of Truth Table

1. The circuit will switch to transmit mode if
   - Both transmit level detectors sense higher signal levels than the respective receive level detectors, and
   - The transmit background-noise monitor indicates the presence of speech

2. The circuit will switch to receive mode if
   - Both receive level detectors sense higher signal levels than the respective transmit level detectors, and
   - The receive background-noise monitor indicates the presence of speech

3. The circuit will switch to the reverse mode if
   - The level detectors disagree on the relative strengths of the signal levels, and
   - At least one of the background-noise monitors indicates speech

4. The circuit will switch to idle mode when
   - Both speakers are quiet (no speech present), or
   - When one speaker speech level is continuously overridden by noise at the other speaker's location

The time required to switch the circuit between transmit, receive and idle is determined by internal current sources and the capacitor at pin CT. A diagram of the CT circuitry is shown in . It operates as follows:

- CCT is typically 4.7µF.
- To switch to transmit mode, ITX is turned on (IRX is off), charging the external capacitor to –240mV below VM. (An internal clamp prevents further charging of the capacitor.)
- To switch to receive mode, IRX is turned on (ITX is off), increasing the voltage on the capacitor to +240mV with respect to VM.
- To switch to reverse mode, the current sources ITX, IRX are turned off, and the current source IFI is switched on, discharging the capacitor to VM.
- To switch to idle mode, the current sources ITX, IRX, IFI are turned off, and the current source ISI charges the capacitor to VM.

**Figure 12-5. Dial Tone Detector**
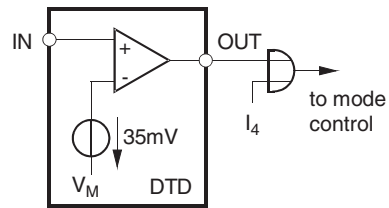


**Figure 12-6. Background Noise Monitor**
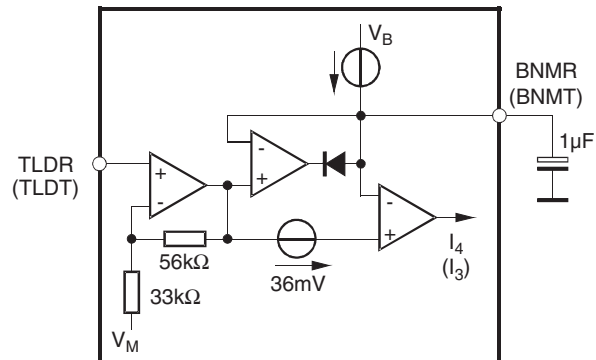


**Figure 12-7. Generation of Control Voltage (CT) for Mode Switching**
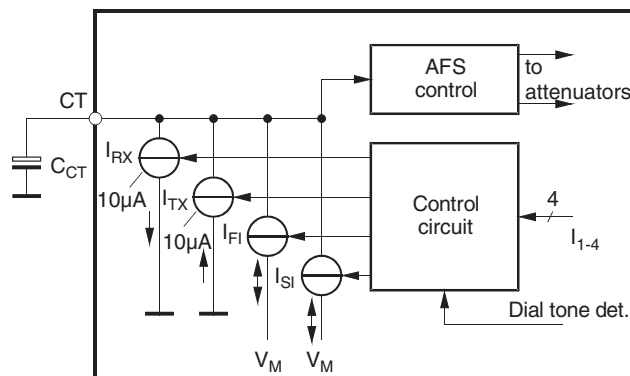
**Figure 12-8. Block Diagram Hands-free Mode Atmel U4091BM-R 2-point Signal Sensing**
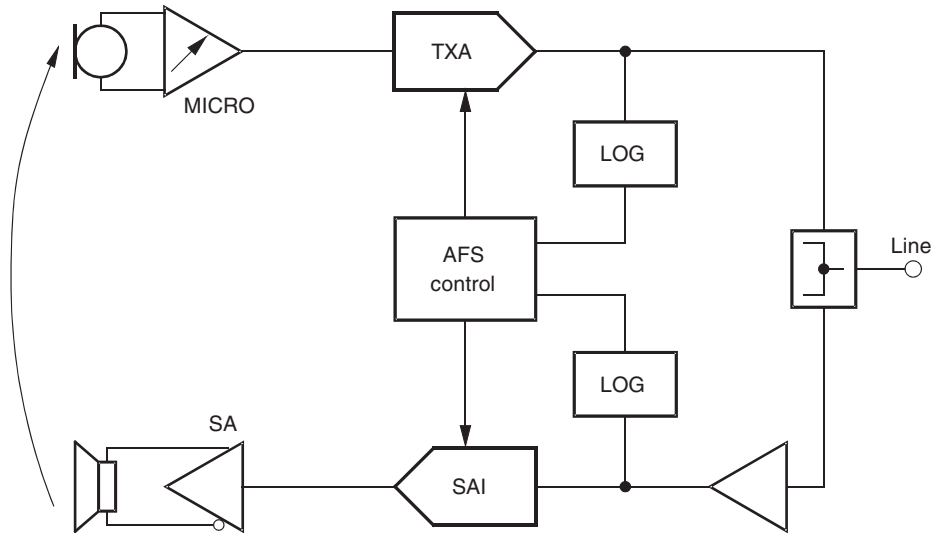


**Figure 12-9. Block Diagram Hands-free Mode Atmel U4091BM-R 4-point Signal Sensing**
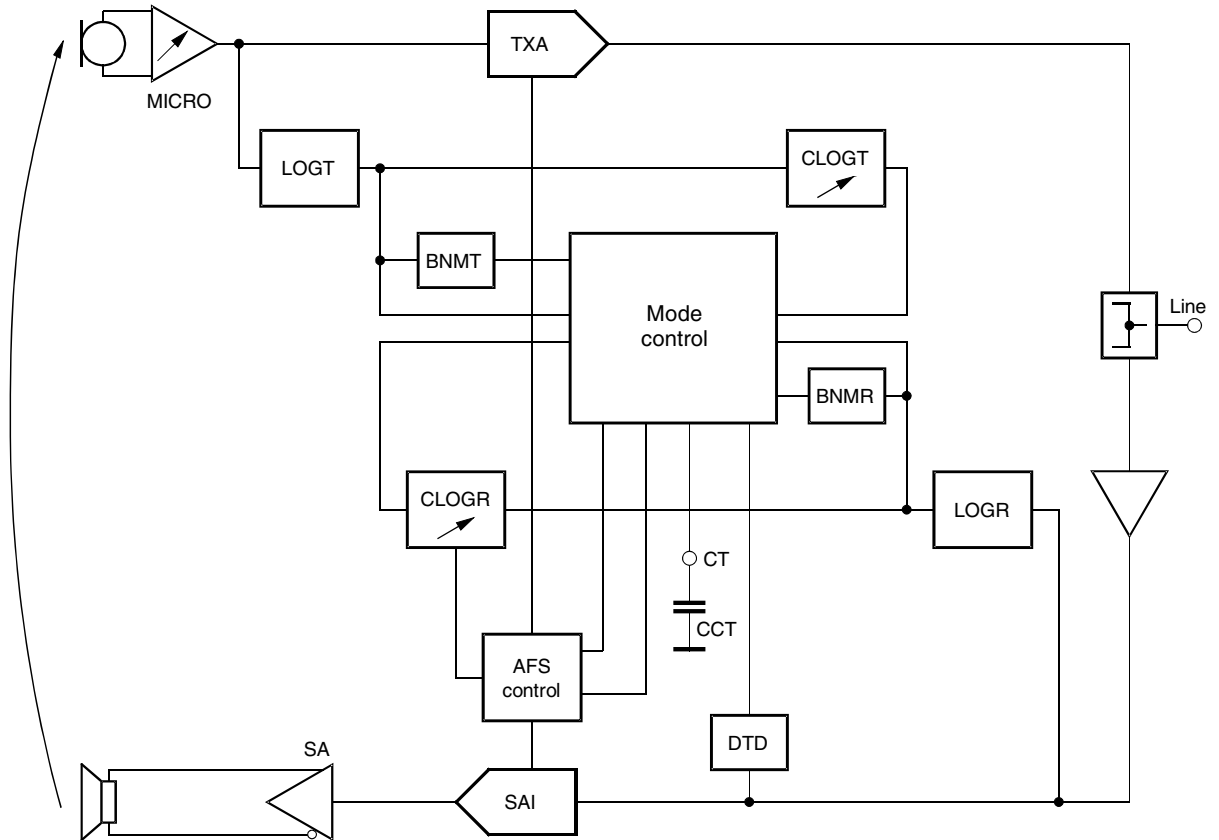
# 13. Analog-to-Digital Converter (ADC)

This circuit is a 7-bit successive-approximation analog-to-digital converter in switched capacitor technique. An internal band gap circuit generates a 1.25-V reference voltage which is the equivalent of 1 MSB (1 LSB = 19.5mV). The possible input voltage at ADIN is 0V to 2.48V.

The ADC needs an SOC (Start Of Conversion) signal. In the High phase of the SOC signal, the ADC is reset. Then, 50µs after the beginning of the Low phase of the SOC signal, the ADC generates an EOC (End Of Conversion) signal which indicates that the conversion is finished. The rising edge of EOC generates an interrupt at the INT output. The result can be read out by the serial bus.

Voltages higher than 2.45V have to be divided. The signal connected to the ADC is determined by 4 bits: ADC0, ADC1, ADC2 and ADC3. TLDR/TLDT measuring is possible relative to a preceding reference measurement. The current range of IL can be doubled by ADCR. If ADCR is High, S has the value 0.5, otherwise S = 1.

The source impedance at ADIN must be lower than 250k$\Omega$

Accuracy: 1 LSB + 3%

**Figure 13-1. Timing of ADC**
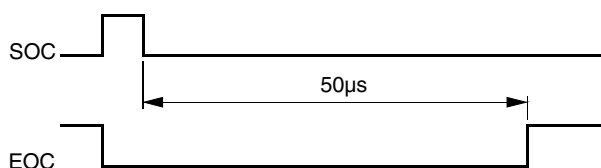


**Figure 13-2. ADC Input Selection**
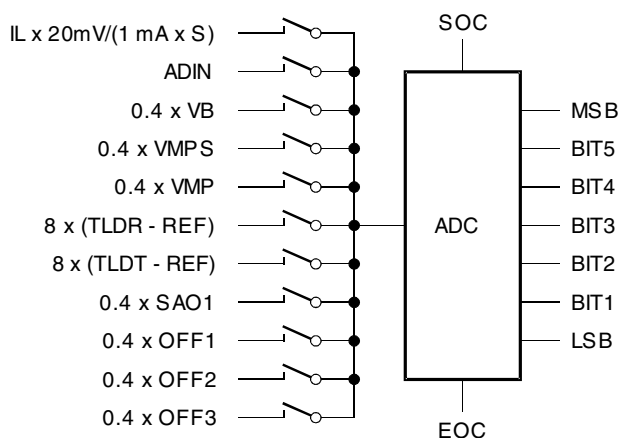
**Table 13-1. Input Selection ADC**

| Decimal | ADC[1:4] | Symbol | Value |
|---------|----------|--------|-------|
| 0 | 0000 | OFF | - |
| 1 | 0001 | IL | $I1 = S \times 127mA \times D / 128$ |
| 2 | 0010 | ADIN extern | $V2 = 2.5V \times D / 128$ (maximum 2.5V) |
| 3 | 0011 | VB | $V3 = (2.5V / 0.4) \times D / 128$ |
| 4 | 0100 | VMPS | $V4 = (2.5V / 0.4) \times D / 128$ |
| 5 | 0101 | VMP | $V5 = (2.5V / 0.4) \times D / 128$ |
| 6 | 0110 | TLDR | $V6 = 8 \times (V_p - Ref) \times D / 128$ |
| 7 | 0111 | TLDT | $V7 = 8 \times (V_p - Ref) \times D / 128$ |
| 8 | 1000 | Not used | - |
| 9 | 1001 | SAO1 | $V4 = (2.5V / 0.4) \times D / 128$ |
| 10 | 1010 | Offcan1 | Atmel's internal use |
| 11 | 1011 | Offcan2 | - |
| 12 | 1100 | Offcan3 | - |
| 13 | 1101 | Not used | - |
| 14 | 1110 | Not used | - |
| 15 | 1111 | Not used | - |

Note:       $D$ = measured digital word ($0 \leq D \leq 127$)
               $S$ = programmable gain 0.5 or 1
               $V_p$ = peak value of the measured signal

# 14. Switch Matrix

The switch matrix has 5 inputs and 5 outputs. Every pair of I/Os except AGCO and AGCI can be connected. The inputs and outputs used must be enabled. If 2 or more inputs are switched to an output, the sum of the inputs is available at the output.

The inputs MIC and LRX have offset cancellers with a 3-dB corner frequency of 270Hz. AMPB has a 60-kΩ input impedance. The TXO output has a digitally-programmable gain stage with a gain of 2dB to 9dB (in 1dB steps) depending on AGATX0 (LSB), AGATX1, AGATX2 (MSB), and a first order low-pass filter with 0.5dB damping at 3300Hz and 3dB damping at 9450Hz. The outputs RXLS, EPO and AMREC have a gain of 0dB. The offset at the outputs of the matrix is less than 30mV. If a switch is open, the path has a damping of more than 60dB.

**Figure 14-1. Switch Matrix Diagram**
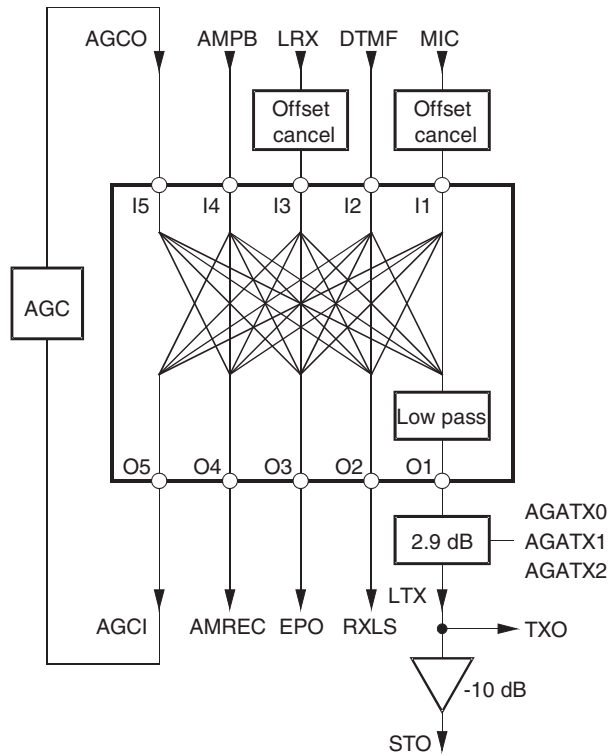
**Table 14-1.   Bits and Corresponding Switches**

| Register | No. | Name | Description |
|---|---|---|---|
| R2 | R2B0 | I1O1 | Switch on MIC/LTX |
| | R2B1 | I1O2 | Switch on MIC/RXLS |
| | R2B2 | I1O3 | Switch on MIC/EPO |
| | R2B3 | I1O4 | Switch on MIC/AMREC |
| | R2B4 | I1O5 | Switch on MIC/AGCI |
| | R2B5 | I2O1 | Switch on DTMF/LTX |
| | R2B6 | I2O2 | Switch on DTMF/RXLS |
| | R2B7 | I2O3 | Switch on DTMF/EPO |
| R3 | R3B0 | I2O4 | Switch on DTMF/AMREC |
| | R3B1 | I2O5 | Switch on DTMF/AGCI |
| | R3B2 | I3O1 | Switch on LRX/LTX |
| | R3B3 | I3O2 | Switch on LRX/RXLS |
| | R3B4 | I3O3 | Switch on LRX/EPO |
| | R3B5 | I3O4 | Switch on LRX/AMREC |
| | R3B6 | I3O5 | Switch on LRX/AGCI |
| | R3B7 | I4O1 | Switch on AMPB/LTX |
| R4 | R4B0 | I4O2 | Switch on AMPB/RXLS |
| | R4B1 | I4O3 | Switch on AMPB/EPO |
| | R4B2 | I4O4 | Switch on AMPB/AMREC |
| | R4B3 | I4O5 | Switch on AMPB/AGCI |
| | R4B4 | I5O1 | Switch on AGCO/LTX |
| | R4B5 | I5O2 | Switch on AGCO/RXLS |
| | R4B6 | I5O3 | Switch on AGCO/EPO |
| | R4B7 | I5O4 | Switch on AGCO/AMREC |

# 15. Sidetone System

**Figure 15-1. Principle Circuit of Sidetone Balancing**
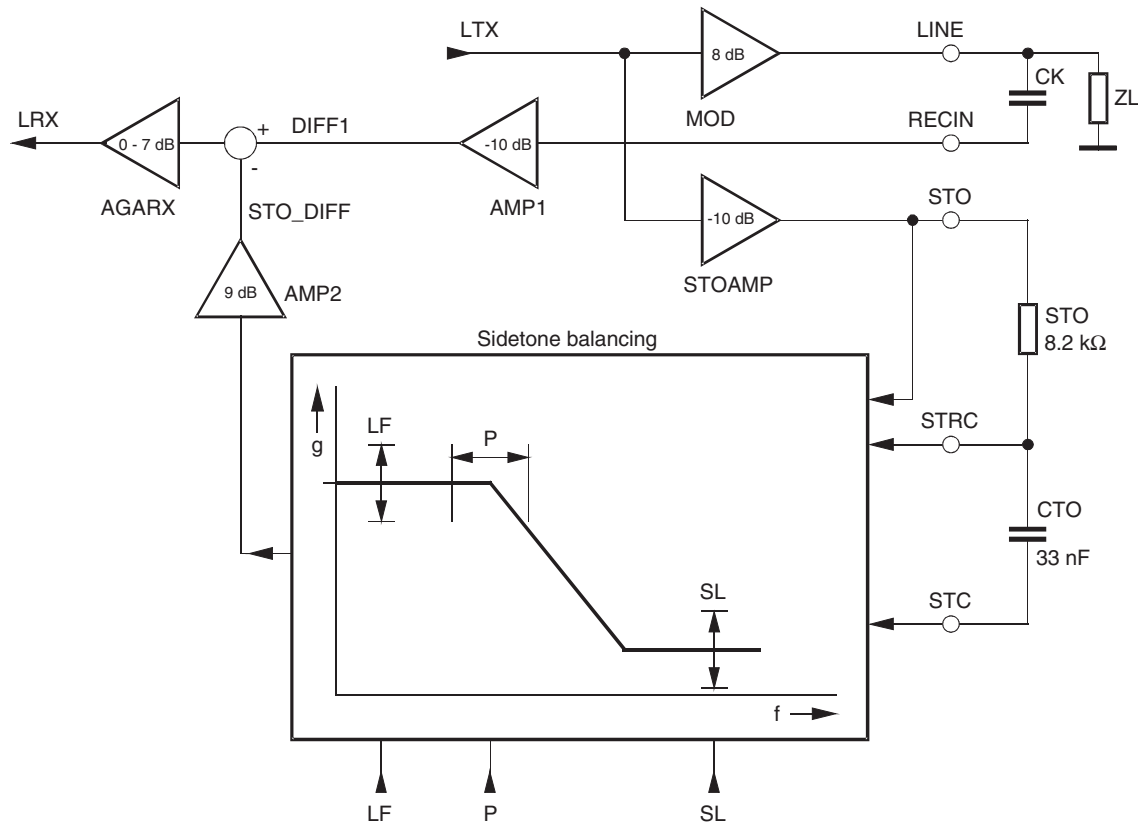


The Sidetone Balancing (STB) has the task of reducing the cross-talk from LTX (microphone) to LRX (earpiece) in the frequency range of 0.3kHz to 3.4kHz. The LTX signal is converted into a current in the MOD block. This current is transformed into a voltage signal (LINE) by the line impedance ZL. The LINE signal is fed into the summing amplifier DIFF1 via capacitor CK and attenuator AMP1.

On the other hand the LTX buffered by STOAMP drives an external low-pass filter (RST, CST). The external low-pass filter and the internal STB have the transfer function drawn in the STB box. The amplified STB output signal drives the negative input of the summing block. If both signals at the DIFF1 block are equal in level and phase, we have good suppression of the LTX signal. In this condition, the frequency and phase response of the STB block will represent the frequency curve on line.

In real life, the line impedance ZL varies strongly for different users. To obtain good suppression with one application for all different line impedances, the STB function is programmable.

The 3 programmable parameters are

1. LF (gain at low frequency)
   LF has 15 programming steps of 0.5dB
   LF(0) provides –2dB gain, LF(15) provides 5.5dB gain
   STO_DIFF(LF) = (–10dB – 2dB + 0.5dB × LF + 9dB) × LTX

2. P (the pole position of the low-pass)
   The P adjustment has 31 steps. P(0) means the lowpass determined by the external application (RST, CST). The internally processed low-pass frequency is fixed by the following equation.

$$f(P) = \frac{1}{2 \times \pi \times CST \times RST} \times 1.122^P$$

3. SL (sidetone slope; the pole frequency of the high-pass)
   The SL has 3 steps. SL(0) is a lower frequency of the high-pass. SL(3) is a higher frequency of the high-pass. SL can be used to influence the suppression at high frequencies.

**Figure 15-2. Audio Frequency Signal Management Atmel U4091BM-R**
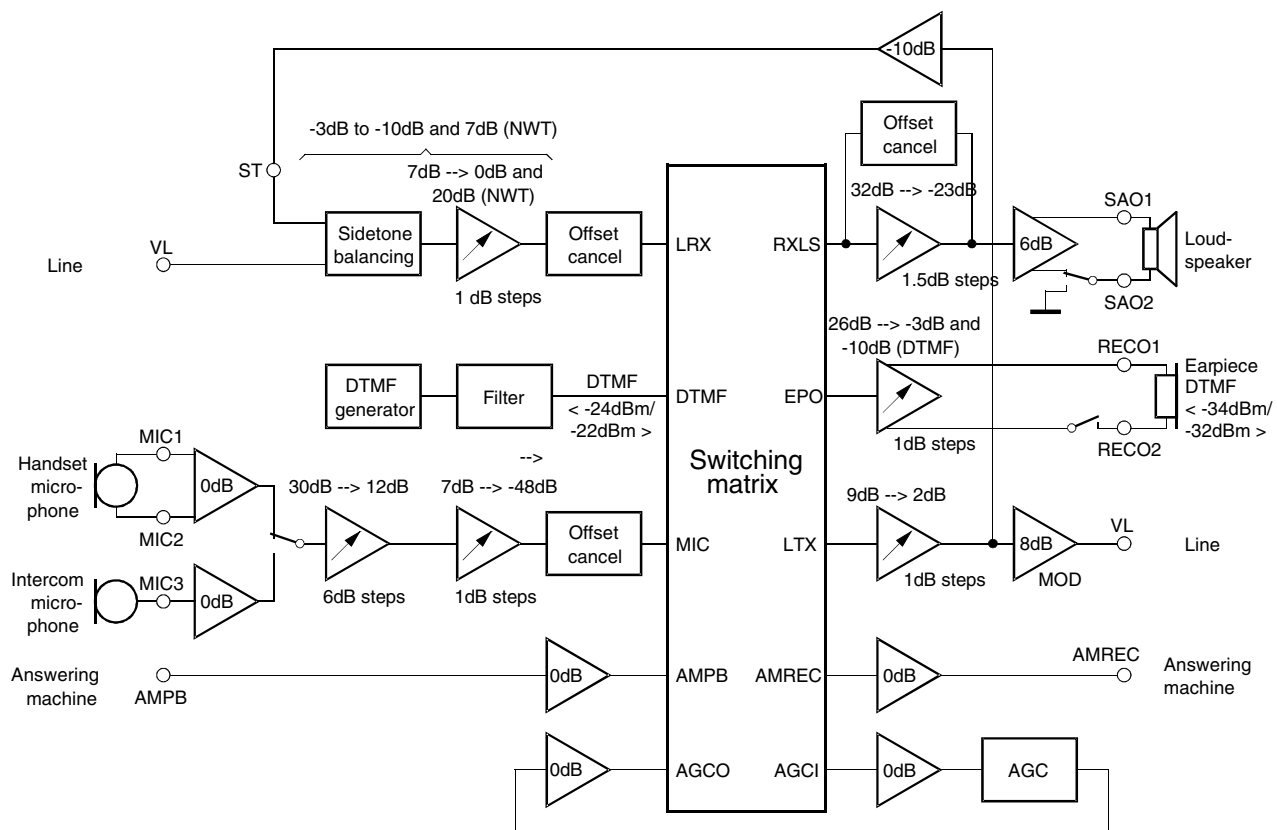
# 16. Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Line current | $I_L$ | 140 | mA |
| DC line voltage | $V_L$ | 12 | V |
| Maximum input current | $I_{RING}$ | 15 | mA |
| Junction temperature | $T_j$ | 125 | °C |
| Ambient temperature | $T_{amb}$ | −25 to +75 | °C |
| Storage temperature | $T_{stg}$ | −55 to +150 | °C |
| Total power dissipation, $T_{amb}$ = 60°C | $P_{tot}$ | 0.9 | W |

# 17. Thermal Resistance

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Junction ambient SSO44 | $R_{thJA}$ | 70 | K/W |

# 18. Electrical Characteristics

f = 1kHz, 0dBm = 775mV$_{rms}$, IVMIC = 0.3mA, IMP = 3mA, $R_{DC}$ = 1.3MΩ, $T_{amb}$ = 25°C, $Z_{ear}$ = 68nF + 100Ω, RLS = 50Ω, $Z_M$ = 68nF, resonator: f = 3.58MHz, all bits in reset condition, unless otherwise specified.

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| DC Characteristics | | | | | | |
| DC voltage drop over circuit | $I_L$ = 2mA<br>$I_L$ = 14mA<br>$I_L$ = 60mA<br>$I_L$ = 100mA | $V_L$ | 4.4<br><br><br>8.6 | 1.6<br>4.8<br>7.2<br>9.2 | <br>5.2<br><br>9.8 | V<br>V<br>V<br>V |
| Transmission Amplifier, $I_L$ = 14mA, $V_{MIC}$ = 2mV, MICG[0:1] = 2, AGATX[0:2] = 7<br>ERX = ETX = ENMIC = ENSTBAL = I1O1 = I3O3 = 1, ($G_T$ = 48dB) | | | | | | |
| Transmit amplification | MICG[0:1] = 2<br>AGATX[0:2] = 7 | $G_T$ | 45.3 | 46.5 | 47.7 | dB |
| Frequency response due to internal filters | $I_L$ ≥ 14mA,<br>f = 1kHz to 3.4kHz | $\Delta G_T$ | −1 | | 0 | dB |
| Gain change with current | $I_L$ = 14mA to 100mA | $\Delta G_T$ | | | ±0.5 | dB |
| Gain deviation | $T_{amb}$ = −10°C to +60°C | $\Delta G_T$ | | | ±0.5 | dB |
| CMRR of microphone amplifier | | CMRR | 60 | 80 | | dB |
| Input resistance of MIC amplifier | | $R_i$ | | 50 | | kΩ |
| Input resistance of MIC3 amplifier | MICHF = 1 | $R_i$ | 75 | 150 | 300 | kΩ |
| Gain difference between MIC1/MIC2 to MIC3 | MICHF = 1 | $\Delta G_T$ | | | ±0.4 | dB |
| Distortion at line | $I_L$ ≥ 14mA, $V_L$ = 700mV$_{rms}$ | $d_t$ | | | 2 | % |

Note: 1. This is a period of time the bus requires from the end of a data transmission and before a new transmission can be started

f = 1kHz, 0dBm = 775mV$_{rms}$, IVMIC = 0.3mA, IMP = 3mA, R$_{DC}$ = 1.3MΩ, T$_{amb}$ = 25°C, Z$_{ear}$ = 68nF + 100Ω, RLS = 50Ω, Z$_M$ = 68nF, resonator: f = 3.58MHz, all bits in reset condition, unless otherwise specified.

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Maximum output voltage | I$_L$ ≥ 19mA, d < 5%, V$_{MIC}$ = 10mV CTXA = 1µF, DBM5 = 0 | V$_{Lmax}$ | 1.8 | 3.0 | 4.2 | dBm |
| | DBM5 = 1 | V$_{Lmax}$ | 4.8 | 6.0 | 6.6 | dBm |
| | V$_{MIC}$ = 20mV, MICG[0:1] = 3 | V$_{MICOmax}$ | | –4.2 | | dBm |
| Noise at line psophometrically weighted | I$_L$ ≥ 14mA, MICG[0:1] = 2 AGATX[0:2] = 7 | No | | –73 | –70 | dBmp |
| Anti-clipping attack time release time | CTXA = 1µF each 3 dB overdrive | t$_a$ t$_r$ | | 2 80 | | ms ms |
| Receiving Amplifier I$_L$ = 14mA, V$_{GEN}$ = 300mV, ERX = ETX = ENMIC = ENSTBAL = I1O1 = I3O3 = 1, SL[0:1] = 0, LF[0:3] = 1, P[0:4] = 31, AFS[0:5] = 54, AGARX[0:2] = 0 | | | | | | |
| Adjustment range of receiving gain | Single ended, I$_L$ ≥ 14mA, Mute = 1, EA[0:4] = 2 to 31 AGARX[0:2] = 0 to 7 | G$_R$ | –19 | | +17 | dB |
| Receiving amplification | Differential AGARX[0:2] = 0 EA[0:4] = 15 EA[0:4] = 31 | G$_R$ | –1 14.7 | 0 15.7 | 1 16.7 | dB dB |
| Frequency response | I$_L$ ≥ 14mA, f = 1kHz to 3.4kHz | ΔG$_{RF}$ | –1 | | 0 | dB |
| Gain change with current | I$_L$ = 14mA to 100mA | ΔG$_R$ | | | ±0.5 | dB |
| Gain deviation | T$_{amb}$ = –10°C to +60°C | ΔG$_R$ | | | ±0.5 | dB |
| Ear protection differential | I$_L$ ≥ 14mA, V$_{GEN}$ = 11V$_{rms}$ EA[0:4] = 15 | EP | | | 3 | V$_{rms}$ |
| MUTE suppression (earpiece disconnect from matrix) | I$_L$ = 14mA, I303 = 0 | ΔG$_R$ | 60 | | | dB |
| Output voltage d < 2% differential | I$_L$ = 14mA Z$_{ear}$ = 68nF + 100Ω EA[0:4] = 11 | | | 0.775 | | V$_{rms}$ |
| Maximum output current d < 2% | Z$_{ear}$ = 100Ω EA[0:4] = 31 | I$_{out}$ | 4 | | | mA$_p$ |
| Receiving noise psophometrically weighted | I$_L$ = 14mA Z$_{ear}$ = 68nF + 100Ω EA[0:4] = 15 | | | –79 | –76 | dBmp |
| Sidetone suppression | Z = 600Ω | | 20 | | | dB |
| Output resistance | Each output against GND | R$_o$ | | | 10 | Ω |
| Adjustment step: earpiece amplifier | DEA[0:4] = 1 for EA[0:4] = 2 to 31 | | 0.8 | 1 | 1.2 | dB |
| Adjustment step: AGARX | DAGARX[0:2] = 1 | | 0.8 | 1 | 1.2 | dB |
| Gain for DTMF signal | AMPB → RECO1/2 EA[0:4] = 1 | | | –10 | | dB |
| AC impedance | IMPH = 0 IMPH = 1 | Z$_{impl}$ Z$_{imph}$ | 595 980 | 625 1030 | 655 1080 | Ω Ω |

Note: 1. This is a period of time the bus requires from the end of a data transmission and before a new transmission can be started

# 18. Electrical Characteristics (Continued)

f = 1kHz, 0dBm = 775mV$_{rms}$, IVMIC = 0.3mA, IMP = 3mA, R$_{DC}$ = 1.3MΩ, T$_{amb}$ = 25°C, Z$_{ear}$ = 68nF + 100Ω, RLS = 50Ω, Z$_M$ = 68nF, resonator: f = 3.58MHz, all bits in reset condition, unless otherwise specified.

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DTMF, I$_L$ = 14 mA, ETX = I201 = 1, AGATX[0:2] = 7, DTMFM[0:2] = 4, DTMFF[0:4] = 0** | | | | | | |
| DTMF level at line (mid gain) | Sum level, 600Ω, DTMFM[0:2] = 4 | | –5.1 | –3.6 | –2.1 | dBm |
| DTMF level at line (low gain) | Sum level, 600Ω, DTMFM[0:2] = 5 | | –7.6 | –6.1 | –4.6 | dBm |
| DTMF level at line (high gain) | Sum level, 600Ω, DTMFM[0:2] = 6 AGATX[0:2] = 1 | | –5.2 | –3.7 | –2.2 | dBm |
| Pre-emphasis | 600Ω, DTMFF4 = 0 DTMFF4 = 1 | | 2<br>3 | 2.5<br>3.5 | 3<br>4 | dBm<br>dBm |
| **Speaker Amplifier, Differential Mode** **AMPB → SAO1/2** **ENSACL = ENSA = ENSAO = ENAM = I4O2 = 1, SA[0:4] = 31,** **ERX = ETX = ENMIC = ENSTBAL = I1O1 = I3O3 = 1** | | | | | | |
| Minimum line current for operation | ENAM = I4O2 = 0 SE = 0, I3O2 = 1 IMP 1mA, V$_{GEN}$ = 300mV | I$_{Lmin}$ | | | 11 | mA |
| Gain from AMPB to SAO | V$_{AMPB}$ = 3mV, I$_L$ = 15mA, SA[0:4] = 31 SA[0:4] = 0 | G$_{SA}$ | 36 | 37<br>–5.5 | 38 | dB |
| Adjustment step speaker amplifier | DSA[0:4] = –1 | | 1.15 | 1.35 | 1.55 | dB |
| Output power single ended | Load resistance: R$_{LS}$ = 50Ω V$_{AMPB}$ = 40mV, SE = 1 I$_L$ = 15mA I$_L$ = 20mA | P$_{SA}$<br>P$_{SA}$ | 3 | 7<br>20 | | mW<br>mW |
| Maximum output power differential | Load resistance: R$_L$ = 50Ω V$_{AMPB}$ = 60mV, SE = 0 V$_B$ = 5V | P$_{SA}$ | | 150 | | mW |
| Output noise (input AMPB open) psophometrically weighted | I$_L$ > 15mA | n$_{SA}$ | | | 240 | µV$_{psoph}$ |
| Gain deviation | I$_L$ = 15mA T$_{amb}$ = –10°C to +60°C | ΔG$_{SA}$ | | | ±1 | dB |
| Mute suppression | I$_L$ = 15mA, V$_L$ = 0dBm, V$_{AMPB}$ = 4mV I4O2 = 0 | VSAO | | | –56 | dBm |
| Gain change with current | I$_L$ = 15mA to 100mA | ΔG$_{SA}$ | | | 1 | dB |
| Gain change with frequency | I$_L$ = 15mA f = 1kHz to 3.4kHz | ΔG$_{SA}$ | –1 | | 0 | dB |
| Attack time of anti-clipping | 20dB overdrive | t$_r$ | | 2 | | ms |
| Release time of anti-clipping | | t$_f$ | | 170 | | ms |
| Adjustment step of charge current | ENSAO = 0, SE = 1 DLSCUR[0:1] = 1 | | –480 | –400 | –320 | µA |

Note:   1.   This is a period of time the bus requires from the end of a data transmission and before a new transmission can be started

## 18. Electrical Characteristics (Continued)

f = 1kHz, 0dBm = 775mV$_{rms}$, IVMIC = 0.3mA, IMP = 3mA, R$_{DC}$ = 1.3MΩ, T$_{amb}$ = 25°C, Z$_{ear}$ = 68nF + 100Ω,
RLS = 50Ω, Z$_M$ = 68nF, resonator: f = 3.58MHz, all bits in reset condition, unless otherwise specified.

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Adjustment step of discharge current | ENSAO = 0, SE = 0 DLSCUR[0:1] = 1 | | 320 | 400 | 480 | µA |
| Charge current Pin SAO2 | ENSAO = 0, SE = 1 LSCUR[0:1] = 3 | I$_{CHA}$ | −1.45 | −1.2 | −0.95 | mA |
| Discharge current pin SAO2 | ENSAO = 0, SE = 0 LSCUR[0:1] = 3 | I$_{DIS}$ | 0.95 | 1.2 | 1.45 | mA |
| **Microphone Amplifier, V$_B$ = 5V, V$_{MIC}$ = 2mV, V$_{MIC3}$ = 2mV, ENMIC = ENAM = I1O4 = 1, MICHF = 0** | | | | | | |
| Gain MIC amp.: MIC1/2 →AMREC | MICG[0:1] = 0 | | 17.4 | 18.1 | 18.8 | dB |
| | MICG[0:1] = 1 | | 23.2 | 23.7 | 24.6 | dB |
| | MICG[0:1] = 2 | | 29.1 | 29.8 | 30.5 | dB |
| | MICG[0:1] = 3 | | 35.0 | 35.7 | 36.4 | dB |
| MIC3 to AMREC | MICHF = 1, MICG[0:1] = 3 | | 35.0 | 35.7 | 36.5 | dB |
| Input suppression: MIC3 to MIC1/2 | MICG[0:1] = 0, MICHF = 0 | | 60 | | | dB |
| MIC1/2 to MIC3 | MICHF = 1 | | 60 | | | dB |
| Settling time offset cancellers | 5τ, FOFFC = 0 | | | 9 | 12 | ms |
| Settling time offset cancellers in speed-up mode | 5τ, FOFFC = 1 | | | 1.8 | 2.4 | ms |
| **AGC for Answering Machine, AMPB to AMREC, ENAM = ENAGC = I4O5 = I5O4 = 1** | | | | | | |
| Nominal gain | V$_{AMPB}$ = 5mV | | 23.5 | 25.5 | 27.5 | dB |
| Maximum output level | V$_{AMPB}$ = 50mV, d< 5% | | 240 | 300 | 360 | mVp |
| Attack time | 20dB overdrive | | | 1 | | ms |
| Release time | | | | 45 | | ms |
| **Switching Matrix, VL = 0, VB = 5V, ENAM = I4O4 = 1, V$_{AMPB}$ = 0.6V$_{rms}$** | | | | | | |
| Input impedance AMPB | | | 50 | 60 | 70 | kΩ |
| Gain AMPB to AMREC | | | −0.7 | −0.3 | +0.1 | dB |
| Maximum input level AMPB | I4O5 = I5O4 = 1, I4O4 = 0 | | | | 600 | mV |
| Maximum output level AMREC | I4O4 = 1 | | | | VB − 600mV | V$_{PP}$ |
| Offset | I4O4: 1 to 0 | ΔV$_{AMREC}$ | | | ±30 | mV |
| Mute switching matrix | I4O4 = 0 | | 60 | | | dB |
| **Power-on Reset VL = 0, V$_{MP}$ = 3.3V, V$_B$ = 5V, U4091 in Power-down Mode** | | | | | | |
| Power-on reset by ES VB high, VMP threshold | VB = 4V, ES = 4V, raise VMP until RESET goes to low | VMP$_{on}$ | 2.65 | 2.75 | 2.85 | V |
| Power-on reset by ES VMP high, VB threshold | VMP = 3V, ES = 4V, raise VB until RESET goes to low | VB$_{on}$ | | 3.2 | | V |

Note:   1.   This is a period of time the bus requires from the end of a data transmission and before a new transmission can be started

# 18. Electrical Characteristics (Continued)

f = 1kHz, 0dBm = 775mV$_{rms}$, IVMIC = 0.3mA, IMP = 3mA, R$_{DC}$ = 1.3MΩ, T$_{amb}$ = 25°C, Z$_{ear}$ = 68nF + 100Ω, RLS = 50Ω, Z$_M$ = 68nF, resonator: f = 3.58MHz, all bits in reset condition, unless otherwise specified.

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Low-voltage Interrupt<br>VL = 0, V$_{MP}$ = 3.3V, V$_B$ = 0V | | | | | | |
| VMP decreasing | Decrease VMP until INT returns to high | VLVI | 2.5 | 2.6 | 2.7 | V |
| Power-off Reset<br>VL = 0, V$_{MP}$ = 3.3V, V$_B$ = 0V | | | | | | |
| Low-voltage reset | Decrease VMP until RESET returns to low | VLVR | 2.35 | 2.45 | 2.55 | V |
| Difference voltage between low-voltage interrupt and reset | VLVI – VLVR | | 100 | 150 | | mV |
| Logical Part<br>V$_{MP}$ = 3.3V, V$_B$ = 5V | | | | | | |
| Output impedance at OSCOUT | | | 0.6 | 0.9 | 1.2 | kΩ |
| Pins SCL,<br>SDA (input mode)<br>Input leakage current | Low level<br>High level<br>0 < V$_i$ < V$_{MP}$ | | 0.8 × V$_{MP}$<br><br>–1 | | 0.2 × V$_{MP}$<br><br>+1 | V<br>V<br>µA |
| Pins INT,<br>SDA (output mode) | Output low<br>(resistance to GND) | | 150 | 230 | 350 | Ω |
| Switch for Additional Impedance (Pin IMPSW)<br>V$_{MP}$ = 3.3V, V$_B$ = 3V | | | | | | |
| Switch-off leakage current | 0 < V$_i$ < V$_{MP}$<br>IMPSW = 0 | | –0.5 | | 5 | µA |
| Resistance to GND | IMPSW = 1 | | | 50 | 80 | Ω |
| Maximum current | IMPSW = 1 | | –5 | | 5 | mA |
| AFS (Acoustic Feedback Suppression), I$_L$ = 14mA, V$_{GEN}$ = 300mV,<br>ERX = ETX = ENMIC = ENSTBAL = I1O1 = I3O3 = 1, SL[0:1] = 0, LF[0:3] = 1, P[0:4] = 31, AGARX[0:2] = 0 | | | | | | |
| Adjustment range of attenuation | I$_L$ ≥ 15mA | | 0 | | 50 | dB |
| Attenuation of transmit gain | I$_L$ ≥ 15mA, I$_{INLDT}$ = 0µA<br>I$_{INLDR}$ = 10µA | ΔG$_T$ | 47 | 50 | 53 | dB |
| Attenuation of speaker amplifier | I$_L$ ≥ 15mA, I$_{INLDT}$ = 10µA<br>I$_{INLDR}$ = 0µA | G$_{SA}$ | 47 | 50 | 53 | dB |
| Supply Voltages, V$_{MIC}$ = 25mV, T$_{amb}$ = –10°C to + 60°C | | | | | | |
| V$_{MP}$ | I$_L$ = 14mA, R$_{DC}$ = 680kΩ<br>I$_{MP}$ = 3mA | V$_{MP}$ | 3.1 | 3.3 | 3.5 | V |
| V$_{MPS}$ | I$_L$ = 100mA, R$_{DC}$ = inf.,<br>I$_{MP}$ = 0mA | V$_{MPS}$ | | | 5.5 | V |
| V$_{MIC}$ | I$_L$ = 14mA, R$_{DC}$ = 1.3MΩ<br>I$_M$ = 700A | V$_{MIC}$ | 1.5 | | 4 | V |
| V$_B$ | I$_B$ = +20mA, I$_L$ = 0mA | V$_B$ | | 5.5 | 6.3 | V |

Note: 1. This is a period of time the bus requires from the end of a data transmission and before a new transmission can be started

## 18. Electrical Characteristics (Continued)

$f = 1kHz$, $0dBm = 775mV_{rms}$, $IVMIC = 0.3mA$, $IMP = 3mA$, $R_{DC} = 1.3M\Omega$, $T_{amb} = 25°C$, $Z_{ear} = 68nF + 100\Omega$, $RLS = 50\Omega$, $Z_M = 68nF$, resonator: $f = 3.58MHz$, all bits in reset condition, unless otherwise specified.

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Ringing Power Converter, IMP = 1mA, IM = 0, $R_{IMPA}$ = 500k$\Omega$** | | | | | | |
| Maximum output power | $V_{RING}$ = 20.6V<br>ENSA = ENSAO = SE = 1 | $P_{SA}$ | | 15 | | mW |
| Threshold | $V_{RING}$: high to low | | | | 7.4 | V |
| | Low to high, RINGTH [0:3] = 0 | | 6.0 | 6.7 | 7.4 | V |
| | Low to high, RINGTH [0:3] = 15 | | 19 | 21 | 23 | V |
| Adjustment steps threshold | DRINGTH = 1 | | 0.8 | 1 | 1.2 | V |
| Input impedance | $V_{RING}$ = 30V | | 4.6 | 5.8 | 7.0 | k$\Omega$ |
| Maximum input voltage | | $V_{RINGmax}$ | 30 | | | V |
| **Serial Bus SCL, SDA, AS, VMP = 3.3V, RSDA = RSCL = RINT = 12k$\Omega$** | | | | | | |
| Input voltage<br>HIGH<br>LOW | SDA, SCL, INT | $V_{iBUS}$ | 3.0<br>0 | | $V_{DD}$<br>1.5 | V<br>V |
| Output voltage<br>Acknowledge LOW | SDA<br>$I_{SDA}$ = 3mA | $V_O$ | | | 0.4 | V |
| Clock frequency | SCL | $f_{SCL}$ | | | 100 | kHz |
| Rise time SDA, SCL | | $t_r$ | | | 1 | µs |
| Fall time SDA, SCL | | $t_f$ | | | 300 | ns |
| Period of SCL<br>HIGH<br>LOW | HIGH<br>LOW | $t_H$<br>$t_L$ | 4.0<br>4.7 | | | µs<br>µs |
| **Setup Time** | | | | | | |
| Start condition<br>Data<br>Stop condition<br>Time space[1] | | $t_{sSTA}$<br>$t_{sDAT}$<br>$t_{sSTOP}$<br>$t_{wSTA}$ | 4.7<br>250<br>4.7<br>4.7 | | | µs<br>ns<br>µs<br>µs |
| **Hold Time** | | | | | | |
| Start condition<br>DATA | | $t_{hSTA}$<br>$t_{hDAT}$ | 4.0<br>0 | | | µs<br>µs |

Note: 1. This is a period of time the bus requires from the end of a data transmission and before a new transmission can be started

**Figure 19-1. Basic Test Circuit**
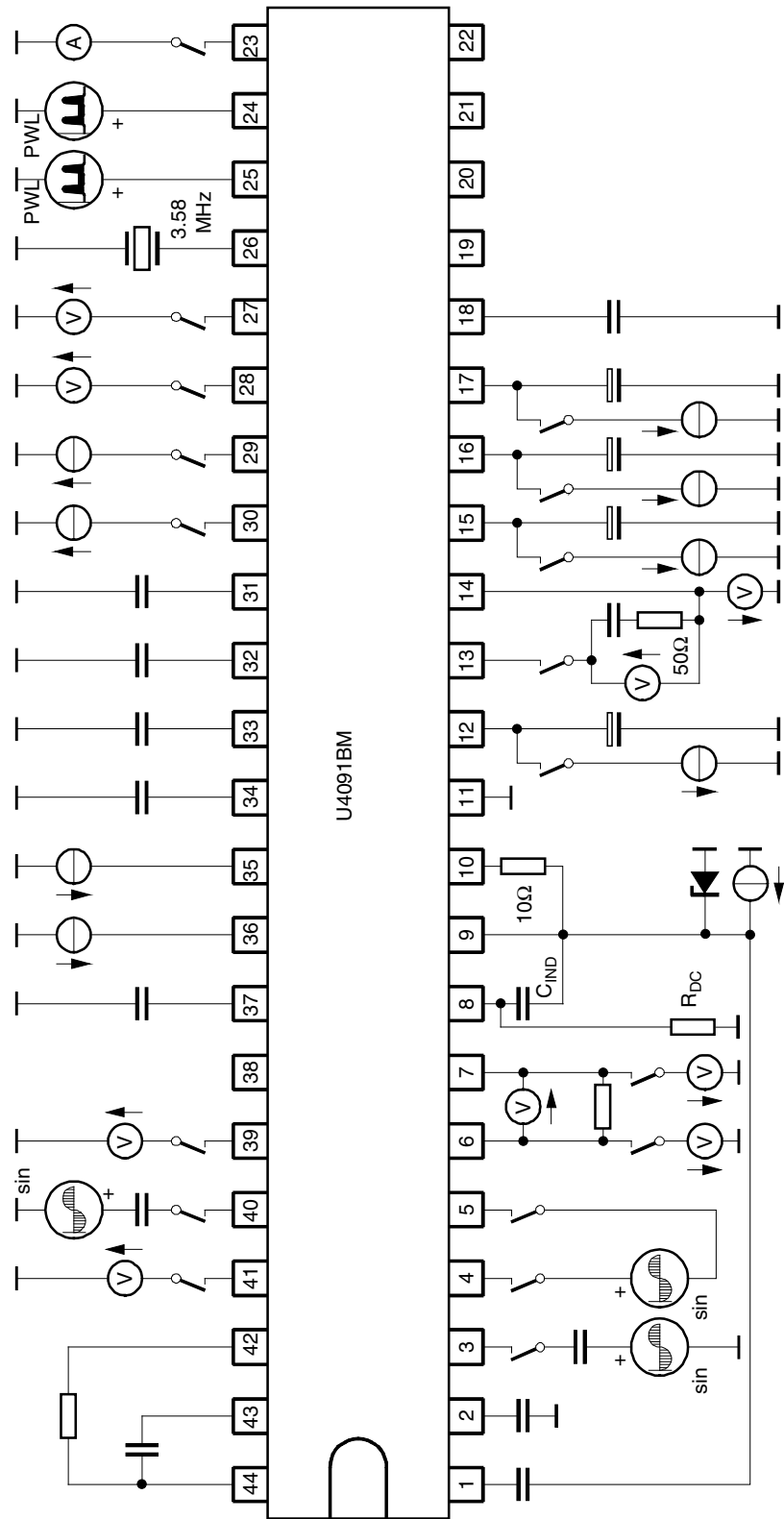
**Figure 19-2. Test Circuit for Ringing**
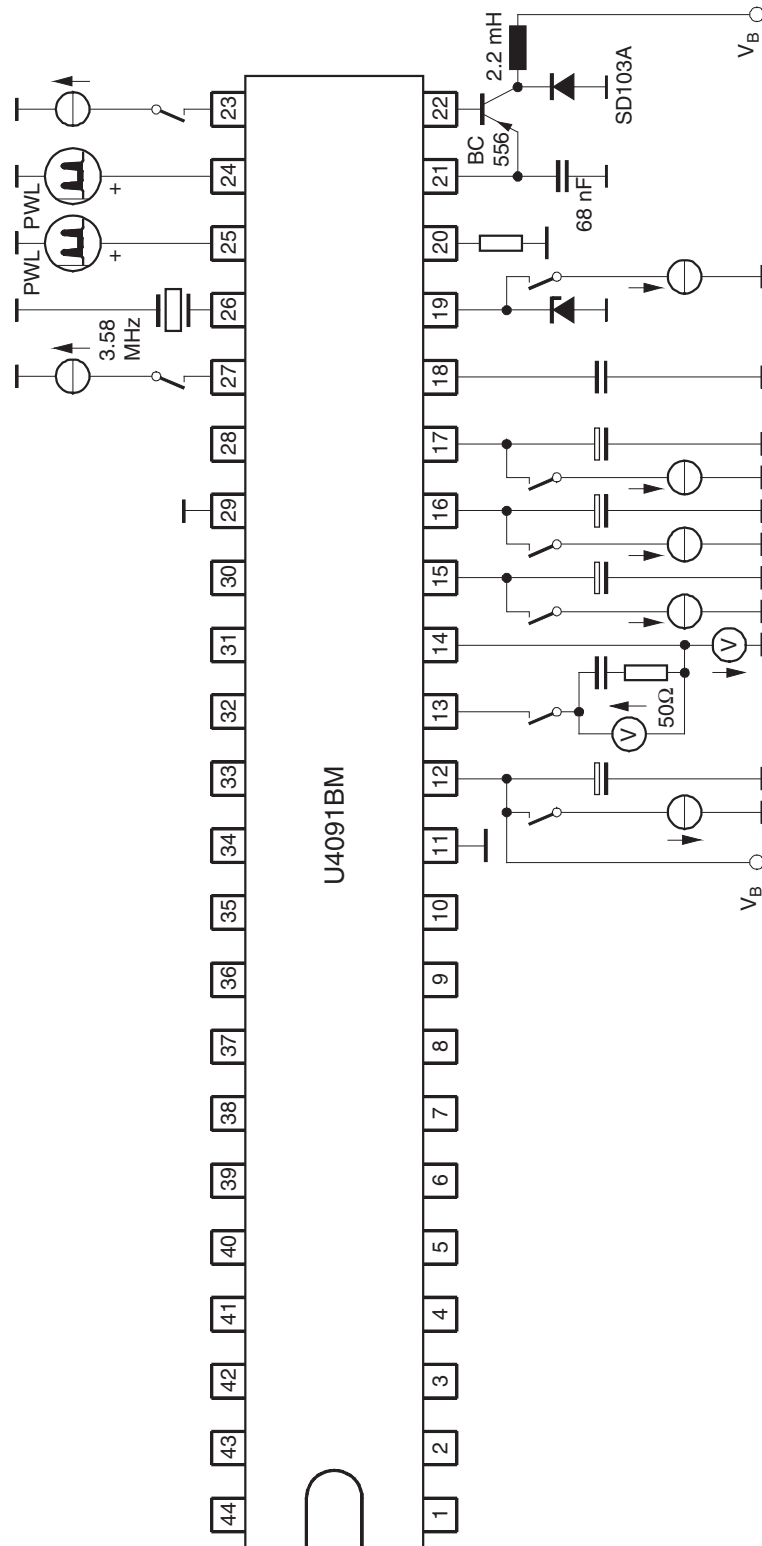
# 20.    Bus Timing

**Figure 20-1. Bus Timing Diagram**



SDA
SCL

P = Stop,  S = Start

$t_{wSTA}$  $t_{hSTA}$  $t_L$  $t_{hDAT}$  $t_H$  $t_{sSTA}$  $t_{hDAT}$  $t_{hSTA}$  $t_{sSTOP}$
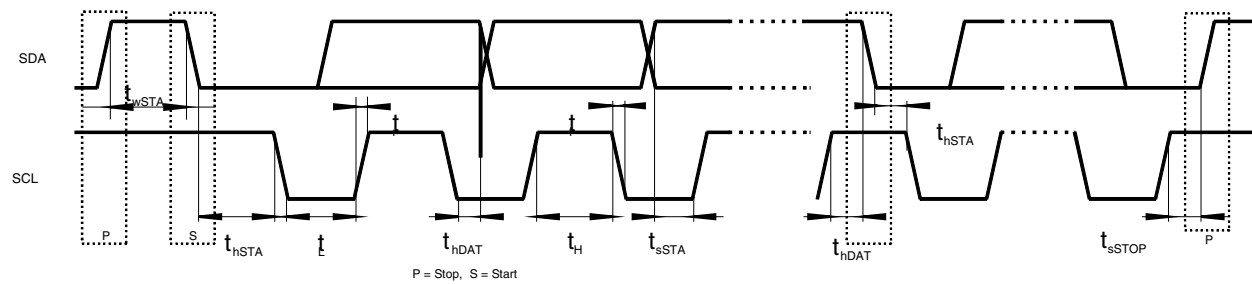
## 21. Ordering Information

| Extended Type Number | Package | Remarks |
|---|---|---|
| U4091BMC-RFNG3Y | SSO44 | Taped and reeled |
| T4091RC-DDB | Die | Die on foil |

## 22. Package Information

Package SSO44
Dimensions in mm



18.05
17.80

9.15
8.65

7.50
7.30

2.35

0.3

0.8

0.25
0.10

16.8

0.25

10.50
10.20

44

23

1

22
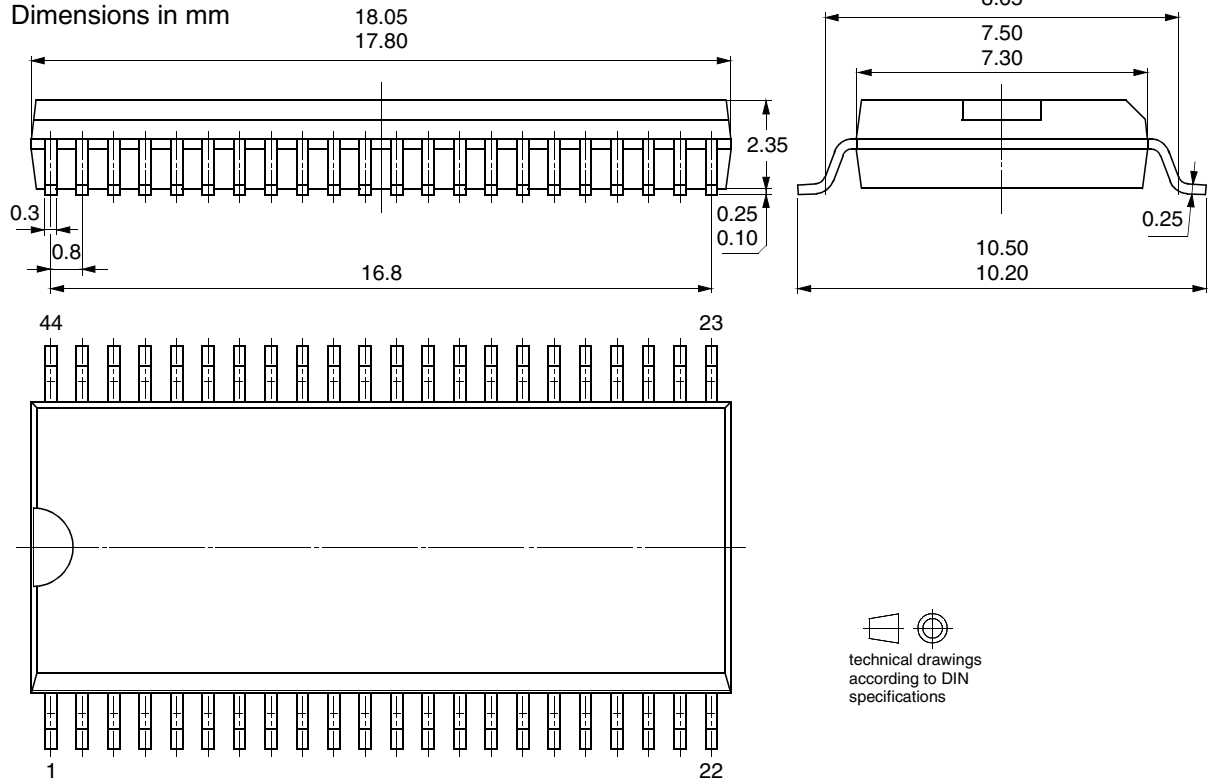
technical drawings
according to DIN
specifications

## 23. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

| Revision No. | History |
|---|---|
| 4872D-CORD-01/13 | • Section 18 "Electrical Characteristics" on pages 30 to 31 changed |
| 4872C-CORD-09/12 | • Section 21 "Ordering Information" on page 39 changed |
| 4872B-CORD-01/11 | • Section 21 "Ordering Information" on page 38 changed |