

74HC259; 74HCT259

8-bit addressable latch

Rev. 5 — 7 August 2012

Product data sheet

1. General description

The 74HC259; 74HCT259 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7-A.

The 74HC259; 74HCT259 are high-speed 8-bit addressable latches designed for general-purpose storage applications in digital systems. They are multifunctional devices capable of storing single-line data in eight addressable latches. They provide a 3-to-8 decoder and multiplexer function with active HIGH outputs (Q0 to Q7). They also incorporate an active LOW common reset ($\overline{\text{MR}}$) for resetting all latches as well as an active LOW enable input ($\overline{\text{LE}}$).

The 74HC259; 74HCT259 has four modes of operation:

- Addressable latch mode, in this mode data on the data line (D) is written into the addressed latch. The addressed latch follows the data input with all non-addressed latches remaining in their previous states.
- Memory mode, in this mode all latches remain in their previous states and are unaffected by the data or address inputs.
- Demultiplexing mode (or 3-to-8 decoding), in this mode the addressed output follows the state of the data input (D) with all other outputs in the LOW state.
- Reset mode, in this mode all outputs are LOW and unaffected by the address inputs (A0 to A2) and data input (D).

When operating the 74HC259; 74HCT259 as an address latch, changing more than one address bit could impose a transient wrong address. Therefore, this should only be done while in the Memory mode.

2. Features and benefits

- Combined demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- Input levels:
 - ◆ For 74HC259: CMOS level
 - ◆ For 74HCT259: TTL level



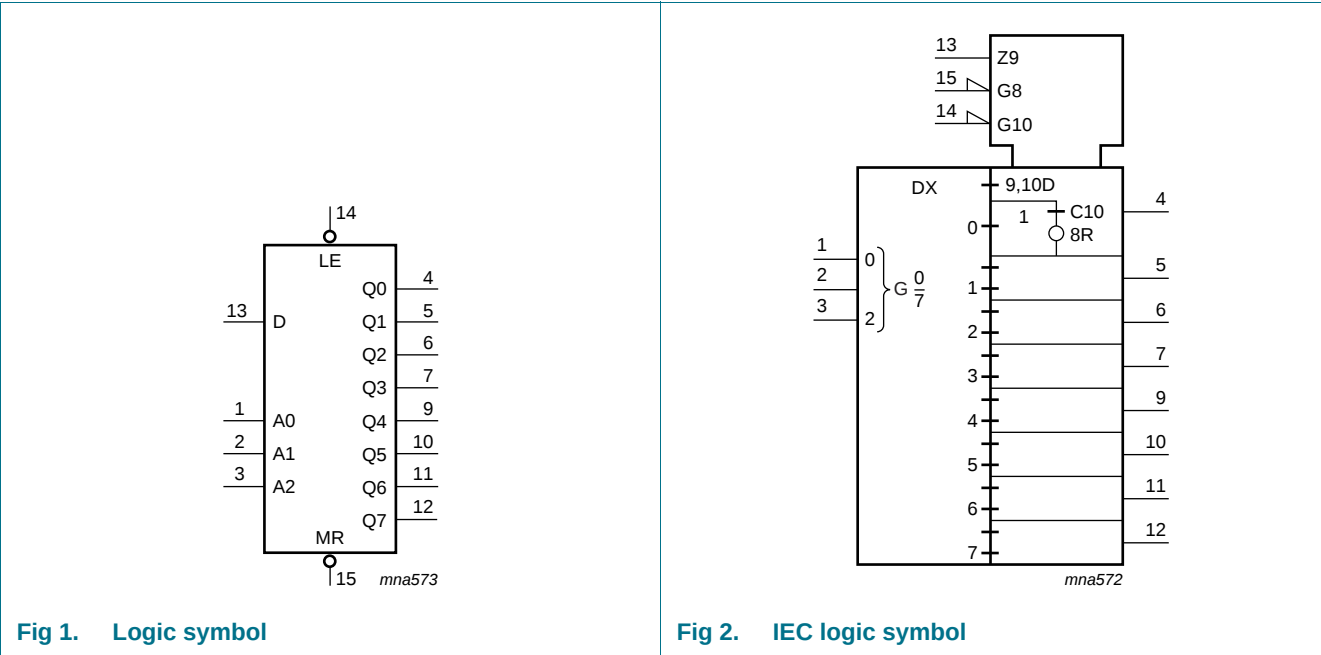
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22E exceeds 1000 V
- Multiple package options
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC259N	−40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT259N				
74HC259D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT259D				
74HC259DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT259DB				
74HC259PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT259PW				
74HC259BQ	−40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT259BQ				

4. Functional diagram



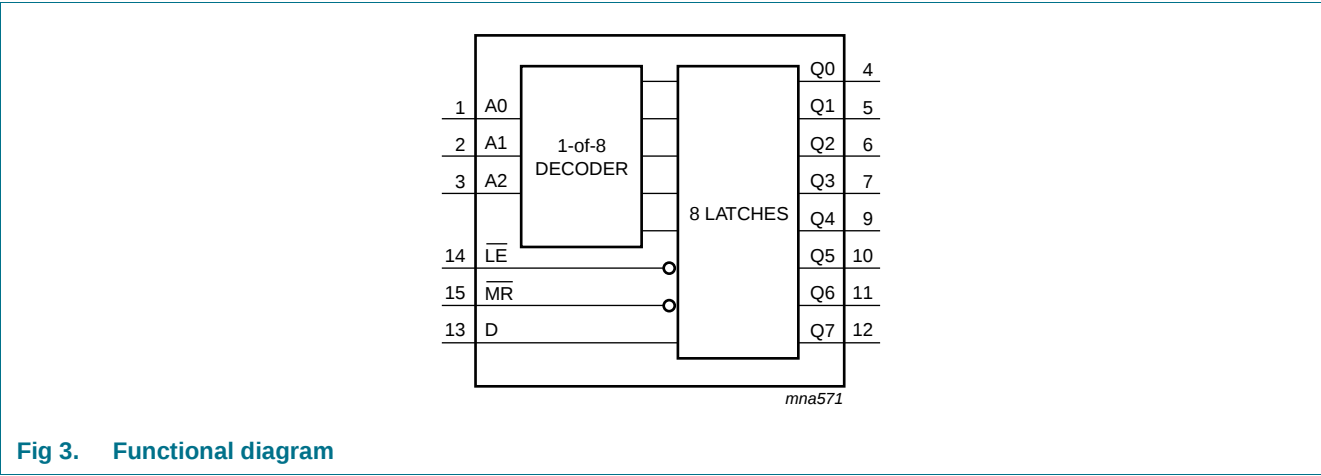


Fig 3. Functional diagram

5. Pinning information

5.1 Pinning

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5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A0, A1, A2	1, 2, 3	address input
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	4, 5, 6, 7, 9, 10, 11, 12	latch output
GND	8	ground (0 V)
D	13	data input
$\overline{\text{LE}}$	14	latch enable input (active LOW)
$\overline{\text{MR}}$	15	conditional reset input (active LOW)
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table^[1]

Operating mode	Input						Output							
	$\overline{\text{MR}}$	$\overline{\text{LE}}$	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Reset (clear)	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplexer (active HIGH 8-channel) decoder (when D = H)	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q = d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q = d	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	Q = d	L	L	L	L
	L	L	d	L	L	H	L	L	L	L	Q = d	L	L	L
	L	L	d	H	L	H	L	L	L	L	L	Q = d	L	L
	L	L	d	L	H	H	L	L	L	L	L	L	Q = d	L
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q = d
Memory (no action)	H	H	X	X	X	X	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
Addressable latch	H	L	d	L	L	L	Q = d	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	H	L	L	q ₀	Q = d	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	H	L	q ₀	q ₁	Q = d	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	H	H	L	q ₀	q ₁	q ₂	Q = d	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	L	H	q ₀	q ₁	q ₂	q ₃	Q = d	q ₅	q ₆	q ₇
	H	L	d	H	L	H	q ₀	q ₁	q ₂	q ₃	q ₄	Q = d	q ₆	q ₇
	H	L	d	L	H	H	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	Q = d	q ₇
	H	L	d	H	H	H	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	Q = d

[1] H = HIGH voltage level;

L = LOW voltage level;

X = don't care;

d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH $\overline{\text{LE}}$ transition;

q = lower case letter indicates the state of the referenced input one set-up time prior to the LOW-to-HIGH transition.

Table 4. Operating mode select table^[1]

LE	MR	Mode
L	H	Addressable latch mode
H	H	Memory mode
L	L	Demultiplexer mode
H	L	Reset mode

[1] H = HIGH voltage level; L = LOW voltage level.

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	^[1] -	±20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	^[1] -	±20	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	±25	mA
I_{CC}	supply current		-	+70	mA
I_{GND}	ground current		-70	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$			
		DIP16 package	^[2] -	750	mW
		SO16 package	^[3] -	500	mW
		(T)SSOP16 package	^[4] -	500	mW
		DHVQFN16 package	^[5] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[5] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC259			74HCT259			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC259										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = −20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = −20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = −20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = −4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = −5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT259										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = –20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = –4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI _{CC}	additional supply current	V _I = V _{CC} – 2.1 V; I _O = 0 A; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V								
		pin An, $\overline{\text{LE}}$	-	150	540	-	675	-	735	µA
		pin D	-	120	432	-	540	-	588	µA
		pin $\overline{\text{MR}}$	-	75	270	-	338	-	368	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
74HC259										
t _{pd}	propagation delay	D to Qn; see Figure 6 ^[2]								
		V _{CC} = 2.0 V	-	58	185	-	230	-	280	ns
		V _{CC} = 4.5 V	-	21	37	-	46	-	56	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	18	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	17	31	-	39	-	48	ns
		An to Qn; see Figure 7 ^[2]								
		V _{CC} = 2.0 V	-	58	185	-	230	-	280	ns
		V _{CC} = 4.5 V	-	21	37	-	46	-	56	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	17	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	17	31	-	39	-	48	ns
		$\overline{\text{LE}}$ to Qn; see Figure 8 ^[2]								
		V _{CC} = 2.0 V	-	55	170	-	215	-	255	ns
		V _{CC} = 4.5 V	-	20	34	-	43	-	51	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	17	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	16	29	-	37	-	43	ns
t _{PHL}	HIGH to LOW propagation delay	$\overline{\text{MR}}$ to Qn; see Figure 9								
		V _{CC} = 2.0 V	-	50	155	-	195	-	235	ns
		V _{CC} = 4.5 V	-	18	31	-	39	-	47	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	15	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	14	26	-	33	-	40	ns
t _t	transition time	see Figure 8 ^[3]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	119	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t _w	pulse width	$\overline{\text{LE}}$ HIGH or LOW; see Figure 8								
		V _{CC} = 2.0 V	70	17	-	90	-	105	-	ns
		V _{CC} = 4.5 V	14	6	-	18	-	21	-	ns
		V _{CC} = 6.0 V	12	5	-	15	-	18	-	ns
		$\overline{\text{MR}}$ LOW; see Figure 9								
		V _{CC} = 2.0 V	70	17	-	90	-	105	-	ns
		V _{CC} = 4.5 V	14	6	-	18	-	21	-	ns
V _{CC} = 6.0 V	12	5	-	15	-	18	-	ns		

Table 8. Dynamic characteristics ...continuedVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
t _{su}	set-up time	D, An to $\overline{\text{LE}}$; see Figure 10 and Figure 11								
		V _{CC} = 2.0 V	80	19	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t _h	hold time	D to $\overline{\text{LE}}$; see Figure 10 and Figure 11								
		V _{CC} = 2.0 V	0	–19	-	0	-	0	-	ns
		V _{CC} = 4.5 V	0	–6	-	0	-	0	-	ns
		V _{CC} = 6.0 V	0	–5	-	0	-	0	-	ns
		An to $\overline{\text{LE}}$; see Figure 10 and Figure 11								
		V _{CC} = 2.0 V	2	–11	-	2	-	2	-	ns
		V _{CC} = 4.5 V	2	–4	-	2	-	2	-	ns
		V _{CC} = 6.0 V	2	–3	-	2	-	2	-	ns
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC}	[4]	-	19	-	-	-	-	pF

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t _{pd}	propagation delay	D to Qn; see Figure 6	[2]							
		V _{CC} = 4.5 V	-	23	39	-	49	-	59	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	20	-	-	-	-	-	ns
		An to Qn; see Figure 7	[2]							
		V _{CC} = 4.5 V	-	25	41		51		62	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	20	-	-	-	-	-	ns
		$\overline{\text{LE}}$ to Qn; see Figure 8	[2]							
		V _{CC} = 4.5 V	-	22	38	-	48	-	57	ns
t _{PHL}	HIGH to LOW propagation delay	$\overline{\text{MR}}$ to Qn; see Figure 9								
		V _{CC} = 4.5 V	-	23	39	-	49	-	59	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	20	-	-	-	-	-	ns
t _t	transition time	see Figure 8	[3]							
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t _w	pulse width	$\overline{\text{LE}}$ HIGH or LOW; see Figure 8								
		V _{CC} = 4.5 V	19	11	-	24	-	29	-	ns
		$\overline{\text{MR}}$ LOW; see Figure 9								
		V _{CC} = 4.5 V	18	10	-	23	-	27	-	ns

Table 8. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
t_{su}	set-up time	D, An to $\overline{LE}$; see Figure 10 and Figure 11 $V_{CC} = 4.5\text{ V}$	17	10	-	21	-	26	-	ns
t_h	hold time	D to $\overline{LE}$; see Figure 10 and Figure 11 $V_{CC} = 4.5\text{ V}$	0	–8	-	0	-	0	-	ns
		An to $\overline{LE}$; see Figure 10 and Figure 11 $V_{CC} = 4.5\text{ V}$	0	–4	-	0	-	0	-	ns
		$f_i = 1\text{ MHz}$; $V_i = \text{GND to } V_{CC} - 1.5\text{ V}$	-	19	-	-	-	-	-	pF
C_{PD}	power dissipation capacitance									

[1] Typical values are measured at nominal supply voltage ($V_{CC} = 3.3\text{ V}$ and $V_{CC} = 5.0\text{ V}$).

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] t_t is the same as t_{THL} and t_{TLH} .

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

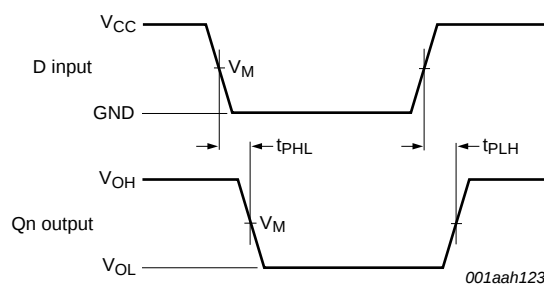
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

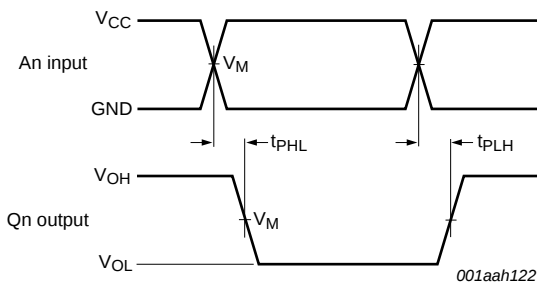
11. Waveforms



Measurement points are given in [Table 9](#).

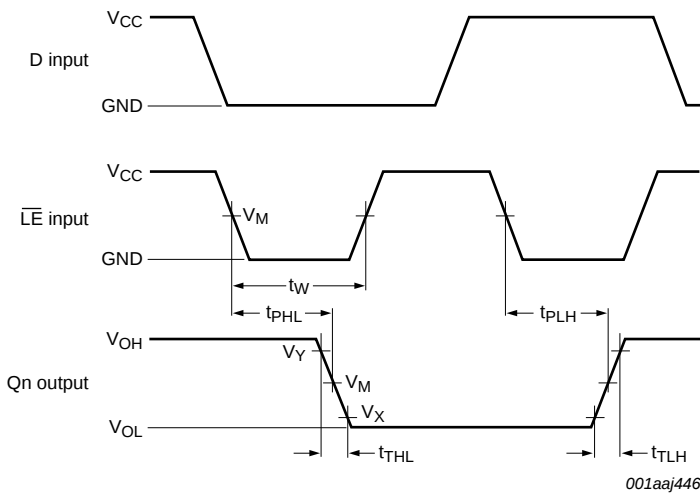
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Data input to output propagation delays



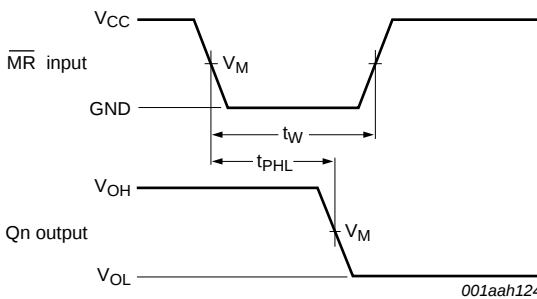
Measurement points are given in [Table 9](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Address input to output propagation delays



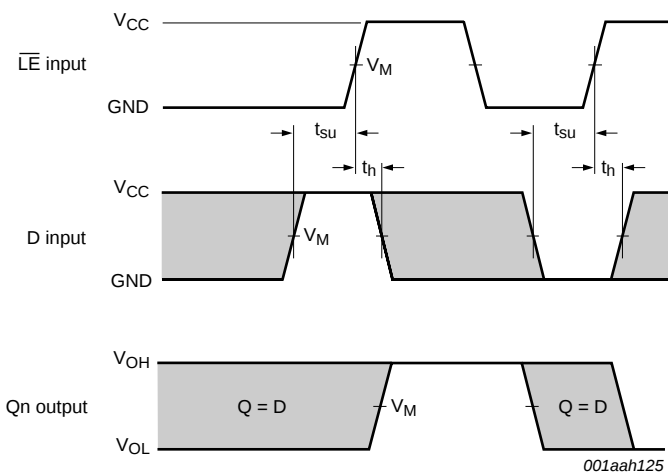
Measurement points are given in [Table 9](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Enable input to output propagation delays and pulse width



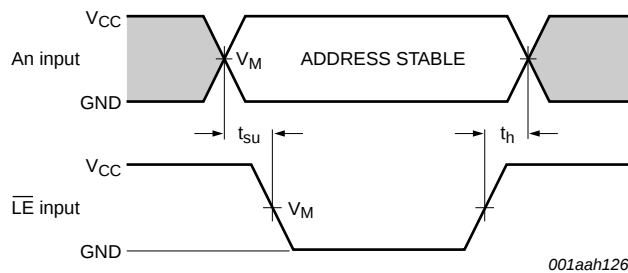
Measurement points are given in [Table 9](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 9. Master reset input to output propagation delays



Measurement points are given in [Table 9](#).
The shaded areas indicate when the input is permitted to change for predictable output performance.
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 10. Data input to latch enable input set-up and hold times



Measurement points are given in [Table 9](#).
The shaded areas indicate when the input is permitted to change for predictable output performance.
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 11. Address input to latch enable input set-up and hold times

Table 9. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC259	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT259	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$

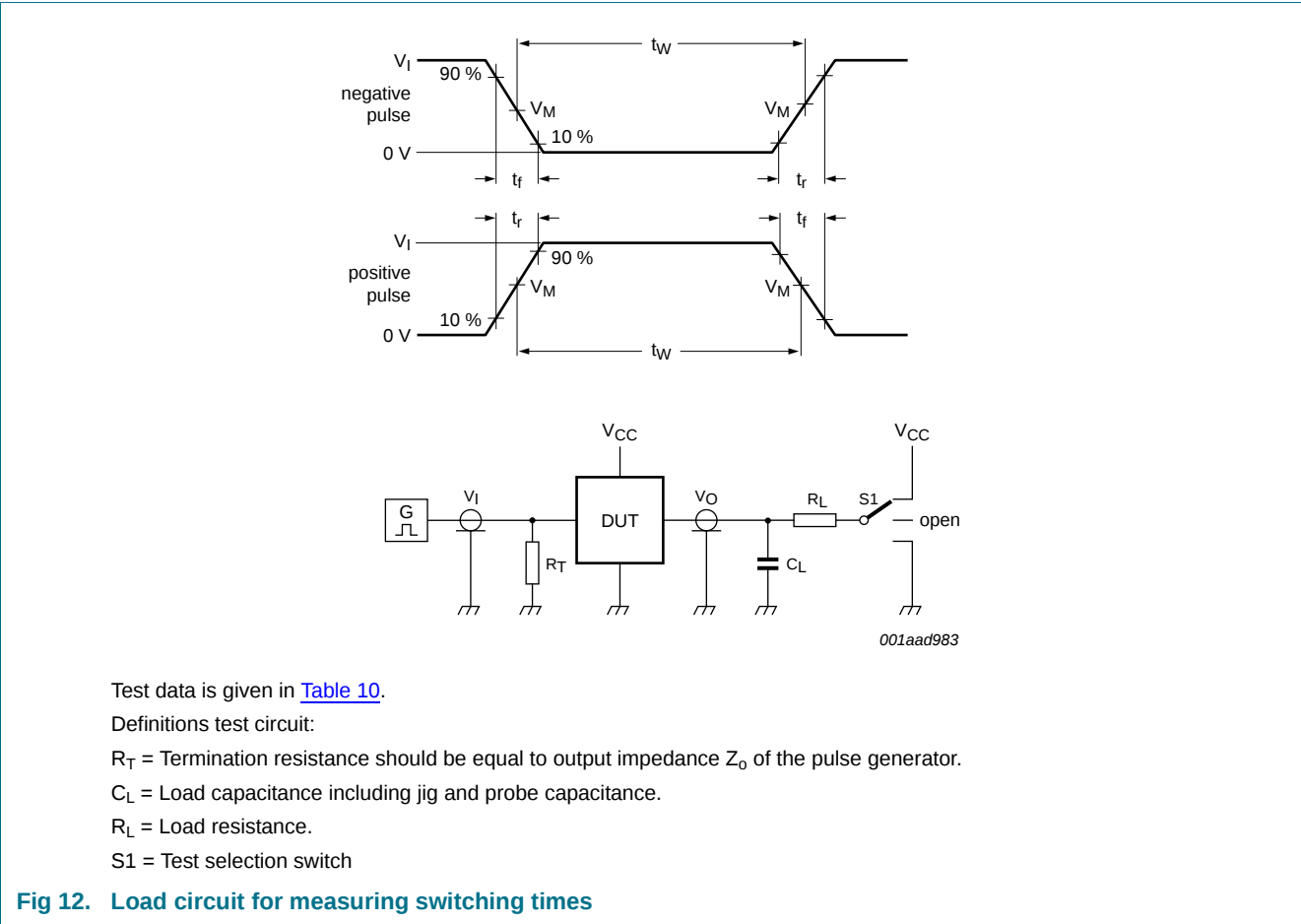


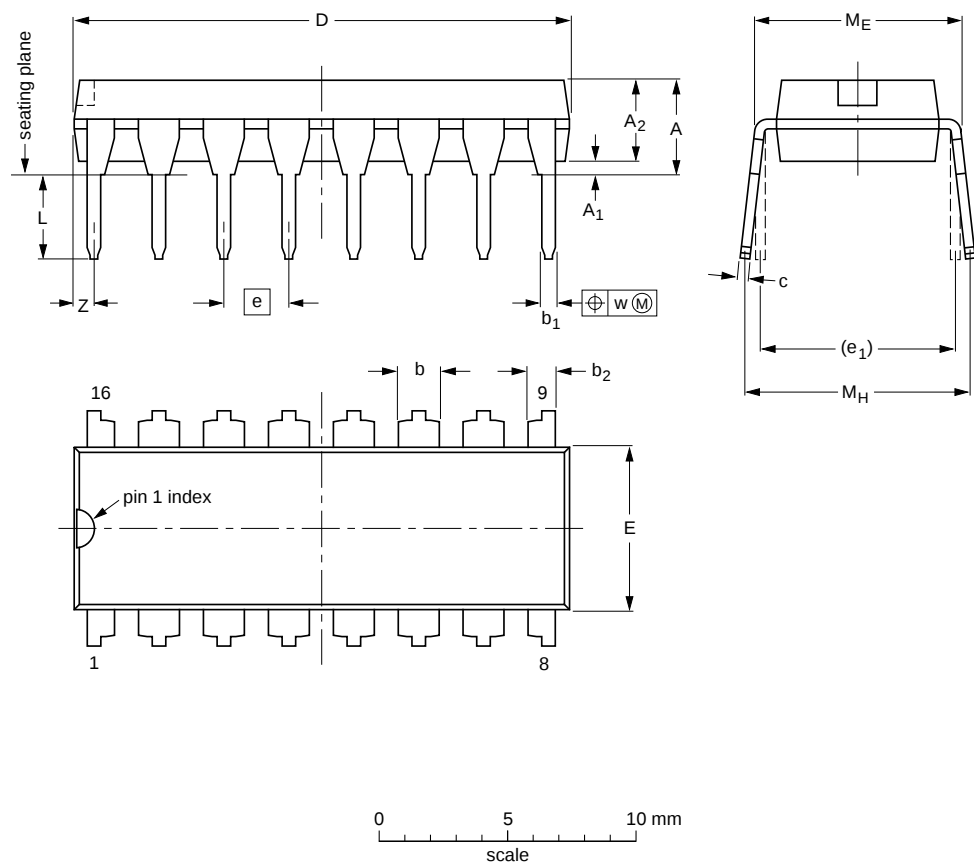
Table 10. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC259	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open
74HCT259	3 V	6 ns	15 pF, 50 pF	1 k Ω	open

12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)																
UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

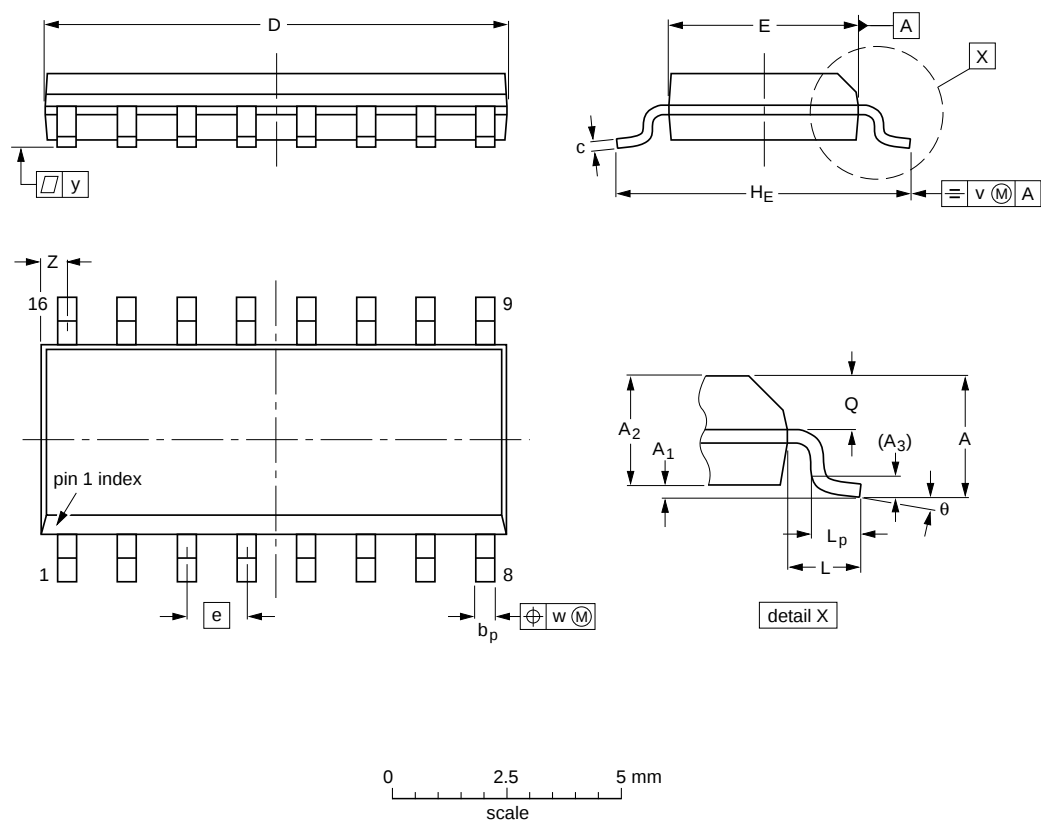
Note
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						95-01-14- 03-02-13

Fig 13. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig 14. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

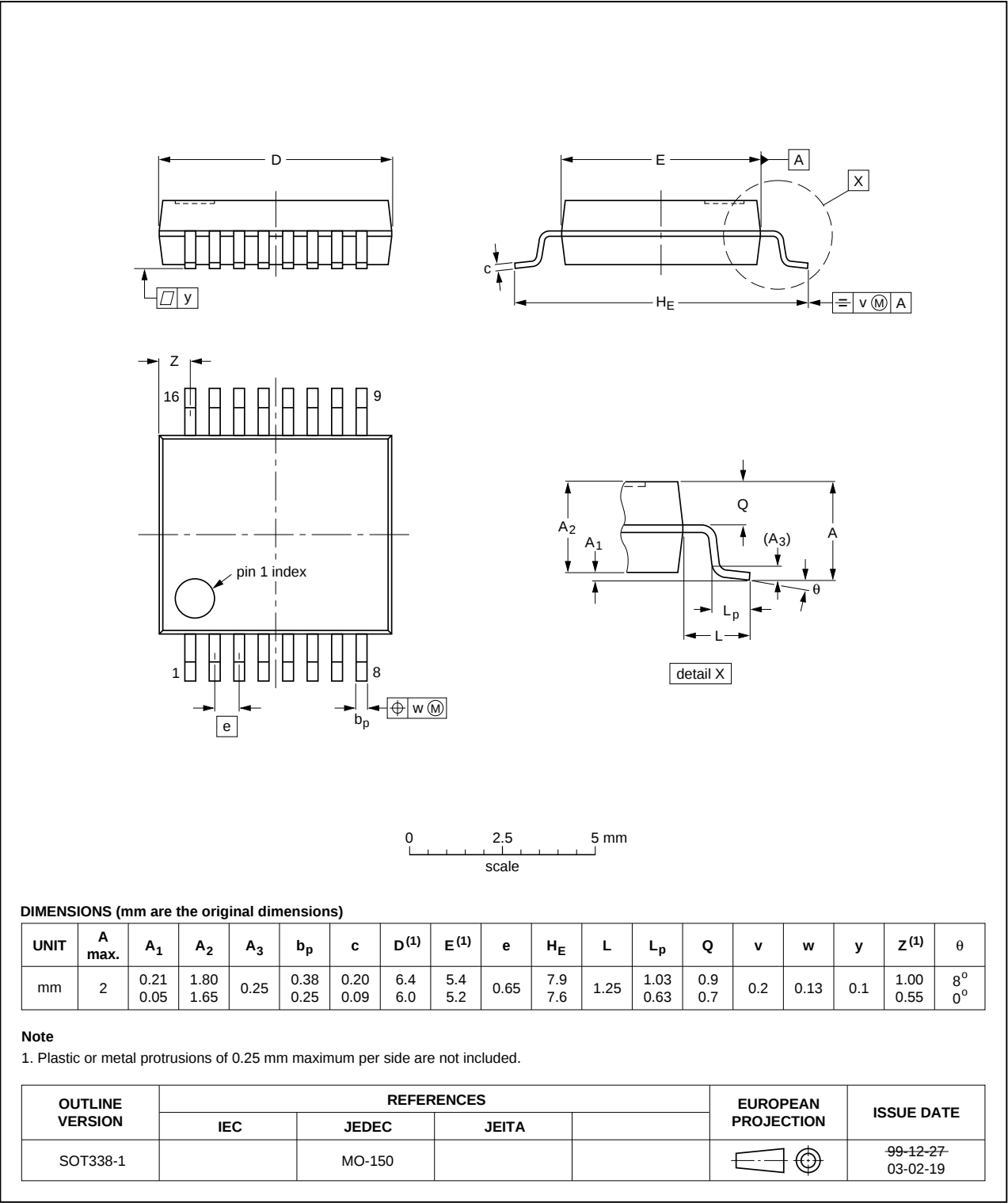


Fig 15. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

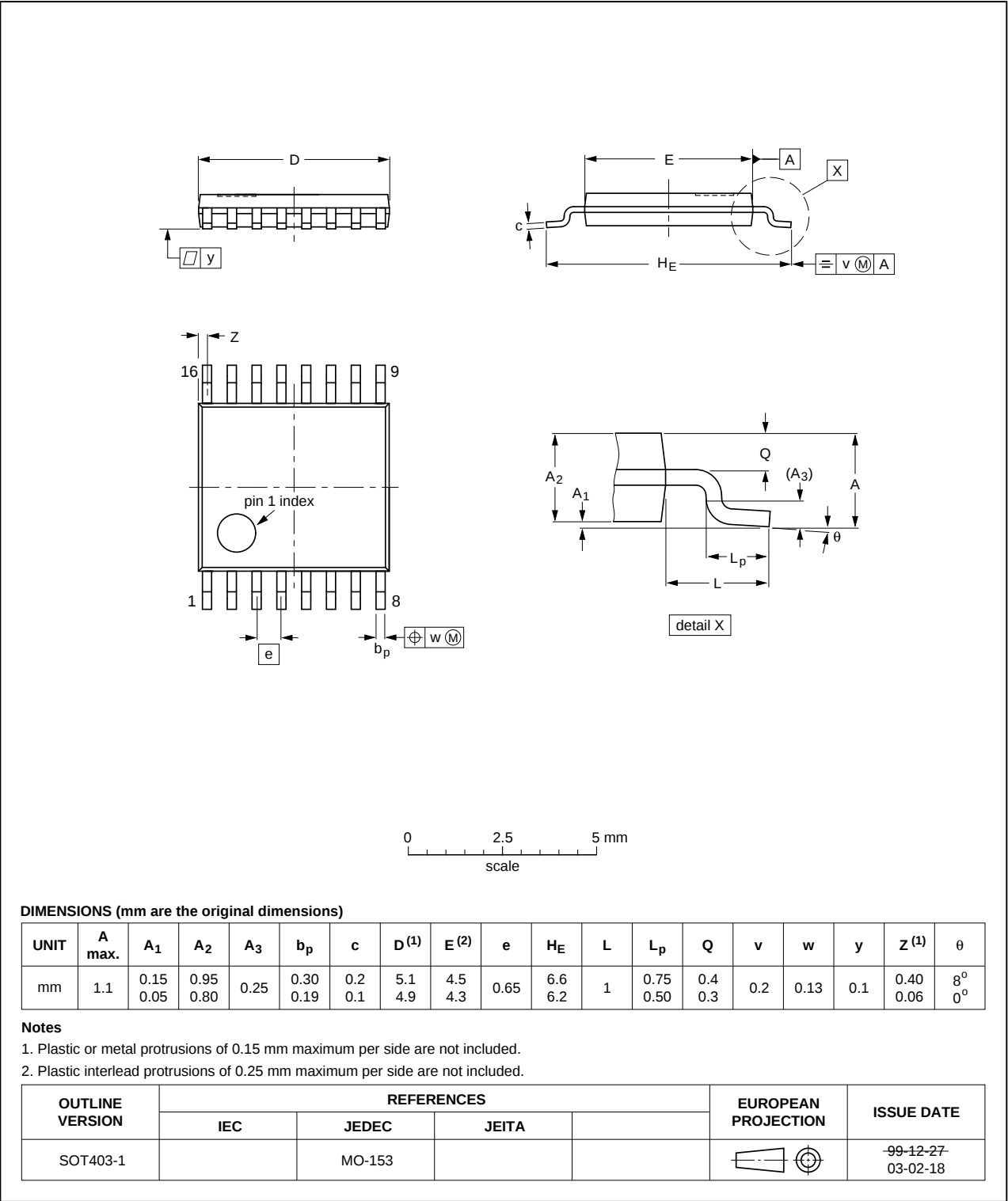


Fig 16. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm
SOT763-1

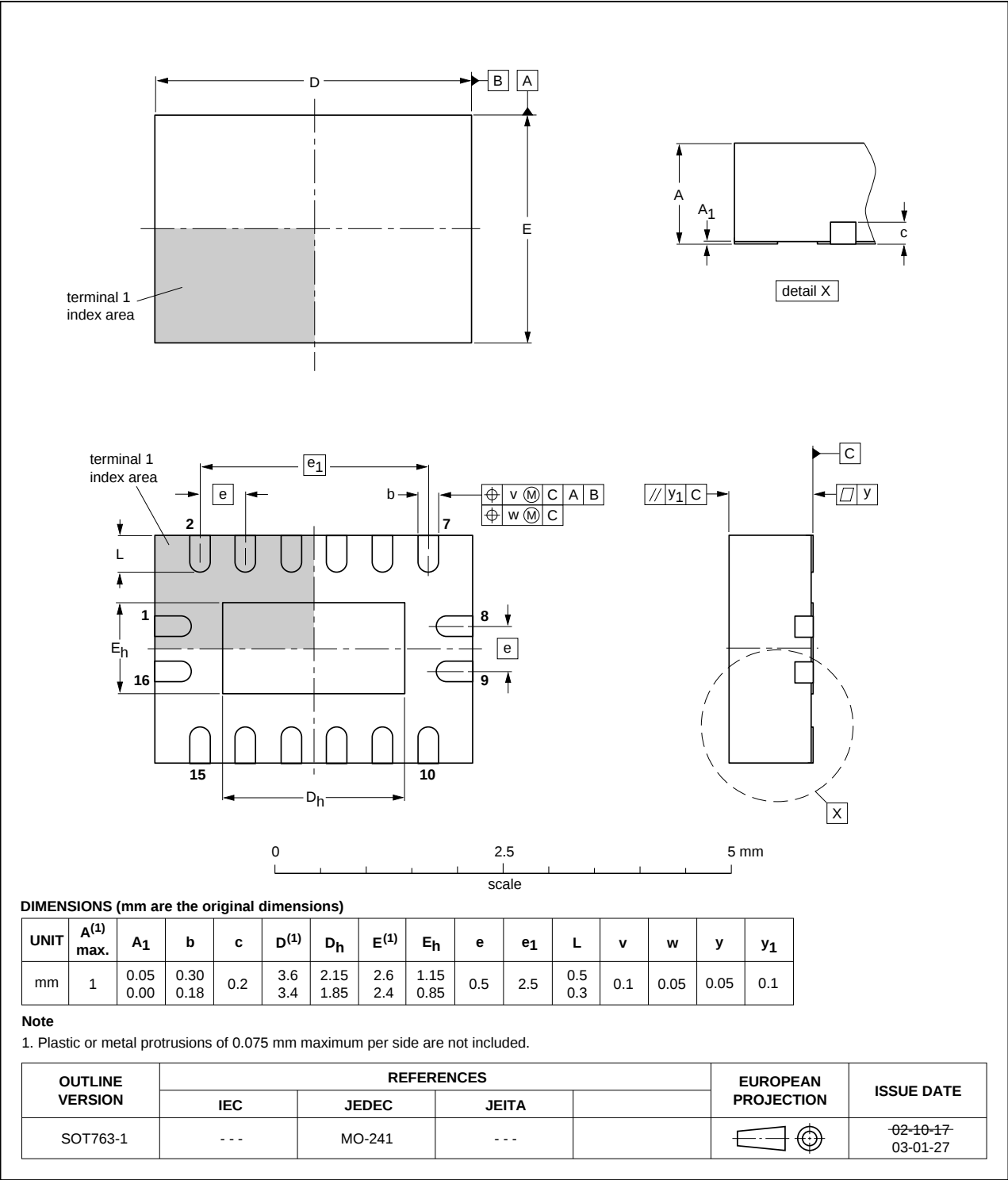


Fig 17. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT259 v.5	20120807	Product data sheet	-	74HC_HCT259 v.4
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT259 v.4	20090225	Product data sheet	-	74HC_HCT259 v.3
Modifications:	- Added type number 74HC259N and 74HCT259N (DIP16 package) - Added type number 74HC259DB and 74HCT259DB (SSOP16 package)			
74HC_HCT259 v.3	20090108	Product data sheet	-	74HC_HCT259_CNV v.2
74HC_HCT259_CNV v.2	19970828	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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