

# N-channel TrenchMOS™ transistor

## Logic level FET

PHP87N03LT, PHB87N03LT  
PHD87N03LT

### FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Low thermal resistance
- Logic level compatible

### SYMBOL



### QUICK REFERENCE DATA

|                                                                        |
|------------------------------------------------------------------------|
| $V_{DSS} = 25 \text{ V}$                                               |
| $I_D = 75 \text{ A}$                                                   |
| $R_{DS(ON)} \leq 9.5 \text{ m}\Omega \text{ (} V_{GS} = 10 \text{ V)}$ |
| $R_{DS(ON)} \leq 10.5 \text{ m}\Omega \text{ (} V_{GS} = 5 \text{ V)}$ |

### GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using 'trench' technology.

#### Applications:-

- High frequency computer motherboard d.c. to d.c. converters
- High current switching

The PHP87N03LT is supplied in the SOT78 (TO220AB) conventional leaded package.

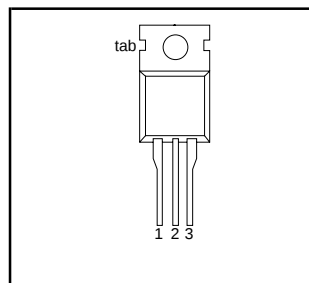
The PHB87N03LT is supplied in the SOT404 (D<sup>2</sup>PAK) surface mounting package.

The PHD87N03LT is supplied in the SOT428 (DPAK)surface mounting package.

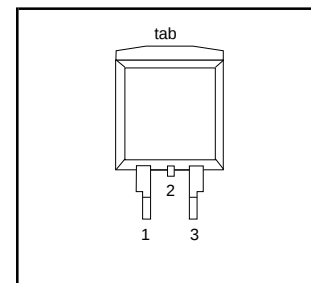
### PINNING

| PIN | DESCRIPTION        |
|-----|--------------------|
| 1   | gate               |
| 2   | drain <sup>1</sup> |
| 3   | source             |
| tab | drain              |

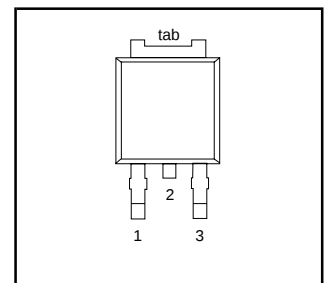
#### SOT78 (TO220AB)



#### SOT404 (D<sup>2</sup>PAK)



#### SOT428 (DPAK)



### LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL         | PARAMETER                                  | CONDITIONS                                                                  | MIN. | MAX.     | UNIT             |
|----------------|--------------------------------------------|-----------------------------------------------------------------------------|------|----------|------------------|
| $V_{DSS}$      | Drain-source voltage                       | $T_j = 25^\circ\text{C to } 175^\circ\text{C}$                              | -    | 25       | V                |
| $V_{DGR}$      | Drain-gate voltage                         | $T_j = 25^\circ\text{C to } 175^\circ\text{C}; R_{GS} = 20 \text{ k}\Omega$ | -    | 25       | V                |
| $V_{GS}$       | Gate-source voltage (DC)                   |                                                                             | -    | $\pm 15$ | V                |
| $V_{GSM}$      | Gate-source voltage (pulse peak value)     | $T_j \leq 150^\circ\text{C}$                                                | -    | $\pm 20$ | V                |
| $I_D$          | Drain current (DC)                         | $T_{mb} = 25^\circ\text{C}$                                                 | -    | 75       | A                |
|                |                                            | $T_{mb} = 100^\circ\text{C}$                                                | -    | 61       | A                |
| $I_{DM}$       | Drain current (pulse peak value)           | $T_{mb} = 25^\circ\text{C}$                                                 | -    | 240      | A                |
| $P_{tot}$      | Total power dissipation                    | $T_{mb} = 25^\circ\text{C}$                                                 | -    | 142      | W                |
| $T_j, T_{stg}$ | Operating junction and storage temperature |                                                                             | - 55 | 175      | $^\circ\text{C}$ |

<sup>1</sup> It is not possible to make connection to pin:2 of the SOT404 or SOT428 packages.

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### THERMAL RESISTANCES

| SYMBOL         | PARAMETER                                    | CONDITIONS                                                                             | MIN. | TYP. | MAX. | UNIT |
|----------------|----------------------------------------------|----------------------------------------------------------------------------------------|------|------|------|------|
| $R_{th\ j-mb}$ | Thermal resistance junction to mounting base |                                                                                        | -    | -    | 1.05 | K/W  |
| $R_{th\ j-a}$  | Thermal resistance junction to ambient       | SOT78 package, in free air<br>SOT404 or SOT428 package, pcb mounted, minimum footprint | -    | 60   | -    | K/W  |
|                |                                              |                                                                                        | -    | 50   | -    | K/W  |

### AVALANCHE LIMITING VALUE

| SYMBOL    | PARAMETER                                                       | CONDITIONS                                                                                                                   | MIN. | MAX. | UNIT |
|-----------|-----------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------|------|------|------|
| $W_{DSS}$ | Drain-source non-repetitive unclamped inductive turn-off energy | $I_D = 45\text{ A}$ ; $V_{DD} \leq 15\text{ V}$ ;<br>$V_{GS} = 5\text{ V}$ ; $R_{GS} = 50\ \Omega$ ; $T_{mb} = 25\text{ °C}$ | -    | 200  | mJ   |

### ELECTRICAL CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified

| SYMBOL        | PARAMETER                        | CONDITIONS                                                                                                                                                         | MIN.          | TYP.          | MAX.                | UNIT                                   |
|---------------|----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------------|---------------------|----------------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage   | $V_{GS} = 0\text{ V}$ ; $I_D = 0.25\text{ mA}$ ;<br>$T_j = -55\text{ °C}$                                                                                          | 25<br>22      | -<br>-        | -<br>-              | V<br>V                                 |
| $V_{GS(TO)}$  | Gate threshold voltage           | $V_{DS} = V_{GS}$ ; $I_D = 1\text{ mA}$ ;<br>$T_j = 175\text{ °C}$<br>$T_j = -55\text{ °C}$                                                                        | 1<br>0.5<br>- | 1.5<br>-<br>- | 2<br>-<br>2.3       | V<br>V<br>V                            |
| $R_{DS(ON)}$  | Drain-source on-state resistance | $V_{GS} = 5\text{ V}$ ; $I_D = 25\text{ A}$<br>$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$<br>$V_{GS} = 5\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 175\text{ °C}$ | -<br>-<br>-   | 9<br>8.5<br>- | 10.5<br>9.5<br>19.5 | m $\Omega$<br>m $\Omega$<br>m $\Omega$ |
| $g_{fs}$      | Forward transconductance         | $V_{DS} = 25\text{ V}$ ; $I_D = 25\text{ A}$                                                                                                                       | 12            | 51            | -                   | S                                      |
| $I_{GSS}$     | Gate source leakage current      | $V_{GS} = \pm 5\text{ V}$ ; $V_{DS} = 0\text{ V}$                                                                                                                  | -             | 10            | 100                 | nA                                     |
| $I_{DSS}$     | Zero gate voltage drain current  | $V_{DS} = 25\text{ V}$ ; $V_{GS} = 0\text{ V}$ ;<br>$T_j = 175\text{ °C}$                                                                                          | -             | 0.05          | 10                  | $\mu\text{A}$                          |
|               |                                  |                                                                                                                                                                    | -             | -             | 500                 | $\mu\text{A}$                          |
| $Q_{g(tot)}$  | Total gate charge                | $I_D = 75\text{ A}$ ; $V_{DD} = 15\text{ V}$ ; $V_{GS} = 5\text{ V}$                                                                                               | -             | 39            | -                   | nC                                     |
| $Q_{gs}$      | Gate-source charge               |                                                                                                                                                                    | -             | 9             | -                   | nC                                     |
| $Q_{gd}$      | Gate-drain (Miller) charge       |                                                                                                                                                                    | -             | 18.5          | -                   | nC                                     |
| $t_{d\ on}$   | Turn-on delay time               | $V_{DD} = 15\text{ V}$ ; $I_D = 25\text{ A}$ ;<br>$V_{GS} = 10\text{ V}$ ; $R_G = 5\ \Omega$                                                                       | -             | 9             | 15                  | ns                                     |
| $t_r$         | Turn-on rise time                |                                                                                                                                                                    | -             | 54            | 70                  | ns                                     |
| $t_{d\ off}$  | Turn-off delay time              | Resistive load                                                                                                                                                     | -             | 136           | 160                 | ns                                     |
| $t_f$         | Turn-off fall time               |                                                                                                                                                                    | -             | 85            | 100                 | ns                                     |
| $L_d$         | Internal drain inductance        | Measured tab to centre of die                                                                                                                                      | -             | 3.5           | -                   | nH                                     |
| $L_d$         | Internal drain inductance        | Measured from drain lead to centre of die (SOT78 package only)                                                                                                     | -             | 4.5           | -                   | nH                                     |
| $L_s$         | Internal source inductance       | Measured from source lead to source bond pad                                                                                                                       | -             | 7.5           | -                   | nH                                     |
| $C_{iss}$     | Input capacitance                | $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$ ; $f = 1\text{ MHz}$                                                                                                | -             | 2304          | -                   | pF                                     |
| $C_{oss}$     | Output capacitance               |                                                                                                                                                                    | -             | 620           | -                   | pF                                     |
| $C_{rss}$     | Feedback capacitance             |                                                                                                                                                                    | -             | 448           | -                   | pF                                     |

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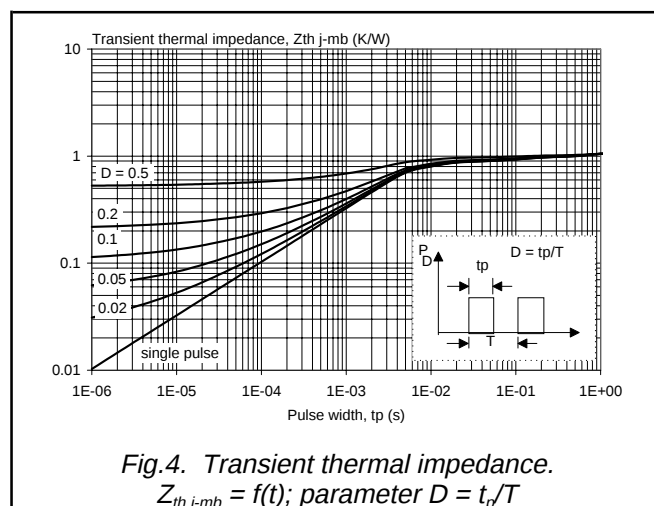
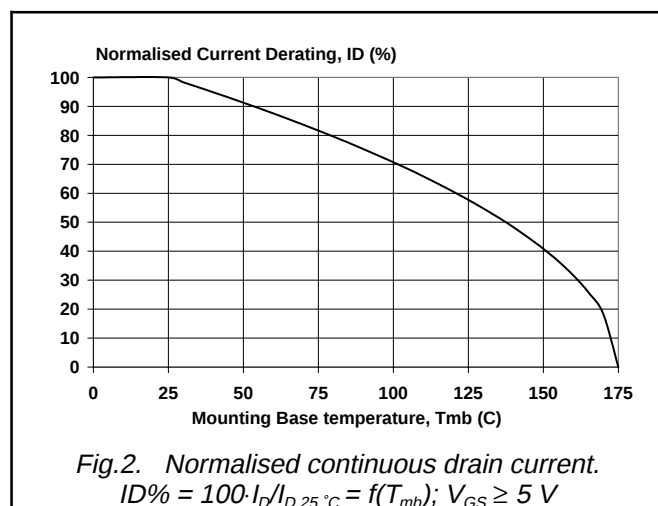
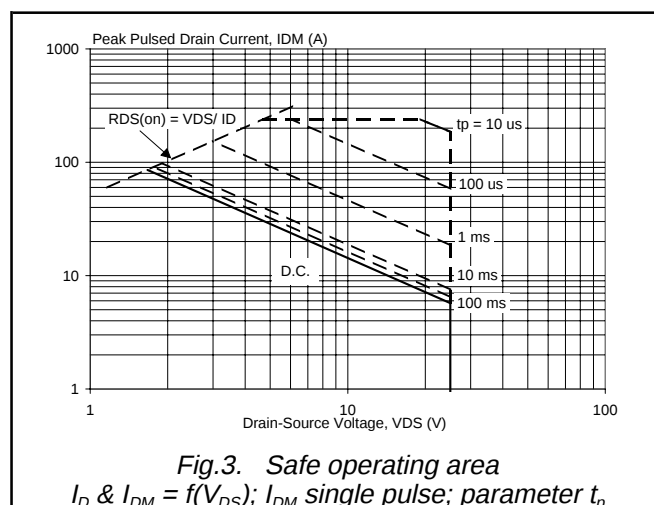
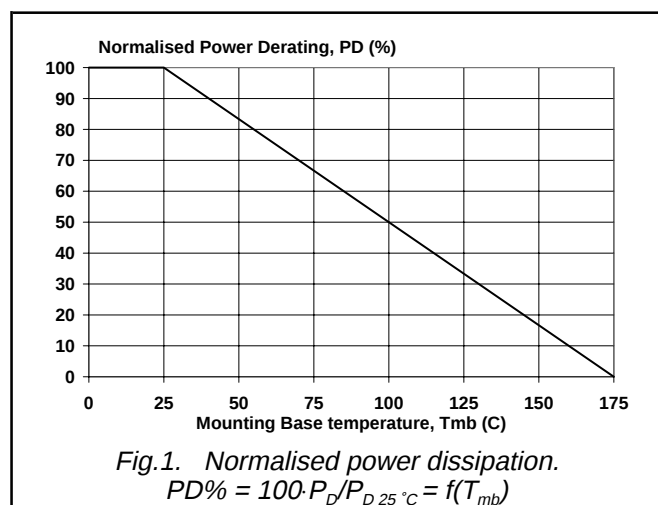
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### REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j = 25^\circ\text{C}$  unless otherwise specified

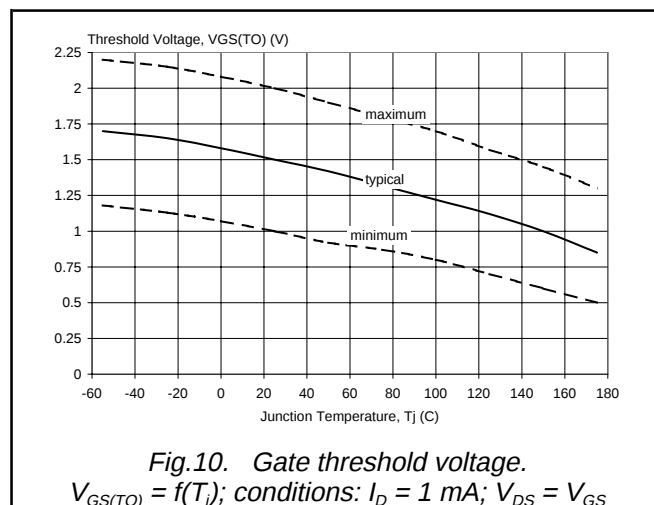
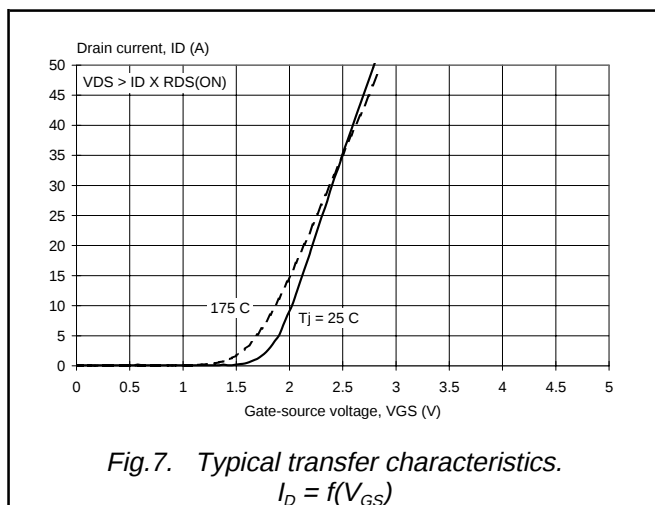
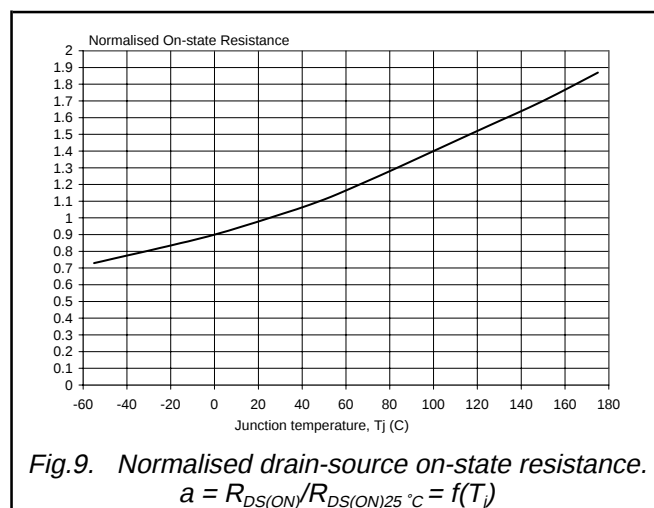
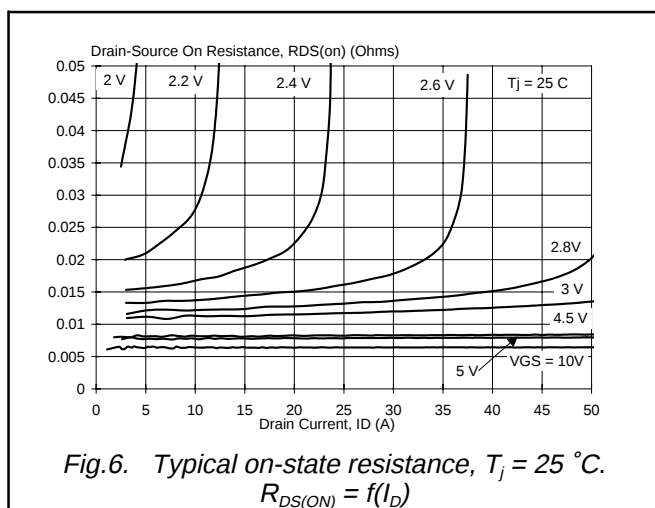
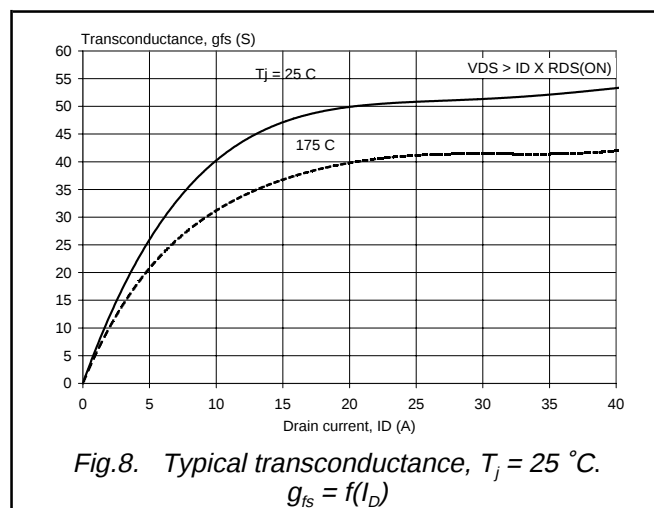
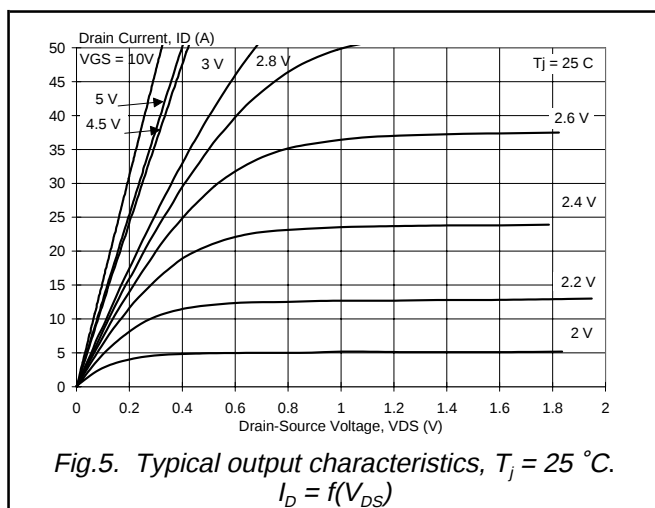
| SYMBOL   | PARAMETER                              | CONDITIONS                                                                                            | MIN. | TYP.        | MAX.     | UNIT          |
|----------|----------------------------------------|-------------------------------------------------------------------------------------------------------|------|-------------|----------|---------------|
| $I_S$    | Continuous source current (body diode) |                                                                                                       | -    | -           | 75       | A             |
| $I_{SM}$ | Pulsed source current (body diode)     |                                                                                                       | -    | -           | 240      | A             |
| $V_{SD}$ | Diode forward voltage                  | $I_F = 25\text{ A}; V_{GS} = 0\text{ V}$<br>$I_F = 40\text{ A}; V_{GS} = 0\text{ V}$                  | -    | 0.85<br>0.9 | 1.2<br>- | V             |
| $t_{rr}$ | Reverse recovery time                  | $I_F = 20\text{ A}; -dI_F/dt = 100\text{ A}/\mu\text{s};$<br>$V_{GS} = 0\text{ V}; V_R = 25\text{ V}$ | -    | 109         | -        | ns            |
| $Q_{rr}$ | Reverse recovery charge                |                                                                                                       | -    | 0.2         | -        | $\mu\text{C}$ |



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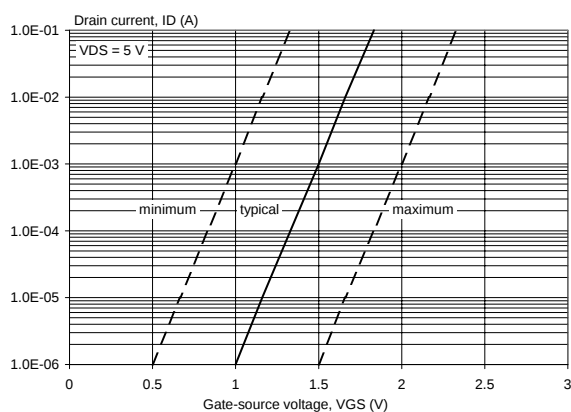


Fig.11. Sub-threshold drain current.  
 $I_D = f(V_{GS})$ ; conditions:  $T_j = 25^\circ\text{C}$ ;  $V_{DS} = V_{GS}$

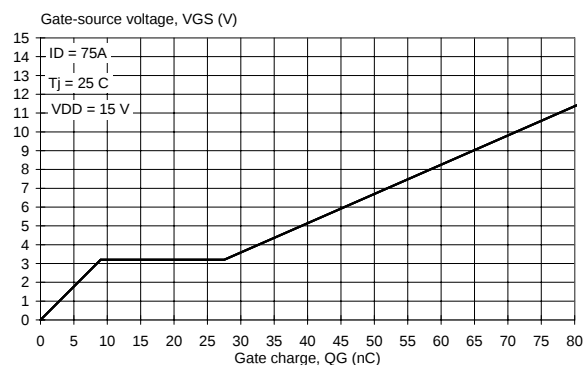


Fig.13. Typical turn-on gate-charge characteristics.  
 $V_{GS} = f(Q_G)$

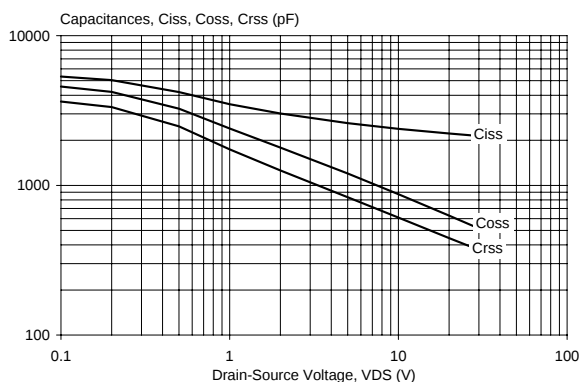


Fig.12. Typical capacitances,  $C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$ .  
 $C = f(V_{DS})$ ; conditions:  $V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

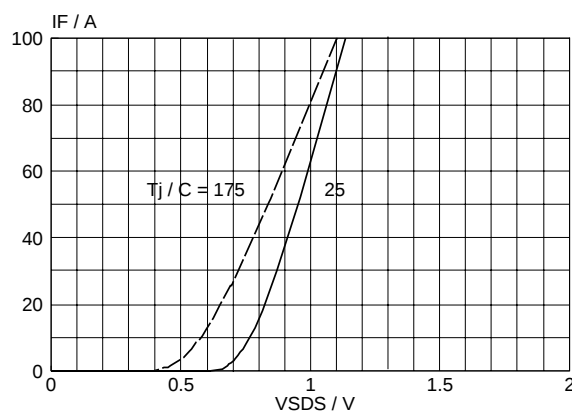
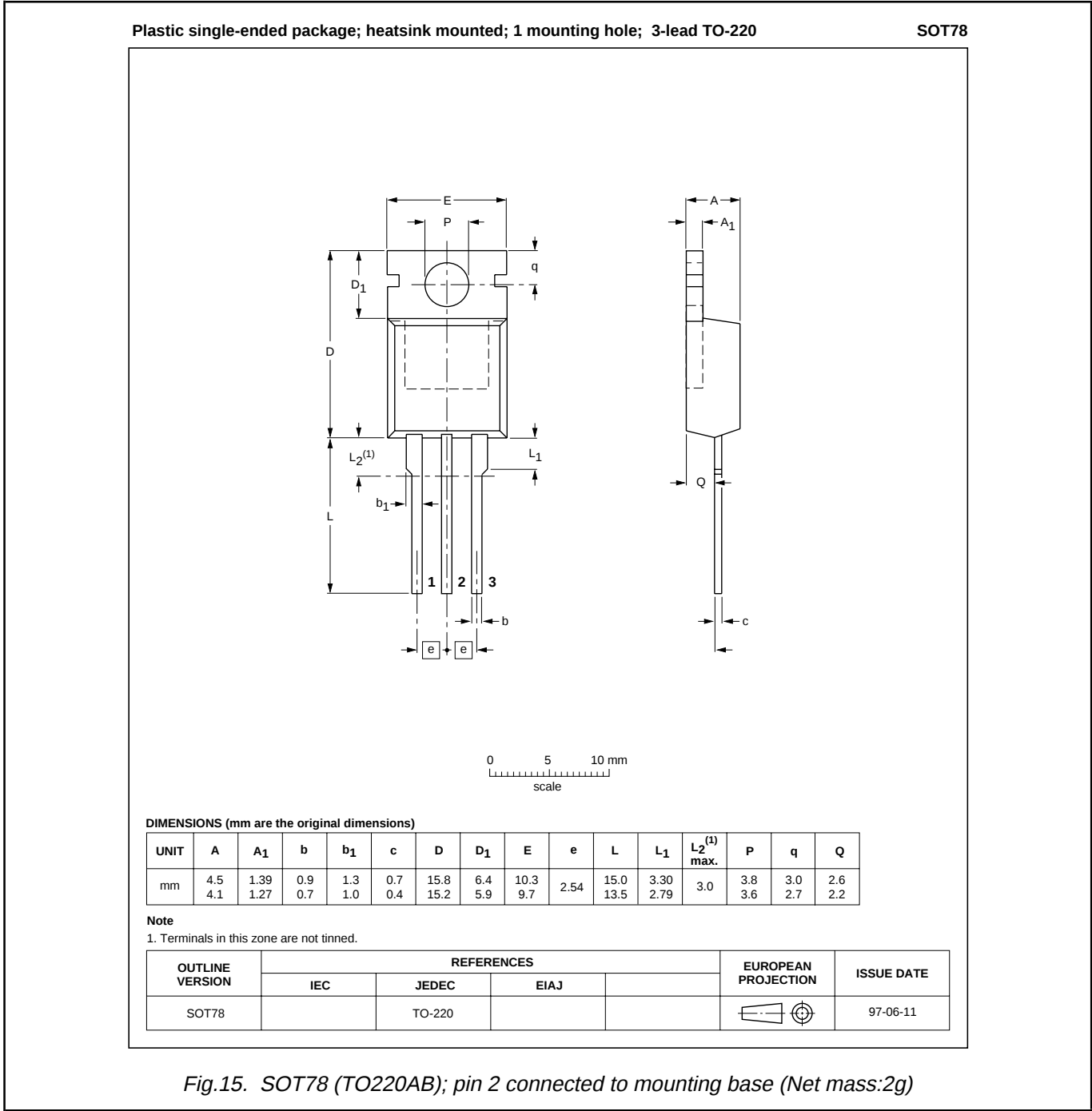


Fig.14. Typical reverse diode current.  
 $I_F = f(V_{SDS})$ ; conditions:  $V_{GS} = 0\text{ V}$ ; parameter  $T_j$

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MECHANICAL DATA



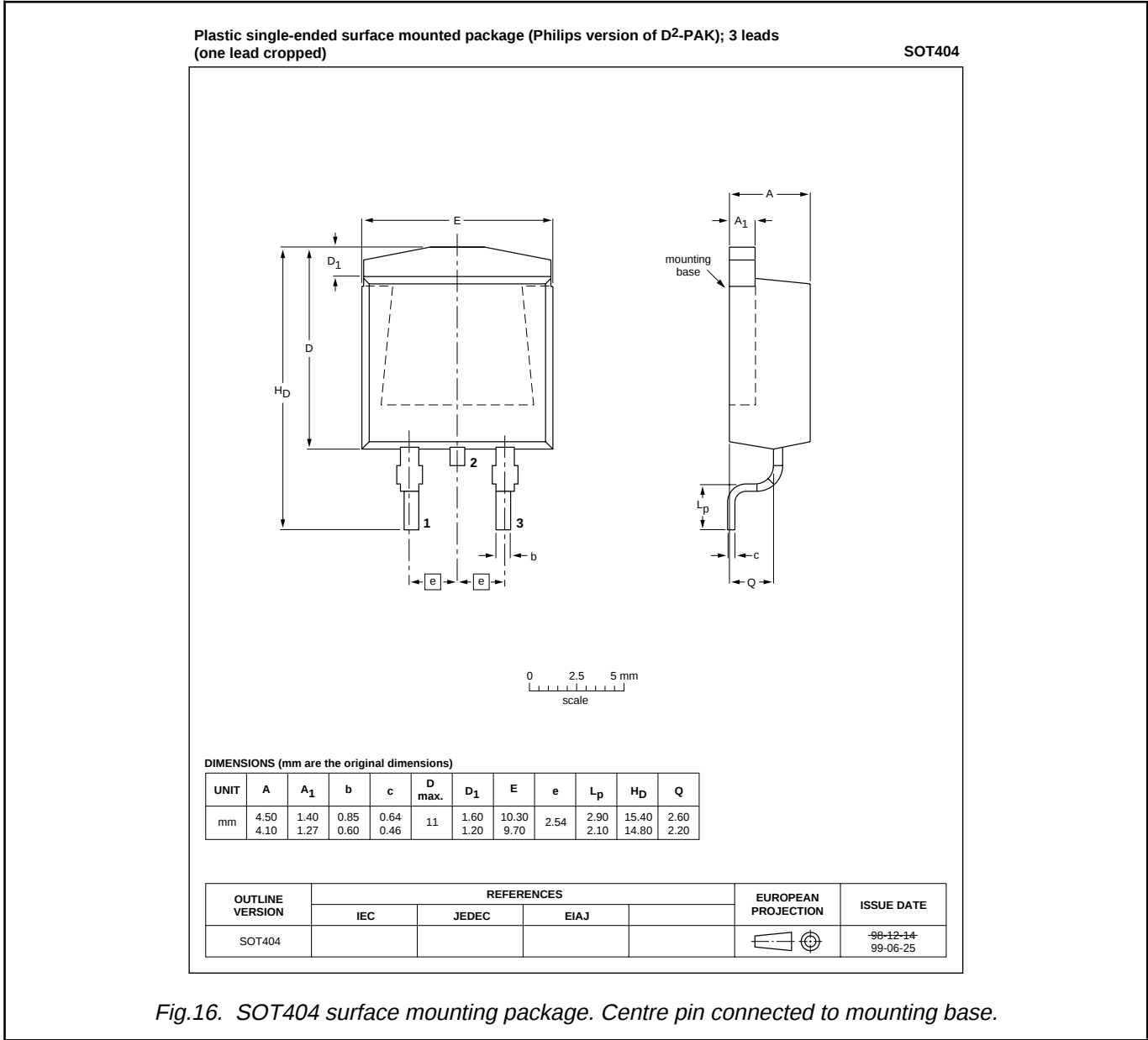
Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to mounting instructions for SOT78 (TO220AB) package.
3. Epoxy meets UL94 V0 at 1/8".

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MECHANICAL DATA



Notes

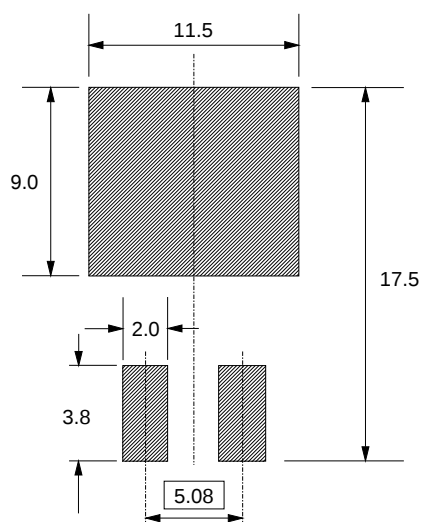
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2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

N-channel TrenchMOS<sup>TM</sup> transistor  
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## MOUNTING INSTRUCTIONS

*Dimensions in mm*

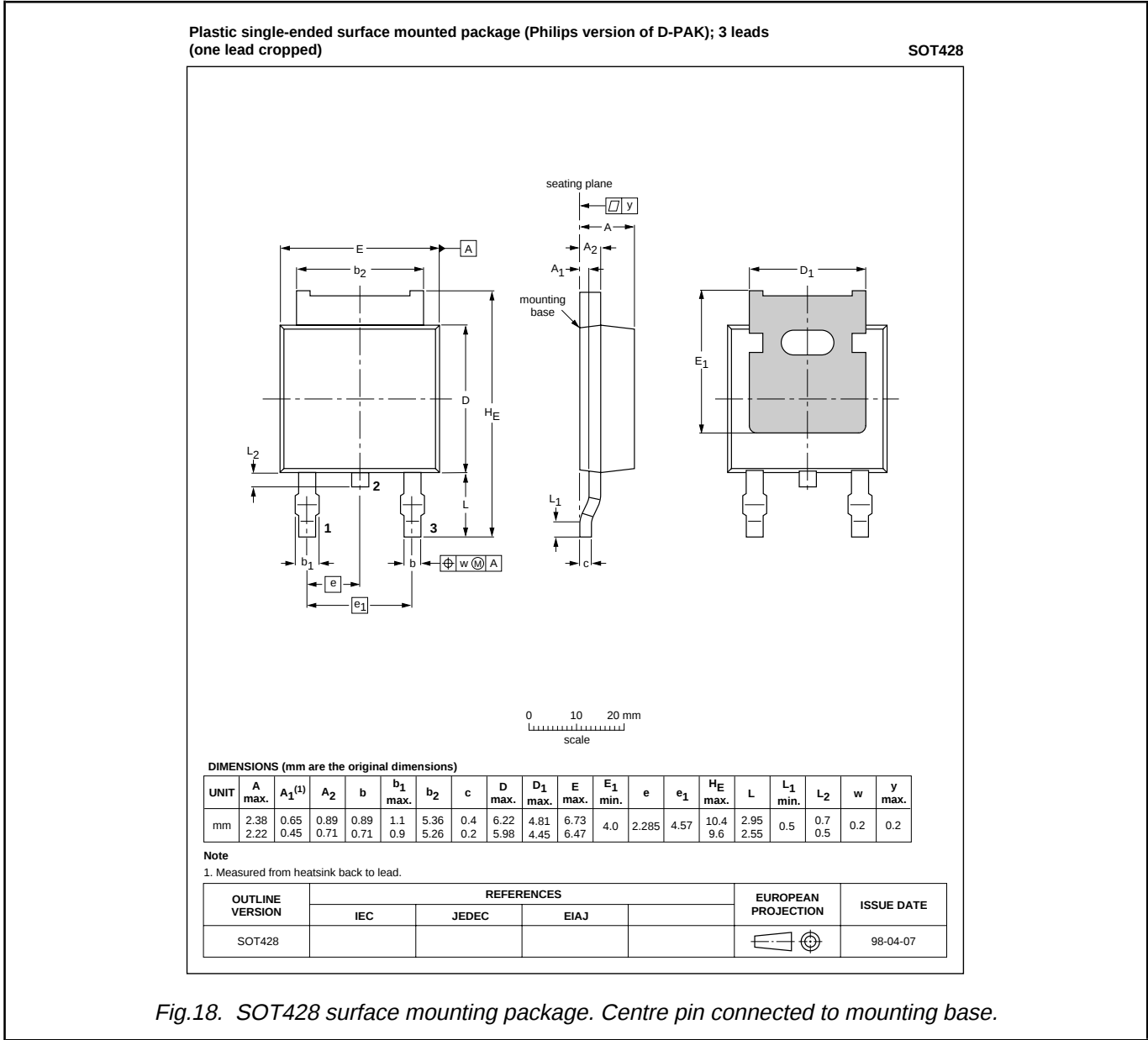


*Fig.17. SOT404 : soldering pattern for surface mounting.*

N-channel TrenchMOS™ transistor  
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MECHANICAL DATA



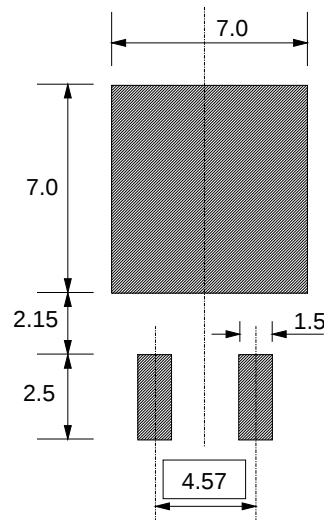
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## MOUNTING INSTRUCTIONS

*Dimensions in mm*



*Fig.19. SOT428 : soldering pattern for surface mounting.*

## N-channel TrenchMOS<sup>TM</sup> transistor Logic level FET

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### DEFINITIONS

| Data sheet status                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                                       |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Objective specification                                                                                                                                                                                                                                                                                                                                                                                                                                    | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification                                                                                                                                                                                                                                                                                                                                                                                                                                  | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification                                                                                                                                                                                                                                                                                                                                                                                                                                      | This data sheet contains final product specifications.                                |
| Limiting values                                                                                                                                                                                                                                                                                                                                                                                                                                            |                                                                                       |
| Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |                                                                                       |
| Application information                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                                                                       |
| Where application information is given, it is advisory and does not form part of the specification.                                                                                                                                                                                                                                                                                                                                                        |                                                                                       |
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### LIFE SUPPORT APPLICATIONS

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