MC74VHCT86A

Quad 2-Input XOR Gate / CMOS Logic Level Shifter
with LSTTL−Compatible Inputs

The MC74VHCT86A is an advanced high speed CMOS 2−input Exclusive−OR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL−type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic−level translator from 3.0 V CMOS logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high−voltage power supply.

The MC74VHCT86A input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows it to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: t_{PD} = 4.8 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- TTL−Compatible Inputs: V_{IL} = 0.8 V; V_{IH} = 2.0 V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
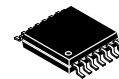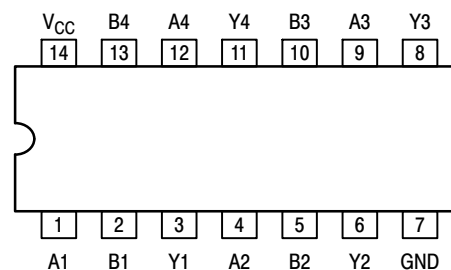- These Devices are Pb−Free and are RoHS Compliant

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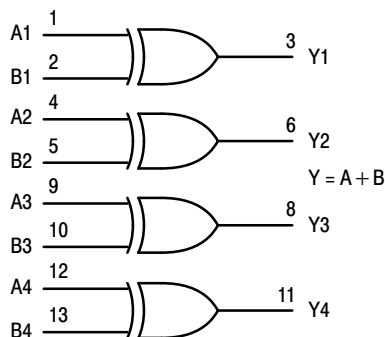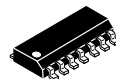
14−LEAD SOIC
D SUFFIX
CASE 751A

14−LEAD TSSOP
DT SUFFIX
CASE 948G

PIN CONNECTION AND
MARKING DIAGRAM (Top View)

V_{CC}	B4	A4	Y4	B3	A3	Y3
14	13	12	11	10	9	8

1	2	3	4	5	6	7
A1	B1	Y1	A2	B2	Y2	GND

For detailed package marking information, see the Marking Diagram section on page 4 of this data sheet.

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

ORDERING INFORMATION

Device	Package	Shipping
MC74VHCT86ADR2G	SOIC−14 (Pb−Free)	2500 / Tape & Reel
MC74VHCT86ADTR2G	TSSOP−14 (Pb−Free)	2500 / Tape & Reel

LOGIC DIAGRAM

$$Y = A + B$$

MC74VHCT86A

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		− 0.5 to + 7.0	V
V_{in}	DC Input Voltage		− 0.5 to + 7.0	V
V_{out}	DC Output Voltage $V_{CC} = 0$ High or Low State		− 0.5 to + 7.0 − 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current		− 20	mA
I_{OK}	Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})		± 20	mA
I_{out}	DC Output Current, per Pin		± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		± 50	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†		500 450	mW
T_{stg}	Storage Temperature		− 65 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
†Derating — SOIC Package: − 7 mW/°C from 65° to 125°C
TSSOP Package: − 6.1 mW/°C from 65° to 125°C

> This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
> Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	2.0	5.5	V
DC Input Voltage		V_{IN}	0.0	5.5	V
DC Output Voltage $V_{CC} = 0$ High or Low State		V_{OUT}	0.0 0.0	5.5 V_{CC}	V
Operating Temperature Range		T_A	−55	+85	°C
Input Rise and Fall Time $V_{CC} = 3.3V \pm 0.3V$ $V_{CC} = 5.0V \pm 0.5V$		t_r, t_f	0 0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	− 0.3	− 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	Typ	Max	$T_A \leq$ 85°C Min	Max	$T_A \leq$ 125°C Min	Max	Unit
V_{IH}	Minimum High–Level Input Voltage		3.0 4.5 5.5	1.2 2.0 2.0			1.2 2.0 2.0		1.2 2.0 2.0		V
V_{IL}	Maximum Low–Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5V or GND	0 to 5.5			±0.1		±1.0		±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	µA
I_{CCT}	Quiescent Supply Current	Input: V_{IN} = 3.4V	5.5			1.35		1.50		1.65	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5V	0.0			0.5		5.0		10	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	Typ	Max	T_A = – 40 to 85°C Min	Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay, A or B to Y	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		7.0 9.5	11.0 14.5	1.0 1.0	13.0 16.5	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		4.8 6.3	6.8 8.8	1.0 1.0	8.0 10.0	
C_{in}	Input Capacitance				4	10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1)	18	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per gate). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.
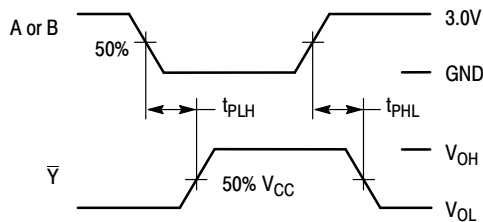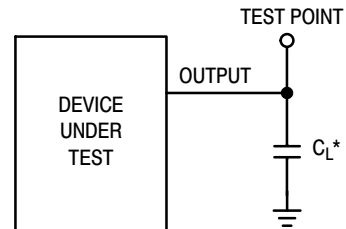

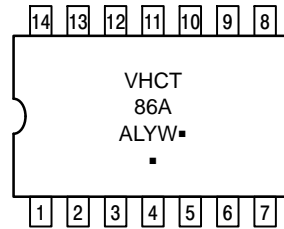**Figure 1. Switching Waveforms**

*Includes all probe and jig capacitance

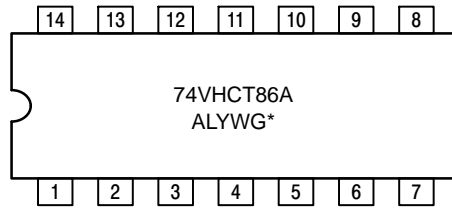**Figure 2. Test Circuit**

MC74VHCT86A

MARKING DIAGRAMS
(Top View)

```
 ┌14──13──12──11──10──9───8─┐
 │                          │
 │      VHCT86AG            │
 )      AWLYWW*             │
 │                          │
 └─1───2───3───4───5──6───7─┘
```

14–LEAD SOIC
D SUFFIX
CASE 751A

```
 ┌14─13─12─11─10─9──8┐
 │                   │
 │     VHCT          │
 )     86A           │
 │     ALYW▪         │
 │       ▪           │
 └─1─2─3─4─5─6─7──────┘
```

14–LEAD TSSOP
DT SUFFIX
CASE 948G

```
 ┌14──13──12──11──10──9───8─┐
 │                          │
 │     74VHCT86A            │
 )     ALYWG*               │
 │                          │
 └─1───2───3───4───5──6───7─┘
```
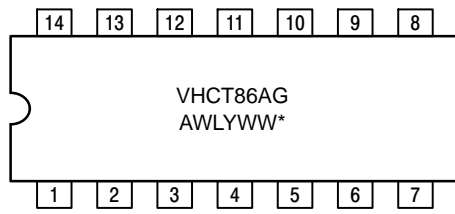
14–LEAD SOEIAJ
M SUFFIX
CASE 965

A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb–Free Package

*See Applications Note #AND8004/D for date code and traceability information.

MC74VHCT86A

PACKAGE DIMENSIONS
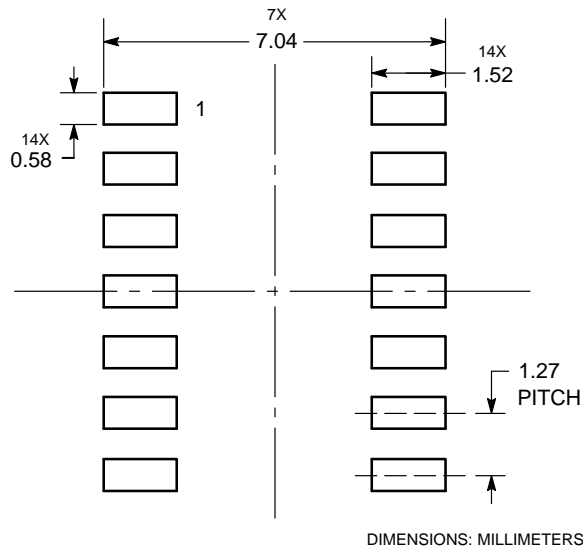
TSSOP−14
CASE 948G
ISSUE B
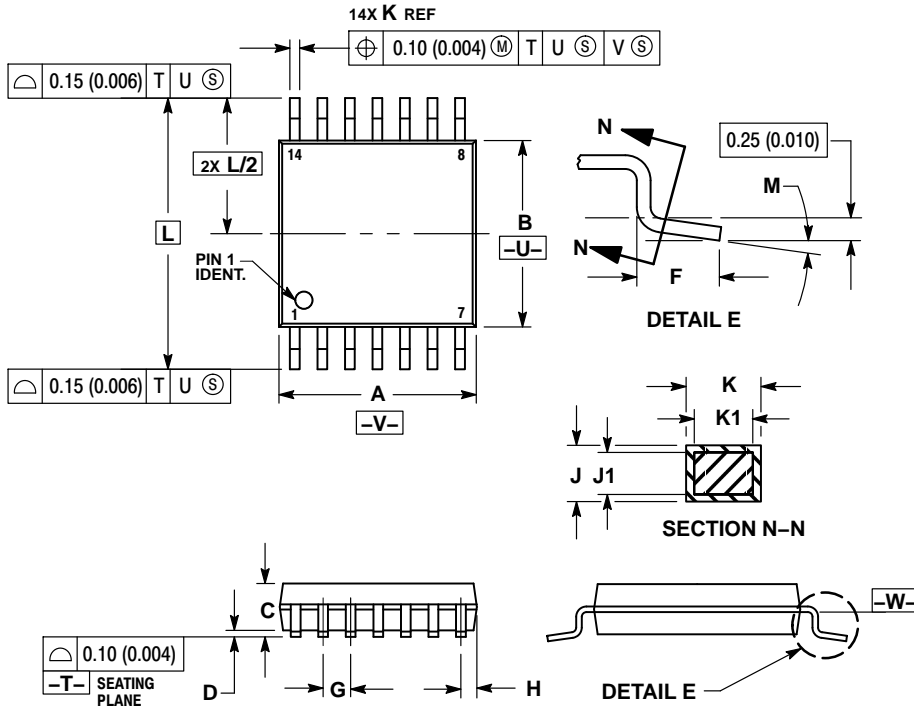
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| DIM | MILLIMETERS | | INCHES | |
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	–––	1.20	–––	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS
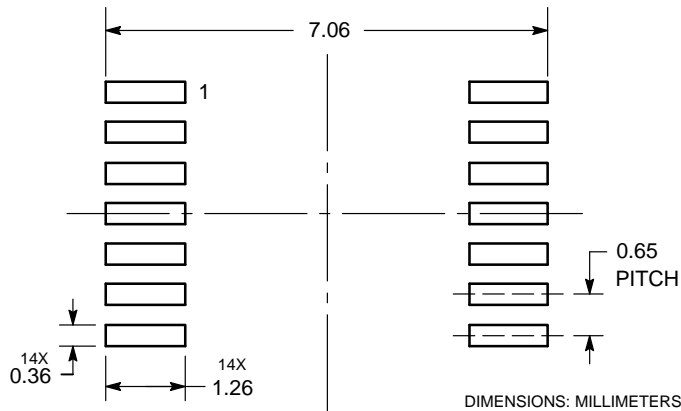
MC74VHCT86A

PACKAGE DIMENSIONS

SOIC–14
D SUFFIX
CASE 751A–03
ISSUE J
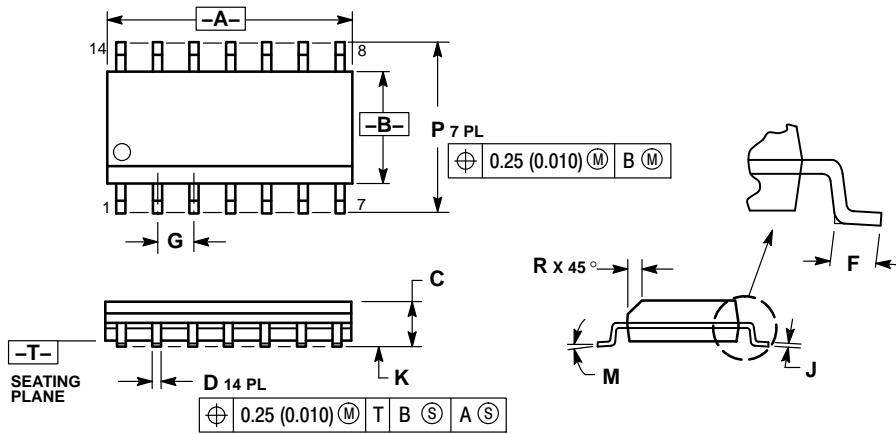
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS

PUBLICATION ORDERING INFORMATION

MC74VHCT86A/D