

2-Mbit (256K x 8) MoBL[®] Static RAM

Features

- **Very high speed: 45 ns**
 - Wide voltage range: 2.20V – 3.60V
- **Pin-compatible with CY62138CV30**
- **Ultra-low standby power**
 - Typical standby current: 1 μ A
 - Maximum standby current: 7 μ A
- **Ultra-low active power**
 - Typical active current: 2 mA @ f = 1 MHz
- **Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Offered in Pb-free 36-ball BGA package**

Functional Description^[1]

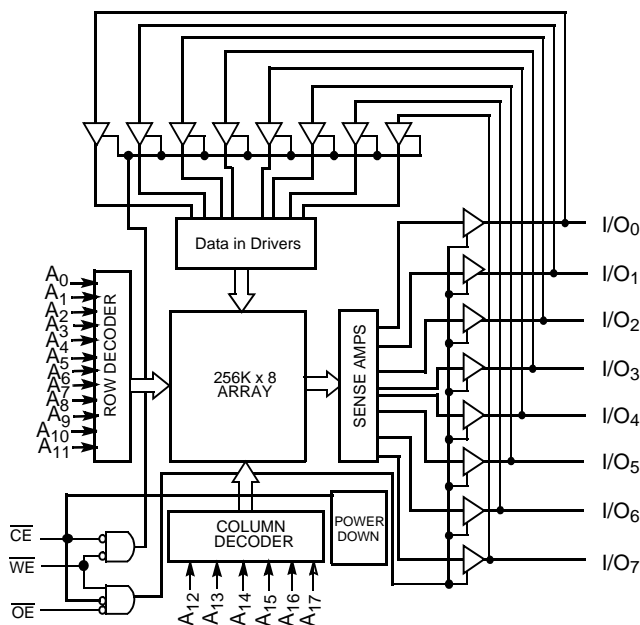
The CY62138EV30 is a high-performance CMOS static RAM organized as 256K words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can be put into standby mode reducing power consumption when deselected ($\overline{\text{CE}}$ HIGH).

Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing Write Enable ($\overline{\text{WE}}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{\text{CE}}$ HIGH), the outputs are disabled ($\overline{\text{OE}}$ HIGH), or during a write operation ($\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW).

Logic Block Diagram

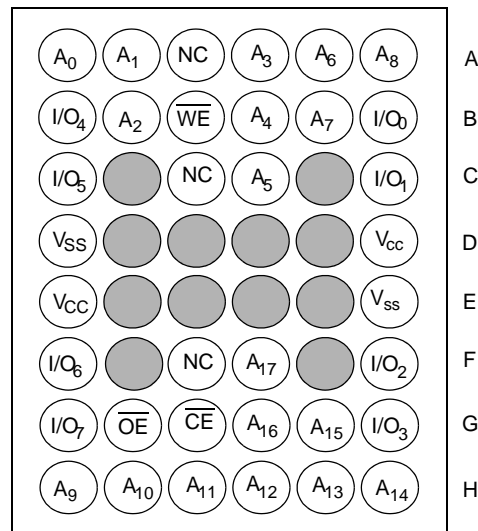


Note:

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Pin Configuration^[2]

FBGA
Top View



Product Portfolio

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
	f = 1 MHz		f = f _{max}		Typ. ^[3]		Max.			
	Typ. ^[3]	Max.	Typ. ^[3]						Max.	
CY62138EV30LL	2.2	3.0	3.6	45	2	2.5	15	20	1	7

Notes:

2. NC pins are not connected on the die.

3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25°C.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied 55°C to +125°C

Supply Voltage to Ground

Potential -0.3V to $V_{CC(MAX)}$ + 0.3V

DC Voltage Applied to Outputs

in High-Z State^[4,5] -0.3V to $V_{CC(MAX)}$ + 0.3V

DC Input Voltage^[4,5] -0.3V to $V_{CC(MAX)}$ + 0.3V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Product	Range	Ambient Temperature	V_{CC} ^[6]
CY62138EV30LL	Industrial	-40°C to +85°C	2.2V to 3.6V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62138EV30-45			Unit
			Min.	Typ. ^[3]	Max.	
V_{OH}	Output HIGH Voltage	$I_{OH} = -0.1$ mA $V_{CC} = 2.20$ V	2.0			V
		$I_{OH} = -1.0$ mA $V_{CC} = 2.70$ V	2.4			V
V_{OL}	Output LOW Voltage	$I_{OL} = 0.1$ mA $V_{CC} = 2.20$ V			0.4	V
		$I_{OL} = 2.1$ mA $V_{CC} = 2.70$ V			0.4	V
V_{IH}	Input HIGH Voltage	$V_{CC} = 2.2$ V to 2.7 V	1.8		$V_{CC} + 0.3$ V	V
		$V_{CC} = 2.7$ V to 3.6 V	2.2		$V_{CC} + 0.3$ V	V
V_{IL}	Input LOW Voltage	$V_{CC} = 2.2$ V to 2.7 V	-0.3		0.6	V
		$V_{CC} = 2.7$ V to 3.6 V	-0.3		0.8	V
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-1		+1	μA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$ $V_{CC} = V_{CCmax}$ $I_{OUT} = 0$ mA CMOS levels		15	20	mA
		$f = 1$ MHz		2	2.5	mA
I_{SB1}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, $f = f_{MAX}$ (Address and Data Only), $f = 0$ (OE, and WE), $V_{CC} = 3.60$ V		1	7	μA
I_{SB2}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$, $V_{CC} = 3.60$ V		1	7	μA

Capacitance for all packages^[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1$ MHz, $V_{CC} = V_{CC(typ.)}$	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

4. $V_{IL(min.)} = -2.0$ V for pulse durations less than 20 ns.

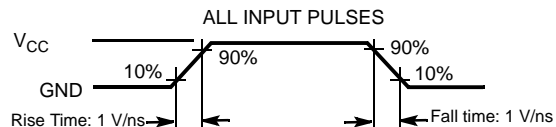
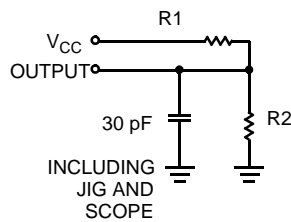
5. $V_{IH(max.)} = V_{CC} + 0.75$ V for pulse durations less than 20 ns.

6. Full device AC operation assumes a 100 μs ramp time from 0 to $V_{CC(min.)}$ and 200 μs wait time after V_{CC} stabilization.

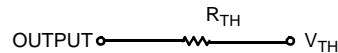
Thermal Resistance

Parameter	Description	Test Conditions	BGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, four-layer printed circuit board	72	$^{\circ}\text{C/W}$
Θ_{JC}	Thermal Resistance (Junction to Case)		8.86	$^{\circ}\text{C/W}$

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

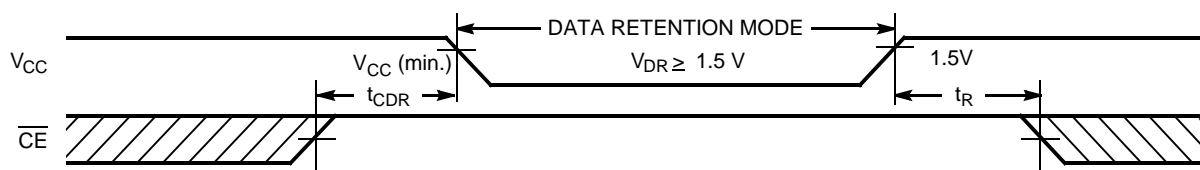


Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[3]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1			V
I_{CCDR}	Data Retention Current	$V_{CC} = 1V, \overline{CE} \geq V_{CC} - 0.2V, V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		0.8	3	μA
$t_{CDR}^{[7]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[8]}$	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform



Notes:

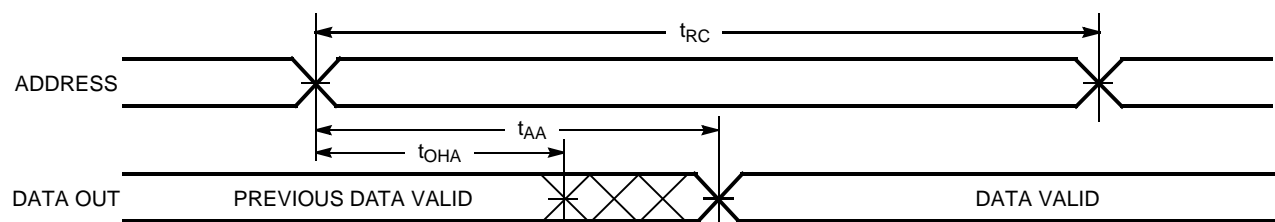
7. Tested initially and after any design or process changes that may affect these parameters.
8. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100 \mu\text{s}$ or stable at $V_{CC(min.)} \geq 100 \mu\text{s}$.

Switching Characteristics (Over the Operating Range)^[9]

Parameter	Description	45 ns		Unit
		Min.	Max.	
Read Cycle				
t _{RC}	Read Cycle Time	45		ns
t _{AA}	Address to Data Valid		45	ns
t _{OHA}	Data Hold from Address Change	10		ns
t _{ACE}	\overline{CE} LOW to Data Valid		45	ns
t _{DOE}	\overline{OE} LOW to Data Valid		22	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[10]	5		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[10,11]		18	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[10]	10		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[10, 11]		18	ns
t _{PU}	\overline{CE} LOW to Power-up	0		ns
t _{PD}	\overline{CE} HIGH to Power-up		45	ns
Write Cycle ^[12]				
t _{WC}	Write Cycle Time	45		ns
t _{SCE}	\overline{CE} LOW to Write End	35		ns
t _{AW}	Address Set-up to Write End	35		ns
t _{HA}	Address Hold from Write End	0		ns
t _{SA}	Address Set-up to Write Start	0		ns
t _{PWE}	\overline{WE} Pulse Width	35		ns
t _{SD}	Data Set-up to Write End	25		ns
t _{HD}	Data Hold from Write End	0		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[10, 11]		18	ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[10]	10		ns

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled)^[13, 14]

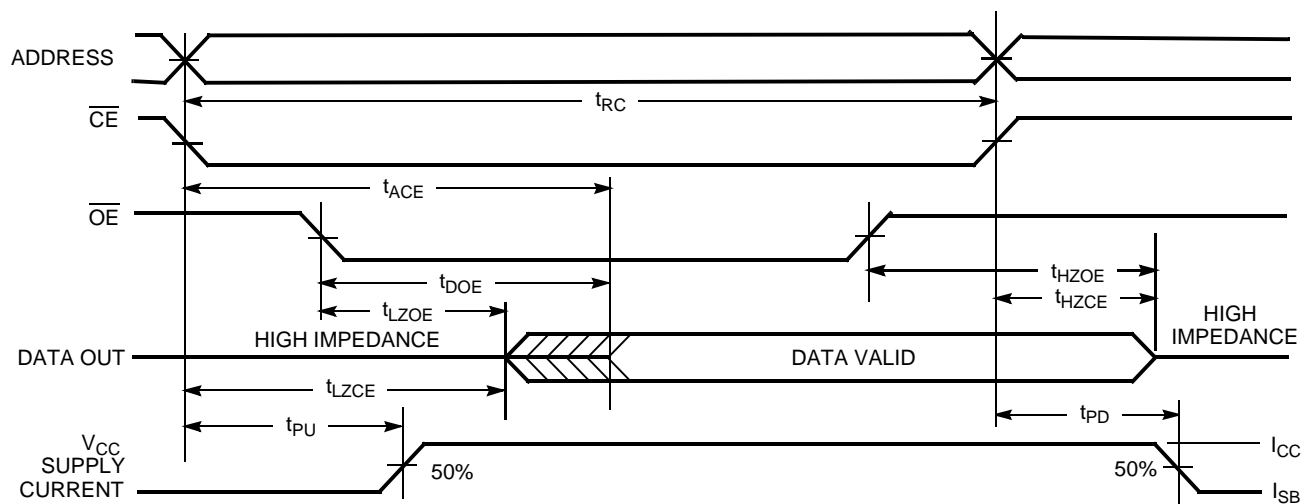


Notes:

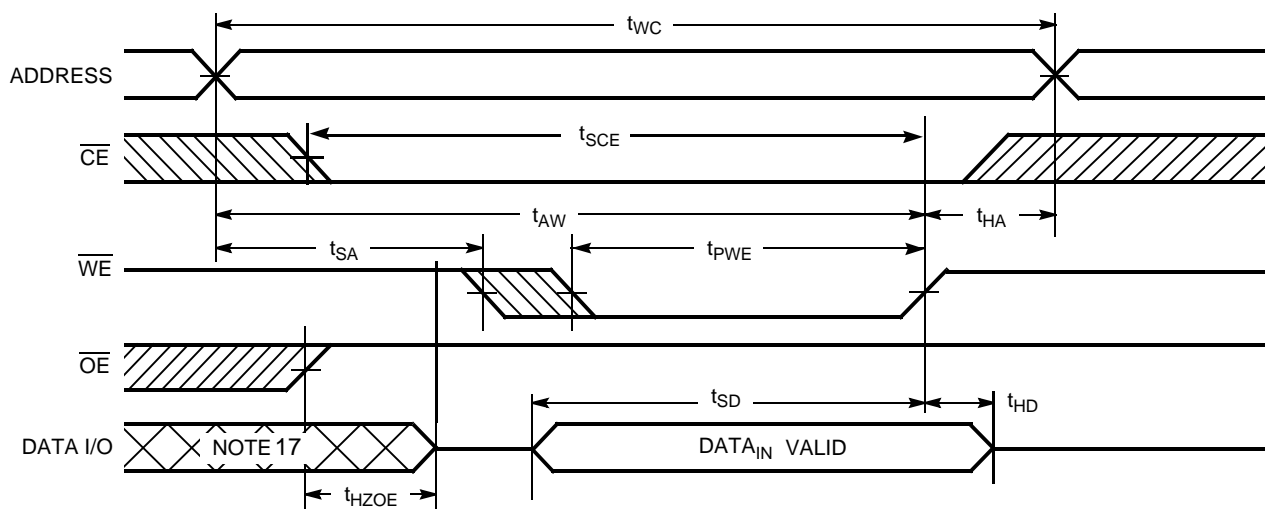
- Test Conditions for all parameters other than three-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} transitions are measured when the output enter a high-impedance state.
- The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
- Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
- \overline{WE} is HIGH for read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 (\overline{OE} Controlled)^[14, 15]



Write Cycle No. 1 (\overline{WE} Controlled)^[16, 18]

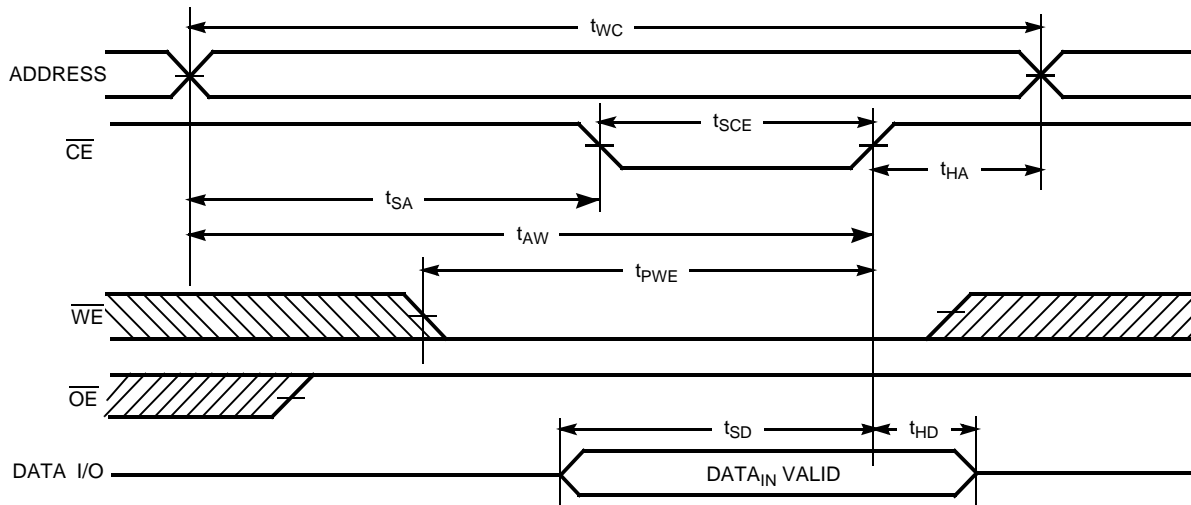


Notes:

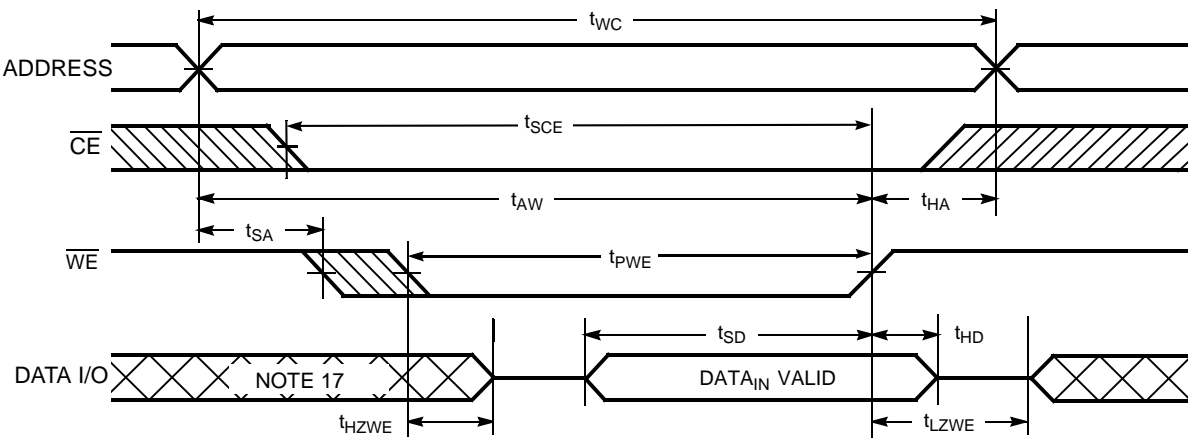
15. Address valid prior to or coincident with \overline{CE} transition LOW.
16. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
17. During this period, the I/Os are in output state and input signals should not be applied.
18. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled)^[16, 18]



Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[18]



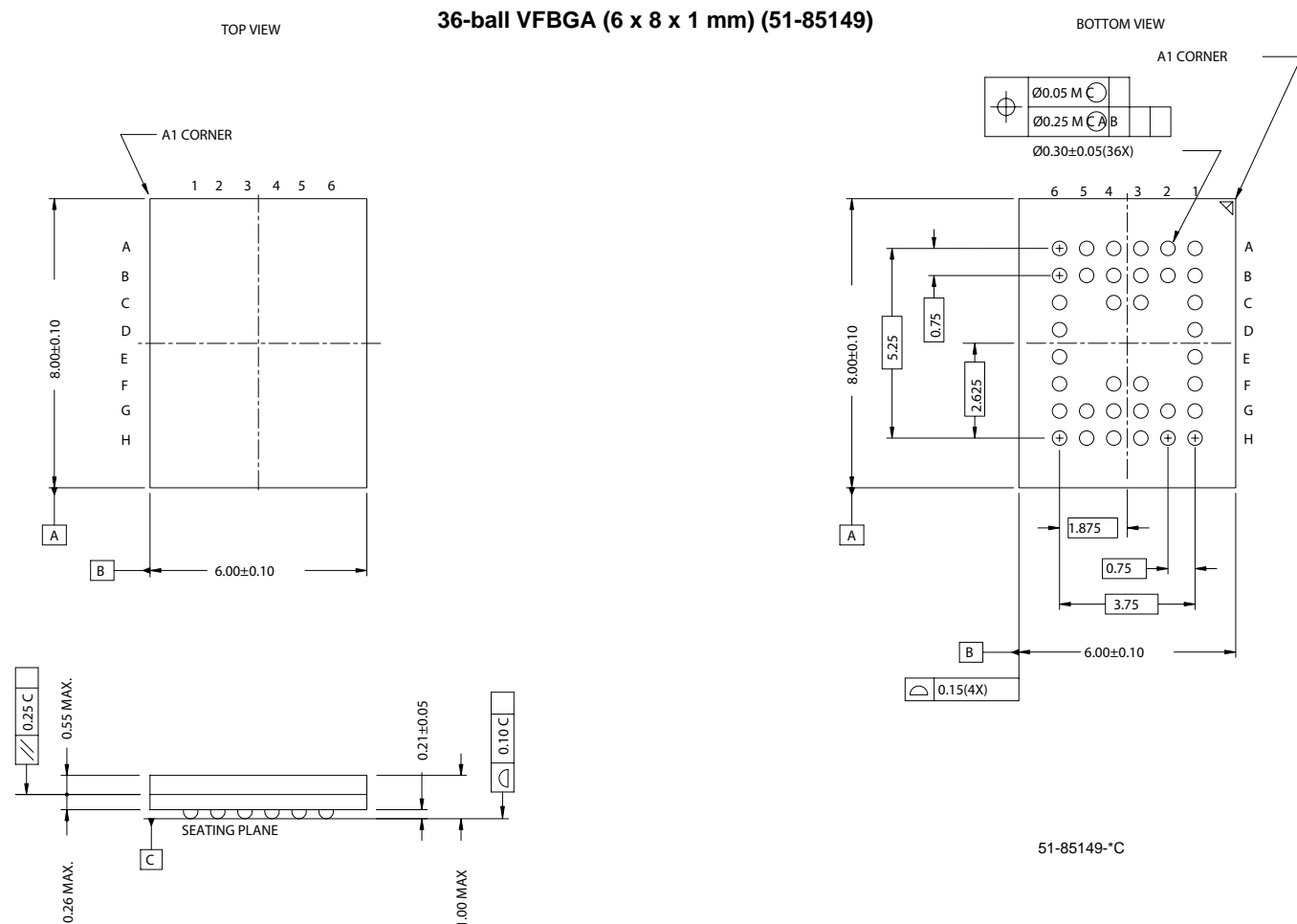
Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	Data Out (I/O_0 – I/O_7)	Read	Active (I_{CC})
L	H	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	Data in (I/O_0 – I/O_7)	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62138EV30LL-45BVXI	51-85149	36-ball Very Fine Pitch BGA (6 mm x 8 mm x 1 mm) (Pb-free)	Industrial

Package Diagrams



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Document History Page

Document Title: CY62138EV30 2-Mbit (256K x 8) MoBL® Static RAM Document Number: 38-05577				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	237432	See ECN	AJU	New data sheet
*A	427817	See ECN	NXR	Removed 35 ns Speed Bin Removed "L" version Removed 32-pin TSOPII package from product Offering. Changed ball C3 from DNU to NC. Removed the redundant footnote on DNU. Moved Product Portfolio from Page # 3 to Page #2. Changed I _{CC} (Max) value from 2 mA to 2.5 mA and I _{CC} (Typ) value from 1.5 mA to 2 mA at f = 1 MHz Changed I _{CC} (Typ) value from 12 mA to 15 mA at f = f _{max} =1/t _{RC} Changed I _{SB1} and I _{SB2} Typ. values from 0.7 μA to 1 μA and Max. values from 2.5 μA to 7 μA. Changed V _{CC} stabilization time in footnote #7 from 100 μs to 200 μs Changed the AC test load capacitance from 50pF to 30pF on Page# 4 Changed V _{DR} from 1.5V to 1V on Page# 4. Changed I _{CCDR} from 1 μA to 3 μA in the Data Retention Characteristics table on Page # 4. Corrected t _R in Data Retention Characteristics from 100 μs to t _{RC} ns Changed t _{OHA} , t _{LZCE} , t _{LZWE} from 6 ns to 10 ns Changed t _{HZOE} , t _{HZCE} , t _{HZWE} from 15 ns to 18 ns Changed t _{LZOE} from 3 ns to 5 ns Changed t _{SCE} and t _{AW} from 40 ns to 35 ns Changed t _{SD} from 20 ns to 25 ns Changed t _{PWE} from 25 ns to 35 ns Updated the Ordering Information table and replaced Package Name column with Package Diagram.