

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change CAGE code to 67268. Add cases B and I. Change to 1.3, V1+ and V1-. Changes to table I: V_{CM} , t_{PLH} , t_{PHL} , and delay time between output A and B.	89-03-09	M. A. FRYE
B	Add CAGE code 0C7V7. Make changes to paragraphs 3.1 and 3.5.1. - ro	00-02-15	R. MONNIN
C	Drawing updated to reflect current requirements. - rrp	03-11-18	R. MONNIN
D	Make correction under the conditions column for I_{IH} and I_{IL} tests as specified in table I. Make changes to figure 2 waveform limits.- ro	05-08-15	R. MONNIN

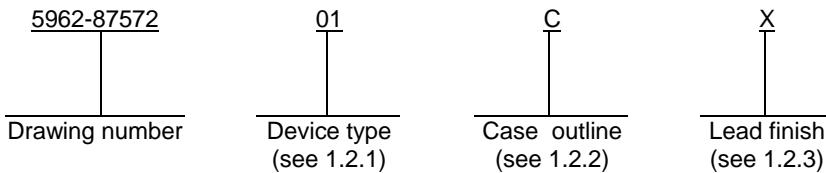
CURRENT CAGE CODE 67268

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	527	High speed voltage comparator with emitter-follower input
02	529	High speed voltage comparator
03	LM161	High speed voltage comparator

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
B 1/	GDFP4-F14	14	Flat pack
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
I	MACY1-X10	10	Can

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Positive supply voltage (V1+):

Device types 01 and 02.....	+15 V dc
Device type 03	+16 V dc

Negative supply voltage (V1-):

Device types 01 and 02.....	-15 V dc
Device type 03	-16 V dc

Gate supply voltage (V2+):

Device type 03	+7 V dc
Output voltage	+7 V dc

Output voltage

Differential input voltage (V _{IN})	±5 V dc
Input common mode voltage.....	±6 V dc

Input common mode voltage.....

Lead temperature (soldering, 10 seconds)	+300°C
DC input current.....	±10 mA

DC input current.....

Power dissipation (P _D).....	600 mW 2/
Junction temperature (T _J)	+175°C

Junction temperature (T_J)

Storage temperature range.....	-65°C to +150°C
Thermal resistance, junction-to-case (θ _{JC}).....	See MIL-STD-1835

Thermal resistance, junction-to-case (θ_{JC}).....

1/ Inactive for new design. Acceptable only for use in equipment designed or redesigned on or before 29 November 1986.

2/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

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1.4 Recommended operating conditions.

Supply voltage:

V1+	+5 V dc to +10 V dc
V1-	-6 V dc to -10 V dc
V2+	+4.5 V dc to +5.5 V dc

Ambient operating temperature (TA)..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input offset voltage	V _{IO}		1	01,02		4	mV
			2,3			6	
			1	03		3	
			2,3			5	
Input bias current	I _B	V _{IN} = 0 V	1	01		2	μA
			2,3			4	
			1	02		12	
			2,3			36	
			1,2,3	03		20	
Input offset current	I _{OFFSET}	V _{IN} = 0 V	1	01		0.5	μA
			2,3			1	
			1	02		3	
			2,3			9	
			1	03		4	
			2,3			8	
Common mode voltage range	V _{CM}		1,2,3	01,02	±5		V
High level output voltage (LOGIC)	V _{OH}	V ₂₊ = 4.5 V, I _{SOURCE} = -1 mA	1,2,3	All	2.4		V
Low level output voltage (LOGIC)	V _{OL}	V ₂₊ = 4.5 V, I _{SINK} = 10 mA	1,2,3	All		0.5	V
High level input voltage (STROBE)	V _{IH}	V ₂₊ = 4.5 V	1	All	2		V
			2,3		2.4		
Low level input voltage (STROBE)	V _{IL}	V ₂₊ = 4.5 V	1,2,3	All		0.8	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input current (STROBE)	I_{IH}	$V_{2+} = 5.5 \text{ V}$, $V_{STROBE} = 2.7 \text{ V}$	1,2,3	All		200	μA
Low level input current (STROBE)	I_{IL}	$V_{2+} = 5.5 \text{ V}$, $V_{STROBE} = 0.4 \text{ V}$	1,2,3	All		-2	mA
Output short circuit current	I_{OS}	$V_{2+} = 5.5 \text{ V}$, $V_{OUT} = 0 \text{ V}$	1,2,3	All		-70	mA
Supply current	I_{1+}	$V_{1+} = 10 \text{ V}$, $V_{1-} = -10 \text{ V}$, $V_{2+} = 5.5 \text{ V}$	1,2,3	All		5	mA
	I_{1-}					-10	
	I_{2+}					20	
Input clamp voltage (STROBE)	V_{IC}	$V_{2+} = 5.5 \text{ V}$, $I_{IN} = -18 \text{ mA}$	1,2,3	All		-1.5	V
Propagation delay time	t_{PLH}	$V_{IN} = \pm 100 \text{ mV step}$, <u>2/</u> $C_L = 15 \text{ pF}$, $T_A = +25^{\circ}\text{C}$, see figure 2	9	01 02 03 01 02 03	01	26	ns
					02	22	
					03	20	
					01	24	
					02	20	
					03	20	
Delay time between output A and B		$V_{IN} = \pm 100 \text{ mV step}$, <u>2/</u> $C_L = 15 \text{ pF}$, $T_A = +25^{\circ}\text{C}$, see figure 2	9	All		5	ns

1/ $V_{1+} = +10 \text{ V}$, $V_{1-} = 10 \text{ V}$, $V_{2+} = +5 \text{ V}$, unless otherwise specified.2/ For device types 01 and 02, $R_4 = 390 \Omega$. For device type 03, $R_4 = 2.43 \text{ k}\Omega$.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

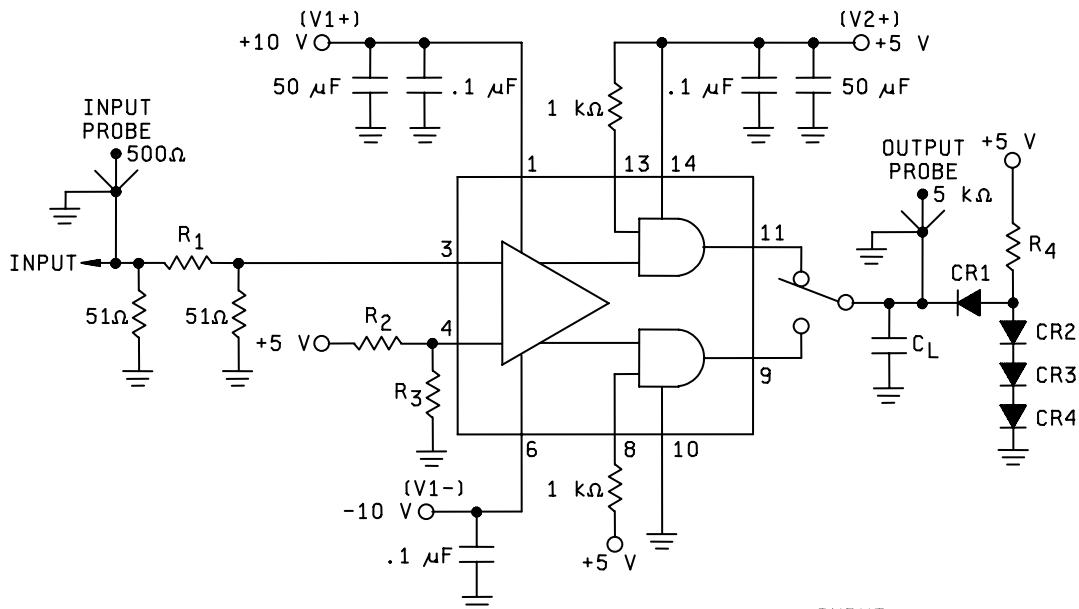
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Device types	01 and 02	03	
Case outlines	C and D	B and C	I
Terminal number	Terminal symbol		
1	V1+	V1+	INPUT A
2	NC	NC	INPUT B
3	INPUT A	INPUT A	V1-
4	INPUT B	INPUT B	STROBE B
5	NC	NC	OUTPUT B
6	V1-	V1-	GND
7	NC	NC	OUTPUT A
8	STROBE B	STROBE B	STROBE A
9	OUTPUT B	OUTPUT B	V2+
10	GND	GND	V1+
11	OUTPUT A	OUTPUT A	---
12	NC	NC	---
13	STROBE A	STROBE A	---
14	V2+	V2+	---

NC = No connection

FIGURE 1. Terminal connections.

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PIN NUMBERS REFER TO CASES B, C, AND D

INPUT

PRR = 1 MHz

Pw = 50 ns

tr = tf = 2 ns

INPUT = 3.00 V

CR1-CR4 = 1N94

R₁ SELECTED FOR 15: 1 DIVIDER

R₂ AND R₃ SELECTED FOR 100 mV AT PIN 4

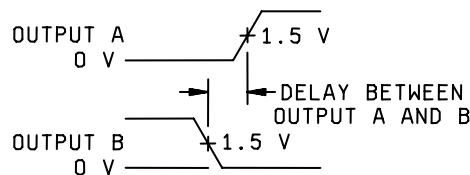
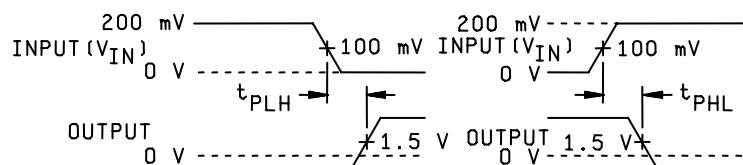


FIGURE 2. Switching time test circuit and waveforms.

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3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, 8, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) $T_A = +125^\circ\text{C}$, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,9
Group A test requirements (method 5005)	1,2,3,9
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-08-15

Approved sources of supply for SMD 5962-87572 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscc.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-8757201CA	<u>3</u> /	527/BCA
5962-8757201DA	<u>3</u> /	527/BDA
5962-8757202CA	0C7V7	529/BCA
5962-8757202DA	0C7V7	529/BDA
5962-8757203BA	0C7V7	LM161/BA
5962-8757203CA	0C7V7	LM161/CA
	3V146	LM161J/883
5962-8757203IA	0C7V7	LM161/IA
	3V146	LM161H/883B

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE
numberVendor name
and address

0C7V7

QP Semiconductor
2945 Oakmead Village Court
Santa Clara, CA 95051

3V146

Rochester Electronics
10 Malcolm Hoyt Drive
Newburyport, MA 01950

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