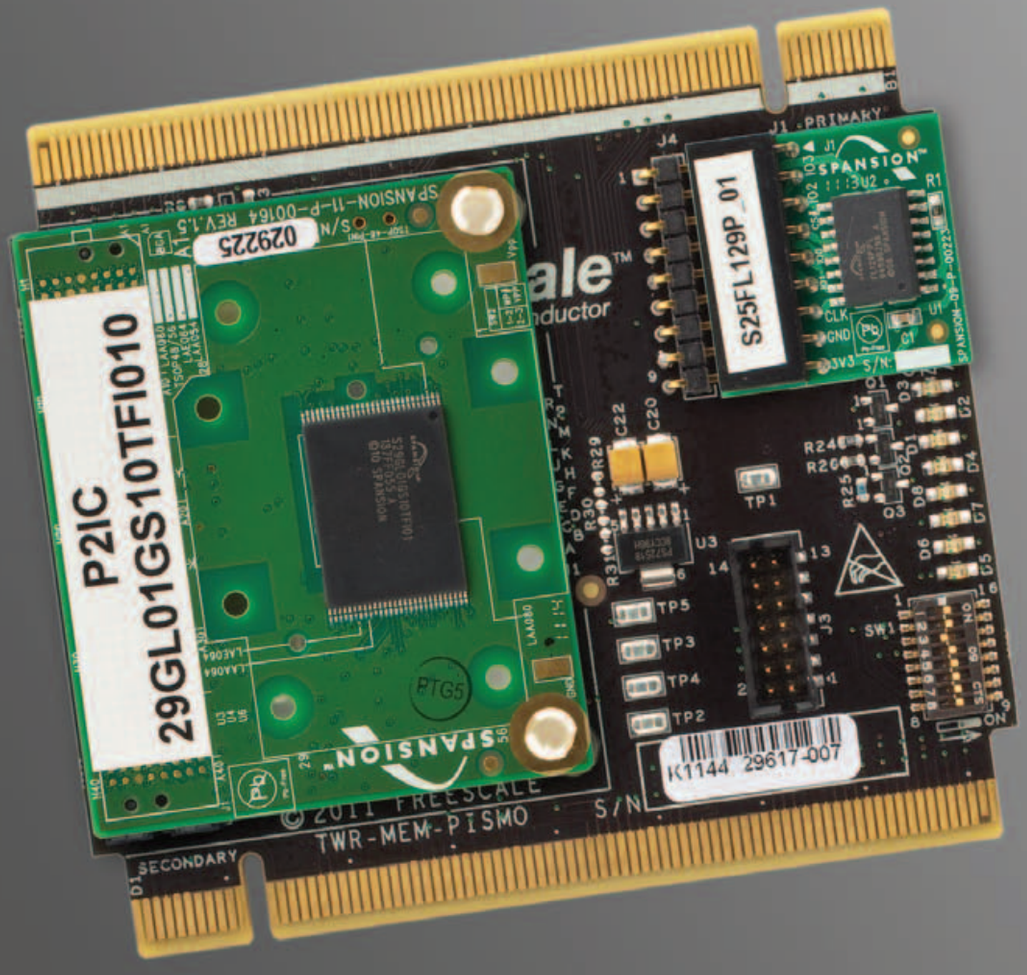


Quick Start Guide

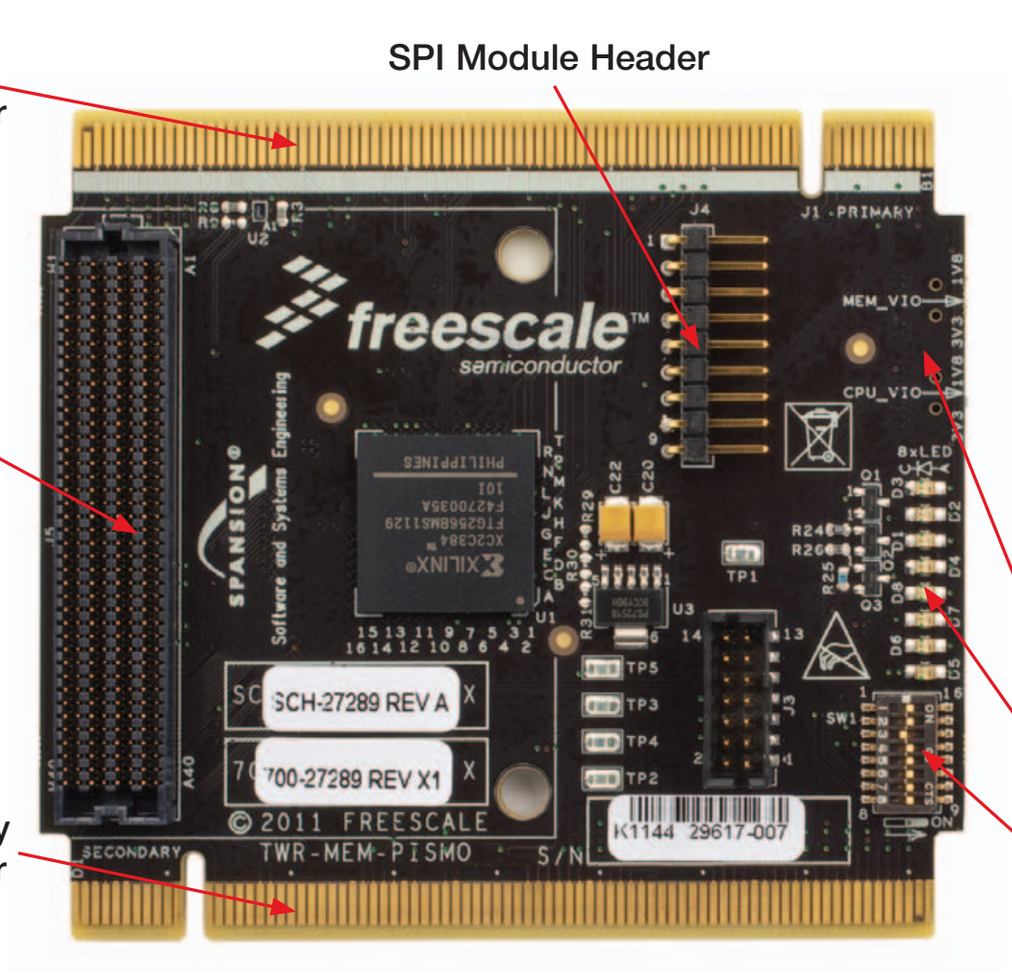
TWR-MEM-PISMO

PISMO2 Memory Module

freescale™

TOWER SYSTEM

Get to Know the TWR-MEM-PISMO



Voltage I/O Switches

LEDs

User Mode Switches

Spansion 128 MB SPI Multi-I/O Flash Module

TWR-MEM-PISMO Freescale Tower System

The TWR-MEM-PISMO module is part of the Freescale Tower System, a modular development platform that enables rapid prototyping and tool re-use through reconfigurable hardware. Take your design to the next level and begin prototyping with the Tower System today.

TWR-MEM-PISMO Features

- Expandable memory platform compatible with the Freescale Tower System
- Included Spansion 1 Gb GL-S MirrorBit Eclipse flash PISMO2 module
- Included Spansion 128 MB MirrorBit SPI multi-I/O flash module
- CLPD supports a variety of FlexBus and LPC bus interfaces
- PISMO2 memory socket supporting:
  - 16-bit ADM memory
  - 6-bit ADP memory
  - Burst NOR memory
  - 4/8-bit eMMC
- Selectable I/O voltage for the PISMO2 interface (1.8 or 3.3 volt)
- MIO SPI connector supporting Spansion multi-I/O SPI

Step-by-Step Installation Instructions

1 Set the “Working Mode” user switch (SW1) and the “VIO” switches (MEM_VIO & CPU_VIO) to the correct configuration for your Tower System controller module. Refer to the jumper settings table for additional details.

2 Attach the included Spansion 1 Gb GL-S MirrorBit Eclipse flash PISMO2 module to the PISMO2 socket on the TWR-MEM-PISMO. Ensure that the keyed connector is securely connected.

3 Attach the included Spansion 128 MB MirrorBit SPI multi-I/O flash module to the 9-pin header. Ensure that the Pin 1 indicator (triangle) on the SPI module is oriented towards Pin 1 of the 9-pin connector (J4).

4 Assemble your Tower System, including at minimum a Tower System controller module and the TWR-MEM-PISMO module with the attached memory modules.

5 Visit **freescale.com/TowerPISMO** for example projects for select Tower System controller modules.

TWR-MEM-PISMO Jumper Options

The following is a list of all jumper options. The default installed jumper settings are shown in white text within the black boxes.

Switch	Option	Setting	Description
SW1 - Dip 1	Memory Interface Type	**On**	FlexBus External Bus Interface
		Off	LPC External Bus Interface
SW1 - Dip 2	Address/ Data Muxing	**On**	Muxed: Data Line Is Shared with Address Line
		Off	Non-Muxed: Data Lines Are Dedicated
SW1 - Dip 3	Data Width	On	8-bit Data
		Off	16-bit Data
SW1 - Dip 4	TWR-ELEV Usage	**On**	Primary Only
		Off	Primary and Secondary*
SW1 - Dip 5	For Future Use	On	
		Off	
SW1 - Dip 6	For Future Use	On	
		Off	

Continued...

* Not all Tower System Controller modules utilize the external bus interface on the secondary side, please refer to the respective Tower System Controller documentation to verify if this setting is applicable.

Jumper Options (continued)

The following is a list of all jumper options. The default installed jumper settings are shown in white text within the black boxes.

Switch	Option	Setting	Description
SW1 - Dip 7	For Future Use	On	
		Off	
SW1 - Dip 8	For Future Use	On	
		Off	
SW2	CPU Voltage I/O	**3V3**	CPLD Interfaces the Controller at 3.3 volts
		1V8	CPLD Interfaces the Controller at 1.8 volts
SW3	MEM Voltage I/O	**3V3**	CPLD Interfaces the PISMO2 Memory at 3.3 volts
		1V8	CPLD Interfaces the PISMO2 Memory at 3.3 volts

* Not all Tower System Controller modules utilize the external bus interface on the secondary side, please refer to the respective Tower System Controller documentation to verify if this setting is applicable.

Example Configuration

The following is a list of example settings for a subset of the supported Tower System Controller Modules.

Controller Module	SW1 Setting (0-On, 1-Off) 1-2-3-4-5-6-7-8	Description
TWR-K60N512	0-1-0-0-0-0-0-0	8-bit Non-Muxed FlexBus (Primary Side Only)
	0-0-1-0-0-0-0-0	16-bit Muxed Flexbus (Primary Side Only)
TWR-MCF5225X	0-1-0-0-0-0-0-0	8-bit Non-Muxed FlexBus (Primary Side Only)
	0-0-1-0-0-0-0-0	16-bit Muxed Flexbus (Primary Side Only)
TWR-MCF5441X	0-1-0-1-0-0-0-0	8-bit Non-Muxed FlexBus (Primary+Secondary)
	0-0-1-1-0-0-0-0	16-bit Muxed Flexbus (Primary+Secondary)
TWR-MPC5125	1-1-0-1-0-0-0-0	8-bit Non-Muxed LPC (Primary+Secondary)
	1-0-1-1-0-0-0-0	16-bit Muxed LPC (Primary+Secondary)
	1-1-1-1-0-0-0-0	16-bit Muxed LPC (Primary+Secondary)*

* In this mode the TWR-MPC5125 is limited to 32MB address space

Visit **freescale.com/TowerPISMO** for information on the TWR-MEM-PISMO module, including:

- User manual
- Schematics
- Example application
- CPLD code

Support

Visit **freescale.com/support** for a list of phone numbers within your region.

Warranty

Visit **freescale.com/warranty** for complete warranty information.

For more information, visit freescale.com/Tower

Join the online Tower community at towergeeks.org

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