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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.)

Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

# MITSUBISHI MICROCOMPUTERS

# 4513/4514 Group

SINGLE-CHIP 4-BIT CMOS MICROCOMPUTER

## DESCRIPTION

The 4513/4514 Group is a 4-bit single-chip microcomputer designed with CMOS technology. Its CPU is that of the 4500 series using a simple, high-speed instruction set. The computer is equipped with serial I/O, four 8-bit timers (each timer has a reload register), and 10-bit A-D converter.

The various microcomputers in the 4513/4514 Group include variations of the built-in memory type and package as shown in the table below.

## FEATURES

- Minimum instruction execution time ..... 0.75  $\mu$ s  
(at 4.0 MHz oscillation frequency, in high-speed mode, VDD = 4.0 V to 5.5 V)
- Supply voltage
  - Middle-speed mode
    - ..... 2.5 V to 5.5 V (at 4.2 MHz oscillation frequency, for Mask ROM version and One Time PROM version)
    - ..... 2.0 V to 5.5 V (at 3.0 MHz oscillation frequency, for Mask ROM version)
    - (Operation voltage of A-D conversion: 2.7 V to 5.5 V)
  - High-speed mode
    - ..... 4.0 V to 5.5 V (at 4.2 MHz oscillation frequency, for Mask ROM version and One Time PROM version)
    - ..... 2.5 V to 5.5 V (at 2.0 MHz oscillation frequency, for Mask ROM version and One Time PROM version)
    - ..... 2.0 V to 5.5 V (at 1.5 MHz oscillation frequency, for Mask ROM version)
    - (Operation voltage of A-D conversion: 2.7 V to 5.5 V)

- Timers
  - Timer 1 ..... 8-bit timer with a reload register
  - Timer 2 ..... 8-bit timer with a reload register
  - Timer 3 ..... 8-bit timer with a reload register
  - Timer 4 ..... 8-bit timer with a reload register
- Interrupt ..... 8 sources
- Serial I/O ..... 8 bit-wide
- A-D converter ..... 10-bit successive comparison method
- Voltage comparator ..... 2 circuits
- Watchdog timer ..... 16 bits
- Voltage drop detection circuit
- Clock generating circuit (ceramic resonator)
- LED drive directly enabled (port D)

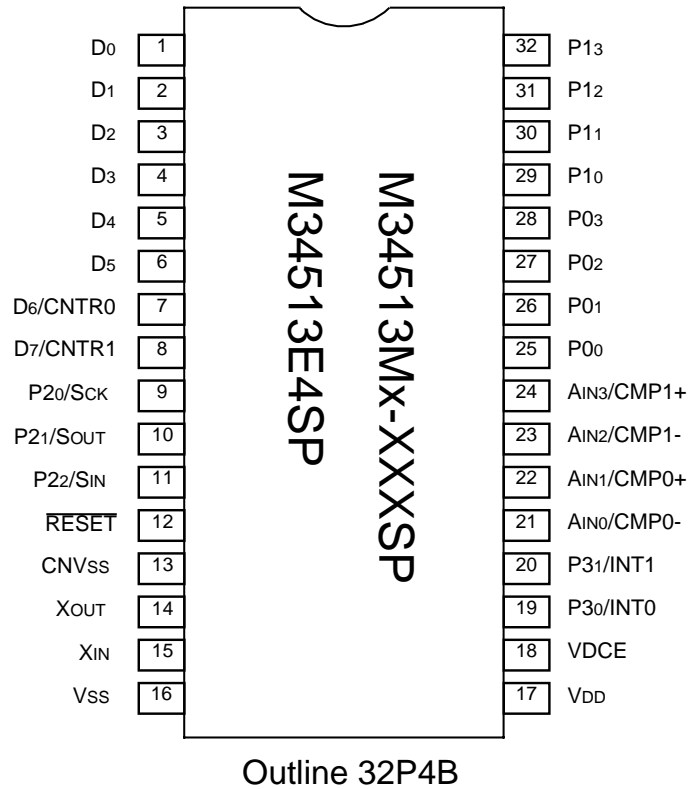
## APPLICATION

Electrical household appliance, consumer electronic products, office automation equipment, etc.

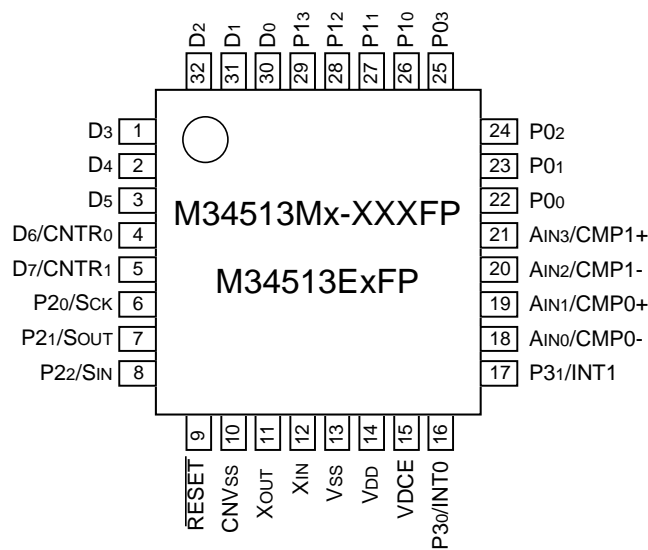
| Product              | ROM (PROM) size<br>(X 10 bits) | RAM size<br>(X 4 bits) | Package               | ROM type      |
|----------------------|--------------------------------|------------------------|-----------------------|---------------|
| M34513M2-XXXSP/FP    | 2048 words                     | 128 words              | SP: 32P4B FP: 32P6U-A | Mask ROM      |
| M34513M4-XXXSP/FP    | 4096 words                     | 256 words              | SP: 32P4B FP: 32P6U-A | Mask ROM      |
| M34513E4SP/FP (Note) | 4096 words                     | 256 words              | SP: 32P4B FP: 32P6U-A | One Time PROM |
| M34513M6-XXXFP       | 6144 words                     | 384 words              | 32P6U-A               | Mask ROM      |
| M34513M8-XXXFP       | 8192 words                     | 384 words              | 32P6U-A               | Mask ROM      |
| M34513E8FP (Note)    | 8192 words                     | 384 words              | 32P6U-A               | One Time PROM |
| M34514M6-XXXFP       | 6144 words                     | 384 words              | 42P2R-A               | Mask ROM      |
| M34514M8-XXXFP       | 8192 words                     | 384 words              | 42P2R-A               | Mask ROM      |
| M34514E8FP (Note)    | 8192 words                     | 384 words              | 42P2R-A               | One Time PROM |

Note: shipped in blank

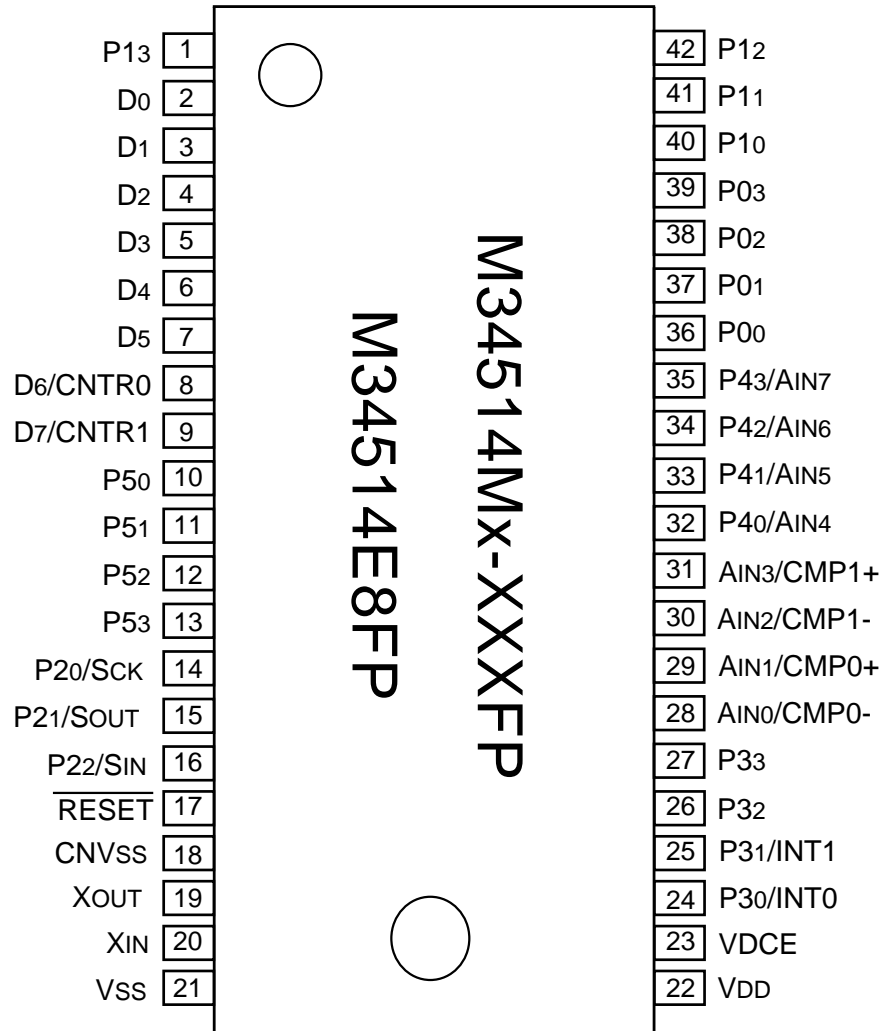
**PIN CONFIGURATION (TOP VIEW) 4513 Group**



Outline 32P4B

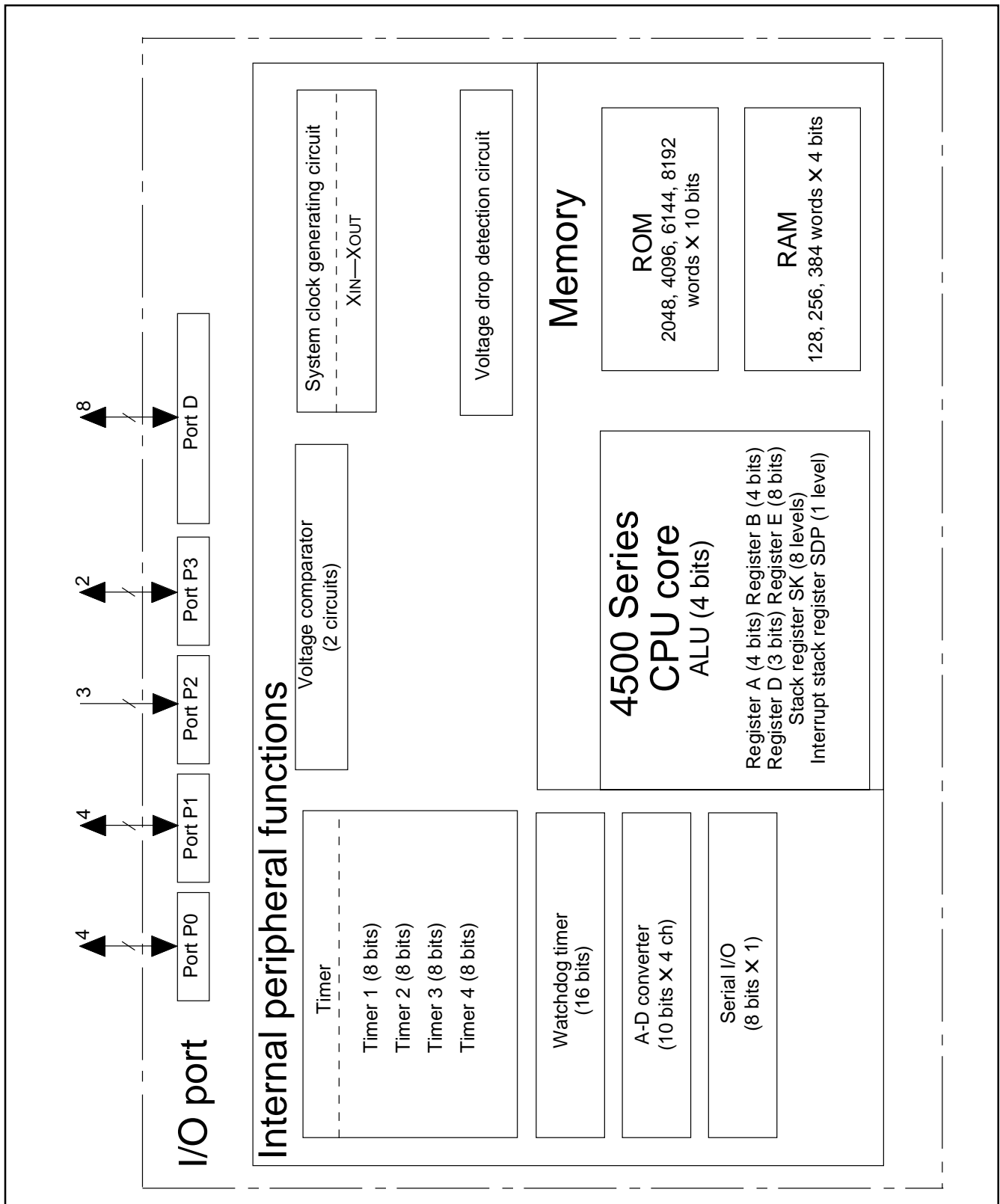


Outline 32P6U-A

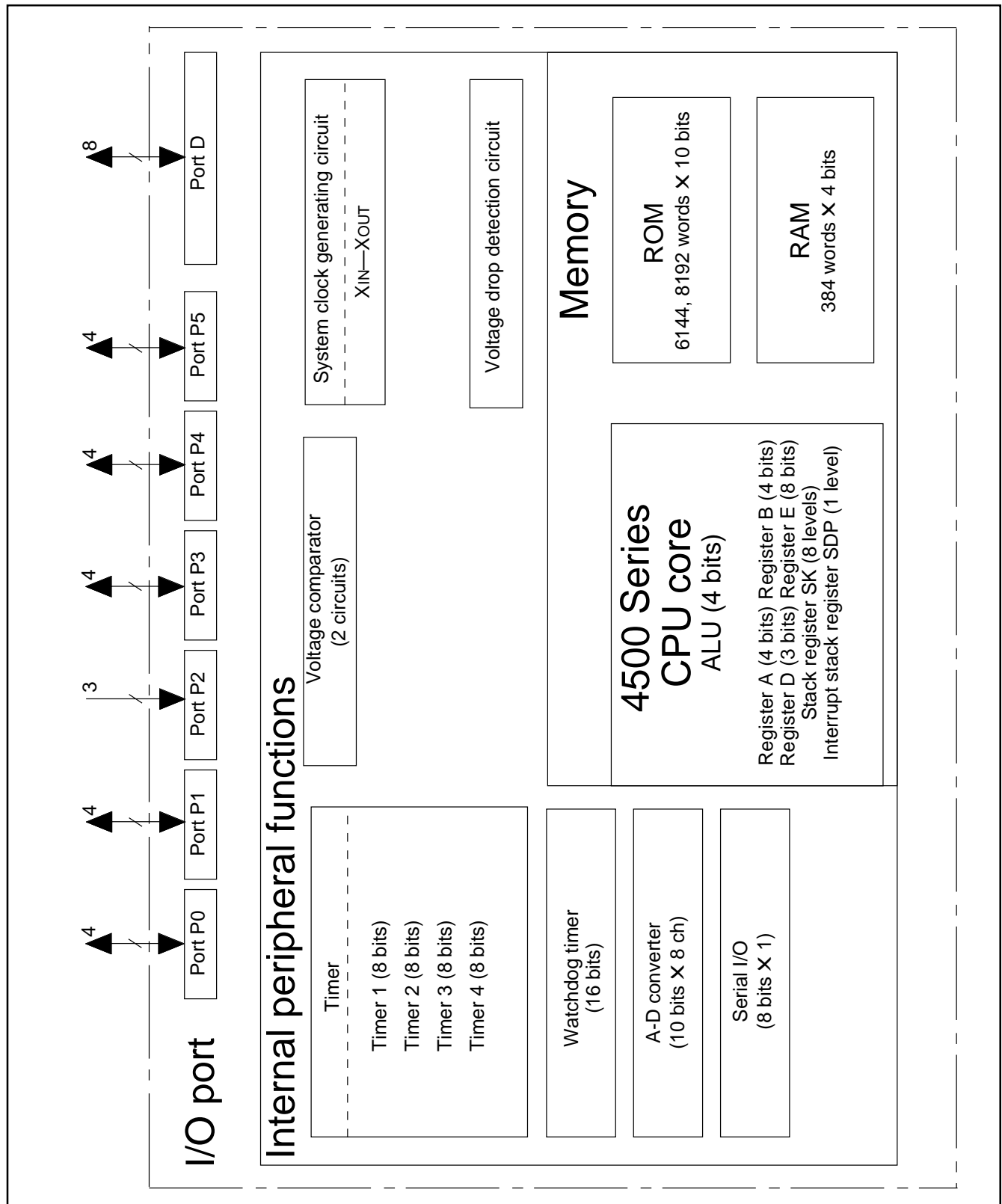
**PIN CONFIGURATION (TOP VIEW) 4514 Group**


Outline 42P2R-A

## BLOCK DIAGRAM (4513 Group)



# BLOCK DIAGRAM (4514 Group)





# PERFORMANCE OVERVIEW

| Parameter                          |                  | Function   |
|------------------------------------|------------------|--|
| Number of basic instructions       | 4513 Group       | 123  |
|                                    | 4514 Group       | 128  |
| Minimum instruction execution time |                  | 0.75 $\mu$ s (at 4.0 MHz oscillation frequency, in high-speed mode)  |
| Memory sizes                       | ROM              | M34513M2 2048 words $\times$ 10 bits   |
|                                    |                  | M34513M4/E4 4096 words $\times$ 10 bits  |
|                                    |                  | M34513M6 6144 words $\times$ 10 bits   |
|                                    |                  | M34513M8/E8 8192 words $\times$ 10 bits  |
|                                    |                  | M34514M6 6144 words $\times$ 10 bits   |
|                                    |                  | M34514M8/E8 8192 words $\times$ 10 bits  |
|                                    | RAM              | M34513M2 128 words $\times$ 4 bits   |
|                                    |                  | M34513M4/E4 256 words $\times$ 4 bits  |
|                                    |                  | M34513M6 384 words $\times$ 4 bits   |
|                                    |                  | M34513M8/E8 384 words $\times$ 4 bits  |
|                                    |                  | M34514M6 384 words $\times$ 4 bits   |
|                                    |                  | M34514M8/E8 384 words $\times$ 4 bits  |
| Input/Output ports                 | D0–D7            | I/O (Input is examined by skip decision)<br>Eight independent I/O ports; ports D6 and D7 are also used as CNTR0 and CNTR1, respectively.   |
|                                    | P00–P03          | I/O<br>4-bit I/O port; each pin is equipped with a pull-up function and a key-on wakeup function. Both functions can be switched by software.  |
|                                    | P10–P13          | I/O<br>4-bit I/O port; each pin is equipped with a pull-up function and a key-on wakeup function. Both functions can be switched by software.  |
|                                    | P20–P22          | Input<br>3-bit input port; ports P20, P21 and P22 are also used as SCK, SOUT and SIN, respectively.  |
|                                    | P30–P33          | I/O<br>4-bit I/O port (2-bit I/O port for the 4513 Group); ports P30 and P31 are also used as INT0 and INT1, respectively. The 4513 Group does not have ports P32, P33.  |
|                                    | P40–P43          | I/O<br>4-bit I/O port; The 4513 Group does not have this port.   |
|                                    | P50–P53          | I/O<br>4-bit I/O port with a direction register; The 4513 Group does not have this port.   |
|                                    | CNTR0            | I/O<br>1-bit I/O; CNTR0 pin is also used as port D6.   |
|                                    | CNTR1            | I/O<br>1-bit I/O; CNTR1 pin is also used as port D7.   |
|                                    | INT0             | Input<br>1-bit input; INT0 pin is also used as port P30 and equipped with a key-on wakeup function.  |
|                                    | INT1             | Input<br>1-bit input; INT1 pin is also used as port P31 and equipped with a key-on wakeup function.  |
| Timers                             | Timer 1          | 8-bit programmable timer with a reload register.   |
|                                    | Timer 2          | 8-bit programmable timer with a reload register is also used as an event counter.  |
|                                    | Timer 3          | 8-bit programmable timer with a reload register.   |
|                                    | Timer 4          | 8-bit programmable timer with a reload register is also used as an event counter.  |
| A-D converter                      |                  | 10-bit wide, This is equipped with an 8-bit comparator function.   |
| Voltage comparator                 |                  | 2 circuits (CMP0, CMP1)  |
| Serial I/O                         |                  | 8-bit $\times$ 1   |
| Interrupt                          | Sources          | 8 (two for external, four for timer, one for A-D, and one for serial I/O)  |
|                                    | Nesting          | 1 level  |
| Subroutine nesting                 |                  | 8 levels   |
| Device structure                   |                  | CMOS silicon gate  |
| Package                            | 4513 Group       | 32-pin plastic molded SDIP (32P4B)/LQFP(32P6U-A)   |
|                                    | 4514 Group       | 42-pin plastic molded SSOP (42P2R-A)   |
| Operating temperature range        |                  | –20 °C to 85 °C  |
| Supply voltage                     |                  | 2.0 V to 5.5 V for Mask ROM version, 2.5 V to 5.5 V for One Time PROM version (Refer to the electrical characteristics because the supply voltage depends on the oscillation frequency.)   |
| Power dissipation (typical value)  | Active mode      | 1.8 mA (at VDD = 5.0 V, 4.0 MHz oscillation frequency, in middle-speed mode, output transistors in the cut-off state)<br>3.0 mA (at VDD = 5.0 V, 4.0 MHz oscillation frequency, in high-speed mode, output transistors in the cut-off state) |
|                                    | RAM back-up mode | 0.1 $\mu$ A (at room temperature, VDD = 5 V, output transistors in the cut-off state)  |

## PIN DESCRIPTION

| Pin          | Name  | Input/Output | Function  |
|--------------|---|--------------|---|
| VDD          | Power supply  | —            | Connected to a plus power supply.   |
| VSS          | Ground  | —            | Connected to a 0 V power supply.  |
| VDCE         | Voltage drop detection circuit enable               | Input        | VDCE pin is used to control the operation/stop of the voltage drop detection circuit. When "H" level is input to this pin, the circuit is operating. When "L" level is input to this pin, the circuit is stopped.   |
| CNVSS        | CNVSS   | —            | Connect CNVSS to VSS and apply "L" (0V) to CNVSS certainly.   |
| RESET        | Reset input   | I/O          | An N-channel open-drain I/O pin for a system reset. When the watchdog timer causes the system to be reset or system reset is performed by the voltage drop detection circuit, the RESET pin outputs "L" level.  |
| XIN          | System clock input                                  | Input        | I/O pins of the system clock generating circuit. XIN and XOUT can be connected to ceramic resonator. A feedback resistor is built-in between them.  |
| XOUT         | System clock output                                 | Output       |   |
| D0–D7        | I/O port D<br>(Input is examined by skip decision.) | I/O          | Each pin of port D has an independent 1-bit wide I/O function. Each pin has an output latch. For input use, set the latch of the specified bit to "1." The output structure is N-channel open-drain. Ports D6 and D7 are also used as CNTR0 and CNTR1, respectively.                        |
| P00–P03      | I/O port P0   | I/O          | Each of ports P0 and P1 serves as a 4-bit I/O port, and it can be used as inputs when the output latch is set to "1." The output structure is N-channel open-drain. Every pin of the ports has a key-on wakeup function and a pull-up function. Both functions can be switched by software. |
| P10–P13      | I/O port P1   | I/O          |   |
| P20–P22      | Input port P2                                       | Input        | 3-bit input port. Ports P20, P21 and P22 are also used as SCK, SOUT and SIN, respectively.  |
| P30–P33      | I/O port P3   | I/O          | 4-bit I/O port (2-bit I/O port for the 4513 Group). For input use, set the latch of the specified bit to "1." The output structure is N-channel open-drain. Ports P30 and P31 are also used as INT0 and INT1, respectively. The 4513 Group does not have ports P32, P33.                    |
| P40–P43      | I/O port P4   | I/O          | 4-bit I/O port. For input use, set the latch of the specified bit to "1." The output structure is N-channel open-drain. Ports P40–P43 are also used as analog input pins AIN4–AIN7, respectively. The 4513 Group does not have port P4.   |
| P50–P53      | I/O port P5   | I/O          | 4-bit I/O port. Each pin has a direction register and an independent 1-bit wide I/O function. For input use, set the direction register to "0." For output use, set the direction register to "1." The output structure is CMOS. The 4513 Group does not have port P5.                      |
| AIN0–AIN7    | Analog input  | Input        | Analog input pins for A-D converter. AIN0–AIN3 are also used as voltage comparator input pins and AIN4–AIN7 are also used as port P4. The 4513 Group does not have AIN4–AIN7.   |
| CNTR0        | Timer input/output                                  | I/O          | CNTR0 pin has the function to input the clock for the timer 2 event counter, and to output the timer 1 underflow signal divided by 2. CNTR0 pin is also used as port D6.  |
| CNTR1        | Timer input/output                                  | I/O          | CNTR1 pin has the function to input the clock for the timer 4 event counter, and to output the timer 3 underflow signal divided by 2. CNTR1 pin is also used as port D7.  |
| INT0, INT1   | Interrupt input                                     | Input        | INT0, INT1 pins accept external interrupts. They also accept the input signal to return the system from the RAM back-up state. INT0, INT1 pins are also used as ports P30 and P31, respectively.  |
| SIN          | Serial data input                                   | Input        | SIN pin is used to input serial data signals by software. SIN pin is also used as port P22.   |
| SOUT         | Serial data output                                  | Output       | SOUT pin is used to output serial data signals by software. SOUT pin is also used as port P21.  |
| SCK          | Serial I/O clock input/output                       | I/O          | SCK pin is used to input and output synchronous clock signals for serial data transfer by software. SCK pin is also used as port P20.   |
| CMP0-, CMP0+ | Voltage comparator input                            | Input        | CMP0-, CMP0+ pins are used as the voltage comparator input pin when the voltage comparator function is selected by software. CMP0-, CMP0+ pins are also used as AIN0 and AIN1.  |
| CMP1-, CMP1+ | Voltage comparator input                            | Input        | CMP1-, CMP1+ pins are used as the voltage comparator input pin when the voltage comparator function is selected by software. CMP1-, CMP1+ pins are also used as AIN2 and AIN3.  |

## MULTIFUNCTION

| Pin | Multifunction | Pin   | Multifunction | Pin  | Multifunction | Pin   | Multifunction |
|-----|---------------|-------|---------------|------|---------------|-------|---------------|
| D6  | CNTR0         | CNTR0 | D6            | AIN0 | CMP0-         | CMP0- | AIN0          |
| D7  | CNTR1         | CNTR1 | D7            | AIN1 | CMP0+         | CMP0+ | AIN1          |
| P20 | SCK           | SCK   | P20           | AIN2 | CMP1-         | CMP1- | AIN2          |
| P21 | SOUT          | SOUT  | P21           | AIN3 | CMP1+         | CMP1+ | AIN3          |
| P22 | SIN           | SIN   | P22           | P40  | AIN4          | AIN4  | P40           |
| P30 | INT0          | INT0  | P30           | P41  | AIN5          | AIN5  | P41           |
| P31 | INT1          | INT1  | P31           | P42  | AIN6          | AIN6  | P42           |
|     |               |       |               | P43  | AIN7          | AIN7  | P43           |

Notes 1: Pins except above have just single function.

2: The input of D6, D7, P20–P22, CMP0-, CMP0+, CMP1-, CMP1+ and the input/output of P30, P31, P40–P43 can be used even when CNTR0, CNTR1, SCK, SOUT, SIN, INT0, INT1, and AIN0–AIN7 are selected.

3: The 4513 Group does not have P40/AIN4–P43/AIN7.

## CONNECTIONS OF UNUSED PINS

| Pin  | Connection   |
|--|--|
| XOUT   | Open (when using an external clock).   |
| VDCE   | Connect to VSS.  |
| D0–D5<br>D6/CNTR0<br>D7/CNTR1                        | Connect to VSS, or set the output latch to "0" and open.   |
| P20/SCK<br>P21/SOUT<br>P22/SIN                       | Connect to VSS.  |
| P30/INT0<br>P31/INT1<br>P32, P33                     | Connect to VSS, or set the output latch to "0" and open.   |
| P40/AIN4–P43/AIN7                                    | Connect to VSS, or set the output latch to "0" and open.   |
| P50–P53 (Note 1)                                     | When the input mode is selected by software, pull-up to VDD through a resistor or pull-down to VDD.<br>When selecting the output mode, open. |
| AIN0/CMP0-<br>AIN1/CMP0+<br>AIN2/CMP1-<br>AIN3/CMP1+ | Connect to VSS.  |
| P00–P03  | Open or connect to VSS (Note 2)  |
| P10–P13  | Open or connect to VSS (Note 2)  |

Notes 1: After system is released from reset, port P5 is in an input mode (direction register FR0 = 00002)

2: When the P00–P03 and P10–P13 are connected to VSS, turn off their pull-up transistors (register PU0i="0") and also invalidate the key-on wakeup functions (register K0i="0") by software. When these pins are connected to VSS while the key-on wakeup functions are left valid, the system fails to return from RAM back-up state. When these pins are open, turn on their pull-up transistors (register PU0i="1") by software, or set the output latch to "0." Be sure to select the key-on wakeup functions and the pull-up functions with every two pins. If only one of the two pins for the key-on wakeup function is used, turn on their pull-up transistors by software and also disconnect the other pin. (i = 0, 1, 2, or 3.)

(Note when the output latch is set to "0" and pins are open)

● After system is released from reset, port is in a high-impedance state until it is set the output latch to "0" by software. Accordingly, the voltage level of pins is undefined and the excess of the supply current may occur while the port is in a high-impedance state.

● To set the output latch periodically by software is recommended because value of output latch may change by noise or a program run away (caused by noise).

(Note when connecting to VSS and VDD)

● Connect the unused pins to VSS and VDD using the thickest wire at the shortest distance against noise.

## PORT FUNCTION

| Port                | Pin                              | Input<br>Output | Output structure     | I/O<br>unit | Control<br>instructions | Control<br>registers | Remark  |
|---------------------|----------------------------------|-----------------|----------------------|-------------|-------------------------|----------------------|---|
| Port D              | D0–D5                            | I/O<br>(8)      | N-channel open-drain | 1           | SD, RD<br>SZD<br>CLD    | W6                   |   |
|                     | D6/CNTR0                         |                 |                      |             |                         |                      |   |
|                     | D7/CNTR1                         |                 |                      |             |                         |                      |   |
| Port P0             | P00–P03                          | I/O<br>(4)      | N-channel open-drain | 4           | OP0A<br>IAP0            | PU0, K0              | Built-in programmable pull-up<br>functions<br>Key-on wakeup functions<br>(programmable) |
| Port P1             | P10–P13                          | I/O<br>(4)      | N-channel open-drain | 4           | OP1A<br>IAP1            | PU0, K0              | Built-in programmable pull-up<br>functions<br>Key-on wakeup functions<br>(programmable) |
| Port P2             | P20/SCK<br>P21/SOUT<br>P22/SIN   | Input<br>(3)    |                      | 3           | IAP2                    | J1                   |   |
| Port P3<br>(Note 1) | P30/INT0<br>P31/INT1<br>P32, P33 | I/O<br>(4)      | N-channel open-drain | 4           | OP3A<br>IAP3            | I1, I2               | Built-in key-on wakeup<br>function<br>(P30/INT0, P31/INT1)                              |
| Port P4<br>(Note 2) | P40/AIN4<br>–P43/AIN7            | I/O<br>(4)      | N-channel open-drain | 4           | OP4A<br>IAP4            | Q2                   |   |
| Port P5<br>(Note 2) | P50–P53                          | I/O<br>(4)      | CMOS                 | 4           | OP5A<br>IAP5            | FR0                  |   |

Notes 1: The 4513 Group does not have P32 and P33.

2: The 4513 Group does not have these ports.

## DEFINITION OF CLOCK AND CYCLE

### ● System clock

The system clock is the basic clock for controlling this product.

The system clock is selected by the bit 3 of the clock control register MR.

**Table Selection of system clock**

| Register MR<br>MR3 | System clock |
|--------------------|--------------|
| 0                  | f(XIN)       |
| 1                  | f(XIN)/2     |

Note: f(XIN)/2 is selected after system is released from reset.

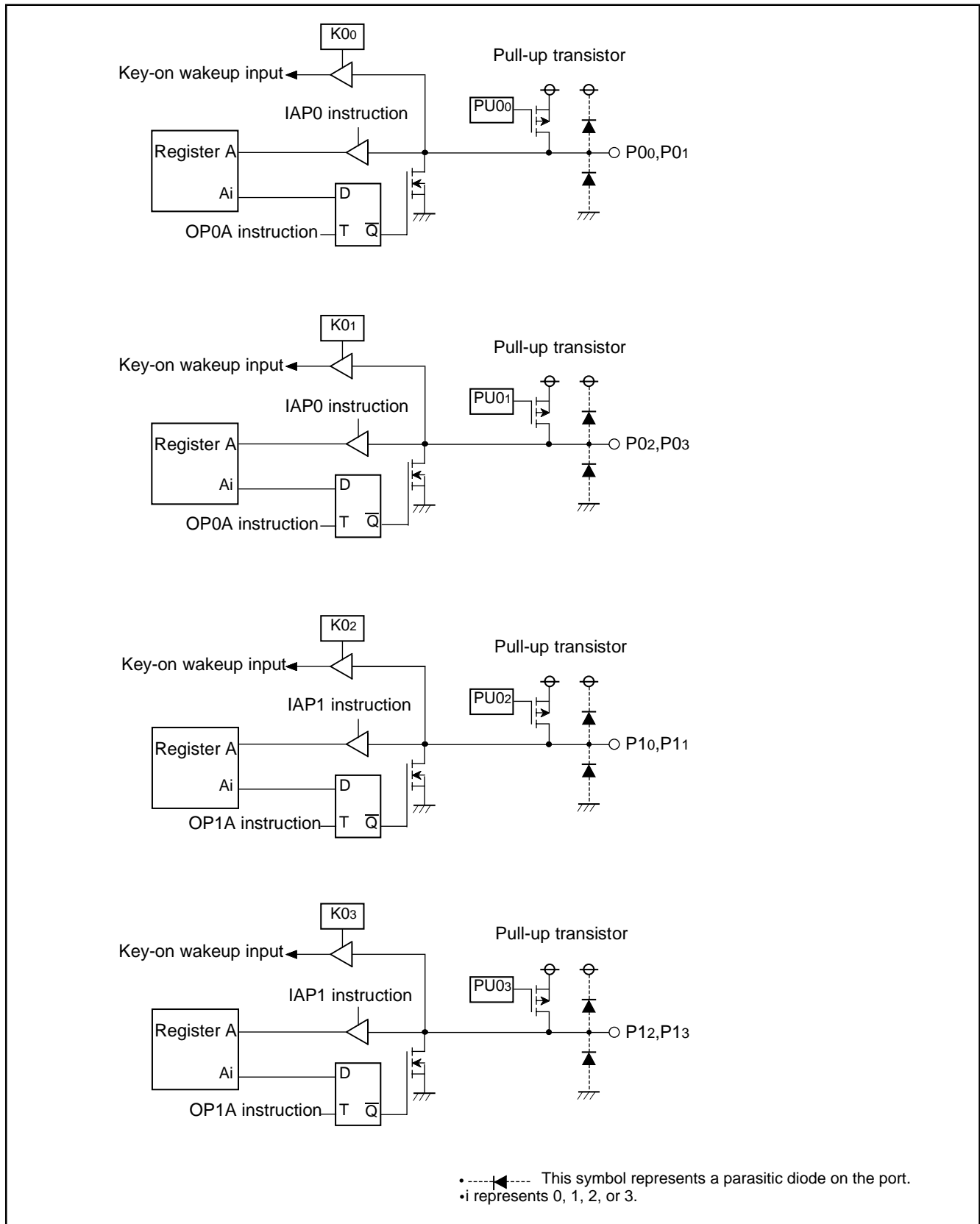
### ● Instruction clock

The instruction clock is a signal derived by dividing the system clock by 3. The one instruction clock cycle generates the one machine cycle.

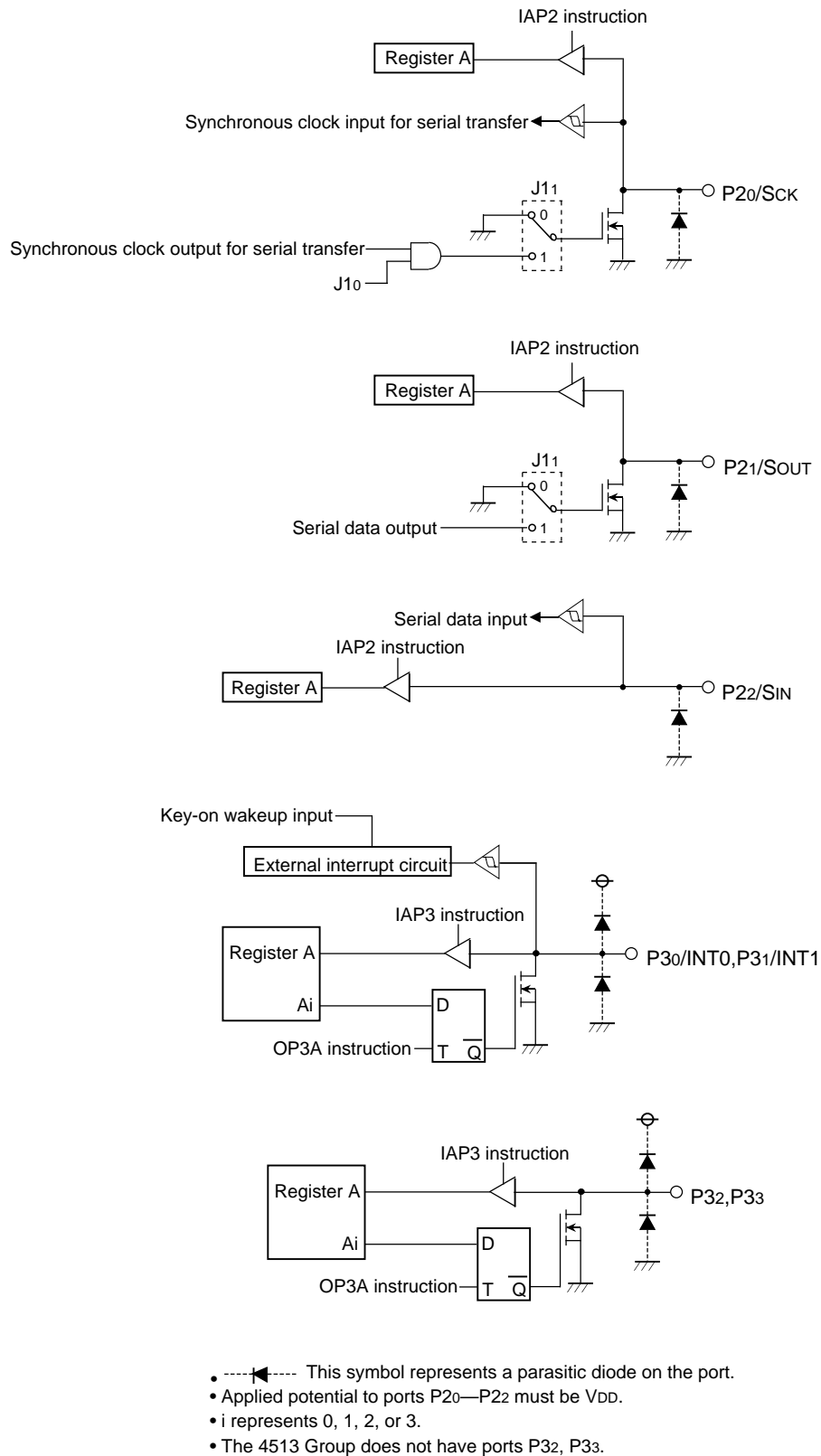
### ● Machine cycle

The machine cycle is the standard cycle required to execute the instruction.

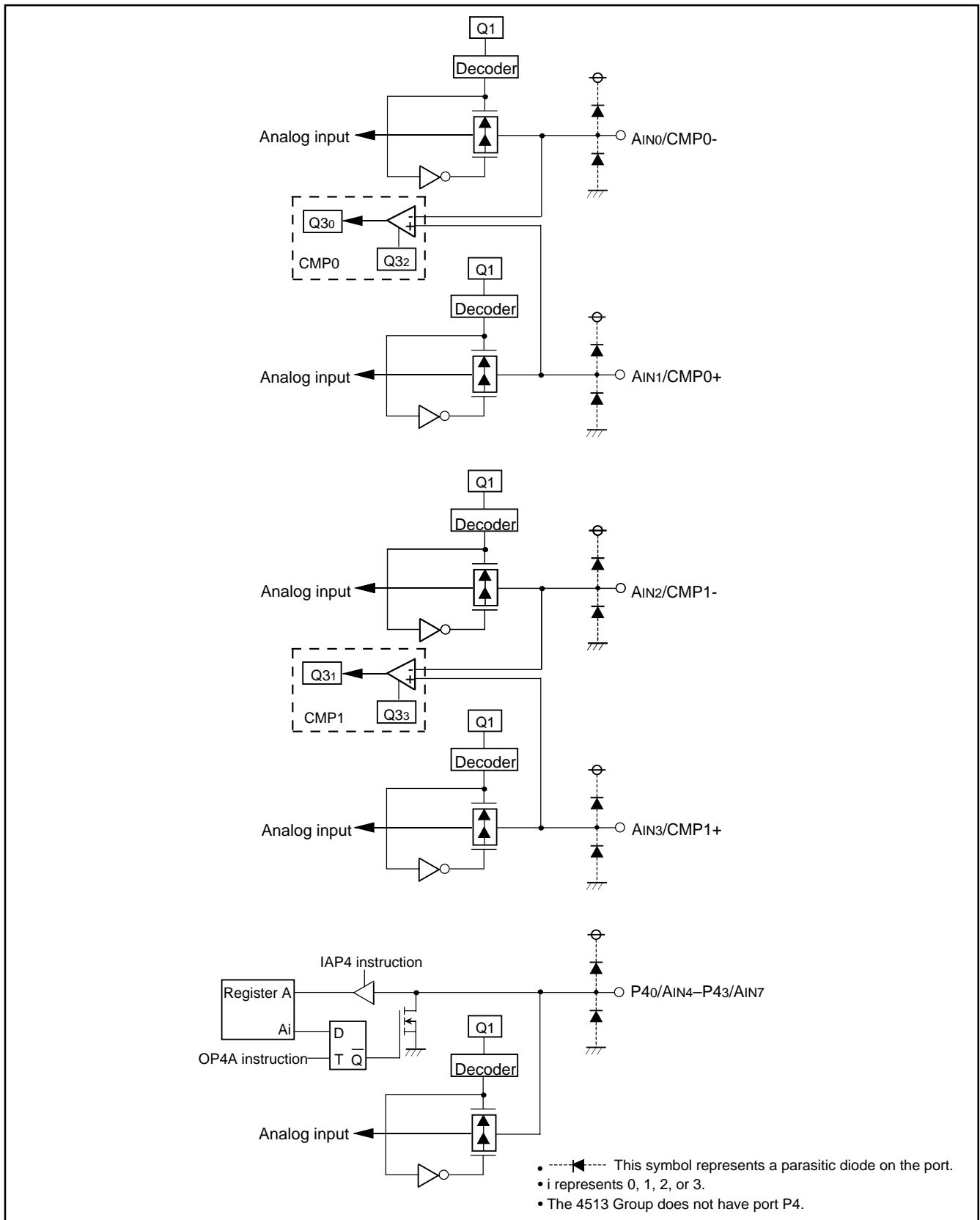
# PORT BLOCK DIAGRAMS



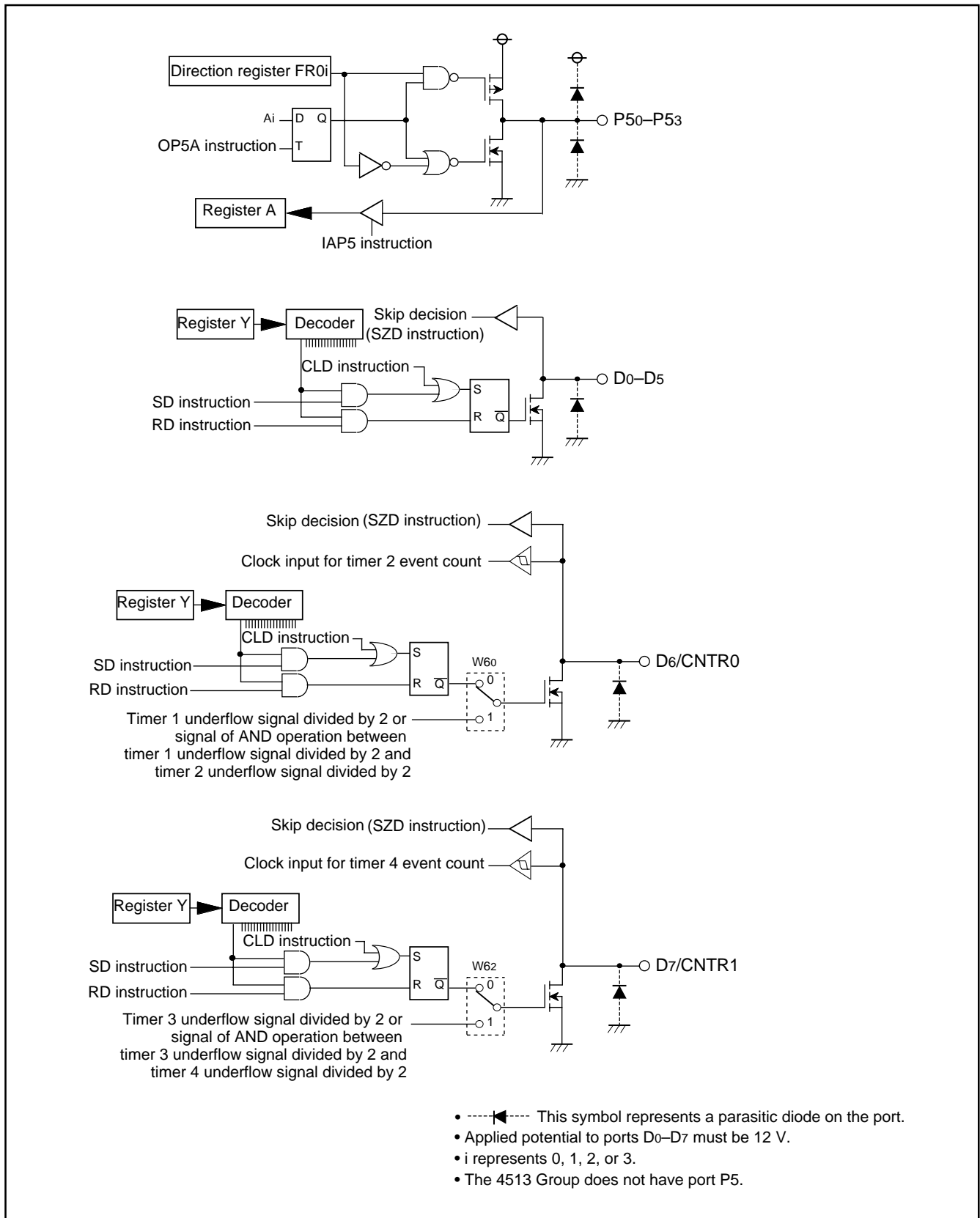
# PORT BLOCK DIAGRAMS (continued)



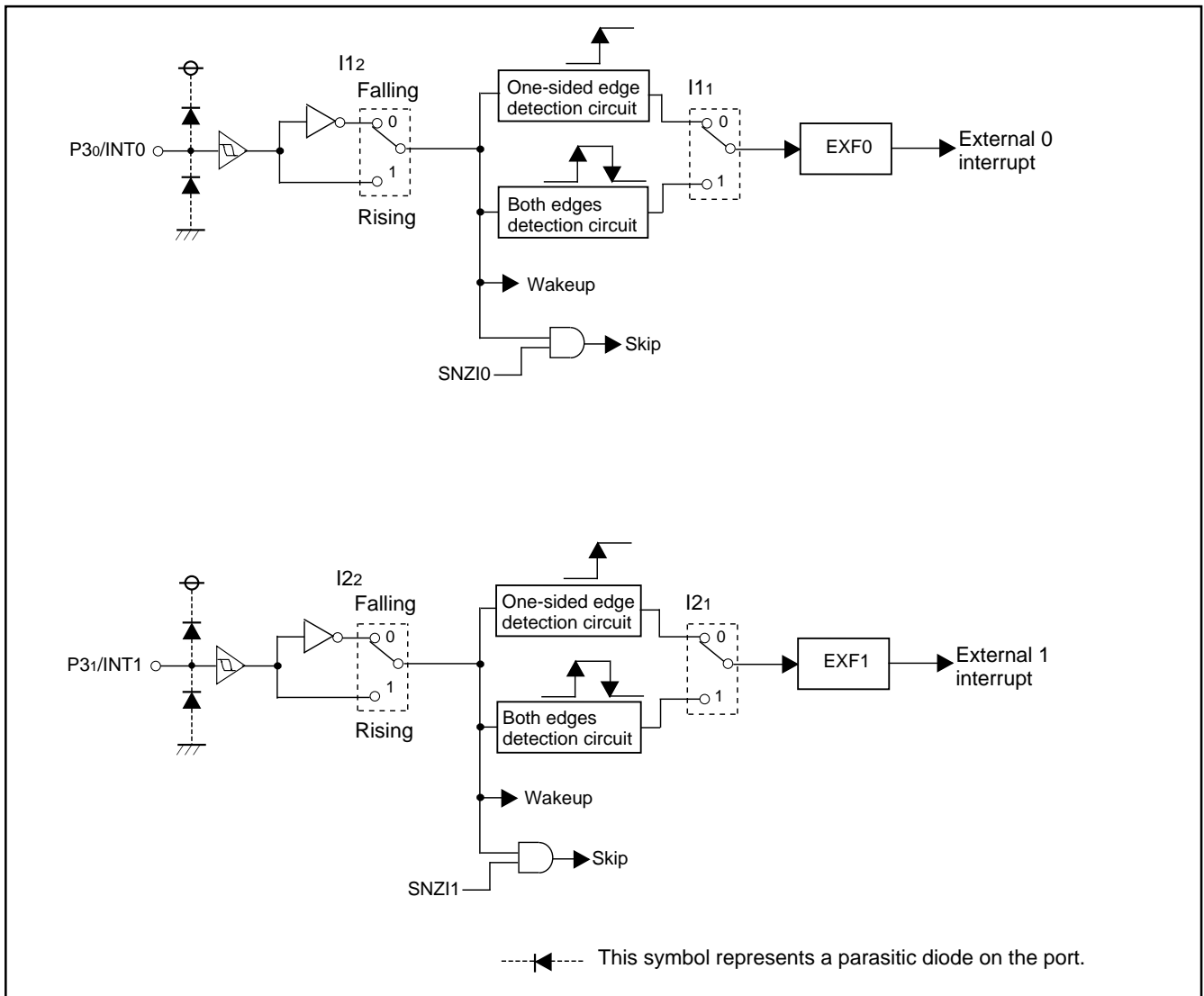
PORT BLOCK DIAGRAMS (continued)



## PORT BLOCK DIAGRAMS (continued)







External interrupt circuit structure

## FUNCTION BLOCK OPERATIONS CPU

### (1) Arithmetic logic unit (ALU)

The arithmetic logic unit ALU performs 4-bit arithmetic such as 4-bit data addition, comparison, AND operation, OR operation, and bit manipulation.

### (2) Register A and carry flag

Register A is a 4-bit register used for arithmetic, transfer, exchange, and I/O operation.

Carry flag CY is a 1-bit flag that is set to "1" when there is a carry with the AMC instruction (Figure 1).

It is unchanged with both A n instruction and AM instruction. The value of A0 is stored in carry flag CY with the RAR instruction (Figure 2).

Carry flag CY can be set to "1" with the SC instruction and cleared to "0" with the RC instruction.

### (3) Registers B and E

Register B is a 4-bit register used for temporary storage of 4-bit data, and for 8-bit data transfer together with register A.

Register E is an 8-bit register. It can be used for 8-bit data transfer with register B used as the high-order 4 bits and register A as the low-order 4 bits (Figure 3).

### (4) Register D

Register D is a 3-bit register.

It is used to store a 7-bit ROM address together with register A and is used as a pointer within the specified page when the TABP p, BLA p, or BMLA p instruction is executed (Figure 4).

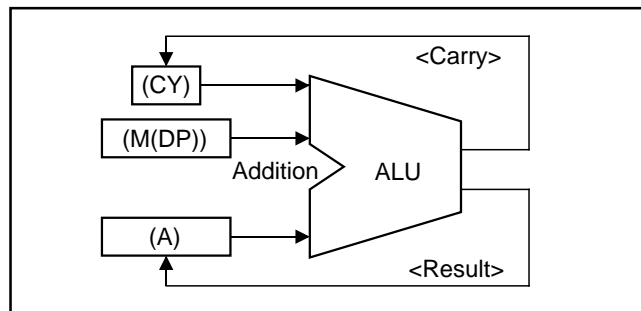


Fig. 1 AMC instruction execution example

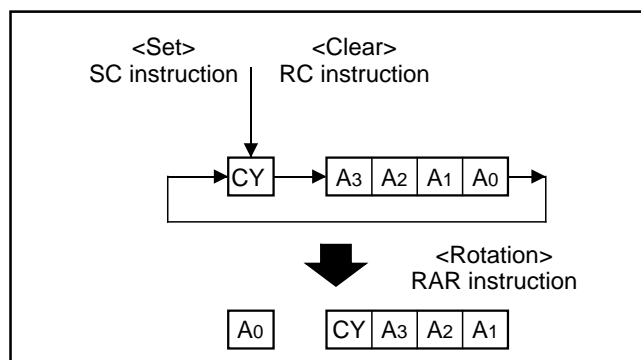


Fig. 2 RAR instruction execution example

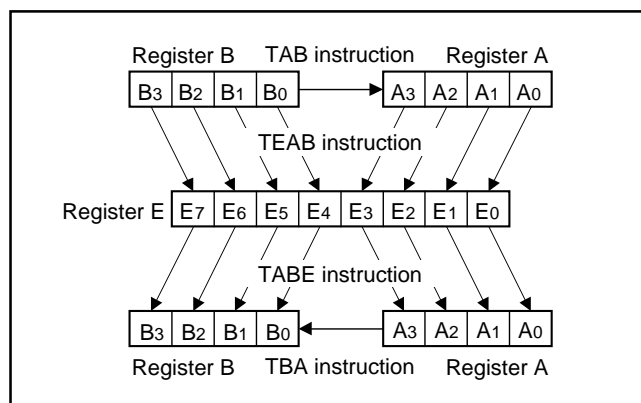


Fig. 3 Registers A, B and register E

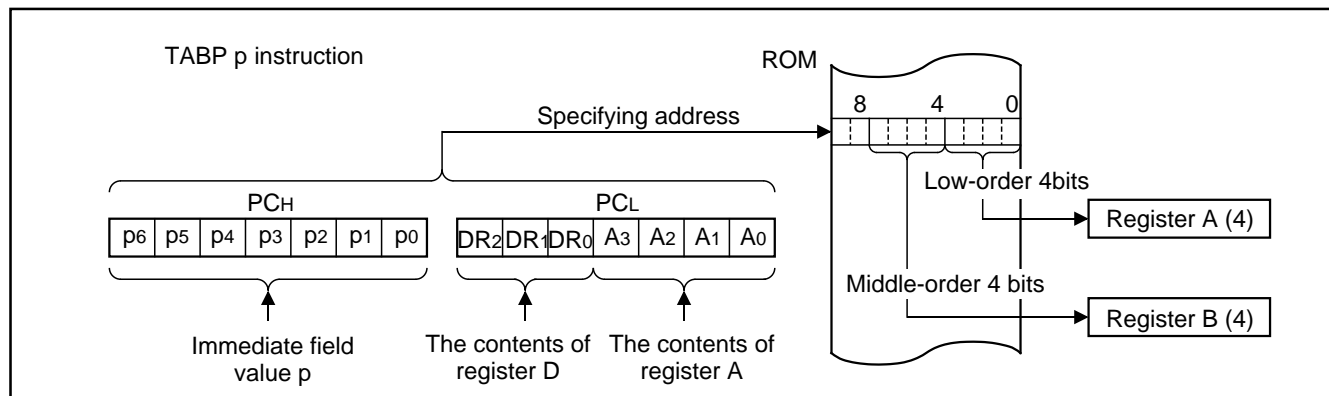


Fig. 4 TABP p instruction execution example

### (5) Stack registers (SKs) and stack pointer (SP)

Stack registers (SKs) are used to temporarily store the contents of program counter (PC) just before branching until returning to the original routine when;

- branching to an interrupt service routine (referred to as an interrupt service routine),
- performing a subroutine call, or
- executing the table reference instruction (TABP p).

Stack registers (SKs) are eight identical registers, so that subroutines can be nested up to 8 levels. However, one of stack registers is used respectively when using an interrupt service routine and when executing a table reference instruction. Accordingly, be careful not to over the stack when performing these operations together. The contents of registers SKs are destroyed when 8 levels are exceeded.

The register SK nesting level is pointed automatically by 3-bit stack pointer (SP). The contents of the stack pointer (SP) can be transferred to register A with the TASP instruction.

Figure 5 shows the stack registers (SKs) structure.

Figure 6 shows the example of operation at subroutine call.

### (6) Interrupt stack register (SDP)

Interrupt stack register (SDP) is a 1-stage register. When an interrupt occurs, this register (SDP) is used to temporarily store the contents of data pointer, carry flag, skip flag, register A, and register B just before an interrupt until returning to the original routine.

Unlike the stack registers (SKs), this register (SDP) is not used when executing the subroutine call instruction and the table reference instruction.

### (7) Skip flag

Skip flag controls skip decision for the conditional skip instructions and continuous described skip instructions. When an interrupt occurs, the contents of skip flag is stored automatically in the interrupt stack register (SDP) and the skip condition is retained.

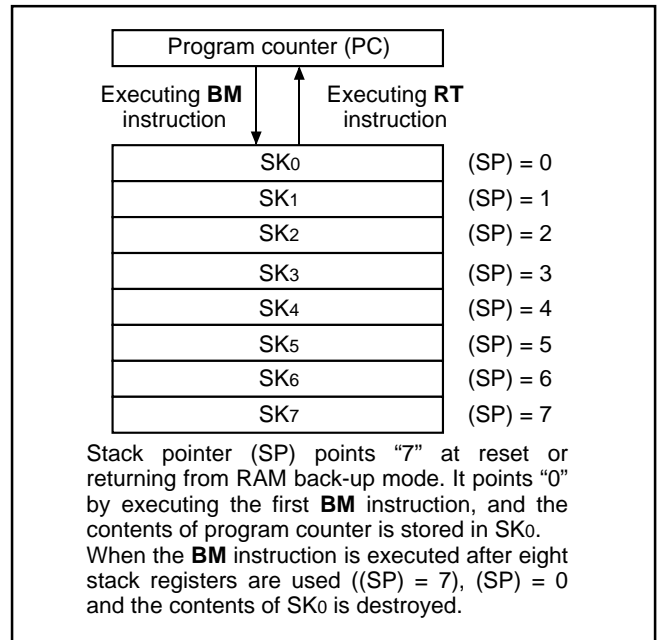


Fig. 5 Stack registers (SKs) structure

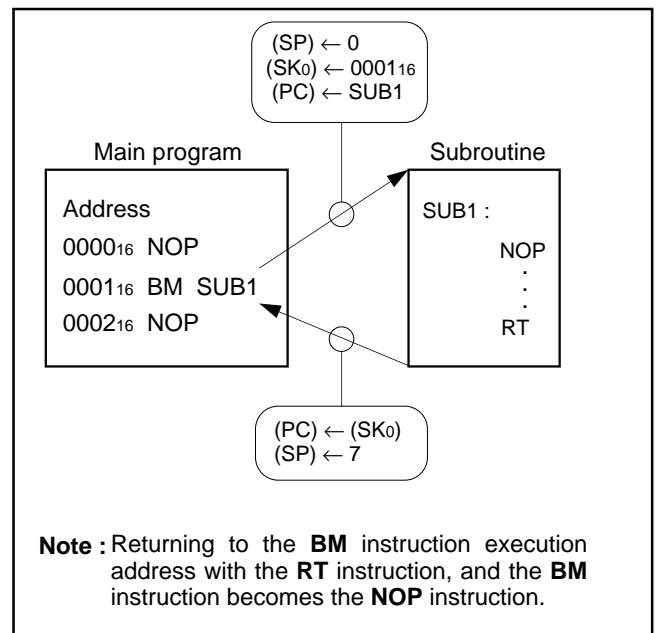


Fig. 6 Example of operation at subroutine call

### (8) Program counter (PC)

Program counter (PC) is used to specify a ROM address (page and address). It determines a sequence in which instructions stored in ROM are read. It is a binary counter that increments the number of instruction bytes each time an instruction is executed. However, the value changes to a specified address when branch instructions, subroutine call instructions, return instructions, or the table reference instruction (TABP p) is executed.

Program counter consists of PCH (most significant bit to bit 7) which specifies to a ROM page and PCL (bits 6 to 0) which specifies an address within a page. After it reaches the last address (address 127) of a page, it specifies address 0 of the next page (Figure 7).

Make sure that the PCH does not specify after the last page of the built-in ROM.

### (9) Data pointer (DP)

Data pointer (DP) is used to specify a RAM address and consists of registers Z, X, and Y. Register Z specifies a RAM file group, register X specifies a file, and register Y specifies a RAM digit (Figure 8).

Register Y is also used to specify the port D bit position.

When using port D, set the port D bit position to register Y certainly and execute the SD, RD, or SZD instruction (Figure 9).

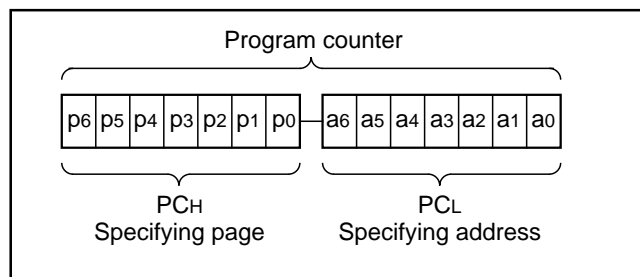


Fig. 7 Program counter (PC) structure

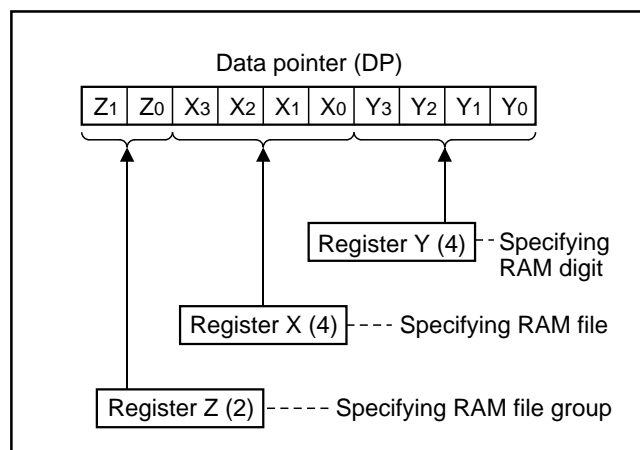


Fig. 8 Data pointer (DP) structure

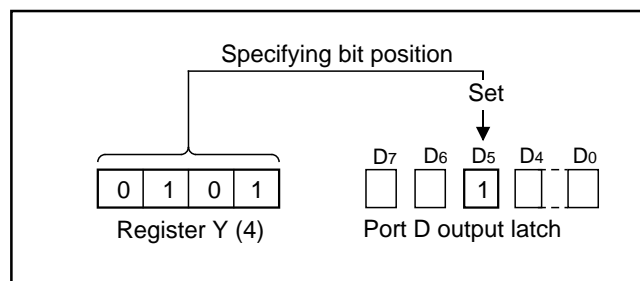


Fig. 9 SD instruction execution example

## PROGRAM MEMORY (ROM)

The program memory is a mask ROM. 1 word of ROM is composed of 10 bits. ROM is separated every 128 words by the unit of page (addresses 0 to 127). Table 1 shows the ROM size and pages. Figure 10 shows the ROM map of M34514M8/E8.

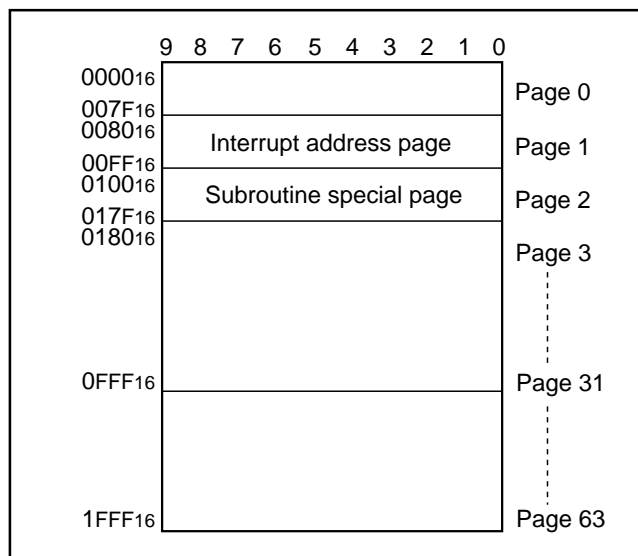
**Table 1 ROM size and pages**

| Product     | ROM size<br>(X 10 bits) | Pages        |
|-------------|-------------------------|--------------|
| M34513M2    | 2048 words              | 16 (0 to 15) |
| M34513M4/E4 | 4096 words              | 32 (0 to 31) |
| M34513M6    | 6144 words              | 48 (0 to 47) |
| M34513M8/E8 | 8192 words              | 64 (0 to 63) |
| M34514M6    | 6144 words              | 48 (0 to 47) |
| M34514M8/E8 | 8192 words              | 64 (0 to 63) |

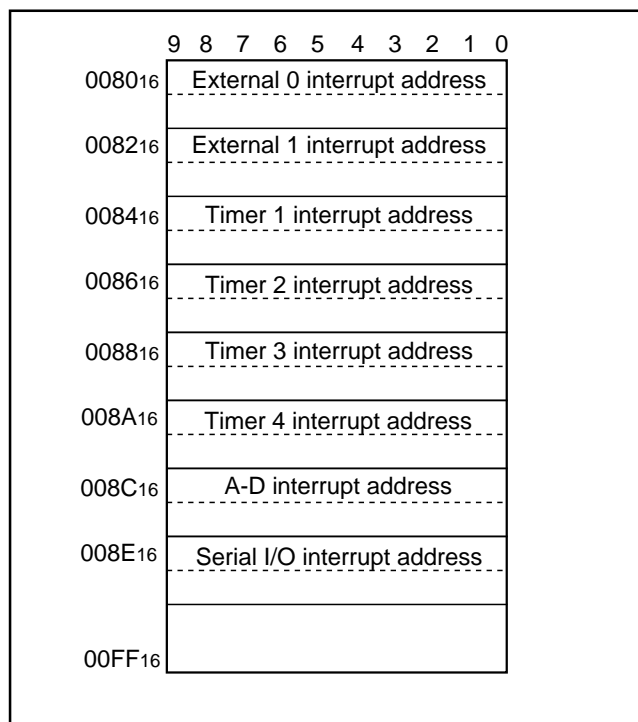
A part of page 1 (addresses 0080<sub>16</sub> to 00FF<sub>16</sub>) is reserved for interrupt addresses (Figure 11). When an interrupt occurs, the address (interrupt address) corresponding to each interrupt is set in the program counter, and the instruction at the interrupt address is executed. When using an interrupt service routine, write the instruction generating the branch to that routine at an interrupt address.

Page 2 (addresses 0100<sub>16</sub> to 017F<sub>16</sub>) is the special page for subroutine calls. Subroutines written in this page can be called from any page with the 1-word instruction (BM). Subroutines extending from page 2 to another page can also be called with the BM instruction when it starts on page 2.

ROM pattern (bits 7 to 0) of all addresses can be used as data areas with the TABP p instruction.



**Fig. 10 ROM map of M34514M8/E8**



**Fig. 11 Page 1 (addresses 0080<sub>16</sub> to 00FF<sub>16</sub>) structure**

# DATA MEMORY (RAM)

1 word of RAM is composed of 4 bits, but 1-bit manipulation (with the SB j, RB j, and SZB j instructions) is enabled for the entire memory area. A RAM address is specified by a data pointer. The data pointer consists of registers Z, X, and Y. Set a value to the data pointer certainly when executing an instruction to access RAM.

Table 2 shows the RAM size. Figure 12 shows the RAM map.

Table 2 RAM size

| Product     | RAM size                       |
|-------------|--------------------------------|
| M34513M2    | 128 words × 4 bits (512 bits)  |
| M34513M4/E4 | 256 words × 4 bits (1024 bits) |
| M34513M6    | 384 words × 4 bits (1536 bits) |
| M34513M8/E8 | 384 words × 4 bits (1536 bits) |
| M34514M6    | 384 words × 4 bits (1536 bits) |
| M34514M8/E8 | 384 words × 4 bits (1536 bits) |

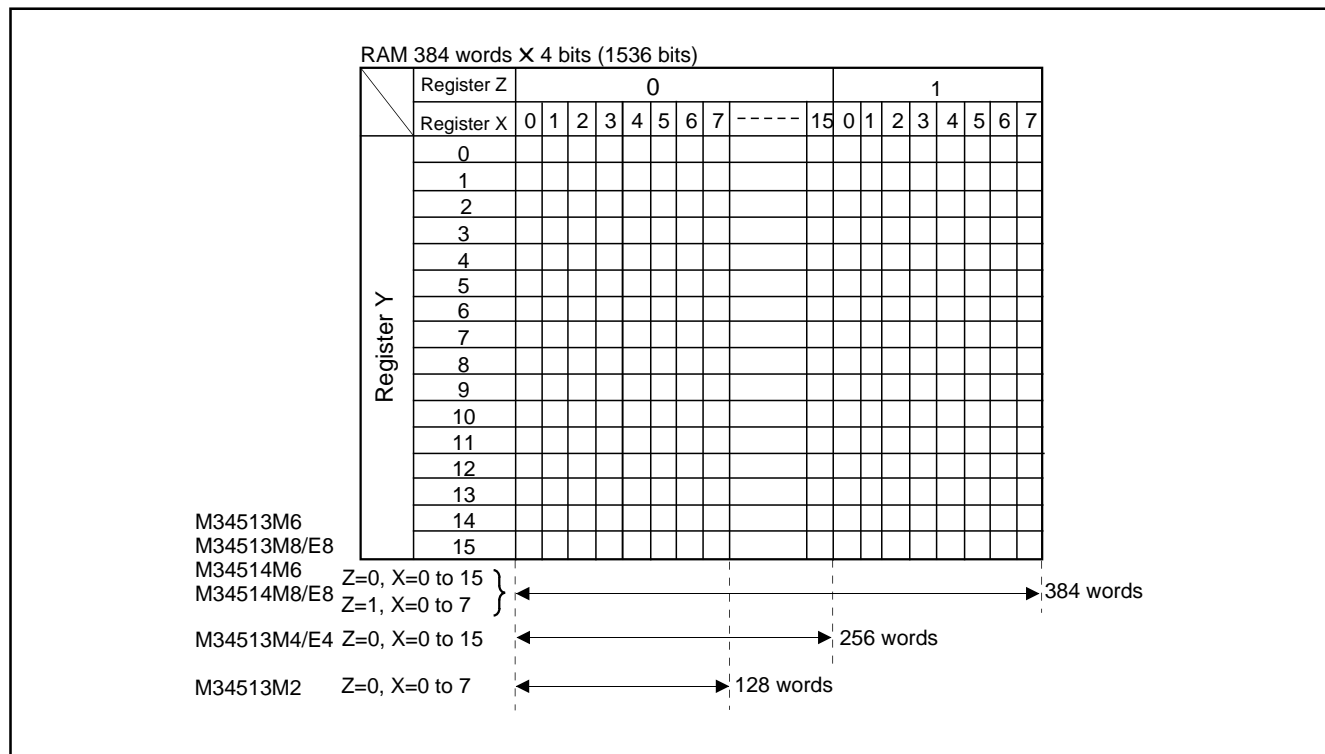


Fig. 12 RAM map

## INTERRUPT FUNCTION

The interrupt type is a vectored interrupt branching to an individual address (interrupt address) according to each interrupt source. An interrupt occurs when the following 3 conditions are satisfied.

- An interrupt activated condition is satisfied (request flag = "1")
- Interrupt enable bit is enabled ("1")
- Interrupt enable flag is enabled (INTE = "1")

Table 3 shows interrupt sources. (Refer to each interrupt request flag for details of activated conditions.)

### (1) Interrupt enable flag (INTE)

The interrupt enable flag (INTE) controls whether the every interrupt enable/disable. Interrupts are enabled when INTE flag is set to "1" with the EI instruction and disabled when INTE flag is cleared to "0" with the DI instruction. When any interrupt occurs, the INTE flag is automatically cleared to "0," so that other interrupts are disabled until the EI instruction is executed.

### (2) Interrupt enable bit

Use an interrupt enable bit of interrupt control registers V1 and V2 to select the corresponding interrupt or skip instruction.

Table 4 shows the interrupt request flag, interrupt enable bit and skip instruction.

Table 5 shows the interrupt enable bit function.

### (3) Interrupt request flag

When the activated condition for each interrupt is satisfied, the corresponding interrupt request flag is set to "1." Each interrupt request flag is cleared to "0" when either;

- an interrupt occurs, or
- the next instruction is skipped with a skip instruction.

Each interrupt request flag is set when the activated condition is satisfied even if the interrupt is disabled by the INTE flag or its interrupt enable bit. Once set, the interrupt request flag retains set until a clear condition is satisfied.

Accordingly, an interrupt occurs when the interrupt disable state is released while the interrupt request flag is set.

If more than one interrupt request flag is set when the interrupt disable state is released, the interrupt priority level is as follows shown in Table 3.

Table 3 Interrupt sources

| Priority level | Interrupt name       | Activated condition               | Interrupt address   |
|----------------|----------------------|-----------------------------------|---------------------|
| 1              | External 0 interrupt | Level change of INT0 pin          | Address 0 in page 1 |
| 2              | External 1 interrupt | Level change of INT1 pin          | Address 2 in page 1 |
| 3              | Timer 1 interrupt    | Timer 1 underflow                 | Address 4 in page 1 |
| 4              | Timer 2 interrupt    | Timer 2 underflow                 | Address 6 in page 1 |
| 5              | Timer 3 interrupt    | Timer 3 underflow                 | Address 8 in page 1 |
| 6              | Timer 4 interrupt    | Timer 4 underflow                 | Address A in page 1 |
| 7              | A-D interrupt        | Completion of A-D conversion      | Address C in page 1 |
| 8              | Serial I/O interrupt | Completion of serial I/O transfer | Address E in page 1 |

Table 4 Interrupt request flag, interrupt enable bit and skip instruction

| Interrupt name       | Request flag | Skip instruction | Enable bit |
|----------------------|--------------|------------------|------------|
| External 0 interrupt | EXF0         | SNZ0             | V10        |
| External 1 interrupt | EXF1         | SNZ1             | V11        |
| Timer 1 interrupt    | T1F          | SNZT1            | V12        |
| Timer 2 interrupt    | T2F          | SNZT2            | V13        |
| Timer 3 interrupt    | T3F          | SNZT3            | V20        |
| Timer 4 interrupt    | T4F          | SNZT4            | V21        |
| A-D interrupt        | ADF          | SNZAD            | V22        |
| Serial I/O interrupt | SIOF         | SNZSI            | V23        |

Table 5 Interrupt enable bit function

| Interrupt enable bit | Occurrence of interrupt | Skip instruction |
|----------------------|-------------------------|------------------|
| 1                    | Enabled                 | Invalid          |
| 0                    | Disabled                | Valid            |

#### (4) Internal state during an interrupt

The internal state of the microcomputer during an interrupt is as follows (Figure 14).

- Program counter (PC)  
An interrupt address is set in program counter. The address to be executed when returning to the main routine is automatically stored in the stack register (SK).
- Interrupt enable flag (INTE)  
INTE flag is cleared to "0" so that interrupts are disabled.
- Interrupt request flag  
Only the request flag for the current interrupt source is cleared to "0."
- Data pointer, carry flag, skip flag, registers A and B  
The contents of these registers and flags are stored automatically in the interrupt stack register (SDP).

#### (5) Interrupt processing

When an interrupt occurs, a program at an interrupt address is executed after branching a data store sequence to stack register. Write the branch instruction to an interrupt service routine at an interrupt address.

Use the RTI instruction to return from an interrupt service routine. Interrupt enabled by executing the EI instruction is performed after executing 1 instruction (just after the next instruction is executed). Accordingly, when the EI instruction is executed just before the RTI instruction, interrupts are enabled after returning the main routine. (Refer to Figure 13)

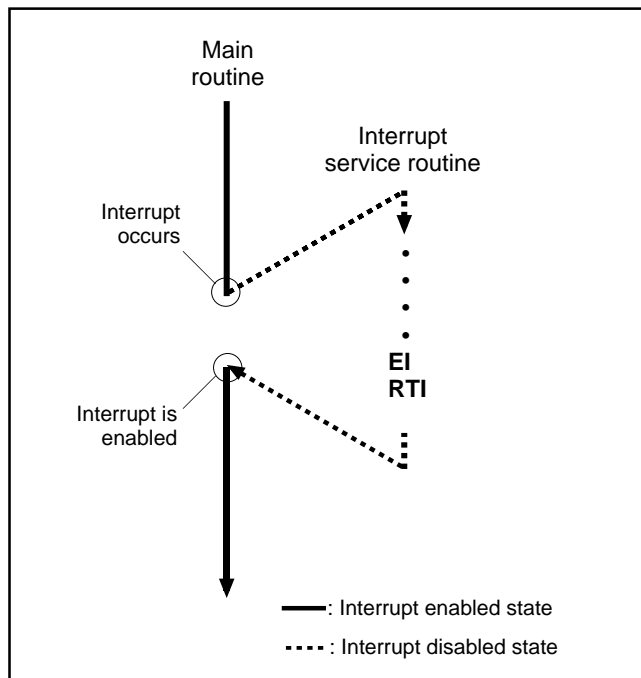


Fig. 13 Program example of interrupt processing

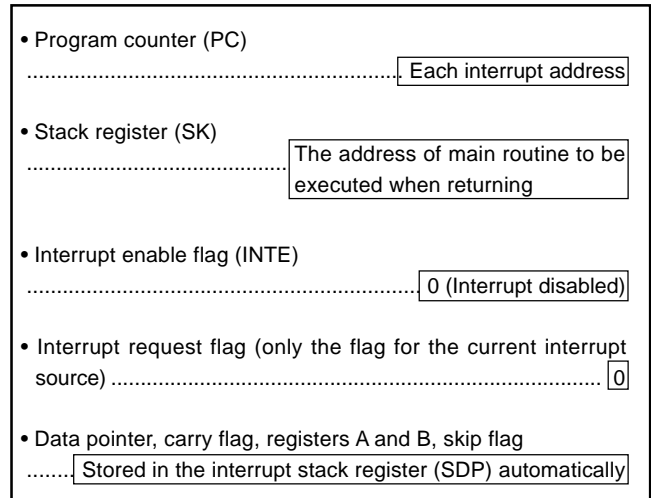


Fig. 14 Internal state when interrupt occurs

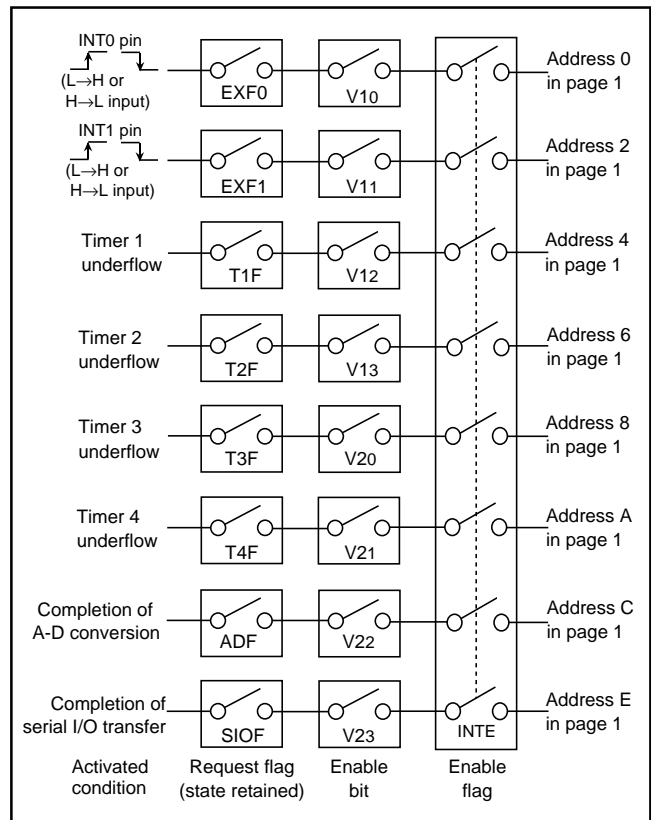


Fig. 15 Interrupt system diagram



## (6) Interrupt control registers

- Interrupt control register V1

Interrupt enable bits of external 0, external 1, timer 1 and timer 2 are assigned to register V1. Set the contents of this register through register A with the TV1A instruction. The TAV1 instruction can be used to transfer the contents of register V1 to register A.

- Interrupt control register V2

Interrupt enable bits of timer 3, timer 4, A-D and serial I/O are assigned to register V2. Set the contents of this register through register A with the TV2A instruction. The TAV2 instruction can be used to transfer the contents of register V2 to register A.

**Table 6 Interrupt control registers**

| Interrupt control register V1 |                                 | at reset : 00002 |  | at RAM back-up : 00002 | R/W |
|-------------------------------|---------------------------------|------------------|--|------------------------|-----|
| V13                           | Timer 2 interrupt enable bit    | 0                | Interrupt disabled (SNZT2 instruction is valid)  |                        |     |
|                               |                                 | 1                | Interrupt enabled (SNZT2 instruction is invalid) |                        |     |
| V12                           | Timer 1 interrupt enable bit    | 0                | Interrupt disabled (SNZT1 instruction is valid)  |                        |     |
|                               |                                 | 1                | Interrupt enabled (SNZT1 instruction is invalid) |                        |     |
| V11                           | External 1 interrupt enable bit | 0                | Interrupt disabled (SNZ1 instruction is valid)   |                        |     |
|                               |                                 | 1                | Interrupt enabled (SNZ1 instruction is invalid)  |                        |     |
| V10                           | External 0 interrupt enable bit | 0                | Interrupt disabled (SNZ0 instruction is valid)   |                        |     |
|                               |                                 | 1                | Interrupt enabled (SNZ0 instruction is invalid)  |                        |     |
| Interrupt control register V2 |                                 | at reset : 00002 |  | at RAM back-up : 00002 | R/W |
| V23                           | Serial I/O interrupt enable bit | 0                | Interrupt disabled (SNZSI instruction is valid)  |                        |     |
|                               |                                 | 1                | Interrupt enabled (SNZSI instruction is invalid) |                        |     |
| V22                           | A-D interrupt enable bit        | 0                | Interrupt disabled (SNZAD instruction is valid)  |                        |     |
|                               |                                 | 1                | Interrupt enabled (SNZAD instruction is invalid) |                        |     |
| V21                           | Timer 4 interrupt enable bit    | 0                | Interrupt disabled (SNZT4 instruction is valid)  |                        |     |
|                               |                                 | 1                | Interrupt enabled (SNZT4 instruction is invalid) |                        |     |
| V20                           | Timer 3 interrupt enable bit    | 0                | Interrupt disabled (SNZT3 instruction is valid)  |                        |     |
|                               |                                 | 1                | Interrupt enabled (SNZT3 instruction is invalid) |                        |     |

Note: "R" represents read enabled, and "W" represents write enabled.

## (7) Interrupt sequence

Interrupts only occur when the respective INTE flag, interrupt enable bits (V10–V13 and V20–V23), and interrupt request flag are “1.” The interrupt actually occurs 2 to 3 machine cycles after the cycle in which all three conditions are satisfied. The interrupt oc-

curs after 3 machine cycles only when the three interrupt conditions are satisfied on execution of other than one-cycle instructions (Refer to Figure 16).

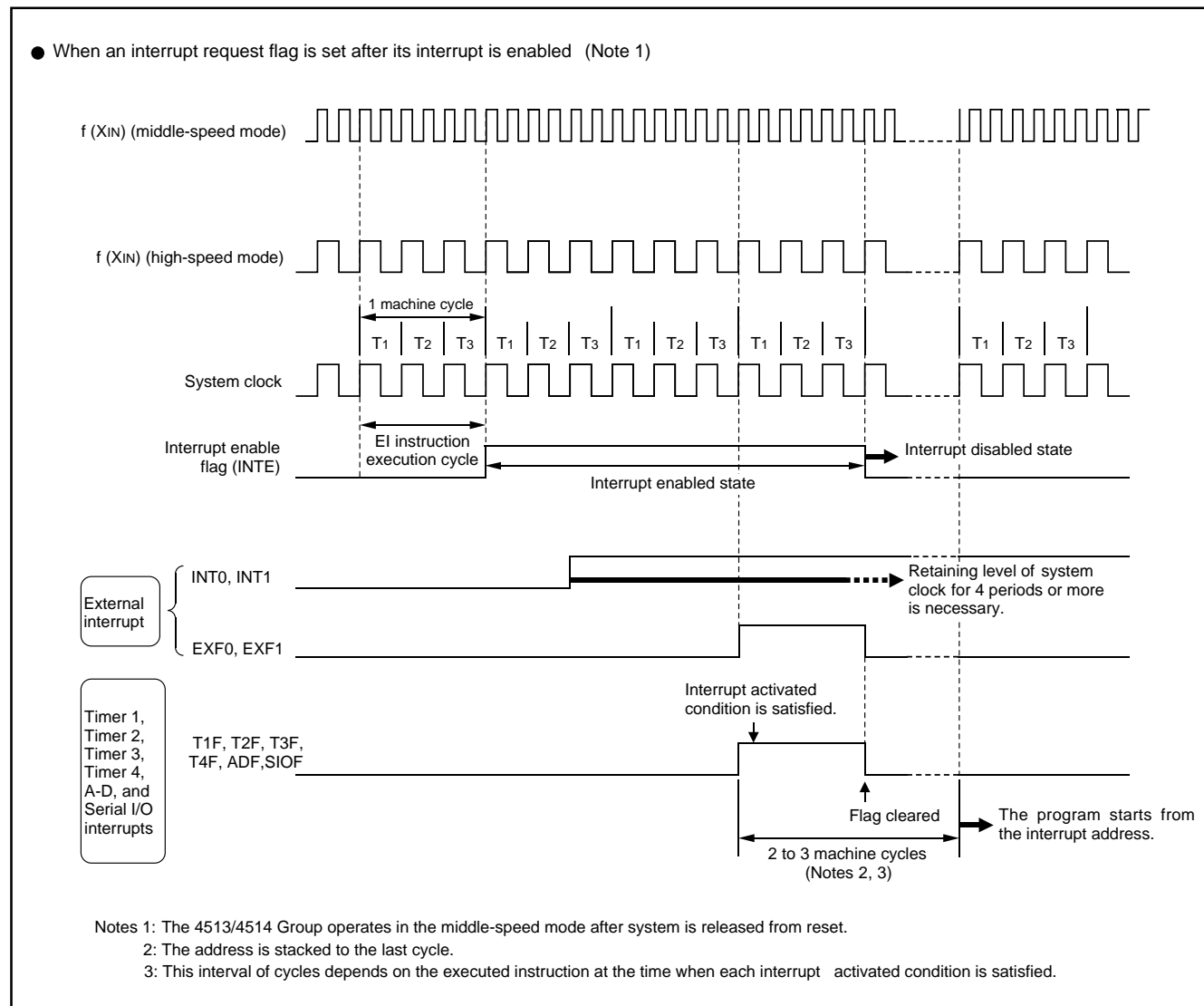


Fig. 16 Interrupt sequence

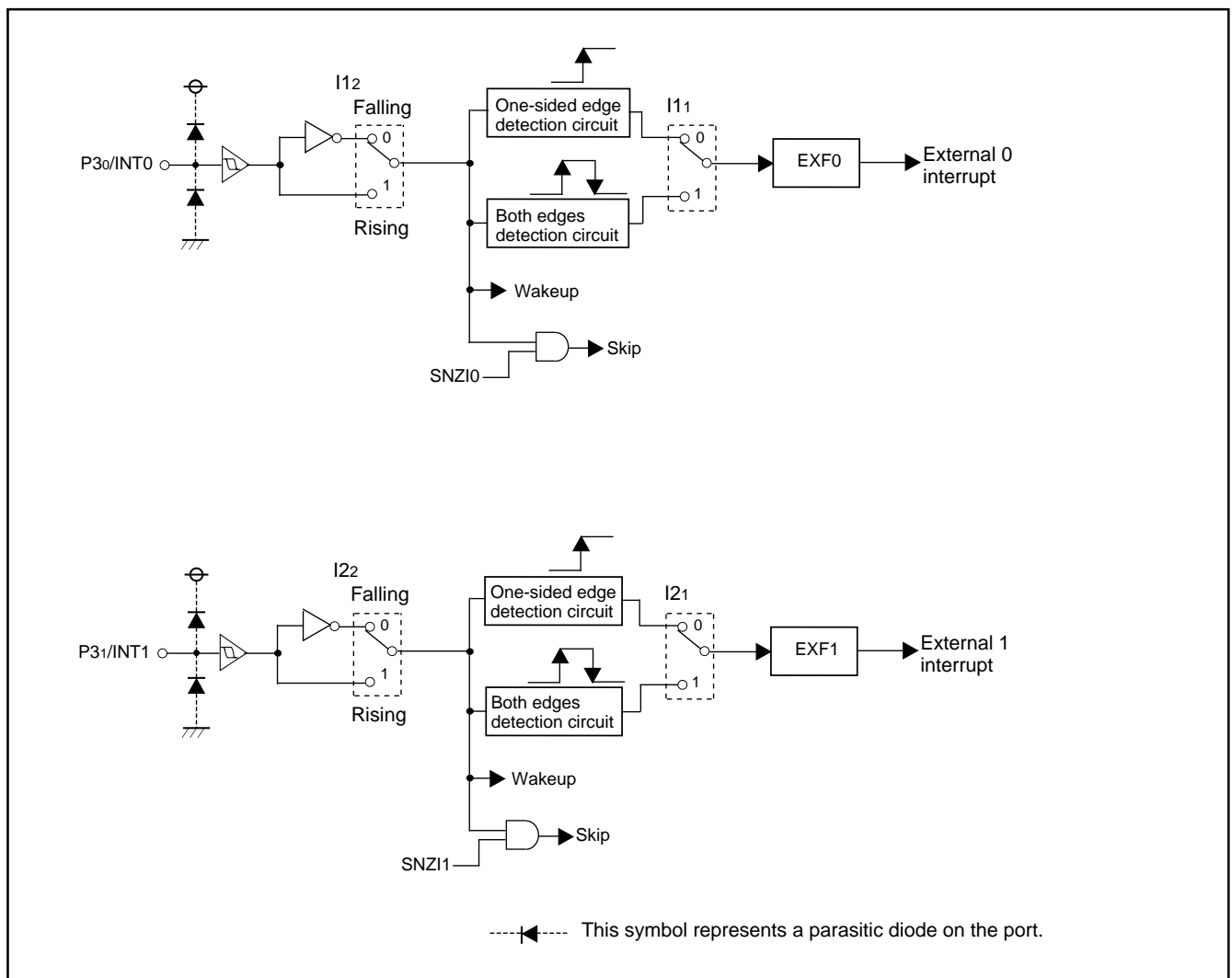
## EXTERNAL INTERRUPTS

The 4513/4514 Group has two external interrupts (external 0 and external 1). An external interrupt request occurs when a valid waveform is input to an interrupt input pin (edge detection).

The external interrupts can be controlled with the interrupt control registers I1 and I2.

**Table 7 External interrupt activated conditions**

| Name                 | Input pin | Activated condition  | Valid waveform selection bit |
|----------------------|-----------|--|------------------------------|
| External 0 interrupt | P30/INT0  | When the next waveform is input to P30/INT0 pin <ul style="list-style-type: none"> <li>Falling waveform ("H"→"L")</li> <li>Rising waveform ("L"→"H")</li> <li>Both rising and falling waveforms</li> </ul> | I11<br>I12                   |
| External 1 interrupt | P31/INT1  | When the next waveform is input to P31/INT1 pin <ul style="list-style-type: none"> <li>Falling waveform ("H"→"L")</li> <li>Rising waveform ("L"→"H")</li> <li>Both rising and falling waveforms</li> </ul> | I21<br>I22                   |



**Fig. 17 External interrupt circuit structure**

### **(1) External 0 interrupt request flag (EXF0)**

External 0 interrupt request flag (EXF0) is set to "1" when a valid waveform is input to P30/INT0 pin.

The valid waveforms causing the interrupt must be retained at their level for 4 clock cycles or more of the system clock (Refer to Figure 16).

The state of EXF0 flag can be examined with the skip instruction (SNZ0). Use the interrupt control register V1 to select the interrupt or the skip instruction. The EXF0 flag is cleared to "0" when an interrupt occurs or when the next instruction is skipped with the skip instruction.

The P30/INT0 pin need not be selected the external interrupt input INT0 function or the normal I/O port P30 function. However, the EXF0 flag is set to "1" when a valid waveform is input even if it is used as an I/O port P30.

**• External 0 interrupt activated condition**

External 0 interrupt activated condition is satisfied when a valid waveform is input to P30/INT0 pin.

The valid waveform can be selected from rising waveform, falling waveform or both rising and falling waveforms. An example of how to use the external 0 interrupt is as follows.

- ① Select the valid waveform with the bits 1 and 2 of register I1.
- ② Clear the EXF0 flag to "0" with the SNZ0 instruction.
- ③ Set the NOP instruction for the case when a skip is performed with the SNZ0 instruction.
- ④ Set both the external 0 interrupt enable bit (V10) and the INTE flag to "1."

The external 0 interrupt is now enabled. Now when a valid waveform is input to the P30/INT0 pin, the EXF0 flag is set to "1" and the external 0 interrupt occurs.

### **(2) External 1 interrupt request flag (EXF1)**

External 1 interrupt request flag (EXF1) is set to "1" when a valid waveform is input to P31/INT1 pin.

The valid waveforms causing the interrupt must be retained at their level for 4 clock cycles or more of the system clock (Refer to Figure 16).

The state of EXF1 flag can be examined with the skip instruction (SNZ1). Use the interrupt control register V1 to select the interrupt or the skip instruction. The EXF1 flag is cleared to "0" when an interrupt occurs or when the next instruction is skipped with the skip instruction.

The P31/INT1 pin need not be selected the external interrupt input INT1 function or the normal I/O port P31 function. However, the EXF1 flag is set to "1" when a valid waveform is input even if it is used as an I/O port P31.

**• External 1 interrupt activated condition**

External 1 interrupt activated condition is satisfied when a valid waveform is input to P31/INT1 pin.

The valid waveform can be selected from rising waveform, falling waveform or both rising and falling waveforms. An example of how to use the external 1 interrupt is as follows.

- ① Select the valid waveform with the bits 1 and 2 of register I2.
- ② Clear the EXF1 flag to "0" with the SNZ1 instruction.
- ③ Set the NOP instruction for the case when a skip is performed with the SNZ1 instruction.
- ④ Set both the external 1 interrupt enable bit (V11) and the INTE flag to "1."

The external 1 interrupt is now enabled. Now when a valid waveform is input to the P31/INT1 pin, the EXF1 flag is set to "1" and the external 1 interrupt occurs.

### (3) External interrupt control registers

• Interrupt control register I1

Register I1 controls the valid waveform for the external 0 interrupt. Set the contents of this register through register A with the TI1A instruction. The TAI1 instruction can be used to transfer the contents of register I1 to register A.

• Interrupt control register I2

Register I2 controls the valid waveform for the external 1 interrupt. Set the contents of this register through register A with the TI2A instruction. The TAI2 instruction can be used to transfer the contents of register I2 to register A.

Table 8 External interrupt control registers

| Interrupt control register I1 |   | at reset : 00002 |   | at RAM back-up : state retained | R/W |
|-------------------------------|---|------------------|---|---------------------------------|-----|
| I13                           | Not used  | 0                | This bit has no function, but read/write is enabled.  |                                 |     |
|                               |   | 1                |   |                                 |     |
| I12                           | Interrupt valid waveform for INT0 pin/<br>return level selection bit (Note 2) | 0                | Falling waveform ("L" level of INT0 pin is recognized with the SNZI0 instruction)/"L" level |                                 |     |
|                               |   | 1                | Rising waveform ("H" level of INT0 pin is recognized with the SNZI0 instruction)/"H" level  |                                 |     |
| I11                           | INT0 pin edge detection circuit control bit                                   | 0                | One-sided edge detected   |                                 |     |
|                               |   | 1                | Both edges detected   |                                 |     |
| I10                           | INT0 pin<br>timer 1 control enable bit  | 0                | Disabled  |                                 |     |
|                               |   | 1                | Enabled   |                                 |     |
| Interrupt control register I2 |   | at reset : 00002 |   | at RAM back-up : state retained | R/W |
| I23                           | Not used  | 0                | This bit has no function, but read/write is enabled.  |                                 |     |
|                               |   | 1                |   |                                 |     |
| I22                           | Interrupt valid waveform for INT1 pin/<br>return level selection bit (Note 3) | 0                | Falling waveform ("L" level of INT1 pin is recognized with the SNZI1 instruction)/"L" level |                                 |     |
|                               |   | 1                | Rising waveform ("H" level of INT1 pin is recognized with the SNZI1 instruction)/"H" level  |                                 |     |
| I21                           | INT1 pin edge detection circuit control bit                                   | 0                | One-sided edge detected   |                                 |     |
|                               |   | 1                | Both edges detected   |                                 |     |
| I20                           | INT1 pin<br>timer 3 control enable bit  | 0                | Disabled  |                                 |     |
|                               |   | 1                | Enabled   |                                 |     |

Notes 1: "R" represents read enabled, and "W" represents write enabled.

2: When the contents of I12 is changed, the external interrupt request flag EXF0 may be set. Accordingly, clear EXF0 flag with the SNZ0 instruction.

3: When the contents of I22 is changed, the external interrupt request flag EXF1 may be set. Accordingly, clear EXF1 flag with the SNZ1 instruction.

## TIMERS

The 4513/4514 Group has the programmable timers.

- Programmable timer

The programmable timer has a reload register and enables the frequency dividing ratio to be set. It is decremented from a setting value  $n$ . When it underflows (count to  $n + 1$ ), a timer interrupt request flag is set to "1," new data is loaded from the reload register, and count continues (auto-reload function).

- Fixed dividing frequency timer

The fixed dividing frequency timer has the fixed frequency dividing ratio ( $n$ ). An interrupt request flag is set to "1" after every  $n$  count of a count pulse.

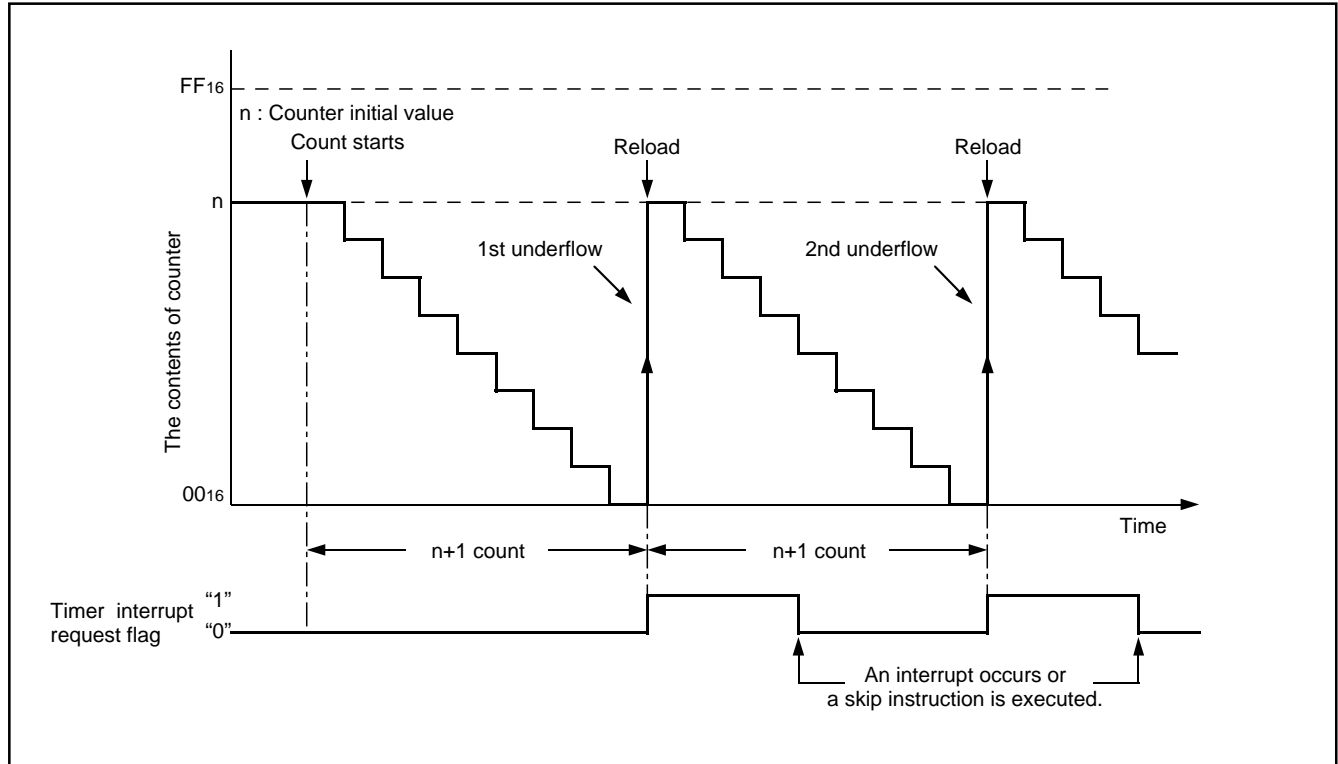


Fig. 18 Auto-reload function

The 4513/4514 Group timer consists of the following circuits.

- Prescaler : frequency divider
- Timer 1 : 8-bit programmable timer
- Timer 2 : 8-bit programmable timer
- Timer 3 : 8-bit programmable timer
- Timer 4 : 8-bit programmable timer
- (Timers 1 to 4 have the interrupt function, respectively)
- 16-bit timer

Prescaler and timers 1 to 4 can be controlled with the timer control registers W1 to W6. The 16-bit timer is a free counter which is not controlled with the control register.

Each function is described below.

**Table 9 Function related timers**

| Circuit      | Structure   | Count source   | Frequency dividing ratio | Use of output signal  | Control register |
|--------------|---|--|--------------------------|---|------------------|
| Prescaler    | Frequency divider   | • Instruction clock  | 4, 16                    | • Timer 1, 2, 3 and 4 count sources   | W1               |
| Timer 1      | 8-bit programmable binary down counter (link to P30/INT0 input) | • Prescaler output (ORCLK)   | 1 to 256                 | • Timer 2 count source<br>• CNTR0 output<br>• Timer 1 interrupt                                     | W1<br>W6         |
| Timer 2      | 8-bit programmable binary down counter                          | • Timer 1 underflow<br>• Prescaler output (ORCLK)<br>• CNTR0 input<br>• 16-bit timer underflow | 1 to 256                 | • Timer 3 count source<br>• Timer 2 interrupt<br>• CNTR0 output                                     | W2<br>W6         |
| Timer 3      | 8-bit programmable binary down counter (link to P31/INT1 input) | • Timer 2 underflow<br>• Prescaler output (ORCLK)  | 1 to 256                 | • Timer 4 count source<br>• Timer 3 interrupt<br>• CNTR1 output                                     | W3<br>W6         |
| Timer 4      | 8-bit programmable binary down counter                          | • Timer 3 underflow<br>• Prescaler output (ORCLK)<br>• CNTR1 input                             | 1 to 256                 | • Timer 4 interrupt<br>• CNTR1 output   | W4<br>W6         |
| 16-bit timer | 16-bit fixed dividing frequency                                 | • Instruction clock  | 65536                    | • Watchdog timer (The 15th bit is counted twice)<br>• Timer 2 count source (16-bit timer underflow) |                  |

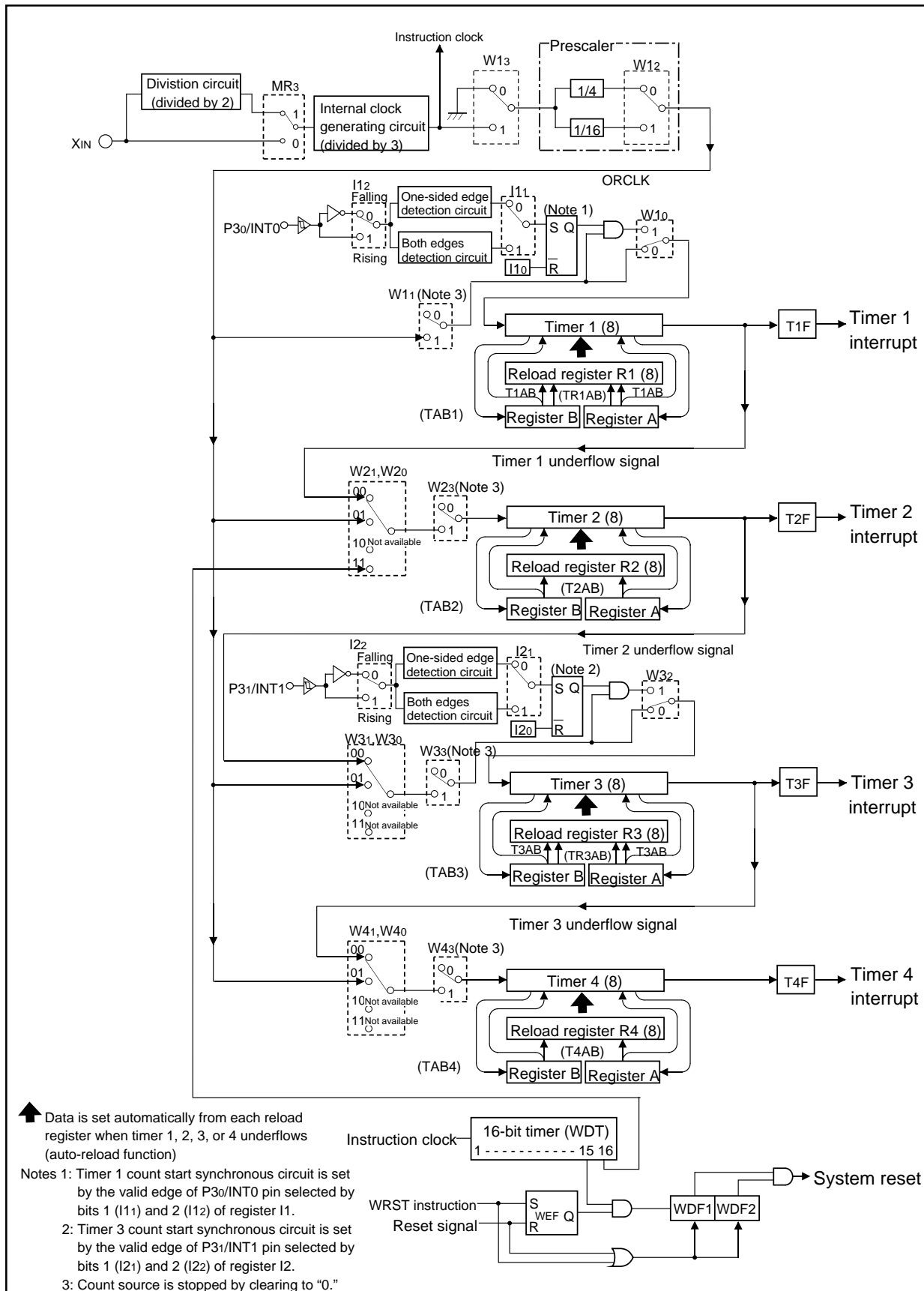


Fig. 19 Timers structure



Table 10 Timer control registers

| Timer control register W1 |   | at reset : 00002 |   | at RAM back-up : 00002              |  | R/W |
|---------------------------|---|------------------|---|-------------------------------------|--|-----|
| W13                       | Prescaler control bit                               | 0                | Stop (state initialized)                                      |                                     |  |     |
|                           |   | 1                | Operating   |                                     |  |     |
| W12                       | Prescaler dividing ratio selection bit              | 0                | Instruction clock divided by 4                                |                                     |  |     |
|                           |   | 1                | Instruction clock divided by 16                               |                                     |  |     |
| W11                       | Timer 1 control bit                                 | 0                | Stop (state retained)   |                                     |  |     |
|                           |   | 1                | Operating   |                                     |  |     |
| W10                       | Timer 1 count start synchronous circuit control bit | 0                | Count start synchronous circuit not selected                  |                                     |  |     |
|                           |   | 1                | Count start synchronous circuit selected                      |                                     |  |     |
| Timer control register W2 |   | at reset : 00002 |   | at RAM back-up : state retained     |  | R/W |
| W23                       | Timer 2 control bit                                 | 0                | Stop (state retained)   |                                     |  |     |
|                           |   | 1                | Operating   |                                     |  |     |
| W22                       | Not used  | 0                | This bit has no function, but read/write is enabled.          |                                     |  |     |
|                           |   | 1                |   |                                     |  |     |
| W21                       | Timer 2 count source selection bits                 | W21              | W20   | Count source                        |  |     |
|                           |   | 0                | 0   | Timer 1 underflow signal            |  |     |
| 0                         |   | 1                | Prescaler output  |                                     |  |     |
| W20                       |   | 1                | 0   | CNTR0 input                         |  |     |
|                           |   | 1                | 1   | 16 bit timer (WDT) underflow signal |  |     |
|                           |   |                  |   |                                     |  |     |
| Timer control register W3 |   | at reset : 00002 |   | at RAM back-up : state retained     |  | R/W |
| W33                       | Timer 3 control bit                                 | 0                | Stop (state retained)   |                                     |  |     |
|                           |   | 1                | Operating   |                                     |  |     |
| W32                       | Timer 3 count start synchronous circuit control bit | 0                | Count start synchronous circuit not selected                  |                                     |  |     |
|                           |   | 1                | Count start synchronous circuit selected                      |                                     |  |     |
| W31                       | Timer 3 count source selection bits                 | W31              | W30   | Count source                        |  |     |
|                           |   | 0                | 0   | Timer 2 underflow signal            |  |     |
| 0                         |   | 1                | Prescaler output  |                                     |  |     |
| W30                       |   | 1                | 0   | Not available                       |  |     |
|                           |   | 1                | 1   | Not available                       |  |     |
|                           |   |                  |   |                                     |  |     |
| Timer control register W4 |   | at reset : 00002 |   | at RAM back-up : state retained     |  | R/W |
| W43                       | Timer 4 control bit                                 | 0                | Stop (state retained)   |                                     |  |     |
|                           |   | 1                | Operating   |                                     |  |     |
| W42                       | Not used  | 0                | This bit has no function, but read/write is enabled.          |                                     |  |     |
|                           |   | 1                |   |                                     |  |     |
| W41                       | Timer 4 count source selection bits                 | W41              | W40   | Count source                        |  |     |
|                           |   | 0                | 0   | Timer 3 underflow signal            |  |     |
| 0                         |   | 1                | Prescaler output  |                                     |  |     |
| W40                       |   | 1                | 0   | CNTR1 input                         |  |     |
|                           |   | 1                | 1   | Not available                       |  |     |
|                           |   |                  |   |                                     |  |     |
| Timer control register W6 |   | at reset : 00002 |   | at RAM back-up : state retained     |  | R/W |
| W63                       | CNTR1 output control bit                            | 0                | Timer 3 underflow signal output divided by 2                  |                                     |  |     |
|                           |   | 1                | CNTR1 output control by timer 4 underflow signal divided by 2 |                                     |  |     |
| W62                       | D7/CNTR1 function selection bit                     | 0                | D7(I/O)/CNTR1 input   |                                     |  |     |
|                           |   | 1                | CNTR1 (I/O)/D7(input)   |                                     |  |     |
| W61                       | CNTR0 output control bit                            | 0                | Timer 1 underflow signal output divided by 2                  |                                     |  |     |
|                           |   | 1                | CNTR0 output control by timer 2 underflow signal divided by 2 |                                     |  |     |
| W60                       | D6/CNTR0 output control bit                         | 0                | D6(I/O)/CNTR0 input   |                                     |  |     |
|                           |   | 1                | CNTR0 (I/O)/D6(input)   |                                     |  |     |

Note: "R" represents read enabled, and "W" represents write enabled.

## (1) Timer control registers

- Timer control register W1  
Register W1 controls the count operation of timer 1, the selection of count start synchronous circuit, and the frequency dividing ratio and count operation of prescaler. Set the contents of this register through register A with the TW1A instruction. The TAW1 instruction can be used to transfer the contents of register W1 to register A.
- Timer control register W2  
Register W2 controls the count operation and count source of timer 2. Set the contents of this register through register A with the TW2A instruction. The TAW2 instruction can be used to transfer the contents of register W2 to register A.
- Timer control register W3  
Register W3 controls the count operation and count source of timer 3 and the selection of count start synchronous circuit. Set the contents of this register through register A with the TW3A instruction. The TAW3 instruction can be used to transfer the contents of register W3 to register A.
- Timer control register W4  
Register W4 controls the count operation and count source of timer 4. Set the contents of this register through register A with the TW4A instruction. The TAW4 instruction can be used to transfer the contents of register W4 to register A.
- Timer control register W6  
Register W6 controls the D6/CNTR0 pin and D7/CNTR1 functions, the selection and operation of the CNTR0 and CNTR1 output. Set the contents of this register through register A with the TW6A instruction. The TAW6 instruction can be used to transfer the contents of register W6 to register A.

## (2) Precautions

Note the following for the use of timers.

- Prescaler  
Stop the prescaler operation to change its frequency dividing ratio.
- Count source  
Stop timer 1, 2, 3, or 4 counting to change its count source.
- Reading the count value  
Stop timer 1, 2, 3, or 4 counting and then execute the TAB1, TAB2, TAB3, or TAB4 instruction to read its data.
- Writing to reload registers R1 and R3  
When writing data to reload registers R1 or R3 while timer 1 or timer 3 is operating, avoid a timing when timer 1 or timer 3 underflows.

## (3) Prescaler

Prescaler is a frequency divider. Its frequency dividing ratio can be selected. The count source of prescaler is the instruction clock. Use the bit 2 of register W1 to select the prescaler dividing ratio and the bit 3 to start and stop its operation. Prescaler is initialized, and the output signal (ORCLK) stops when the bit 3 of register W1 is cleared to "0."

## (4) Timer 1 (interrupt function)

Timer 1 is an 8-bit binary down counter with the timer 1 reload register (R1). Data can be set simultaneously in timer 1 and the reload register (R1) with the T1AB instruction. Data can be written to reload register (R1) with the TR1AB instruction.

When writing data to reload register R1 with the TR1AB instruction, the downcount after the underflow is started from the setting value of reload register R1.

Timer 1 starts counting after the following process;

- ① set data in timer 1, and
- ② set the bit 1 of register W1 to "1."

However, P30/INT0 pin input can be used as the start trigger for timer 1 count operation by setting the bit 0 of register W1 to "1."

When a value set in timer 1 is n, timer 1 divides the count source signal by  $n + 1$  ( $n = 0$  to 255).

Once count is started, when timer 1 underflows (the next count pulse is input after the contents of timer 1 becomes "0"), the timer 1 interrupt request flag (T1F) is set to "1," new data is loaded from reload register R1, and count continues (auto-reload function).

Data can be read from timer 1 with the TAB1 instruction. When reading the data, stop the counter and then execute the TAB1 instruction. Timer 1 underflow signal divided by 2 can be output from D6/CNTR0 pin.

## (5) Timer 2 (interrupt function)

Timer 2 is an 8-bit binary down counter with the timer 2 reload register (R2). Data can be set simultaneously in timer 2 and the reload register (R2) with the T2AB instruction.

Timer 2 starts counting after the following process;

- ① set data in timer 2,
- ② select the count source with the bits 0 and 1 of register W2, and
- ③ set the bit 3 of register W2 to "1."

When a value set in timer 2 is n, timer 2 divides the count source signal by  $n + 1$  ( $n = 0$  to 255).

Once count is started, when timer 2 underflows (the next count pulse is input after the contents of timer 2 becomes "0"), the timer 2 interrupt request flag (T2F) is set to "1," new data is loaded from reload register R2, and count continues (auto-reload function).

Data can be read from timer 2 with the TAB2 instruction. When reading the data, stop the counter and then execute the TAB2 instruction. The output from D6/CNTR0 pin by timer 2 underflow signal divided by 2 can be controlled.

## (6) Timer 3 (interrupt function)

Timer 3 is an 8-bit binary down counter with the timer 3 reload register (R3). Data can be set simultaneously in timer 3 and the reload register (R3) with the T3AB instruction. Data can be written to reload register (R3) with the TR3AB instruction.

When writing data to reload register R3 with the TR3AB instruction, the downcount after the underflow is started from the setting value of reload register R3.

Timer 3 starts counting after the following process;

- ① set data in timer 3,
- ② select the count source with the bits 0 and 1 of register W3, and
- ③ set the bit 3 of register W3 to "1."

However, P31/INT1 pin input can be used as the start trigger for timer 3 count operation by setting the bit 2 of register W3 to "1."

When a value set in timer 3 is  $n$ , timer 3 divides the count source signal by  $n + 1$  ( $n = 0$  to 255).

Once count is started, when timer 3 underflows (the next count pulse is input after the contents of timer 3 becomes "0"), the timer 3 interrupt request flag (T3F) is set to "1," new data is loaded from reload register R3, and count continues (auto-reload function).

Data can be read from timer 3 with the TAB3 instruction. When reading the data, stop the counter and then execute the TAB3 instruction. Timer 3 underflow signal divided by 2 can be output from D7/CNTR1 pin.

## (7) Timer 4 (interrupt function)

Timer 4 is an 8-bit binary down counter with the timer 4 reload register (R4). Data can be set simultaneously in timer 4 and the reload register (R4) with the T4AB instruction.

Timer 4 starts counting after the following process;

- ① set data in timer 4,
- ② select the count source with the bits 0 and 1 of register W4, and
- ③ set the bit 3 of register W4 to "1."

When a value set in timer 4 is  $n$ , timer 4 divides the count source signal by  $n + 1$  ( $n = 0$  to 255).

Once count is started, when timer 4 underflows (the next count pulse is input after the contents of timer 4 becomes "0"), the timer 4 interrupt request flag (T4F) is set to "1," new data is loaded from reload register R4, and count continues (auto-reload function).

Data can be read from timer 4 with the TAB4 instruction. When reading the data, stop the counter and then execute the TAB4 instruction. The output from D7/CNTR1 pin by timer 4 underflow signal divided by 2 can be controlled.

## (8) Timer interrupt request flags (T1F, T2F, T3F, and T4F)

Each timer interrupt request flag is set to "1" when each timer underflows. The state of these flags can be examined with the skip instructions (SNZT1, SNZT2, SNZT3, and SNZT4).

Use the interrupt control registers V1, V2 to select an interrupt or a skip instruction.

An interrupt request flag is cleared to "0" when an interrupt occurs or when the next instruction is skipped with a skip instruction.

## (9) Timer I/O pin (D6/CNTR0, D7/CNTR1)

D6/CNTR0 pin has functions to input the timer 2 count source, and to output the timer 1 and timer 2 underflow signals divided by 2. D7/CNTR1 pin has functions to input the timer 4 count source, and to output the timer 3 and timer 4 underflow signals divided by 2.

The selection of D6/CNTR0 pin function can be controlled with the bit 0 of register W6. The selection of D7/CNTR1 pin function can be controlled with the bit 2 of register W6.

The following signals can be selected for the CNTR0 output signal with the bit 1 of register W6.

- timer 1 underflow signal divided by 2
- the signal of AND operation between timer 1 underflow signal divided by 2 and timer 2 underflow signal divide by 2

The following signals can be selected for the CNTR1 output signal with the bit 3 of register W6.

- timer 3 underflow signal divided by 2
- the signal of AND operation between timer 3 underflow signal divided by 2 and timer 4 underflow signal divide by 2

Timer 2 counts the rising waveform of CNTR0 input when the CNTR0 input is selected as the count source.

Timer 4 counts the rising waveform of CNTR1 input when the CNTR1 input is selected as the count source.

## (10) Count start synchronous circuit (timer 1 and 3)

Each of timer 1 and timer 3 has the count start synchronous circuit which synchronizes P30/INT0 pin and P31/INT1 pin, respectively, and can start the timer count operation.

Timer 1 count start synchronous circuit function is selected by setting the bit 0 of register W1 to "1." The control by P30/INT0 pin input can be performed by setting the bit 0 of register I1 to "1."

The count start synchronous circuit is set by level change ("H"→"L" or "L"→"H") of P30/INT0 pin input. This valid waveform is selected by bits 1 (I11) and 2 (I12) of register I1 as follows;

- I11 = "0": Synchronized with one-sided edge (falling or rising)
- I11 = "1": Synchronized with both edges (both falling and rising)

When register I11="0" (synchronized with the one-sided edge), the rising or falling waveform can be selected by bit 2 of register I1;

- I12 = "0": Falling waveform
- I12 = "1": Rising waveform

Timer 3 count start synchronous circuit function is selected by setting the bit 2 of register W3 to "1." The control by P31/INT1 pin input can be performed by setting the bit 0 of register I2 to "1."

The count start synchronous circuit is set by level change ("H"→"L" or "L"→"H") of P31/INT1 pin input. This valid waveform is selected by bits 1 (I21) and 2 (I22) of register I2 as follows;

- I21 = "0": Synchronized with one-sided edge (falling or rising)
- I21 = "1": Synchronized with both edges (both falling and rising)

When register I21="0" (synchronized with the one-sided edge), the rising or falling waveform can be selected by bit 2 of register I2;

- I22 = "0": Falling waveform
- I22 = "1": Rising waveform

When timer 1 and timer 3 count start synchronous circuits are used, the count start synchronous circuits are set, the count source is input to each timer by inputting valid waveform to P30/INT0 pin and P31/INT1 pin. Once set, the count start synchronous circuit is cleared by clearing the bit I10 or I20 to "0" or reset.

## WATCHDOG TIMER

Watchdog timer provides a method to reset the system when a program runs wild. Watchdog timer consists of a 16-bit timer (WDT), watchdog timer enable flag (WEF), and watchdog timer flags (WDF1, WDF2).

The timer WDT downcounts the instruction clocks as the count source. The underflow signal is generated when the count value reaches "0000<sub>16</sub>." This underflow signal can be used as the timer 2 count source.

When the WRST instruction is executed after system is released from reset, the WEF flag is set to "1". At this time, the watchdog timer starts operating.

When the count value of timer WDT reaches "BFFF<sub>16</sub>" or "3FFF<sub>16</sub>," the WDF1 flag is set to "1." If the WRST instruction is never executed while timer WDT counts 32767, WDF2 flag is set to "1," and the  $\overline{\text{RESET}}$  pin outputs "L" level to reset the microcomputer. Execute the WRST instruction at each period of 32766 machine cycle or less by software when using watchdog timer to keep the microcomputer operating normally.

To prevent the WDT stopping in the event of misoperation, WEF flag is designed not to initialize once the WRST instruction has been executed. Note also that, if the WRST instruction is never executed, the watchdog timer does not start.

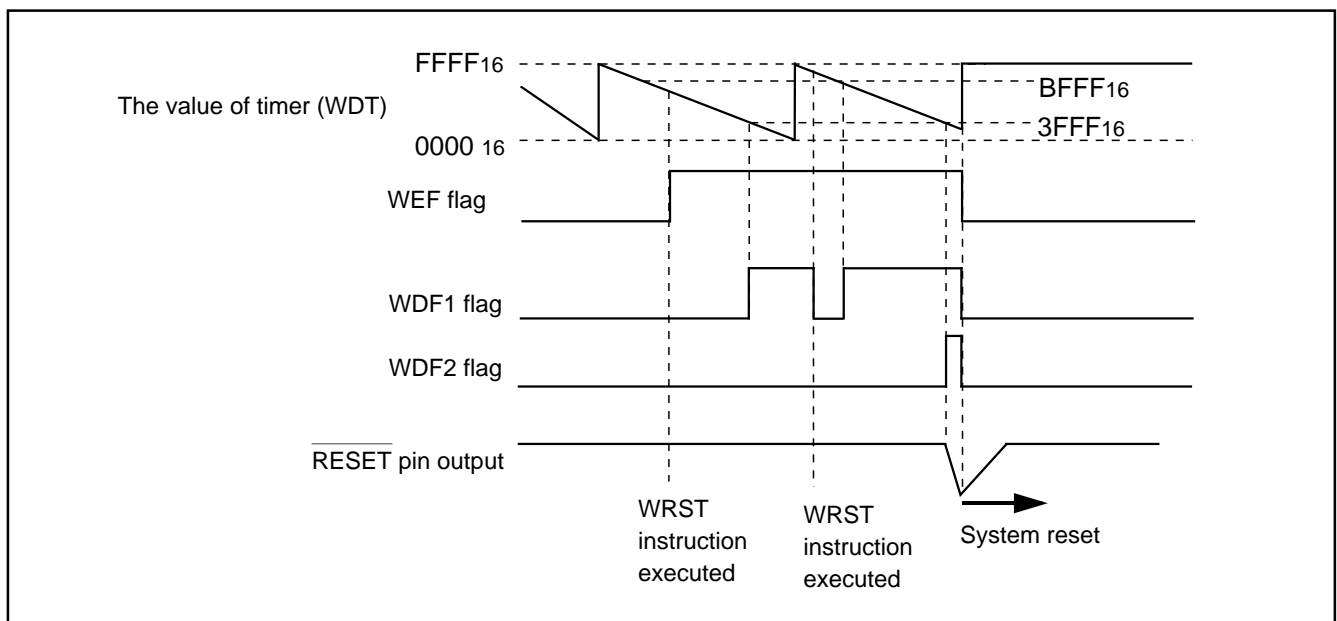


Fig. 20 Watchdog timer function

The contents of WEF, WDF1 and WDF2 flags and timer WDT are initialized at the RAM back-up mode.

If WDF2 flag is set to "1" at the same time that the microcomputer enters the RAM back-up state, system reset may be performed.

When using the watchdog timer and the RAM back-up mode, initialize the WDF1 flag with the WRST instruction just before the microcomputer enters the RAM back-up state (refer to Figure 21)

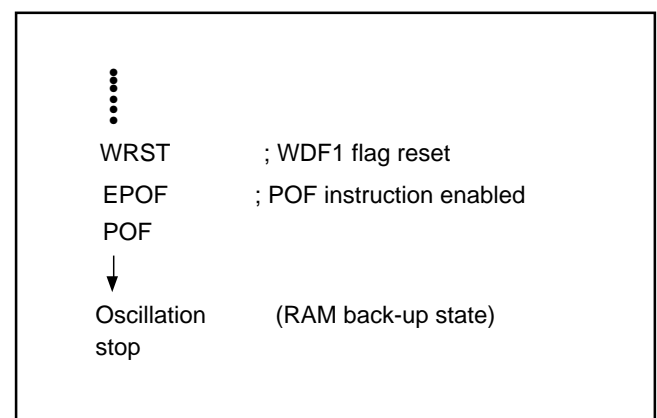


Fig. 21 Program example to enter the RAM back-up mode when using the watchdog timer

## SERIAL I/O

The 4513/4514 Group has a built-in clock synchronous serial I/O which can serially transmit or receive 8-bit data.

Serial I/O consists of;

- serial I/O register SI
- serial I/O mode register J1
- serial I/O transmission/reception completion flag (SIOF)
- serial I/O counter

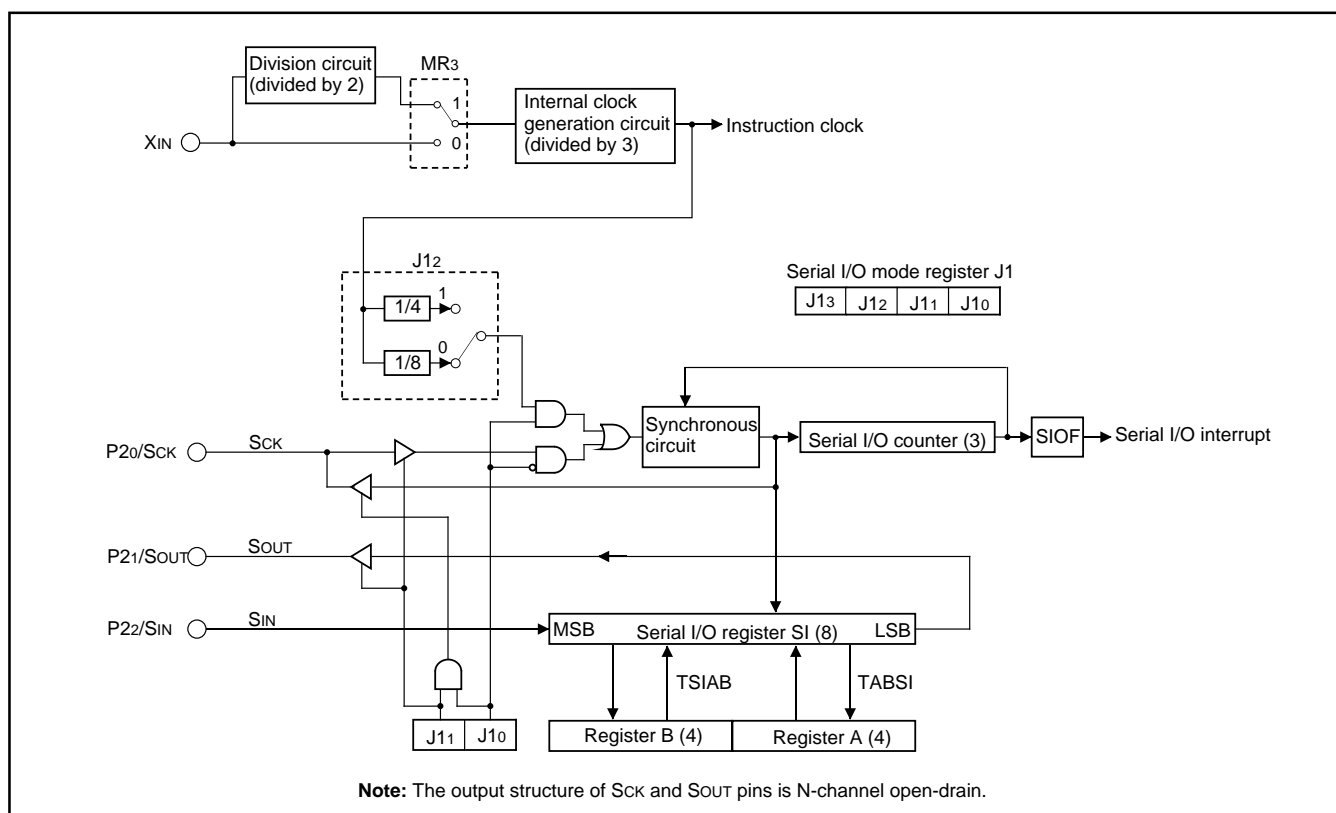
Registers A and B are used to perform data transfer with internal CPU, and the serial I/O pins are used for external data transfer.

The pin functions of the serial I/O pins can be set with the register J1.

**Table 11 Serial I/O pins**

| Pin      | Pin function when selecting serial I/O |
|----------|--|
| P20/SCK  | Clock I/O (SCK)                        |
| P21/SOUT | Serial data output (SOUT)              |
| P22/SIN  | Serial data input (SIN)                |

Note: Input ports P20–P22 can be used regardless of register J1.



**Fig. 22 Serial I/O structure**

**Table 12 Serial I/O mode register**

| Serial I/O mode register J1 |  | at reset : 00002 |  | at RAM back-up : state retained | R/W |
|-----------------------------|--|------------------|--|---------------------------------|-----|
| J13                         | Not used   | 0                | This bit has no function, but read/write is enabled.               |                                 |     |
|                             |  | 1                |  |                                 |     |
| J12                         | Serial I/O internal clock dividing ratio selection bit | 0                | Instruction clock signal divided by 8                              |                                 |     |
|                             |  | 1                | Instruction clock signal divided by 4                              |                                 |     |
| J11                         | Serial I/O port selection bit                          | 0                | Input ports P20, P21, P22 selected                                 |                                 |     |
|                             |  | 1                | Serial I/O ports SCK, SOUT, SIN/input ports P20, P21, P22 selected |                                 |     |
| J10                         | Serial I/O synchronous clock selection bit             | 0                | External clock   |                                 |     |
|                             |  | 1                | Internal clock (instruction clock divided by 4 or 8)               |                                 |     |

Note: "R" represents read enabled, and "W" represents write enabled.

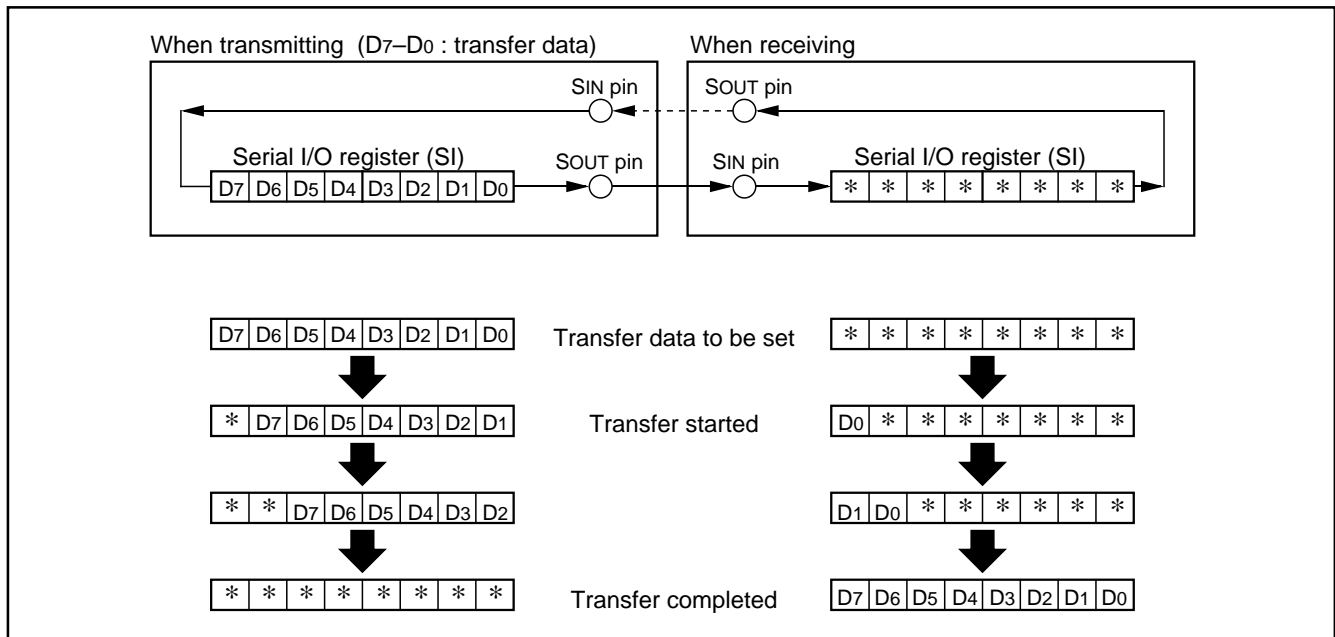


Fig. 23 Serial I/O register state when transferring

**(1) Serial I/O register SI**

Serial I/O register SI is the 8-bit data transfer serial/parallel conversion register. Data can be set to register SI through registers A and B with the TSIAB instruction. The contents of register A is transmitted to the low-order 4 bits of register SI, and the contents of register B is transmitted to the high-order 4 bits of register SI. During transmission, each bit data is transmitted LSB first from the lowermost bit (bit 0) of register SI, and during reception, each bit data is received LSB first to register SI starting from the topmost bit (bit 7).

When register SI is used as a work register without using serial I/O, pull up the Sck pin or set the pin function to an input port P20.

**(2) Serial I/O transmission/reception completion flag (SIOF)**

Serial I/O transmission/reception completion flag (SIOF) is set to "1" when serial data transmission or reception completes. The state of SIOF flag can be examined with the skip instruction (SNZSI). Use the interrupt control register V2 to select the interrupt or the skip instruction.

The SIOF flag is cleared to "0" when the interrupt occurs or when the next instruction is skipped with the skip instruction.

**(3) Serial I/O start instruction (SST)**

When the SST instruction is executed, the SIOF flag is cleared to "0" and then serial I/O transmission/reception is started.

**(4) Serial I/O mode register J1**

Register J1 controls the synchronous clock, P20/Sck, P21/Sout and P22/Sin pin function. Set the contents of this register through register A with the TJ1A instruction. The TAJ1 instruction can be used to transfer the contents of register J1 to register A.

## (5) How to use serial I/O

Figure 24 shows the serial I/O connection example. Serial I/O interrupt is not used in this example. In the actual wiring, pull up the

wiring between each pin with a resistor. Figure 25 shows the data transfer timing and Table 13 shows the data transfer sequence.

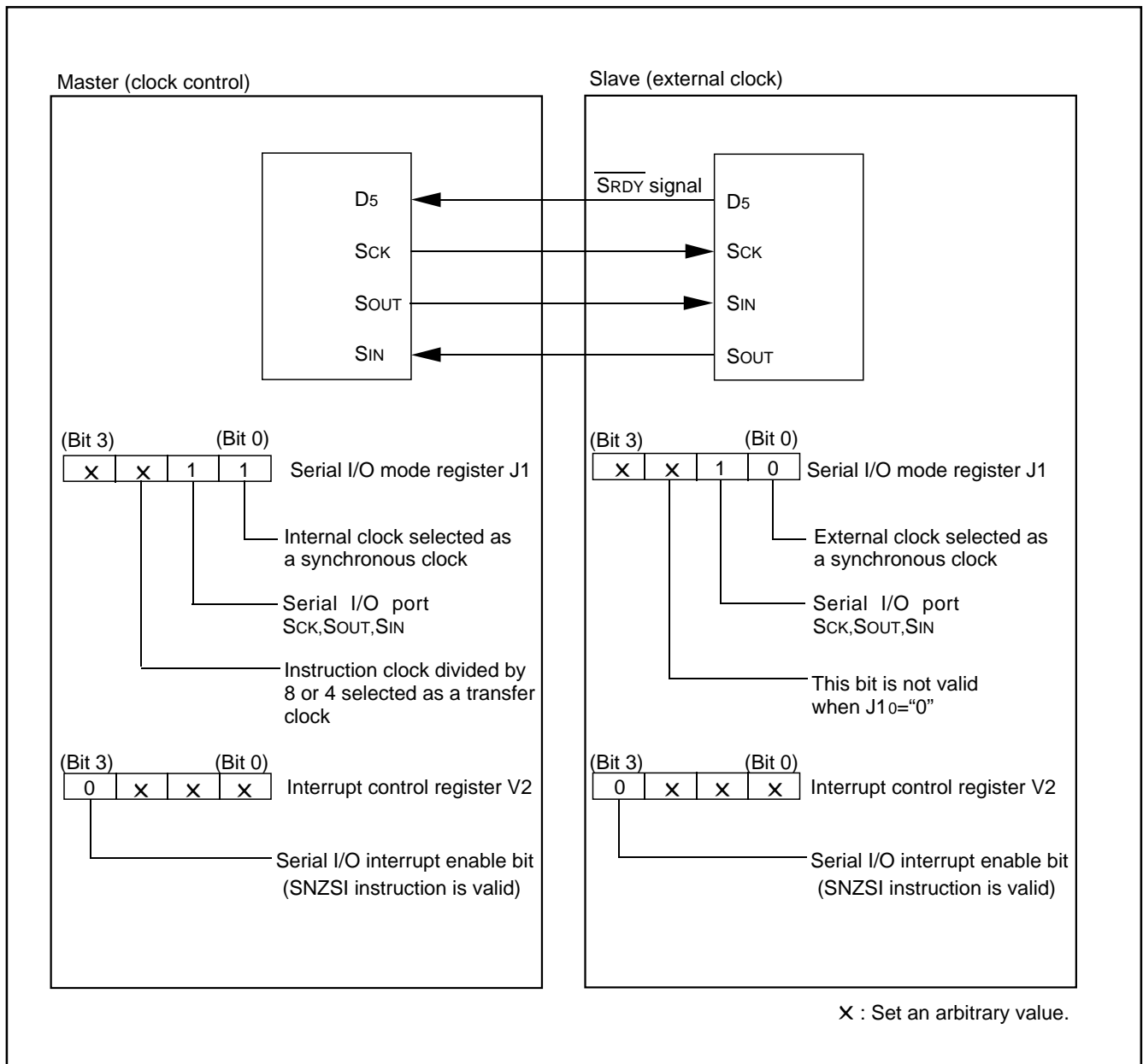


Fig. 24 Serial I/O connection example

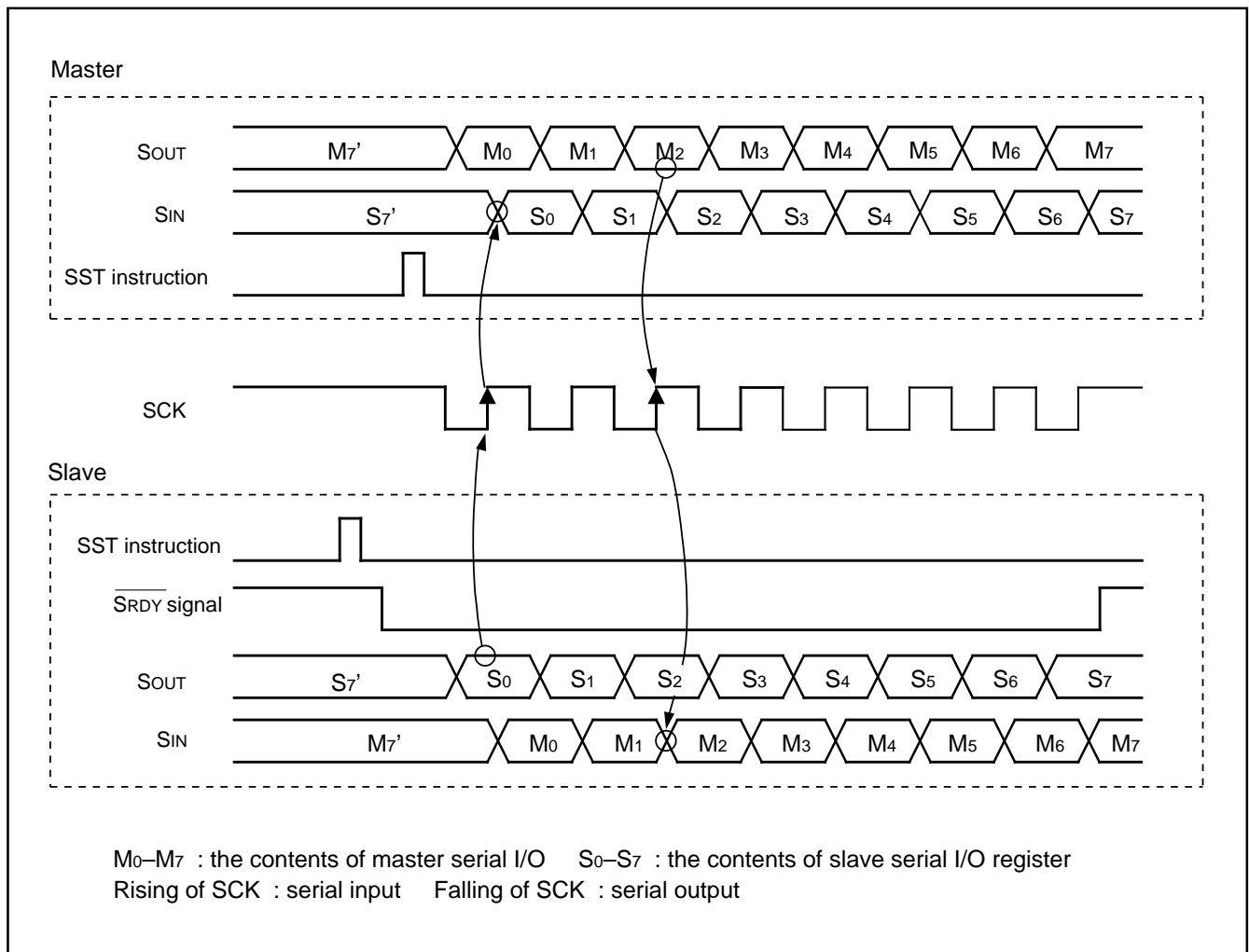


Fig. 25 Timing of serial I/O data transfer



**Table 13 Processing sequence of data transfer from master to slave**

| Master (transmission)  | Slave (reception)   |
|--|---|
| [Initial setting]<br>• Setting the serial I/O mode register J1 and interrupt control register V2 shown in Figure 24.   | [Initial setting]<br>• Setting serial I/O mode register J1, and interrupt control register V2 shown in Figure 24.                                       |
| TJ1A and TV2A instructions   | TJ1A and TV2A instructions  |
| • Setting the port received the reception enable signal (SRDY) to the input mode.<br>(Port D5 is used in this example) | • Setting the port transmitted the reception enable signal (SRDY) and outputting "H" level (reception impossible).<br>(Port D5 is used in this example) |
| SD instruction   | SD instruction  |
| * [Transmission enable state]<br>• Storing transmission data to serial I/O register SI.                                | *[Reception enable state]<br>• The SIOF flag is cleared to "0."   |
| TSIAB instruction  | SST instruction   |
|  | • "L" level (reception possible) is output from port D5.  |
|  | RD instruction  |
| [Transmission]<br>• Check port D5 is "L" level.  | [Reception]<br><br><br><br>• Check reception completes.   |
| SZD instruction  |   |
| • Serial transfer starts.  |   |
| SST instruction  |   |
| • Check transmission completes.  |   |
| SNZSI instruction  | SNZSI instruction   |
| • Wait (timing when continuously transferring)   | • "H" level is output from port D5.   |
|  | SD instruction  |
|  | [Data processing]   |

1-byte data is serially transferred on this process. Subsequently, data can be transferred continuously by repeating the process from \*.

When an external clock is selected as a synchronous clock, the clock is not controlled internally. Control the clock externally because serial transfer is performed as long as clock is externally input. (Unlike an internal clock, an external clock is not stopped when serial transfer is completed.) However, the SIOF flag is set to "1" when the clock is counted 8 times after executing the SST instruction. Be sure to set the initial level of the external clock to "H."

## A-D CONVERTER

The 4513/4514 Group has a built-in A-D conversion circuit that performs conversion by 10-bit successive comparison method. Table 14 shows the characteristics of this A-D converter. This A-D converter can also be used as an 8-bit comparator to compare analog voltages input from the analog input pin with preset values.

Table 14 A-D converter characteristics

| Parameter         | Characteristics  |
|-------------------|--|
| Conversion format | Successive comparison method   |
| Resolution        | 10 bits  |
| Relative accuracy | Linearity error: $\pm 2\text{LSB}$<br>Non-linearity error: $\pm 0.9\text{LSB}$ |
| Conversion speed  | 46.5 $\mu\text{s}$ (High-speed mode at 4.0 MHz oscillation frequency)          |
| Analog input pin  | 4 for 4513 Group<br>8 for 4514 Group   |

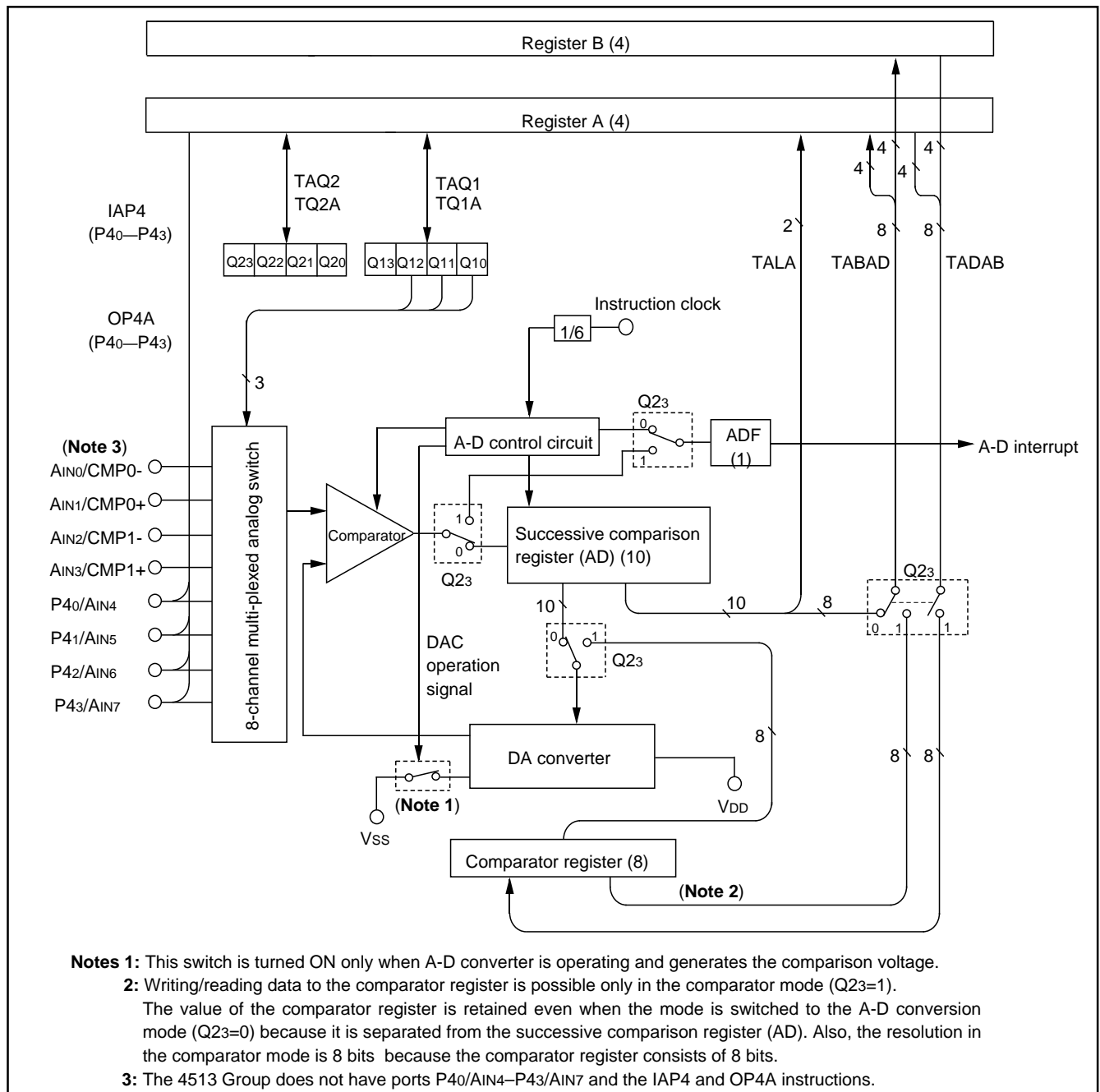


Fig. 26 A-D conversion circuit structure

Table 15 A-D control registers

| A-D control register Q1 |  | at reset : 00002 |   | at RAM back-up : state retained | R/W                                     |
|-------------------------|--|------------------|---|---------------------------------|---|
| Q13                     | Not used   | 0                | This bit has no function, but read/write is enabled.        |                                 |   |
|                         |  | 1                |   |                                 |   |
| Q12                     | Analog input pin selection bits (Note 2)                                       | Q12              | Q11   | Q10                             | Selected pins                           |
|                         |  | 0                | 0   | 0                               | AIN0                                    |
|                         |  | 0                | 0   | 1                               | AIN1                                    |
|                         |  | 0                | 1   | 0                               | AIN2                                    |
| Q11                     |  | 0                | 1   | 1                               | AIN3                                    |
|                         |  | 1                | 0   | 0                               | AIN4 (Not available for the 4513 Group) |
|                         |  | 1                | 0   | 1                               | AIN5 (Not available for the 4513 Group) |
| Q10                     |  | 1                | 1   | 0                               | AIN6 (Not available for the 4513 Group) |
|                         |  | 1                | 1   | 1                               | AIN7 (Not available for the 4513 Group) |
| A-D control register Q2 |  | at reset : 00002 |   | at RAM back-up : state retained | R/W                                     |
| Q23                     | A-D operation mode selection bit   | 0                | A-D conversion mode   |                                 |   |
|                         |  | 1                | Comparator mode   |                                 |   |
| Q22                     | P43/AIN7 and P42/AIN6 pin function selection bit (Not used for the 4513 Group) | 0                | P43, P42 (read/write enabled for the 4513 Group)            |                                 |   |
|                         |  | 1                | AIN7, AIN6/P43, P42 (read/write enabled for the 4513 Group) |                                 |   |
| Q21                     | P41/AIN5 pin function selection bit (Not used for the 4513 Group)              | 0                | P41 (read/write enabled for the 4513 Group)                 |                                 |   |
|                         |  | 1                | AIN5/P41 (read/write enabled for the 4513 Group)            |                                 |   |
| Q20                     | P40/AIN4 pin function selection bit (Not used for the 4513 Group)              | 0                | P40 (read/write enabled for the 4513 Group)                 |                                 |   |
|                         |  | 1                | AIN4/P40 (read/write enabled for the 4513 Group)            |                                 |   |

Notes 1: "R" represents read enabled, and "W" represents write enabled.

2: Select AIN4–AIN7 with register Q1 after setting register Q2.

### (1) Operating at A-D conversion mode

The A-D conversion mode is set by setting the bit 3 of register Q2 to "0."

### (2) Successive comparison register AD

Register AD stores the A-D conversion result of an analog input in 10-bit digital data format. The contents of the high-order 8 bits of this register can be stored in register B and register A with the TABAD instruction. The contents of the low-order 2 bits of this register can be stored into the high-order 2 bits of register A with the TALA instruction. However, do not execute this instruction during A-D conversion.

When the contents of register AD is n, the logic value of the comparison voltage  $V_{ref}$  generated from the built-in DA converter can be obtained with the reference voltage  $V_{DD}$  by the following formula:

Logic value of comparison voltage  $V_{ref}$

$$V_{ref} = \frac{V_{DD}}{1024} \times n$$

n: The value of register AD (n = 0 to 1023)

### (3) A-D conversion completion flag (ADF)

A-D conversion completion flag (ADF) is set to "1" when A-D conversion completes. The state of ADF flag can be examined with the skip instruction (SNZAD). Use the interrupt control register V2 to select the interrupt or the skip instruction.

The ADF flag is cleared to "0" when the interrupt occurs or when the next instruction is skipped with the skip instruction.

### (4) A-D conversion start instruction (ADST)

A-D conversion starts when the ADST instruction is executed. The conversion result is automatically stored in the register AD.

### (5) A-D control register Q1

Register Q1 is used to select one of analog input pins. The 4513 Group does not have AIN4–AIN7. Accordingly, do not select these pins with register Q1.

### (6) A-D control register Q2

Register Q2 is used to select the pin function of P40/AIN4, P41/AIN5, P42/AIN6, and P43/AIN7. The A-D conversion mode is selected when the bit 3 of register Q2 is "0," and the comparator mode is selected when the bit 3 of register Q2 is "1." After set this register, select the analog input with register Q1.

Even when register Q2 is used to set the pins for analog input, P40/AIN4–P43/AIN7 continue to function as P40–P43 I/O. Accordingly, when any of them are used as I/O port P4 and others are used as analog input pins, make sure to set the outputs of pins that are set for analog input to "1." Also, for the port input, the port input function of the pin functions as analog input is undefined.

## (7) Operation description

A-D conversion is started with the A-D conversion start instruction (ADST). The internal operation during A-D conversion is as follows:

- ① When A-D conversion starts, the register AD is cleared to "00016."
- ② Next, the topmost bit of the register AD is set to "1," and the comparison voltage  $V_{ref}$  is compared with the analog input voltage  $V_{IN}$ .
- ③ When the comparison result is  $V_{ref} < V_{IN}$ , the topmost bit of the register AD remains set to "1." When the comparison result is  $V_{ref} > V_{IN}$ , it is cleared to "0."

The 4513/4514 Group repeats this operation to the lowermost bit of the register AD to convert an analog value to a digital value. A-D conversion stops after 62 machine cycles (46.5  $\mu$ s when  $f(X_{IN}) = 4.0$  MHz in high-speed mode) from the start, and the conversion result is stored in the register AD. An A-D interrupt activated condition is satisfied and the ADF flag is set to "1" as soon as A-D conversion completes (Figure 27).

**Table 16 Change of successive comparison register AD during A-D conversion**

| At starting conversion          | Change of successive comparison register AD |    |    |      |    |    |    | Comparison voltage ( $V_{ref}$ ) value                       |  |  |
|---------------------------------|---|----|----|------|----|----|----|--|--|--|
| 1st comparison                  | 1   | 0  | 0  | ---- | 0  | 0  | 0  | $\frac{V_{DD}}{2}$   |  |  |
| 2nd comparison                  | *1  | 1  | 0  | ---- | 0  | 0  | 0  | $\frac{V_{DD}}{2} \pm \frac{V_{DD}}{4}$                      |  |  |
| 3rd comparison                  | *1  | *2 | 1  | ---- | 0  | 0  | 0  | $\frac{V_{DD}}{2} \pm \frac{V_{DD}}{4} \pm \frac{V_{DD}}{8}$ |  |  |
| After 10th comparison completes | A-D conversion result                       |    |    |      |    |    |    | $\frac{V_{DD}}{2} \pm \dots \pm \frac{V_{DD}}{1024}$         |  |  |
|                                 | *1  | *2 | *3 | ---- | *8 | *9 | *A |  |  |  |

\*1: 1st comparison result

\*2: 2nd comparison result

\*3: 3rd comparison result

\*8: 8th comparison result

\*9: 9th comparison result

\*A: 10th comparison result

## (8) A-D conversion timing chart

Figure 27 shows the A-D conversion timing chart.

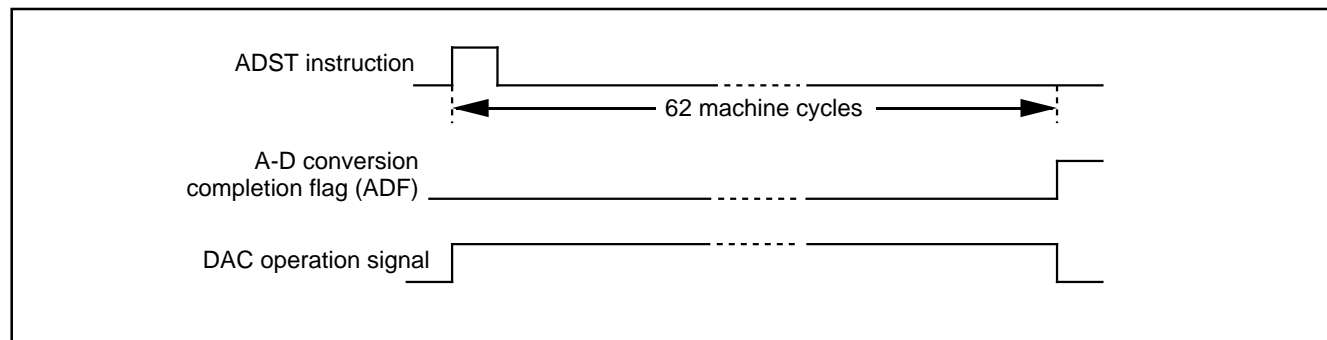


Fig. 27 A-D conversion timing chart

## (9) How to use A-D conversion

How to use A-D conversion is explained using as example in which the analog input from P40/AIN4 pin is A-D converted, and the high-order 4 bits of the converted data are stored in address  $M(Z, X, Y) = (0, 0, 0)$ , the middle-order 4 bits in address  $M(Z, X, Y) = (0, 0, 1)$ , and the low-order 2 bits in address  $M(Z, X, Y) = (0, 0, 2)$  of RAM. The A-D interrupt is not used in this example.

- ① After selecting the AIN4 pin function with the bit 0 of the register Q2, select AIN4 pin and A-D conversion mode with the register Q1 (refer to Figure 28).
- ② Execute the ADST instruction and start A-D conversion.
- ③ Examine the state of ADF flag with the SNZAD instruction to determine the end of A-D conversion.
- ④ Transfer the low-order 2 bits of converted data to the high-order 2 bits of register A (TALA instruction).
- ⑤ Transfer the contents of register A to  $M(Z, X, Y) = (0, 0, 2)$ .
- ⑥ Transfer the high-order 8 bits of converted data to registers A and B (TABAD instruction).
- ⑦ Transfer the contents of register A to  $M(Z, X, Y) = (0, 0, 1)$ .
- ⑧ Transfer the contents of register B to register A, and then, store into  $M(Z, X, Y) = (0, 0, 0)$ .

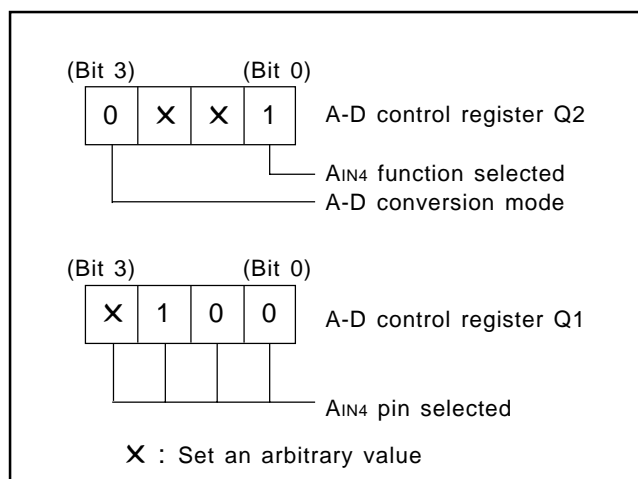


Fig. 28 Setting registers

**(10) Operation at comparator mode**

The A-D converter is set to comparator mode by setting bit 3 of the register Q2 to "1."

Below, the operation at comparator mode is described.

**(11) Comparator register**

In comparator mode, the built-in DA comparator is connected to the comparator register as a register for setting comparison voltages. The contents of register B is stored in the high-order 4 bits of the comparator register and the contents of register A is stored in the low-order 4 bits of the comparator register with the TADAB instruction.

When changing from A-D conversion mode to comparator mode, the result of A-D conversion (register AD) is undefined.

However, because the comparator register is separated from register AD, the value is retained even when changing from comparator mode to A-D conversion mode. Note that the comparator register can be written and read at only comparator mode.

If the value in the comparator register is  $n$ , the logic value of comparison voltage  $V_{ref}$  generated by the built-in DA converter can be determined from the following formula:

Logic value of comparison voltage  $V_{ref}$

$$V_{ref} = \frac{V_{DD}}{256} \times n$$

$n$ : The value of register AD ( $n = 0$  to  $255$ )

**(12) Comparison result store flag (ADF)**

In comparator mode, the ADF flag, which shows completion of A-D conversion, stores the results of comparing the analog input voltage with the comparison voltage. When the analog input voltage is lower than the comparison voltage, the ADF flag is set to "1." The state of ADF flag can be examined with the skip instruction (SNZAD). Use the interrupt control register V2 to select the interrupt or the skip instruction.

The ADF flag is cleared to "0" when the interrupt occurs or when the next instruction is skipped with the skip instruction.

**(13) Comparator operation start instruction (ADST instruction)**

In comparator mode, executing ADST starts the comparator operation.

The comparator stops 8 machine cycles after it has started ( $6 \mu s$  at  $f(X_{IN}) = 4.0 \text{ MHz}$  in high-speed mode). When the analog input voltage is lower than the comparison voltage, the ADF flag is set to "1."

**(14) Notes for the use of A-D conversion 1**

Note the following when using the analog input pins also for I/O port P4 functions:

- Even when P40/AIN4–P43/AIN7 are set to pins for analog input, they continue to function as P40–P43 I/O. Accordingly, when any of them are used as I/O port P4 and others are used as analog input pins, make sure to set the outputs of pins that are set for analog input to "1." Also, the port input function of the pin functions as an analog input is undefined.
- TALA instruction  
When the TALA instruction is executed, the low-order 2 bits of register AD is transferred to the high-order 2 bits of register A, simultaneously, the low-order 2 bits of register A is "0."

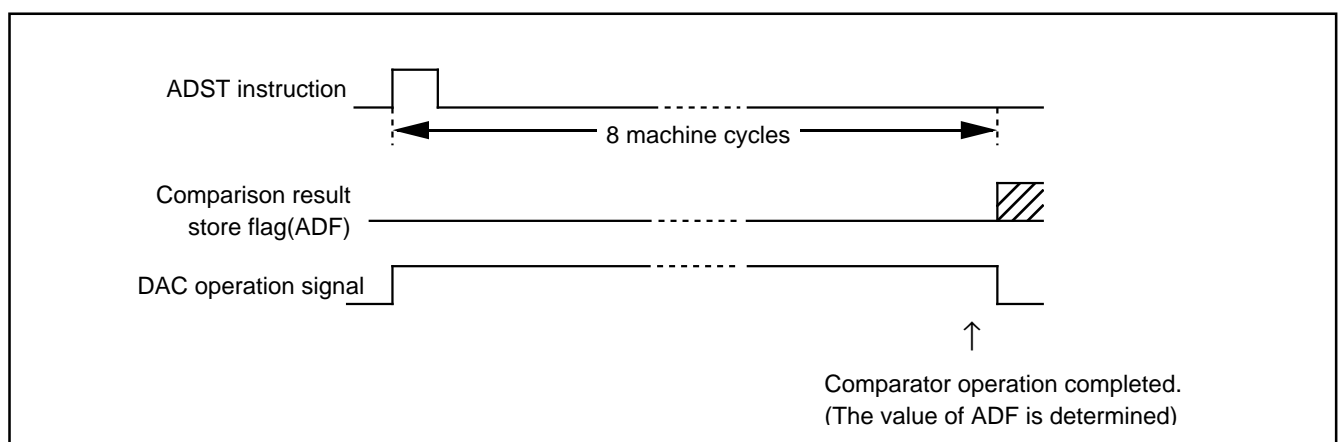


Fig. 29 Comparator operation timing chart

### (15) Notes for the use of A-D conversion 2

Do not change the operating mode (both A-D conversion mode and comparator mode) of A-D converter with bit 3 of register Q2 while A-D converter is operating.

When the operating mode of A-D converter is changed from the comparator mode to A-D conversion mode with the bit 3 of register Q2, note the following;

- Clear bit 2 of register V2 to "0" to change the operating mode of the A-D converter from the comparator mode to A-D conversion mode with the bit 3 of register Q2.
- The A-D conversion completion flag (ADF) may be set when the operating mode of the A-D converter is changed from the comparator mode to the A-D conversion mode. Accordingly, set a value to register Q2, and execute the SNZAD instruction to clear the ADF flag.

### (16) Definition of A-D converter accuracy

The A-D conversion accuracy is defined below (refer to Figure 30).

#### • Relative accuracy

##### ① Zero transition voltage ( $V_{0T}$ )

This means an analog input voltage when the actual A-D conversion output data changes from "0" to "1."

##### ② Full-scale transition voltage ( $V_{FST}$ )

This means an analog input voltage when the actual A-D conversion output data changes from "1023" to "1022."

##### ③ Linearity error

This means a deviation from the line between  $V_{0T}$  and  $V_{FST}$  of a converted value between  $V_{0T}$  and  $V_{FST}$ .

##### ④ Differential non-linearity error

This means a deviation from the input potential difference required to change a converter value between  $V_{0T}$  and  $V_{FST}$  by 1 LSB at the relative accuracy.

#### • Absolute accuracy

This means a deviation from the ideal characteristics between 0 to  $V_{DD}$  of actual A-D conversion characteristics.

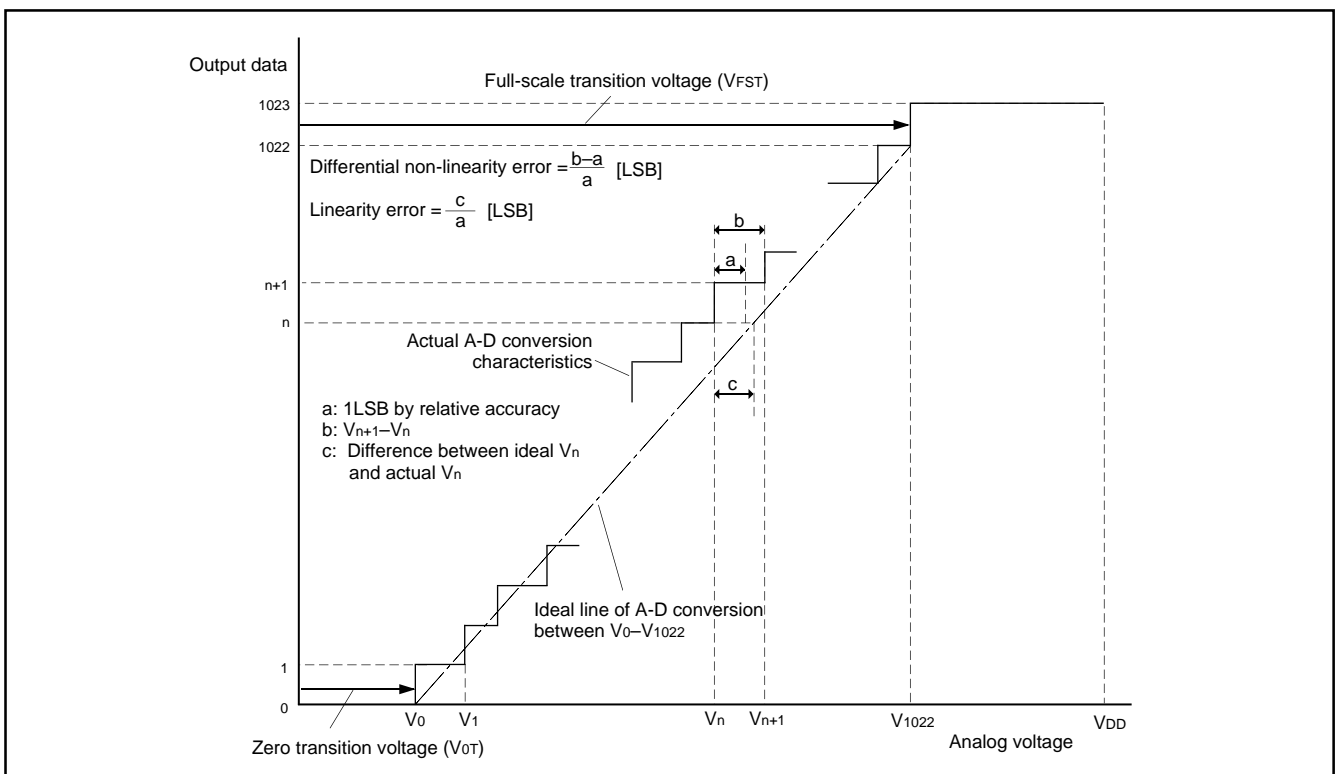


Fig. 30 Definition of A-D conversion accuracy

$V_n$ : Analog input voltage when the output data changes from "n" to "n+1" (n = 0 to 1022)

• 1LSB at relative accuracy  $\rightarrow \frac{V_{FST} - V_{0T}}{1022}$  (V)

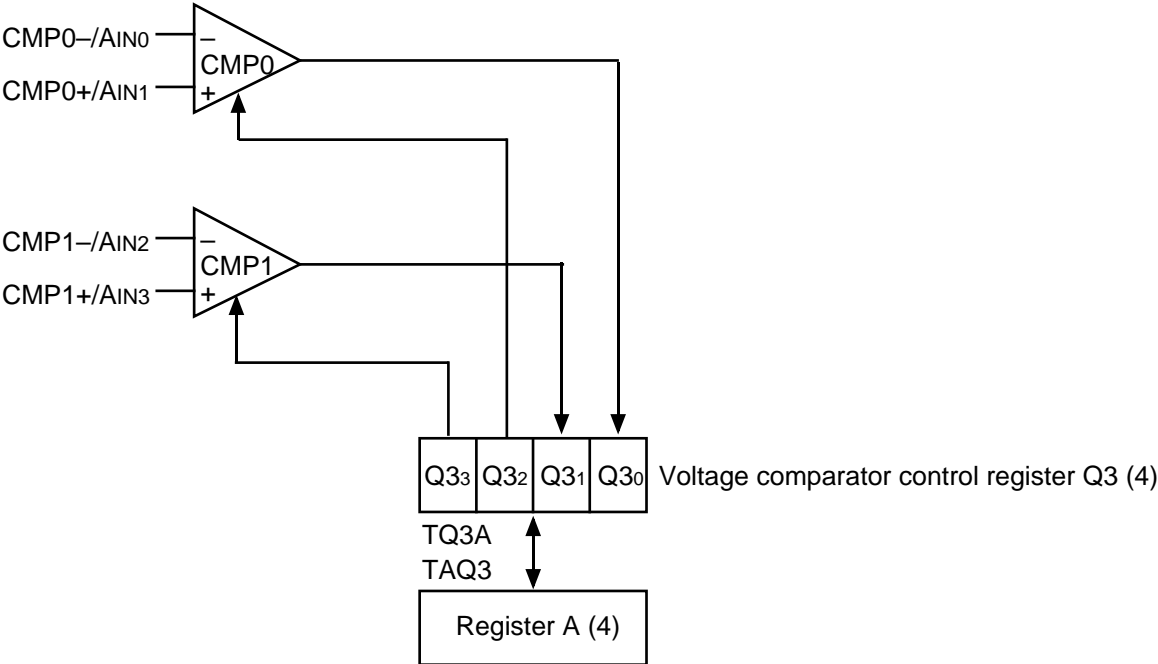
• 1LSB at absolute accuracy  $\rightarrow \frac{V_{DD}}{1024}$  (V)

VOLTAGE COMPARATOR

The 4513/4514 Group has 2 voltage comparator circuits that perform comparison of voltage between 2 pins. Table 17 shows the characteristics of this voltage comparison.

Table 17 Voltage comparator characteristics

| Parameter                   | Characteristics  |
|-----------------------------|--|
| Voltage comparator function | 2 circuits (CMP0, CMP1)  |
| Input pin                   | CMP0-, CMP0+<br>(also used as AIN0, AIN1)<br>CMP1-, CMP1+<br>(also used as AIN2, AIN3) |
| Supply voltage              | 3.0 V to 5.5 V   |
| Input voltage               | 0.3 VDD to 0.7 VDD   |
| Comparison check error      | Typ. 20 mV, Max. 100 mV  |
| Response time               | Max. 20 μs   |



Note: Bits 0 and 1 of register Q3 can be only read.

Fig. 31 Voltage comparator structure



Table 18 Voltage comparator control register Q3

| Voltage comparator control register Q3 (Note 2) |                                       | at reset : 00002 |                                   | at RAM back-up : state retained | R/W |
|---|---------------------------------------|------------------|-----------------------------------|---------------------------------|-----|
| Q33   | Voltage comparator (CMP1) control bit | 0                | Voltage comparator (CMP1) invalid |                                 |     |
|   |                                       | 1                | Voltage comparator (CMP1) valid   |                                 |     |
| Q32   | Voltage comparator (CMP0) control bit | 0                | Voltage comparator (CMP0) invalid |                                 |     |
|   |                                       | 1                | Voltage comparator (CMP0) valid   |                                 |     |
| Q31   | CMP1 comparison result store bit      | 0                | CMP1- > CMP1+                     |                                 |     |
|   |                                       | 1                | CMP1- < CMP1+                     |                                 |     |
| Q30   | CMP0 comparison result store bit      | 0                | CMP0- > CMP0+                     |                                 |     |
|   |                                       | 1                | CMP0- < CMP0+                     |                                 |     |

Notes 1: "R" represents read enabled, and "W" represents write enabled.

2: Bits 0 and 1 of register Q3 can be only read.

### (1) Voltage comparator control register Q3

Register Q3 controls the function of the voltage comparator.

The function of the voltage comparator CMP0 becomes valid by setting bit 2 of register Q3 to "1," and becomes invalid by setting bit 2 of register Q3 to "0." The comparison result of the voltage comparator CMP0 is stored into bit 0 of register Q3.

The function of the voltage comparator CMP1 becomes valid by setting bit 3 of register Q3 to "1," and becomes invalid by setting bit 3 of register Q3 to "0." The comparison result of the voltage comparator CMP1 is stored into bit 1 of register Q3.

### (2) Operation description of voltage comparator

The voltage comparator function becomes valid by setting each control bit of register Q3 to "1" and compares the voltage of the input pin. The comparison result is stored into each comparison result store bit of register Q3.

The comparison result is as follows;

- When CMP0- > CMP0+, Q30 = "0"  
When CMP0- < CMP0+, Q30 = "1"
- When CMP1- > CMP1+, Q31 = "0"  
When CMP1- < CMP1+, Q31 = "1"

### (3) Precautions

When the voltage comparator is used, note the following;

- Voltage comparator function  
When the voltage comparator function is valid with the voltage comparator control register Q3, it is operating even in the RAM back-up mode. Accordingly, be careful about such state because it causes the increase of the operation current in the RAM back-up mode.  
In order to reduce the operation current in the RAM back-up mode, invalidate (bits 2 and 3 of register Q3 = "0") the voltage comparator function by software before the POF instruction is executed.  
Also, while the voltage comparator function is valid, current is always consumed by voltage comparator. On the system required for the low-power dissipation, invalidate the voltage comparator by software when it is unused.
- Register Q3  
Bits 0 and 1 of register Q3 can be only read. Note that they cannot be written.
- Reading the comparison result of voltage comparator  
Read the voltage comparator comparison result from register Q3 after the voltage comparator response time (max. 20  $\mu$ s) is passed from the voltage comparator function becomes valid.

# RESET FUNCTION

System reset is performed by applying "L" level to  $\overline{\text{RESET}}$  pin for 1 machine cycle or more when the following condition is satisfied; the value of supply voltage is the minimum value or more of the recommended operating conditions.  
 Then when "H" level is applied to  $\overline{\text{RESET}}$  pin, software starts from address 0 in page 0.

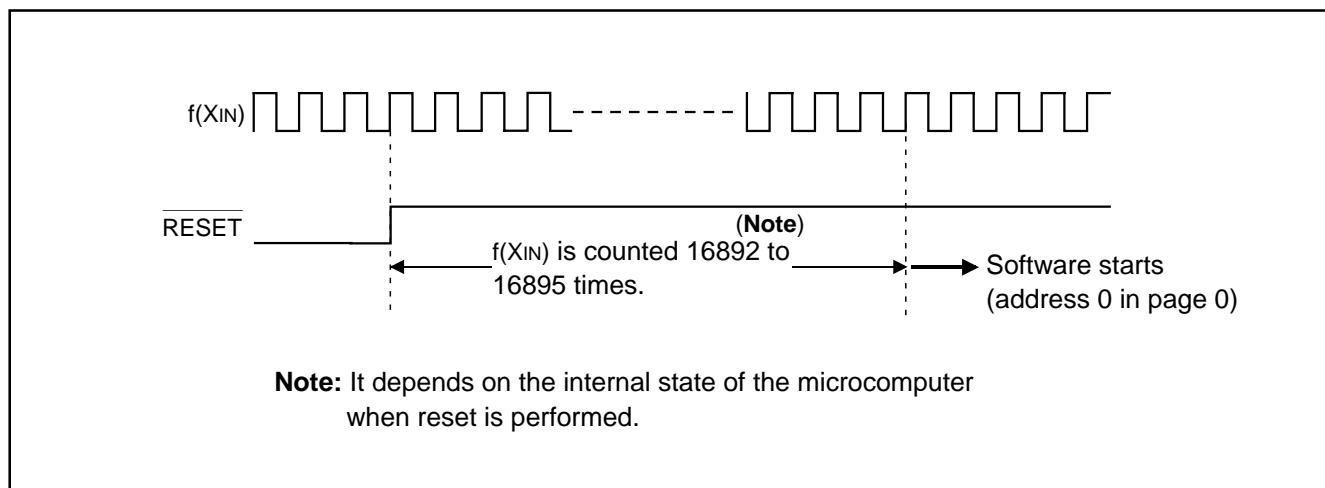


Fig. 32 Reset release timing

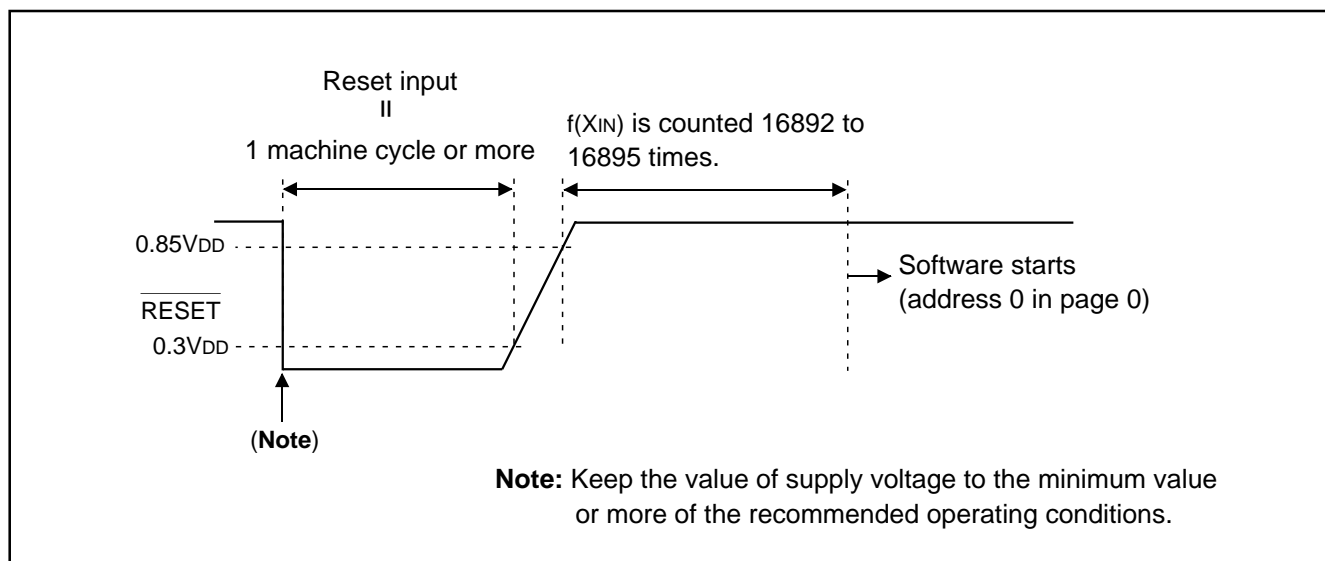


Fig. 33  $\overline{\text{RESET}}$  pin input waveform and reset operation

## (1) Power-on reset

Reset can be performed automatically at power on (power-on reset) by connecting resistors, a diode, and a capacitor to RESET pin. Connect RESET pin and the external circuit at the shortest distance.

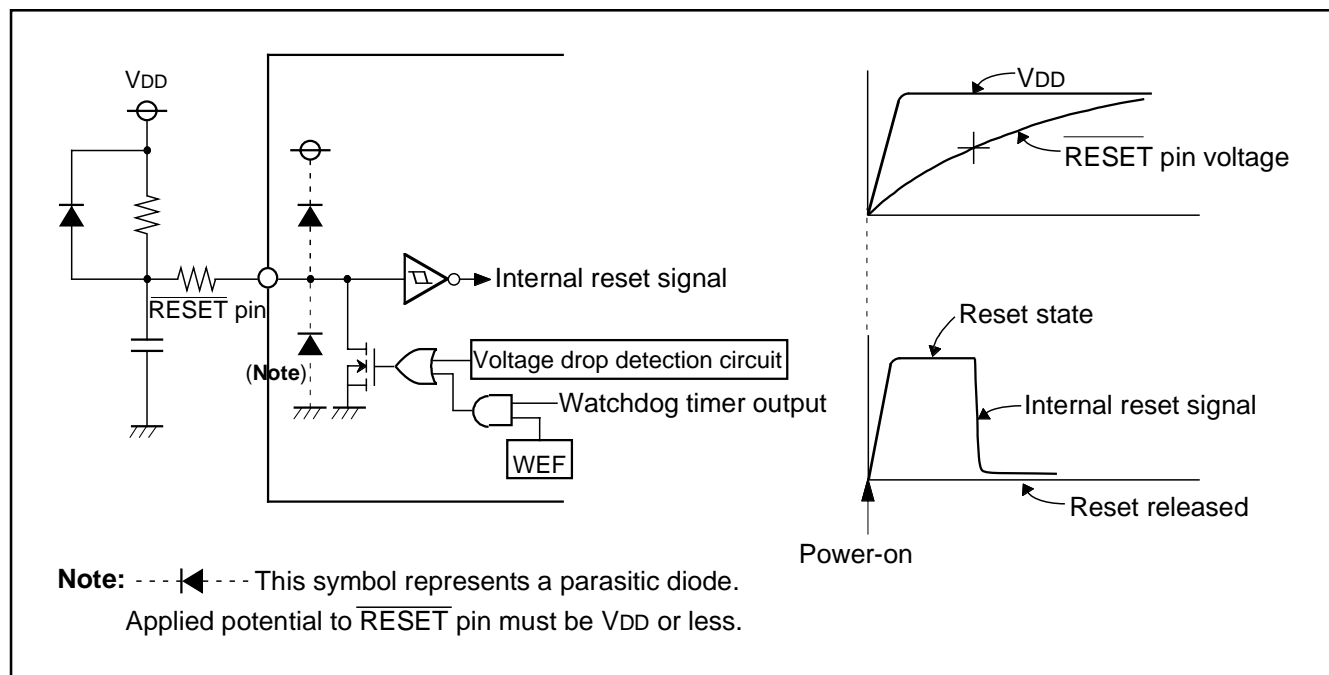


Fig. 34 Power-on reset circuit example

## (2) Internal state at reset

Table 19 shows port state at reset, and Figure 35 shows internal state at reset (they are the same after system is released from reset). The contents of timers, registers, flags and RAM except shown in Figure 35 are undefined, so set the initial value to them.

Table 19 Port state at reset

| Name                       | Function | State                       |
|----------------------------|----------|-----------------------------|
| D0–D5                      | D0–D5    | High impedance (Note)       |
| D6/CNTR0, D7/CNTR1         | D6, D7   |                             |
| P00–P03                    | P00–P03  | High impedance (Notes 1, 2) |
| P10–P13                    | P10–P13  |                             |
| P20/SCK, P21/SOUT, P22/SIN | P20–P22  | High impedance              |
| P30/INT0, P31/INT1         | P30, P31 | High impedance (Note 1)     |
| P32, P33 (Note 4)          | P32, P33 |                             |
| P40/AIN4–P43/AIN7 (Note 4) | P40–P43  | High impedance (Note 1)     |
| P50–P53 (Note 4)           | P50–P53  | High impedance (Note 3)     |

Notes 1: Output latch is set to "1."

2: Pull-up transistor is turned OFF.

3: After system is released from reset, port P5 is in the input mode. (Direction register FR0 = 00002)

4: The 4513 Group does not have these ports.

|  |                               |  |
|--|-------------------------------|--|
| • Program counter (PC) .....                                     | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |
| Address 0 in page 0 is set to program counter.                   |                               |  |
| • Interrupt enable flag (INTE) .....                             | 0                             | (Interrupt disabled)                                       |
| • Power down flag (P) .....                                      | 0                             |  |
| • External 0 interrupt request flag (EXF0) .....                 | 0                             |  |
| • External 1 interrupt request flag (EXF1) .....                 | 0                             |  |
| • Interrupt control register V1 .....                            | 0 0 0 0                       | (Interrupt disabled)                                       |
| • Interrupt control register V2 .....                            | 0 0 0 0                       | (Interrupt disabled)                                       |
| • Interrupt control register I1 .....                            | 0 0 0 0                       |  |
| • Interrupt control register I2 .....                            | 0 0 0 0                       |  |
| • Timer 1 interrupt request flag (T1F) .....                     | 0                             |  |
| • Timer 2 interrupt request flag (T2F) .....                     | 0                             |  |
| • Timer 3 interrupt request flag (T3F) .....                     | 0                             |  |
| • Timer 4 interrupt request flag (T4F) .....                     | 0                             |  |
| • Watchdog timer flags (WDF1, WDF2) .....                        | 0                             |  |
| • Watchdog timer enable flag (WEF) .....                         | 0                             |  |
| • Timer control register W1 .....                                | 0 0 0 0                       | (Prescaler and timer 1 stopped)                            |
| • Timer control register W2 .....                                | 0 0 0 0                       | (Timer 2 stopped)  |
| • Timer control register W3 .....                                | 0 0 0 0                       | (Timer 3 stopped)  |
| • Timer control register W4 .....                                | 0 0 0 0                       | (Timer 4 stopped)  |
| • Timer control register W6 .....                                | 0 0 0 0                       |  |
| • Clock control register MR .....                                | 1 0 0 0                       |  |
| • Serial I/O transmission/reception completion flag (SIOF) ..... | 0                             |  |
| • Serial I/O mode register J1 .....                              | 0 0 0 0                       | (External clock selected and serial I/O port not selected) |
| • Serial I/O register SI .....                                   | X X X X X X X X               |  |
| • A-D conversion completion flag (ADF) .....                     | 0                             |  |
| • A-D control register Q1 .....                                  | 0 0 0 0                       |  |
| • A-D control register Q2 .....                                  | 0 0 0 0                       |  |
| • Voltage comparator control register Q3 .....                   | 0 0 0 0                       |  |
| • Successive comparison register AD .....                        | X X X X X X X X X X           |  |
| • Comparator register .....                                      | X X X X X X X X               |  |
| • Key-on wakeup control register K0 .....                        | 0 0 0 0                       |  |
| • Pull-up control register PU0 .....                             | 0 0 0 0                       |  |
| • Direction register FR0 .....                                   | 0 0 0 0                       | (Port P5: input mode)                                      |
| • Carry flag (CY) .....  | 0                             |  |
| • Register A .....   | 0 0 0 0                       |  |
| • Register B .....   | 0 0 0 0                       |  |
| • Register D .....   | X X X                         |  |
| • Register E .....   | X X X X X X X X               |  |
| • Register X .....   | 0 0 0 0                       |  |
| • Register Y .....   | 0 0 0 0                       |  |
| • Register Z .....   | X X                           |  |
| • Stack pointer (SP) .....                                       | 1 1 1                         |  |

“X” represents undefined.

Fig. 35 Internal state at reset

## VOLTAGE DROP DETECTION CIRCUIT

The built-in voltage drop detection circuit is designed to detect a drop in voltage and to reset the microcomputer if the supply voltage drops below a set value.

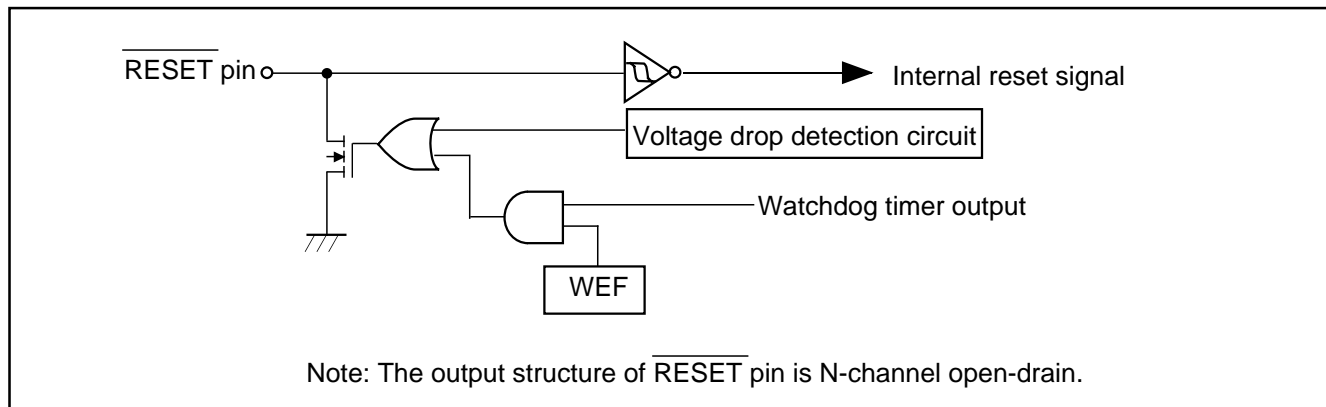


Fig. 36 Voltage drop detection reset circuit

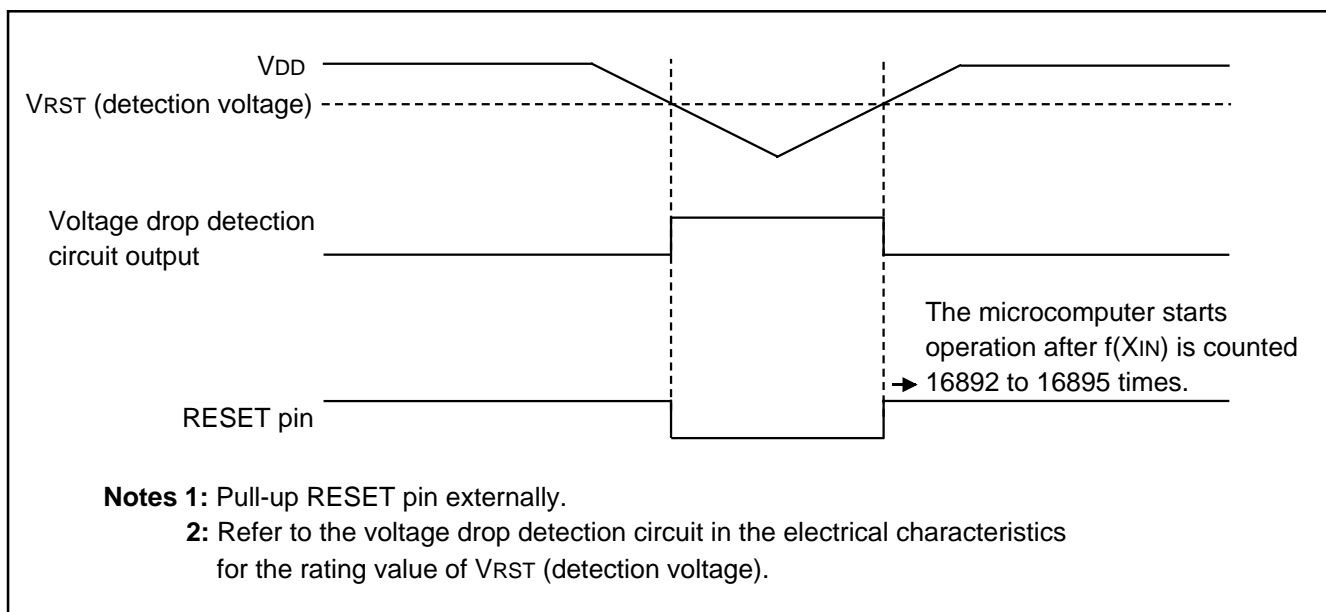


Fig. 37 Voltage drop detection circuit operation waveform

## RAM BACK-UP MODE

The 4513/4514 Group has the RAM back-up mode.

When the EPOF and POF instructions are executed continuously, system enters the RAM back-up state. The POF instruction is equal to the NOP instruction when the EPOF instruction is not executed before the POF instruction.

As oscillation stops retaining RAM, the function of reset circuit and states at RAM back-up mode, current dissipation can be reduced without losing the contents of RAM. Table 20 shows the function and states retained at RAM back-up. Figure 38 shows the state transition.

### (1) Identification of the start condition

Warm start (return from the RAM back-up state) or cold start (return from the normal reset state) can be identified by examining the state of the power down flag (P) with the SNZP instruction.

### (2) Warm start condition

When the external wakeup signal is input after the system enters the RAM back-up state by executing the EPOF and POF instructions continuously, the CPU starts executing the program from address 0 in page 0. In this case, the P flag is "1."

### (3) Cold start condition

The CPU starts executing the program from address 0 in page 0 when;

- reset pulse is input to  $\overline{\text{RESET}}$  pin, or
- reset by watchdog timer is performed, or
- voltage drop detection circuit detects the voltage drop.

In this case, the P flag is "0."

**Table 20 Functions and states retained at RAM back-up**

| Function   | RAM back-up |
|--|-------------|
| Program counter (PC), registers A, B, carry flag (CY), stack pointer (SP) (Note 2) | X           |
| Contents of RAM  | O           |
| Port level   | O           |
| Timer control register W1  | X           |
| Timer control registers W2 to W4, W6   | O           |
| Clock control register MR  | X           |
| Interrupt control registers V1, V2   | X           |
| Interrupt control registers I1, I2   | O           |
| Timer 1 function   | X           |
| Timer 2 function   | (Note 3)    |
| Timer 3 function   | (Note 3)    |
| Timer 4 function   | (Note 3)    |
| A-D conversion function  | X           |
| A-D control registers Q1, Q2   | O           |
| Voltage comparator function  | O (Note 5)  |
| Voltage comparator control register Q3   | O           |
| Serial I/O function  | X           |
| Serial I/O mode register J1  | O           |
| Pull-up control register PU0   | O           |
| Key-on wakeup control register K0  | O           |
| Direction register FR0   | O           |
| External 0 interrupt request flag (EXF0)   | X           |
| External 1 interrupt request flag (EXF1)   | X           |
| Timer 1 interrupt request flag (T1F)   | X           |
| Timer 2 interrupt request flag (T2F)   | (Note 3)    |
| Timer 3 interrupt request flag (T3F)   | (Note 3)    |
| Timer 4 interrupt request flag (T4F)   | (Note 3)    |
| Watchdog timer flags (WDF1, WDF2)  | X (Note 4)  |
| Watchdog timer enable flag (WEF)   | X (Note 4)  |
| 16-bit timer (WDT)   | X (Note 4)  |
| A-D conversion completion flag (ADF)   | X           |
| Serial I/O transmission/reception completion flag (SIOF)                           | X           |
| Interrupt enable flag (INTE)   | X           |

Notes 1: "O" represents that the function can be retained, and "X" represents that the function is initialized.

Registers and flags other than the above are undefined at RAM back-up, and set an initial value after returning.

2: The stack pointer (SP) points the level of the stack register and is initialized to "7" at RAM back-up.

3: The state of the timer is undefined.

4: Initialize the watchdog timer with the WRST instruction, and then execute the POF instruction.

5: The state is retained when the voltage comparator function is selected with the voltage comparator control register Q3.

#### (4) Return signal

An external wakeup signal is used to return from the RAM back-up mode because the oscillation is stopped. Table 21 shows the return condition for each return source.

#### (5) Ports P0 and P1 control registers

- Key-on wakeup control register K0  
Register K0 controls the ports P0 and P1 key-on wakeup function. Set the contents of this register through register A with the TK0A instruction. In addition, the TAK0 instruction can be used to transfer the contents of register K0 to register A.
- Pull-up control register PU0  
Register PU0 controls the ON/OFF of the ports P0 and P1 pull-up transistor. Set the contents of this register through register A with the TPU0A instruction. In addition, the TAPU0 instruction can be used to transfer the contents of register PU0 to register A.

**Table 21 Return source and return condition**

| Return source          |               | Return condition   | Remarks  |
|------------------------|---------------|--|--|
| External wakeup signal | Ports P0, P1  | Return by an external falling edge input ("H"→"L").                              | Set the port using the key-on wakeup function selected with register K0 to "H" level before going into the RAM back-up state because the port P0 shares the falling edge detection circuit with port P1. |
|                        | Port P30/INT0 | Return by an external "H" level or "L" level input.<br>The EXF0 flag is not set. | Select the return level ("L" level or "H" level) with the bit 2 of register I1 according to the external state before going into the RAM back-up state.  |
|                        | Port P31/INT1 | Return by an external "H" level or "L" level input.<br>The EXF1 flag is not set. | Select the return level ("L" level or "H" level) with the bit 2 of register I2 according to the external state before going into the RAM back-up state.  |

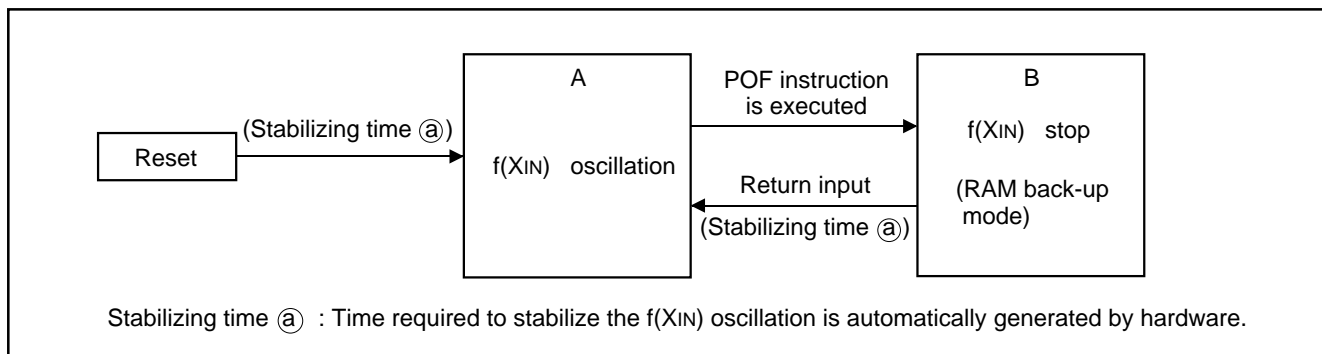


Fig. 38 State transition

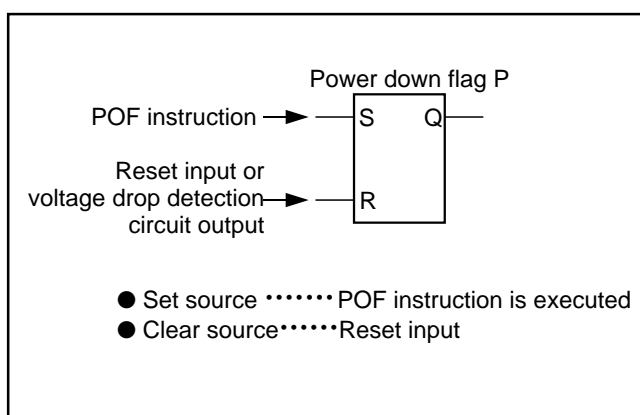


Fig. 39 Set source and clear source of the P flag

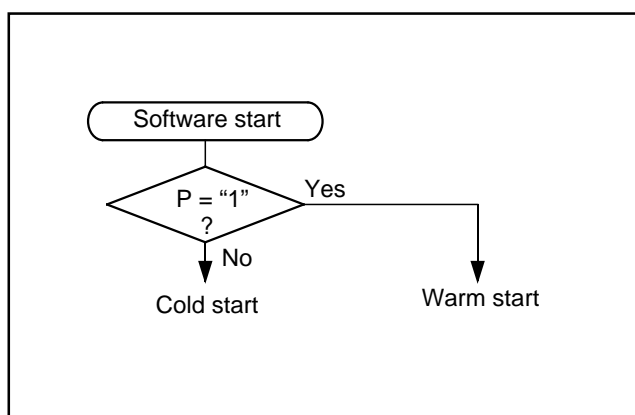


Fig. 40 Start condition identified example using the SNZP instruction



Table 22 Key-on wakeup control register, pull-up control register, and interrupt control register

| Key-on wakeup control register K0 |   | at reset : 00002 |   | at RAM back-up : state retained | R/W |
|-----------------------------------|---|------------------|---|---------------------------------|-----|
| K03                               | Pins P12 and P13 key-on wakeup control bit                                    | 0                | Key-on wakeup not used  |                                 |     |
|                                   |   | 1                | Key-on wakeup used  |                                 |     |
| K02                               | Pins P10 and P11 key-on wakeup control bit                                    | 0                | Key-on wakeup not used  |                                 |     |
|                                   |   | 1                | Key-on wakeup used  |                                 |     |
| K01                               | Pins P02 and P03 key-on wakeup control bit                                    | 0                | Key-on wakeup not used  |                                 |     |
|                                   |   | 1                | Key-on wakeup used  |                                 |     |
| K00                               | Pins P00 and P01 key-on wakeup control bit                                    | 0                | Key-on wakeup not used  |                                 |     |
|                                   |   | 1                | Key-on wakeup used  |                                 |     |
| Pull-up control register PU0      |   | at reset : 00002 |   | at RAM back-up : state retained | R/W |
| PU03                              | Pins P12 and P13 pull-up transistor control bit                               | 0                | Pull-up transistor OFF  |                                 |     |
|                                   |   | 1                | Pull-up transistor ON   |                                 |     |
| PU02                              | Pins P10 and P11 pull-up transistor control bit                               | 0                | Pull-up transistor OFF  |                                 |     |
|                                   |   | 1                | Pull-up transistor ON   |                                 |     |
| PU01                              | Pins P02 and P03 pull-up transistor control bit                               | 0                | Pull-up transistor OFF  |                                 |     |
|                                   |   | 1                | Pull-up transistor ON   |                                 |     |
| PU00                              | Pins P00 and P01 pull-up transistor control bit                               | 0                | Pull-up transistor OFF  |                                 |     |
|                                   |   | 1                | Pull-up transistor ON   |                                 |     |
| Interrupt control register I1     |   | at reset : 00002 |   | at RAM back-up : state retained | R/W |
| I13                               | Not used  | 0                | This bit has no function, but read/write is enabled.  |                                 |     |
|                                   |   | 1                |   |                                 |     |
| I12                               | Interrupt valid waveform for INT0 pin/<br>return level selection bit (Note 2) | 0                | Falling waveform ("L" level of INT0 pin is recognized with the SNZI0 instruction)/"L" level |                                 |     |
|                                   |   | 1                | Rising waveform ("H" level of INT0 pin is recognized with the SNZI0 instruction)/"H" level  |                                 |     |
| I11                               | INT0 pin edge detection circuit control bit                                   | 0                | One-sided edge detected   |                                 |     |
|                                   |   | 1                | Both edges detected   |                                 |     |
| I10                               | INT0 pin<br>timer 1 control enable bit  | 0                | Disabled  |                                 |     |
|                                   |   | 1                | Enabled   |                                 |     |
| Interrupt control register I2     |   | at reset : 00002 |   | at RAM back-up : state retained | R/W |
| I23                               | Not used  | 0                | This bit has no function, but read/write is enabled.  |                                 |     |
|                                   |   | 1                |   |                                 |     |
| I22                               | Interrupt valid waveform for INT1 pin/<br>return level selection bit (Note 3) | 0                | Falling waveform ("L" level of INT1 pin is recognized with the SNZI1 instruction)/"L" level |                                 |     |
|                                   |   | 1                | Rising waveform ("H" level of INT1 pin is recognized with the SNZI1 instruction)/"H" level  |                                 |     |
| I21                               | INT1 pin edge detection circuit control bit                                   | 0                | One-sided edge detected   |                                 |     |
|                                   |   | 1                | Both edges detected   |                                 |     |
| I20                               | INT1 pin<br>timer 3 control enable bit  | 0                | Disabled  |                                 |     |
|                                   |   | 1                | Enabled   |                                 |     |

Notes 1: "R" represents read enabled, and "W" represents write enabled.

2: When the contents of I12 is changed, the external interrupt request flag EXF0 may be set. Accordingly, clear EXF0 flag with the SNZ0 instruction.

3: When the contents of I22 is changed, the external interrupt request flag EXF1 may be set. Accordingly, clear EXF1 flag with the SNZ1 instruction.

## CLOCK CONTROL

The clock control circuit consists of the following circuits.

- System clock generating circuit
- Control circuit to stop the clock oscillation
- Control circuit to switch the middle-speed mode and high-speed mode
- Control circuit to return from the RAM back-up state

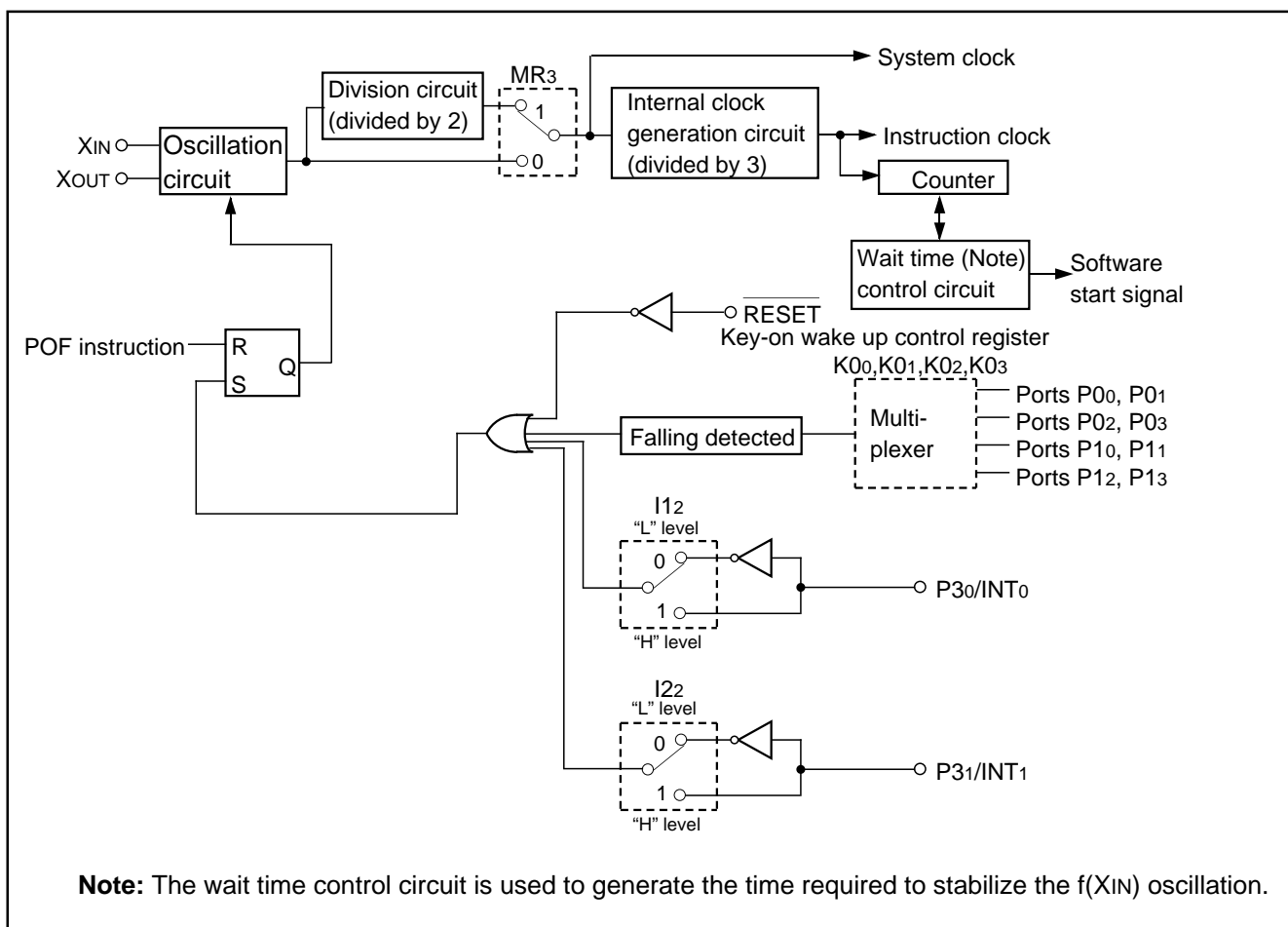


Fig. 41 Clock control circuit structure

Table 23 Clock control register MR

| Clock control register MR |                            | at reset : 10002 |  | at RAM back-up : 10002 | R/W |
|---------------------------|----------------------------|------------------|--|------------------------|-----|
| MR3                       | System clock selection bit | 0                | f(XIN) (high-speed mode)                             |                        |     |
|                           |                            | 1                | f(XIN)/2 (middle-speed mode)                         |                        |     |
| MR2                       | Not used                   | 0                | This bit has no function, but read/write is enabled. |                        |     |
|                           |                            | 1                |  |                        |     |
| MR1                       | Not used                   | 0                | This bit has no function, but read/write is enabled. |                        |     |
|                           |                            | 1                |  |                        |     |
| MR0                       | Not used                   | 0                | This bit has no function, but read/write is enabled. |                        |     |
|                           |                            | 1                |  |                        |     |

Note : "R" represents read enabled, and "W" represents write enabled.

Clock signal  $f(XIN)$  is obtained by externally connecting a ceramic resonator.

Connect this external circuit to pins XIN and XOUT at the shortest distance. A feedback resistor is built in between pins XIN and XOUT. When an external clock signal is input, connect the clock source to XIN and leave XOUT open. When using an external clock, the maximum value of external clock oscillating frequency is shown in Table 24.

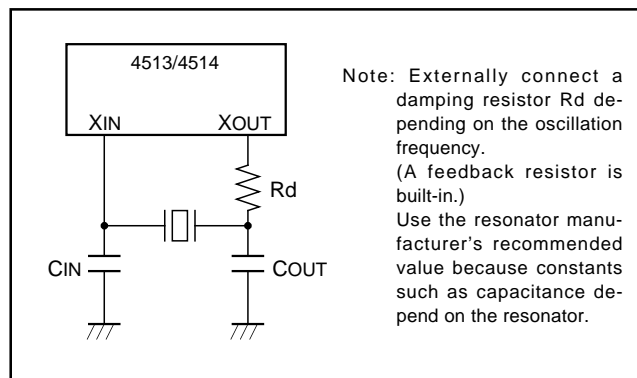


Fig. 42 Ceramic resonator external circuit

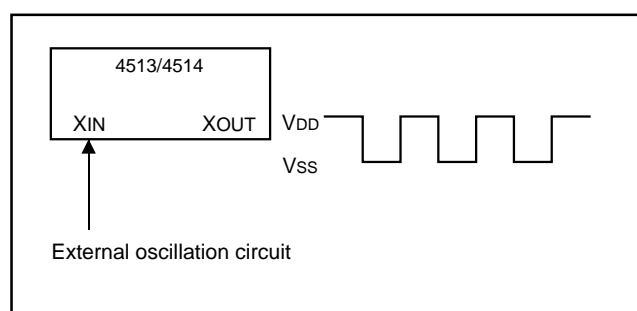


Fig. 43 External clock input circuit

Table 24 Maximum value of external clock oscillation frequency

|                       |                   | Supply voltage                             | Oscillation frequency (duty ratio) |
|-----------------------|-------------------|--|------------------------------------|
| Mask ROM version      | Middle-speed mode | $V_{DD} = 2.0 \text{ V to } 5.5 \text{ V}$ | 3.0 MHz (40 % to 60 %)             |
|                       | High-speed mode   | $V_{DD} = 4.0 \text{ V to } 5.5 \text{ V}$ | 3.0 MHz (40 % to 60 %)             |
|                       |                   | $V_{DD} = 2.5 \text{ V to } 5.5 \text{ V}$ | 1.0 MHz (40 % to 60 %)             |
|                       |                   | $V_{DD} = 2.0 \text{ V to } 5.5 \text{ V}$ | 0.8 MHz (40 % to 60 %)             |
| One Time PROM version | Middle-speed mode | $V_{DD} = 2.5 \text{ V to } 5.5 \text{ V}$ | 3.0 MHz (40 % to 60 %)             |
|                       | High-speed mode   | $V_{DD} = 4.0 \text{ V to } 5.5 \text{ V}$ | 3.0 MHz (40 % to 60 %)             |
|                       |                   | $V_{DD} = 2.5 \text{ V to } 5.5 \text{ V}$ | 1.0 MHz (40 % to 60 %)             |

## ROM ORDERING METHOD

- 1.Mask ROM Order Confirmation Form\*
- 2.Mark Specification Form\*
- 3.Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk.

\*For the mask ROM confirmation and the mark specifications, refer to the "Mitsubishi MCU Technical Information" Homepage (<http://www.infocom.maec.co.jp/indexe.htm>).

## LIST OF PRECAUTIONS

### ① Noise and latch-up prevention

Connect a capacitor on the following condition to prevent noise and latch-up;

- connect a bypass capacitor (approx. 0.1  $\mu$ F) between pins VDD and VSS at the shortest distance,
- equalize its wiring in width and length, and
- use relatively thick wire.

In the One Time PROM version, CNVSS pin is also used as VPP pin. Accordingly, when using this pin, connect this pin to VSS through a resistor about 5 k $\Omega$  in series at the shortest distance.

### ② Prescaler

Stop the prescaler operation to change its frequency dividing ratio.

### ③ Timer count source

Stop timer 1, 2, 3, or 4 counting to change its count source.

### ④ Reading the count value

Stop timer 1, 2, 3, or 4 counting and then execute the TAB1, TAB2, TAB3, or TAB4 instruction to read its data.

### ⑤ Writing to reload registers R1 and R3

When writing data to reload registers R1 or R3 while timer 1 or timer 3 is operating, avoid a timing when timer 1 or timer 3 underflows.

### ⑥ P30/INT0 pin

When the interrupt valid waveform of the P30/INT0 pin is changed with the bit 2 of register I1 in software, be careful about the following notes.

- Clear the bit 0 of register V1 to "0" before the interrupt valid waveform of P30/INT0 pin is changed with the bit 2 of register I1 (refer to Figure 44①).
- Depending on the input state of the P30/INT0 pin, the external 0 interrupt request flag (EXF0) may be set when the interrupt valid waveform is changed. Accordingly, clear bit 2 of register I1, and execute the SNZ0 instruction to clear the EXF0 flag after executing at least one instruction (refer to Figure 44②)

```

:
LA    4      ; (XXX02)
TV1A   ; The SNZ0 instruction is valid ..... ①
LA    4      ;
TI1A   ; Interrupt valid waveform is changed
NOP    ..... ②
SNZ0   ; The SNZ0 instruction is executed
NOP
:
X : this bit is not related to the setting of INT0 pin.
```

Fig. 44 External 0 interrupt program example

### ⑦ P31/INT1 pin

When the interrupt valid waveform of P31/INT1 pin is changed with the bit 2 of register I2 in software, be careful about the following notes.

- Clear the bit 1 of register V1 to "0" before the interrupt valid waveform of P31/INT1 pin is changed with the bit 2 of register I2 (refer to Figure 45③).
- Depending on the input state of the P31/INT1 pin, the external 1 interrupt request flag (EXF1) may be set when the interrupt valid waveform is changed. Accordingly, clear bit 2 of register I2 and execute the SNZ1 instruction to clear the EXF1 flag after executing at least one instruction (refer to Figure 45④).

```

:
LA    8      ; (XX0X2)
TV1A   ; The SNZ1 instruction is valid ..... ③
LA    8      ;
TI2A   ; Change of the interrupt valid waveform
NOP    ..... ④
SNZ1   ; The SNZ1 instruction is executed
NOP
:
X : this bit is not related to the setting of INT1.
```

Fig. 45 External 1 interrupt program example

### ⑧ One Time PROM version

The operating power voltage of the One Time PROM version is 2.5 V to 5.5 V.

### ⑨ Multifunction

The input of D6, D7, P20–P22, I/O of P30 and P31, input of CMP0-, CMP0+, CMP1-, CMP1+, and I/O of P40–P43 can be used even when CNTR0, CNTR1, Sck, SOUT, SIN, INT0, INT1, AIN0–AIN3 and AIN4–AIN7 are selected.

## ⑩ A-D converter-1

When the operating mode of the A-D converter is changed from the comparator mode to the A-D conversion mode with the bit 3 of register Q2 in a program, be careful about the following notes.

- Clear the bit 2 of register V2 to "0" to change the operating mode of the A-D converter from the comparator mode to the A-D conversion mode with the bit 3 of register Q2 (refer to Figure 46⑤).
- The A-D conversion completion flag (ADF) may be set when the operating mode of the A-D converter is changed from the comparator mode to the A-D conversion mode. Accordingly, set a value to register Q2, and execute the SNZAD instruction to clear the ADF flag.

Do not change the operating mode (both A-D conversion mode and comparator mode) of A-D converter with the bit 3 of register Q2 during operating the A-D converter.

|       |   |   |
|-------|---|---|
| ⋮     |   |   |
| LA    | 8 | ; (X0XX2)   |
| TV2A  |   | ; The SNZAD instruction is valid.....⑤  |
| LA    | 0 | ; (0XXX2)   |
| TQ2A  |   | ; Change of the operating mode of the A-D converter from the comparator mode to the A-D conversion mode |
| SNZAD |   |   |
| NOP   |   |   |
| ⋮     |   |   |
|       |   | X: this bit is not related to the change of the operating mode of the A-D conversion.                   |

Fig. 46 A-D converter operating mode program example

## ⑪ A-D converter-2

Each analog input pin is equipped with a capacitor which is used to compare the analog voltage. Accordingly, when the analog voltage is input from the circuit with high-impedance and, charge/discharge noise is generated and the sufficient A-D accuracy may not be obtained. Therefore, reduce the impedance or, connect a capacitor (0.01  $\mu$ F to 1  $\mu$ F) to analog input pins (Figure 47).

When the overvoltage applied to the A-D conversion circuit may occur, connect an external circuit in order to keep the voltage within the rated range as shown the Figure 48. In addition, test the application products sufficiently.

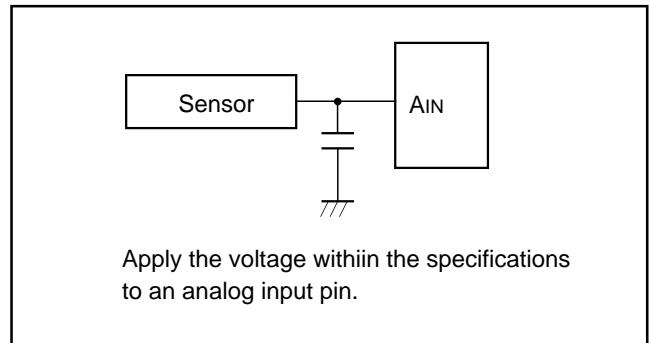


Fig. 47 Analog input external circuit example-1

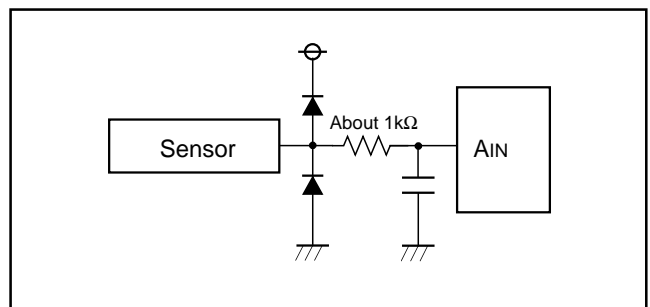


Fig. 48 Analog input external circuit example-2

## ⑫ POF instruction

Execute the POF instruction immediately after executing the EPOF instruction to enter the RAM back-up.

Note that system cannot enter the RAM back-up state when executing only the POF instruction.

Be sure to disable interrupts by executing the DI instruction before executing the EPOF instruction.

## ⑬ Analog input pins

Note the following when using the analog input pins also for I/O port P4 functions:

- Even when P40/AIN4–P43/AIN7 are set to pins for analog input, they continue to function as P40–P43 I/O. Accordingly, when any of them are used as I/O port P4 and others are used as analog input pins, make sure to set the outputs of pins that are set for analog input to "1." Also, the port input function of the pin functions as an analog input is undefined.
- TALA instruction  
When the TALA instruction is executed, the low-order 2 bits of register AD is transferred to the high-order 2 bits of register A, simultaneously, the low-order 2 bits of register A is "0."

## ⑭ Program counter

Make sure that the PCH does not specify after the last page of the built-in ROM.

## ⑮ Port P3

In the 4513 Group, when the IAP3 instruction is executed, note that the high-order 2 bits of register A is undefined.

#### ⑮ Voltage comparator function

When the voltage comparator function is valid with the voltage comparator control register Q3, it is operating even in the RAM back-up mode. Accordingly, be careful about such state because it causes the increase of the operation current in the RAM back-up mode.

In order to reduce the operation current in the RAM back-up mode, invalidate (bits 2 and 3 of register Q3 = "0") the voltage comparator function by software before the POF instruction is executed.

Also, while the voltage comparator function is valid, current is always consumed by voltage comparator. On the system required for the low-power dissipation, invalidate the voltage comparator when it is unused by software.

#### ⑯ Register Q3

Bits 0 and 1 of register Q3 can be only read. Note that they cannot be written.

#### ⑰ Reading the comparison result of voltage comparator

Read the voltage comparator comparison result from register Q3 after the voltage comparator response time (max. 20  $\mu$ s) is passed from the voltage comparator function become valid.

# SYMBOL

The symbols shown below are used in the following instruction function table and instruction list.

| Symbol          | Contents   | Symbol   | Contents   |
|-----------------|--|----------|--|
| A               | Register A (4 bits)  | T1F      | Timer 1 interrupt request flag   |
| B               | Register B (4 bits)  | T2F      | Timer 2 interrupt request flag   |
| DR              | Register D (3 bits)  | T3F      | Timer 3 interrupt request flag   |
| E               | Register E (8 bits)  | T4F      | Timer 4 interrupt request flag   |
| Q1              | A-D control register Q1 (4 bits)                                 | WDF1     | Watchdog timer flag  |
| Q2              | A-D control register Q2 (4 bits)                                 | WEF      | Watchdog timer enable flag   |
| Q3              | Voltage comparator control register Q3 (4 bits)                  | INTE     | Interrupt enable flag  |
| AD              | Successive comparison register AD (10 bits)                      | EXF0     | External 0 interrupt request flag  |
| J1              | Serial I/O mode register J1 (4 bits)                             | EXF1     | External 1 interrupt request flag  |
| SI              | Serial I/O register SI (8 bits)                                  | P        | Power down flag  |
| V1              | Interrupt control register V1 (4 bits)                           | ADF      | A-D conversion completion flag   |
| V2              | Interrupt control register V2 (4 bits)                           | SIOF     | Serial I/O transmission/reception completion flag                          |
| I1              | Interrupt control register I1 (4 bits)                           |          |  |
| I2              | Interrupt control register I2 (4 bits)                           | D        | Port D (8 bits)  |
| W1              | Timer control register W1 (4 bits)                               | P0       | Port P0 (4 bits)   |
| W2              | Timer control register W2 (4 bits)                               | P1       | Port P1 (4 bits)   |
| W3              | Timer control register W3 (4 bits)                               | P2       | Port P2 (3 bits)   |
| W4              | Timer control register W4 (4 bits)                               | P3       | Port P3 (4 bits)   |
| W6              | Timer control register W6 (4 bits)                               | P4       | Port P4 (4 bits)   |
| MR              | Clock control register MR (4 bits)                               | P5       | Port P5 (4 bits)   |
| K0              | Key-on wakeup control register K0 (4 bits)                       |          |  |
| PU0             | Pull-up control register PU0 (4 bits)                            | x        | Hexadecimal variable   |
| FR0             | Direction register FR0 (4 bits)                                  | y        | Hexadecimal variable   |
| X               | Register X (4 bits)  | z        | Hexadecimal variable   |
| Y               | Register Y (4 bits)  | p        | Hexadecimal variable   |
| Z               | Register Z (2 bits)  | n        | Hexadecimal constant   |
| DP              | Data pointer (10 bits)<br>(It consists of registers X, Y, and Z) | i        | Hexadecimal constant   |
| PC              | Program counter (14 bits)  | j        | Hexadecimal constant   |
| PC <sub>H</sub> | High-order 7 bits of program counter                             | A3A2A1A0 | Binary notation of hexadecimal variable A<br>(same for others)             |
| PC <sub>L</sub> | Low-order 7 bits of program counter                              |          |  |
| SK              | Stack register (14 bits X 8)                                     | ←        | Direction of data movement   |
| SP              | Stack pointer (3 bits)   | ↔        | Data exchange between a register and memory                                |
| CY              | Carry flag   | ?        | Decision of state shown before “?”   |
| R1              | Timer 1 reload register  | ( )      | Contents of registers and memories   |
| R2              | Timer 2 reload register  | —        | Negate, Flag unchanged after executing instruction                         |
| R3              | Timer 3 reload register  | M(DP)    | RAM address pointed by the data pointer                                    |
| R4              | Timer 4 reload register  | a        | Label indicating address a6 a5 a4 a3 a2 a1 a0                              |
| T1              | Timer 1  | p, a     | Label indicating address a6 a5 a4 a3 a2 a1 a0<br>in page p5 p4 p3 p2 p1 p0 |
| T2              | Timer 2  |          |  |
| T3              | Timer 3  | C        | Hex. C + Hex. number x (also same for others)                              |
| T4              | Timer 4  | +        |  |
|                 |  | x        |  |

Note : The 4513/4514 Group just invalidates the next instruction when a skip is performed. The contents of program counter is not increased by 2. Accordingly, the number of cycles does not change even if skip is not performed. However, the cycle count becomes “1” if the TABP p, RT, or RTS instruction is skipped.

## LIST OF INSTRUCTION FUNCTION

| Group-ing                     | Mnemonic | Function  | Group-ing                | Mnemonic | Function  | Group-ing            | Mnemonic | Function  |
|-------------------------------|----------|---|--------------------------|----------|---|----------------------|----------|---|
| Register to register transfer | TAB      | $(A) \leftarrow (B)$  | RAM to register transfer | XAMI j   | $(A) \leftarrow \rightarrow (M(DP))$<br>$(X) \leftarrow (X) \text{EXOR}(j)$<br>$j = 0 \text{ to } 15$<br>$(Y) \leftarrow (Y) + 1$   | Bit operation        | SB j     | $(Mj(DP)) \leftarrow 1$<br>$j = 0 \text{ to } 3$  |
|                               | TBA      | $(B) \leftarrow (A)$  |                          | TMA j    | $(M(DP)) \leftarrow (A)$<br>$(X) \leftarrow (X) \text{EXOR}(j)$<br>$j = 0 \text{ to } 15$   |                      | RB j     | $(Mj(DP)) \leftarrow 0$<br>$j = 0 \text{ to } 3$  |
|                               | TAY      | $(A) \leftarrow (Y)$  |                          |          |   |                      | SZB j    | $(Mj(DP)) = 0 ?$<br>$j = 0 \text{ to } 3$   |
|                               | TYA      | $(Y) \leftarrow (A)$  |                          |          |   | Comparison operation | SEAM     | $(A) = (M(DP)) ?$   |
|                               | TEAB     | $(E7-E4) \leftarrow (B)$<br>$(E3-E0) \leftarrow (A)$  |                          | LA n     | $(A) \leftarrow n$<br>$n = 0 \text{ to } 15$  |                      | SEA n    | $(A) = n ?$<br>$n = 0 \text{ to } 15$   |
|                               | TABE     | $(B) \leftarrow (E7-E4)$<br>$(A) \leftarrow (E3-E0)$  |                          | TABP p   | $(SP) \leftarrow (SP) + 1$<br>$(SK(SP)) \leftarrow (PC)$<br>$(PCH) \leftarrow p$<br>$(PCL) \leftarrow (DR2-DR0, A3-A0)$<br>$(B) \leftarrow (ROM(PC))^{7-4}$<br>$(A) \leftarrow (ROM(PC))^{3-0}$<br>$(PC) \leftarrow (SK(SP))$<br>$(SP) \leftarrow (SP) - 1$ | Branch operation     | B a      | $(PCL) \leftarrow a6-a0$  |
|                               | TDA      | $(DR2-DR0) \leftarrow (A2-A0)$  |                          | AM       | $(A) \leftarrow (A) + (M(DP))$  |                      | BL p, a  | $(PCH) \leftarrow p$<br>$(PCL) \leftarrow a6-a0$  |
|                               | TAD      | $(A2-A0) \leftarrow (DR2-DR0)$<br>$(A3) \leftarrow 0$   |                          | AMC      | $(A) \leftarrow (A) + (M(DP)) + (CY)$<br>$(CY) \leftarrow \text{Carry}$   |                      | BLA p    | $(PCH) \leftarrow p$<br>$(PCL) \leftarrow (DR2-DR0, A3-A0)$   |
|                               | TAZ      | $(A1, A0) \leftarrow (Z1, Z0)$<br>$(A3, A2) \leftarrow 0$   | Arithmetic operation     | A n      | $(A) \leftarrow (A) + n$<br>$n = 0 \text{ to } 15$  | Subroutine operation | BM a     | $(SP) \leftarrow (SP) + 1$<br>$(SK(SP)) \leftarrow (PC)$<br>$(PCH) \leftarrow 2$<br>$(PCL) \leftarrow a6-a0$            |
|                               | TAX      | $(A) \leftarrow (X)$  |                          | AND      | $(A) \leftarrow (A) \text{AND} (M(DP))$   |                      | BML p, a | $(SP) \leftarrow (SP) + 1$<br>$(SK(SP)) \leftarrow (PC)$<br>$(PCH) \leftarrow p$<br>$(PCL) \leftarrow a6-a0$            |
| RAM addresses                 | LXY x, y | $(X) \leftarrow x, x = 0 \text{ to } 15$<br>$(Y) \leftarrow y, y = 0 \text{ to } 15$  |                          | OR       | $(A) \leftarrow (A) \text{OR} (M(DP))$  |                      | BMLA p   | $(SP) \leftarrow (SP) + 1$<br>$(SK(SP)) \leftarrow (PC)$<br>$(PCH) \leftarrow p$<br>$(PCL) \leftarrow (DR2-DR0, A3-A0)$ |
|                               | LZ z     | $(Z) \leftarrow z, z = 0 \text{ to } 3$   |                          | SC       | $(CY) \leftarrow 1$   | Return operation     | RTI      | $(PC) \leftarrow (SK(SP))$<br>$(SP) \leftarrow (SP) - 1$  |
|                               | INY      | $(Y) \leftarrow (Y) + 1$  |                          | RC       | $(CY) \leftarrow 0$   |                      | RT       | $(PC) \leftarrow (SK(SP))$<br>$(SP) \leftarrow (SP) - 1$  |
|                               | DEY      | $(Y) \leftarrow (Y) - 1$  |                          | SZC      | $(CY) = 0 ?$  |                      | RTS      | $(PC) \leftarrow (SK(SP))$<br>$(SP) \leftarrow (SP) - 1$  |
| RAM to register transfer      | TAM j    | $(A) \leftarrow (M(DP))$<br>$(X) \leftarrow (X) \text{EXOR}(j)$<br>$j = 0 \text{ to } 15$   |                          | CMA      | $(A) \leftarrow \bar{A}$  |                      |          |   |
|                               | XAM j    | $(A) \leftarrow \rightarrow (M(DP))$<br>$(X) \leftarrow (X) \text{EXOR}(j)$<br>$j = 0 \text{ to } 15$                             |                          | RAR      | $\rightarrow \boxed{CY} \rightarrow \boxed{A3A2A1A0}$   |                      |          |   |
|                               | XAMD j   | $(A) \leftarrow \rightarrow (M(DP))$<br>$(X) \leftarrow (X) \text{EXOR}(j)$<br>$j = 0 \text{ to } 15$<br>$(Y) \leftarrow (Y) - 1$ |                          |          |   |                      |          |   |



LIST OF INSTRUCTION FUNCTION (continued)

| Group-<br>ing       | Mnemonic | Function   | Group-<br>ing   | Mnemonic | Function   | Group-<br>ing          | Mnemonic | Function                                   |
|---------------------|----------|--|-----------------|----------|--|------------------------|----------|--|
| Interrupt operation | DI       | (INTE) ← 0   | Timer operation | TAW4     | (A) ← (W4)   | Timer operation        | SNZT1    | (T1F) = 1 ?<br>After skipping<br>(T1F) ← 0 |
|                     | EI       | (INTE) ← 1   |                 | TW4A     | (W4) ← (A)   |                        | SNZT2    | (T2F) = 1 ?<br>After skipping<br>(T2F) ← 0 |
|                     | SNZ0     | (EXF0) = 1 ?<br>After skipping<br>(EXF0) ← 0         |                 | TAW6     | (A) ← (W6)   |                        | SNZT3    | (T3F) = 1 ?<br>After skipping<br>(T3F) ← 0 |
|                     | SNZ1     | (EXF1) = 1 ?<br>After skipping<br>(EXF1) ← 0         |                 | TW6A     | (W6) ← (A)   |                        | SNZT4    | (T4F) = 1 ?<br>After skipping<br>(T4F) ← 0 |
|                     | SNZI0    | I12 = 1 : (INT0) = "H" ?<br>I12 = 0 : (INT0) = "L" ? |                 | TAB1     | (B) ← (T17–T14)<br>(A) ← (T13–T10)                                       | Input/Output operation | IAP0     | (A) ← (P0)                                 |
|                     | SNZI1    | I22 = 1 : (INT1) = "H" ?<br>I22 = 0 : (INT1) = "L" ? |                 | T1AB     | (R17–R14) ← (B)<br>(T17–T14) ← (B)<br>(R13–R10) ← (A)<br>(T13–T10) ← (A) |                        | OP0A     | (P0) ← (A)                                 |
|                     | TAV1     | (A) ← (V1)   |                 | TAB2     | (B) ← (T27–T24)<br>(A) ← (T23–T20)                                       |                        | IAP1     | (A) ← (P1)                                 |
|                     | TV1A     | (V1) ← (A)   |                 | T2AB     | (R27–R24) ← (B)<br>(T27–T24) ← (B)<br>(R23–R20) ← (A)<br>(T23–T20) ← (A) |                        | OP1A     | (P1) ← (A)                                 |
|                     | TAV2     | (A) ← (V2)   |                 | TAB3     | (B) ← (T37–T34)<br>(A) ← (T33–T30)                                       |                        | IAP2     | (A2–A0) ← (P22–P20)<br>(A3) ← 0            |
|                     | TV2A     | (V2) ← (A)   |                 | T3AB     | (R37–R34) ← (B)<br>(T37–T34) ← (B)<br>(R33–R30) ← (A)<br>(T33–T30) ← (A) |                        | IAP3     | (A) ← (P3)                                 |
|                     | TAI1     | (A) ← (I1)   |                 | TAB4     | (B) ← (T47–T44)<br>(A) ← (T43–T40)                                       |                        | OP3A     | (P3) ← (A)                                 |
|                     | TI1A     | (I1) ← (A)   |                 | T4AB     | (R47–R44) ← (B)<br>(T47–T44) ← (B)<br>(R43–R40) ← (A)<br>(T43–T40) ← (A) |                        | IAP4*    | (A) ← (P4)                                 |
|                     | TAI2     | (A) ← (I2)   |                 | TR1AB    | (R17–R14) ← (B)<br>(R13–R10) ← (A)                                       |                        | OP4A*    | (P4) ← (A)                                 |
|                     | TI2A     | (I2) ← (A)   |                 | TR3AB    | (R37–R34) ← (B)<br>(R33–R30) ← (A)                                       |                        | IAP5*    | (A) ← (P5)                                 |
| Timer operation     | TAW1     | (A) ← (W1)   |                 |          |  |                        | OP5A*    | (P5) ← (A)                                 |
|                     | TW1A     | (W1) ← (A)   |                 |          |  |                        | CLD      | (D) ← 1                                    |
|                     | TAW2     | (A) ← (W2)   |                 |          |  |                        | RD       | (D(Y)) ← 0<br>(Y) = 0 to 7                 |
|                     | TW2A     | (W2) ← (A)   |                 |          |  |                        | SD       | (D(Y)) ← 1<br>(Y) = 0 to 7                 |
|                     | TAW3     | (A) ← (W3)   |                 |          |  |                        | SZD      | (D(Y)) = 0 ?<br>(Y) = 0 to 7               |
|                     | TW3A     | (W3) ← (A)   |                 |          |  |                        |          |  |

\*: The 4513 Group does not have these instructions.

**LIST OF INSTRUCTION FUNCTION (continued)**

| Group-<br>ing                | Mnemonic | Function  | Group-<br>ing            | Mnemonic | Function   |
|------------------------------|----------|---|--------------------------|----------|--|
| Input/Output operation       | TK0A     | $(K0) \leftarrow (A)$                                     | A-D conversion operation | TABAD    | $(A) \leftarrow (AD5-AD2)$<br>$(B) \leftarrow (AD9-AD6)$<br>However, in the com-<br>parator mode,<br>$(A) \leftarrow (AD3-AD0)$<br>$(B) \leftarrow (AD7-AD4)$          |
|                              | TAK0     | $(A) \leftarrow (K0)$                                     |                          | TALA     | $(A) \leftarrow (AD1, AD0, 0, 0)$  |
|                              | TPU0A    | $(PU0) \leftarrow (A)$                                    |                          | TADAB    | $(AD3-AD0) \leftarrow (A)$<br>$(AD7-AD4) \leftarrow (B)$   |
|                              | TAPU0    | $(A) \leftarrow (PU0)$                                    |                          | TAQ1     | $(A) \leftarrow (Q1)$  |
|                              | TFR0A*   | $(FR0) \leftarrow (A)$                                    |                          | TQ1A     | $(Q1) \leftarrow (A)$  |
| Serial I/O control operation | TABSI    | $(A) \leftarrow (SI3-SI0)$<br>$(B) \leftarrow (SI7-SI4)$  |                          | ADST     | $(ADF) \leftarrow 0$<br>A-D conversion starting  |
|                              | TSIAB    | $(SI3-SI0) \leftarrow (A)$<br>$(SI7-SI4) \leftarrow (B)$  |                          | SNZAD    | $(ADF) = 1 ?$<br>After skipping<br>$(ADF) \leftarrow 0$  |
|                              | TAJ1     | $(A) \leftarrow (J1)$                                     |                          | TAQ2     | $(A) \leftarrow (Q2)$  |
|                              | TJ1A     | $(J1) \leftarrow (A)$                                     |                          | TQ2A     | $(Q2) \leftarrow (A)$  |
|                              | SST      | $(SIOF) \leftarrow 0$<br>Serial I/O starting              |                          |          |  |
|                              | SNZSI    | $(SIOF) = 1 ?$<br>After skipping<br>$(SIOF) \leftarrow 0$ |                          |          |  |
|                              |          |   | Other operation          | NOP      | $(PC) \leftarrow (PC) + 1$   |
|                              |          |   |                          | POF      | RAM back-up  |
|                              |          |   |                          | EPOF     | POF instruction valid  |
|                              |          |   |                          | SNZP     | $(P) = 1 ?$  |
|                              |          |   |                          | WRST     | $(WDF1) \leftarrow 0, (WEF) \leftarrow 1$  |
|                              |          |   |                          | TAMR     | $(A) \leftarrow (MR)$  |
|                              |          |   |                          | TMRA     | $(MR) \leftarrow (A)$  |
|                              |          |   |                          | TAQ3     | $(A) \leftarrow (Q3)$  |
|                              |          |   |                          | TQ3A     | $(Q33, Q32) \leftarrow (A3, A2)$<br>$(Q31) \leftarrow (CMP1 \text{ com-} \\ \text{parison result})$<br>$(Q30) \leftarrow (CMP0 \text{ com-} \\ \text{parison result})$ |

\*: The 4513 Group does not have these instructions.

# 4513/4514 Group

SINGLE-CHIP 4-BIT CMOS MICROCOMPUTER

**INSTRUCTION CODE TABLE (for 4513 Group)**

| D3-D0 | Hex. notation | D9-D4 |      |       |       |      |      | D3-D0 |       |         |            |           |          | D3-D0 |        |    |       |       |       | 010000 011000 |               |
|-------|---------------|-------|------|-------|-------|------|------|-------|-------|---------|------------|-----------|----------|-------|--------|----|-------|-------|-------|---------------|---------------|
|       |               | 00    | 01   | 02    | 03    | 04   | 05   | 06    | 07    | 08      | 09         | 0A        | 0B       | 0C    | 0D     | 0E | 0F    | 10-17 | 18-1F | 010011 011111 | 011000 011000 |
| 0000  | 0             | NOP   | BLA  | SZB 0 | BMLA  | —    | TASP | A 0   | LA 0  | TABP 0  | TABP 16*** | TABP 32** | TABP 48* | BML   | BML*** | BL | BL*** | BM    | B     |               |               |
| 0001  | 1             | —     | CLD  | SZB 1 | —     | —    | TAD  | A 1   | LA 1  | TABP 1  | TABP 17*** | TABP 33** | TABP 49* | BML   | BML*** | BL | BL*** | BM    | B     |               |               |
| 0010  | 2             | POF   | —    | SZB 2 | —     | —    | TAX  | A 2   | LA 2  | TABP 2  | TABP 18*** | TABP 34** | TABP 50* | BML   | BML*** | BL | BL*** | BM    | B     |               |               |
| 0011  | 3             | SNZP  | INY  | SZB 3 | —     | —    | TAZ  | A 3   | LA 3  | TABP 3  | TABP 19*** | TABP 35** | TABP 51* | BML   | BML*** | BL | BL*** | BM    | B     |               |               |
| 0100  | 4             | DI    | RD   | SZD   | —     | RT   | TAV1 | A 4   | LA 4  | TABP 4  | TABP 20*** | TABP 36** | TABP 52* | BML   | BML*** | BL | BL*** | BM    | B     |               |               |
| 0101  | 5             | EI    | SD   | SEAn  | —     | RTS  | TAV2 | A 5   | LA 5  | TABP 5  | TABP 21*** | TABP 37** | TABP 53* | BML   | BML*** | BL | BL*** | BM    | B     |               |               |
| 0110  | 6             | RC    | —    | SEAM  | —     | RTI  | —    | A 6   | LA 6  | TABP 6  | TABP 22*** | TABP 38** | TABP 54* | BML   | BML*** | BL | BL*** | BM    | B     |               |               |
| 0111  | 7             | SC    | DEY  | —     | —     | —    | —    | A 7   | LA 7  | TABP 7  | TABP 23*** | TABP 39** | TABP 55* | BML   | BML*** | BL | BL*** | BM    | B     |               |               |
| 1000  | 8             | —     | AND  | —     | SNZ0  | LZ 0 | —    | A 8   | LA 8  | TABP 8  | TABP 24*** | TABP 40** | TABP 56* | BML   | BML*** | BL | BL*** | BM    | B     |               |               |
| 1001  | 9             | —     | OR   | TDA   | SNZ1  | LZ 1 | —    | A 9   | LA 9  | TABP 9  | TABP 25*** | TABP 41** | TABP 57* | BML   | BML*** | BL | BL*** | BM    | B     |               |               |
| 1010  | A             | AM    | TEAB | TABE  | SNZI0 | LZ 2 | —    | A 10  | LA 10 | TABP 10 | TABP 26*** | TABP 42** | TABP 58* | BML   | BML*** | BL | BL*** | BM    | B     |               |               |
| 1011  | B             | AMC   | —    | —     | SNZI1 | LZ 3 | EPOF | A 11  | LA 11 | TABP 11 | TABP 27*** | TABP 43** | TABP 59* | BML   | BML*** | BL | BL*** | BM    | B     |               |               |
| 1100  | C             | TYA   | CMA  | —     | —     | RB 0 | SB 0 | A 12  | LA 12 | TABP 12 | TABP 28*** | TABP 44** | TABP 60* | BML   | BML*** | BL | BL*** | BM    | B     |               |               |
| 1101  | D             | —     | RAR  | —     | —     | RB 1 | SB 1 | A 13  | LA 13 | TABP 13 | TABP 29*** | TABP 45** | TABP 61* | BML   | BML*** | BL | BL*** | BM    | B     |               |               |
| 1110  | E             | TBA   | TAB  | —     | TV2A  | RB 2 | SB 2 | A 14  | LA 14 | TABP 14 | TABP 30*** | TABP 46** | TABP 62* | BML   | BML*** | BL | BL*** | BM    | B     |               |               |
| 1111  | F             | —     | TAY  | SZC   | TV1A  | RB 3 | SB 3 | A 15  | LA 15 | TABP 15 | TABP 31*** | TABP 47** | TABP 63* | BML   | BML*** | BL | BL*** | BM    | B     |               |               |

The above table shows the relationship between machine language codes and machine language instructions. D3-D0 show the low-order 4 bits of the machine language code, and D9-D4 show the high-order 6 bits of the machine language code. The hexadecimal representation of the code is also provided. There are one-word instructions and two-word instructions, but only the first word of each instruction is shown. Do not use code marked “—.”

The codes for the second word of a two-word instruction are described below.

|      | The second word |           |
|------|-----------------|-----------|
| BL   | 10              | paaa aaaa |
| BML  | 10              | paaa aaaa |
| BLA  | 10              | pp00 pppp |
| BMLA | 10              | pp00 pppp |
| SEA  | 00              | 0111 nnnn |
| SZD  | 00              | 0010 1011 |

- \*, \*\*, and \*\*\* cannot be used in the M34513M2-XXXSP/FP.
- \* and \*\* cannot be used in the M34513M4-XXXSP/FP.
- \* and \*\* cannot be used in the M34513E4FP.
- \* cannot be used in the M34513M6-XXXFP.

# 4513/4514 Group

## SINGLE-CHIP 4-BIT CMOS MICROCOMPUTER

### INSTRUCTION CODE TABLE (continued) (for 4513 Group)

| D3-D0 | D9-D4            | 100000 | 100001 | 100010 | 100011 | 100100 | 100101 | 100110 | 100111 | 101000 | 101001 | 101010 | 101011    | 101100    | 101101    | 101110     | 101111     | 110000<br>111111 |
|-------|------------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|-----------|-----------|-----------|------------|------------|------------------|
|       | Hex.<br>notation | 20     | 21     | 22     | 23     | 24     | 25     | 26     | 27     | 28     | 29     | 2A     | 2B        | 2C        | 2D        | 2E         | 2F         | 30-3F            |
| 0000  | 0                | –      | TW3A   | OP0A   | T1AB   | –      | TAW6   | IAP0   | TAB1   | SNZT1  | –      | WRST   | TMA<br>0  | TAM<br>0  | XAM<br>0  | XAMI<br>0  | XAMD<br>0  | LXY              |
| 0001  | 1                | –      | TW4A   | OP1A   | T2AB   | –      | –      | IAP1   | TAB2   | SNZT2  | –      | –      | TMA<br>1  | TAM<br>1  | XAM<br>1  | XAMI<br>1  | XAMD<br>1  | LXY              |
| 0010  | 2                | TJ1A   | –      | –      | T3AB   | TAJ1   | TAMR   | IAP2   | TAB3   | SNZT3  | –      | –      | TMA<br>2  | TAM<br>2  | XAM<br>2  | XAMI<br>2  | XAMD<br>2  | LXY              |
| 0011  | 3                | –      | TW6A   | OP3A   | T4AB   | –      | TAI1   | IAP3   | TAB4   | SNZT4  | –      | –      | TMA<br>3  | TAM<br>3  | XAM<br>3  | XAMI<br>3  | XAMD<br>3  | LXY              |
| 0100  | 4                | TQ1A   | –      | –      | –      | TAQ1   | TAI2   | –      | –      | –      | –      | –      | TMA<br>4  | TAM<br>4  | XAM<br>4  | XAMI<br>4  | XAMD<br>4  | LXY              |
| 0101  | 5                | TQ2A   | –      | –      | –      | TAQ2   | –      | –      | –      | –      | –      | –      | TMA<br>5  | TAM<br>5  | XAM<br>5  | XAMI<br>5  | XAMD<br>5  | LXY              |
| 0110  | 6                | TQ3A   | TMRA   | –      | –      | TAQ3   | TAK0   | –      | –      | –      | –      | –      | TMA<br>6  | TAM<br>6  | XAM<br>6  | XAMI<br>6  | XAMD<br>6  | LXY              |
| 0111  | 7                | –      | TI1A   | –      | –      | –      | TAPU0  | –      | –      | SNZAD  | –      | –      | TMA<br>7  | TAM<br>7  | XAM<br>7  | XAMI<br>7  | XAMD<br>7  | LXY              |
| 1000  | 8                | –      | TI2A   | –      | TSIAB  | –      | –      | –      | TABSI  | SNZSI  | –      | –      | TMA<br>8  | TAM<br>8  | XAM<br>8  | XAMI<br>8  | XAMD<br>8  | LXY              |
| 1001  | 9                | –      | –      | –      | TADAB  | TALA   | –      | –      | TABAD  | –      | –      | –      | TMA<br>9  | TAM<br>9  | XAM<br>9  | XAMI<br>9  | XAMD<br>9  | LXY              |
| 1010  | A                | –      | –      | –      | –      | –      | –      | –      | –      | –      | –      | –      | TMA<br>10 | TAM<br>10 | XAM<br>10 | XAMI<br>10 | XAMD<br>10 | LXY              |
| 1011  | B                | –      | TK0A   | –      | TR3AB  | TAW1   | –      | –      | –      | –      | –      | –      | TMA<br>11 | TAM<br>11 | XAM<br>11 | XAMI<br>11 | XAMD<br>11 | LXY              |
| 1100  | C                | –      | –      | –      | –      | TAW2   | –      | –      | –      | –      | –      | –      | TMA<br>12 | TAM<br>12 | XAM<br>12 | XAMI<br>12 | XAMD<br>12 | LXY              |
| 1101  | D                | –      | –      | TPU0A  | –      | TAW3   | –      | –      | –      | –      | –      | –      | TMA<br>13 | TAM<br>13 | XAM<br>13 | XAMI<br>13 | XAMD<br>13 | LXY              |
| 1110  | E                | TW1A   | –      | –      | –      | TAW4   | –      | –      | –      | –      | SST    | –      | TMA<br>14 | TAM<br>14 | XAM<br>14 | XAMI<br>14 | XAMD<br>14 | LXY              |
| 1111  | F                | TW2A   | –      | –      | TR1AB  | –      | –      | –      | –      | –      | ADST   | –      | TMA<br>15 | TAM<br>15 | XAM<br>15 | XAMI<br>15 | XAMD<br>15 | LXY              |

The above table shows the relationship between machine language codes and machine language instructions. D3-D0 show the low-order 4 bits of the machine language code, and D9-D4 show the high-order 6 bits of the machine language code. The hexadecimal representation of the code is also provided. There are one-word instructions and two-word instructions, but only the first word of each instruction is shown. Do not use code marked "-."

The codes for the second word of a two-word instruction are described below.

|      | The second word |      |      |
|------|-----------------|------|------|
| BL   | 10              | paaa | aaaa |
| BML  | 10              | paaa | aaaa |
| BLA  | 10              | pp00 | pppp |
| BMLA | 10              | pp00 | pppp |
| SEA  | 00              | 0111 | nnnn |
| SZD  | 00              | 0010 | 1011 |

# 4513/4514 Group

## SINGLE-CHIP 4-BIT CMOS MICROCOMPUTER

### INSTRUCTION CODE TABLE (for 4514 Group)

| D3-D0 | Hex.<br>notation | D9-D4 |      |          |       |         |         |         |          |            |            |            |             |     |     |    |    | 010000 011000 |       |
|-------|------------------|-------|------|----------|-------|---------|---------|---------|----------|------------|------------|------------|-------------|-----|-----|----|----|---------------|-------|
|       |                  | 00    | 01   | 02       | 03    | 04      | 05      | 06      | 07       | 08         | 09         | 0A         | 0B          | 0C  | 0D  | 0E | 0F | 10-17         | 18-1F |
| 0000  | 0                | NOP   | BLA  | SZB<br>0 | BMLA  | —       | TASP    | A<br>0  | LA<br>0  | TABP<br>0  | TABP<br>16 | TABP<br>32 | TABP<br>48* | BML | BML | BL | BL | BM            | B     |
| 0001  | 1                | —     | CLD  | SZB<br>1 | —     | —       | TAD     | A<br>1  | LA<br>1  | TABP<br>1  | TABP<br>17 | TABP<br>33 | TABP<br>49* | BML | BML | BL | BL | BM            | B     |
| 0010  | 2                | POF   | —    | SZB<br>2 | —     | —       | TAX     | A<br>2  | LA<br>2  | TABP<br>2  | TABP<br>18 | TABP<br>34 | TABP<br>50* | BML | BML | BL | BL | BM            | B     |
| 0011  | 3                | SNZP  | INY  | SZB<br>3 | —     | —       | TAZ     | A<br>3  | LA<br>3  | TABP<br>3  | TABP<br>19 | TABP<br>35 | TABP<br>51* | BML | BML | BL | BL | BM            | B     |
| 0100  | 4                | DI    | RD   | SZD      | —     | RT      | TAV1    | A<br>4  | LA<br>4  | TABP<br>4  | TABP<br>20 | TABP<br>36 | TABP<br>52* | BML | BML | BL | BL | BM            | B     |
| 0101  | 5                | EI    | SD   | SEAn     | —     | RTS     | TAV2    | A<br>5  | LA<br>5  | TABP<br>5  | TABP<br>21 | TABP<br>37 | TABP<br>53* | BML | BML | BL | BL | BM            | B     |
| 0110  | 6                | RC    | —    | SEAM     | —     | RTI     | —       | A<br>6  | LA<br>6  | TABP<br>6  | TABP<br>22 | TABP<br>38 | TABP<br>54* | BML | BML | BL | BL | BM            | B     |
| 0111  | 7                | SC    | DEY  | —        | —     | —       | —       | A<br>7  | LA<br>7  | TABP<br>7  | TABP<br>23 | TABP<br>39 | TABP<br>55* | BML | BML | BL | BL | BM            | B     |
| 1000  | 8                | —     | AND  | —        | SNZ0  | LZ<br>0 | —       | A<br>8  | LA<br>8  | TABP<br>8  | TABP<br>24 | TABP<br>40 | TABP<br>56* | BML | BML | BL | BL | BM            | B     |
| 1001  | 9                | —     | OR   | TDA      | SNZ1  | LZ<br>1 | —       | A<br>9  | LA<br>9  | TABP<br>9  | TABP<br>25 | TABP<br>41 | TABP<br>57* | BML | BML | BL | BL | BM            | B     |
| 1010  | A                | AM    | TEAB | TABE     | SNZI0 | LZ<br>2 | —       | A<br>10 | LA<br>10 | TABP<br>10 | TABP<br>26 | TABP<br>42 | TABP<br>58* | BML | BML | BL | BL | BM            | B     |
| 1011  | B                | AMC   | —    | —        | SNZI1 | LZ<br>3 | EPOF    | A<br>11 | LA<br>11 | TABP<br>11 | TABP<br>27 | TABP<br>43 | TABP<br>59* | BML | BML | BL | BL | BM            | B     |
| 1100  | C                | TYA   | CMA  | —        | —     | RB<br>0 | SB<br>0 | A<br>12 | LA<br>12 | TABP<br>12 | TABP<br>28 | TABP<br>44 | TABP<br>60* | BML | BML | BL | BL | BM            | B     |
| 1101  | D                | —     | RAR  | —        | —     | RB<br>1 | SB<br>1 | A<br>13 | LA<br>13 | TABP<br>13 | TABP<br>29 | TABP<br>45 | TABP<br>61* | BML | BML | BL | BL | BM            | B     |
| 1110  | E                | TBA   | TAB  | —        | TV2A  | RB<br>2 | SB<br>2 | A<br>14 | LA<br>14 | TABP<br>14 | TABP<br>30 | TABP<br>46 | TABP<br>62* | BML | BML | BL | BL | BM            | B     |
| 1111  | F                | —     | TAY  | SZC      | TV1A  | RB<br>3 | SB<br>3 | A<br>15 | LA<br>15 | TABP<br>15 | TABP<br>31 | TABP<br>47 | TABP<br>63* | BML | BML | BL | BL | BM            | B     |

The above table shows the relationship between machine language codes and machine language instructions. D3-D0 show the low-order 4 bits of the machine language code, and D9-D4 show the high-order 6 bits of the machine language code. The hexadecimal representation of the code is also provided. There are one-word instructions and two-word instructions, but only the first word of each instruction is shown. Do not use code marked "—."

The codes for the second word of a two-word instruction are described below.

|      | The second word |      |      |
|------|-----------------|------|------|
| BL   | 10              | paaa | aaaa |
| BML  | 10              | paaa | aaaa |
| BLA  | 10              | pp00 | pppp |
| BMLA | 10              | pp00 | pppp |
| SEA  | 00              | 0111 | nnnn |
| SZD  | 00              | 0010 | 1011 |

• \* cannot be used in the M34514M6-XXXXP.

# 4513/4514 Group

SINGLE-CHIP 4-BIT CMOS MICROCOMPUTER

## INSTRUCTION CODE TABLE (continued) (for 4514 Group)

| D3—D0 | D9—D4            | 100000 | 100001 | 100010 | 100011 | 100100 | 100101 | 100110 | 100111 | 101000 | 101001 | 101010 | 101011 | 101100 | 101101 | 101110 | 101111 | 110000 |
|-------|------------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
|       | Hex.<br>notation | 20     | 21     | 22     | 23     | 24     | 25     | 26     | 27     | 28     | 29     | 2A     | 2B     | 2C     | 2D     | 2E     | 2F     | 111111 |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       |                  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |

The above table shows the relationship between machine language codes and machine language instructions. D3-D0 show the low-order 4 bits of the machine language code, and D9-D4 show the high-order 6 bits of the machine language code. The hexadecimal representation of the code is also provided. There are one-word instructions and two-word instructions, but only the first word of each instruction is shown. Do not use code marked "-."

The codes for the second word of a two-word instruction are described below.

| The second word |    |      |      |
|-----------------|----|------|------|
| BL              | 10 | paaa | aaaa |
| BML             | 10 | paaa | aaaa |
| BLA             | 10 | pp00 | pppp |
| BMLA            | 10 | pp00 | pppp |
| SEA             | 00 | 0111 | nnnn |
| SZD             | 00 | 0010 | 1011 |

# MACHINE INSTRUCTIONS

| Parameter<br><br>Type of instructions | Mnemonic | Instruction code |    |    |    |    |    |    |    |    |    |                      | Number of words | Number of cycles | Function  |
|---------------------------------------|----------|------------------|----|----|----|----|----|----|----|----|----|----------------------|-----------------|------------------|---|
|                                       |          | D9               | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hexadecimal notation |                 |                  |   |
| Register to register transfer         | TAB      | 0                | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 0  | 0 1 E                | 1               | 1                | (A) ← (B)   |
|                                       | TBA      | 0                | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 0 0 E                | 1               | 1                | (B) ← (A)   |
|                                       | TAY      | 0                | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 0 1 F                | 1               | 1                | (A) ← (Y)   |
|                                       | TYA      | 0                | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0 0 C                | 1               | 1                | (Y) ← (A)   |
|                                       | TEAB     | 0                | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0  | 0 1 A                | 1               | 1                | (E7–E4) ← (B)<br>(E3–E0) ← (A)                                      |
|                                       | TABE     | 0                | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 0 2 A                | 1               | 1                | (B) ← (E7–E4)<br>(A) ← (E3–E0)                                      |
|                                       | TDA      | 0                | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 0 2 9                | 1               | 1                | (DR2–DR0) ← (A2–A0)   |
|                                       | TAD      | 0                | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 0  | 1  | 0 5 1                | 1               | 1                | (A2–A0) ← (DR2–DR0)<br>(A3) ← 0                                     |
|                                       | TAZ      | 0                | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 1  | 0 5 3                | 1               | 1                | (A1, A0) ← (Z1, Z0)<br>(A3, A2) ← 0                                 |
|                                       | TAX      | 0                | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 0  | 0 5 2                | 1               | 1                | (A) ← (X)   |
|                                       | TASP     | 0                | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 0  | 0  | 0 5 0                | 1               | 1                | (A2–A0) ← (SP2–SP0)<br>(A3) ← 0                                     |
| RAM addresses                         | LXY x, y | 1                | 1  | x3 | x2 | x1 | x0 | y3 | y2 | y1 | y0 | 3 x y                | 1               | 1                | (X) ← x, x = 0 to 15<br>(Y) ← y, y = 0 to 15                        |
|                                       | LZ z     | 0                | 0  | 0  | 1  | 0  | 0  | 1  | 0  | z1 | z0 | 0 4 8<br>+z          | 1               | 1                | (Z) ← z, z = 0 to 3   |
|                                       | INY      | 0                | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 1  | 0 1 3                | 1               | 1                | (Y) ← (Y) + 1   |
|                                       | DEY      | 0                | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 1  | 1  | 0 1 7                | 1               | 1                | (Y) ← (Y) – 1   |
| RAM to register transfer              | TAM j    | 1                | 0  | 1  | 1  | 0  | 0  | j  | j  | j  | j  | 2 C j                | 1               | 1                | (A) ← (M(DP))<br>(X) ← (X)EXOR(j)<br>j = 0 to 15                    |
|                                       | XAM j    | 1                | 0  | 1  | 1  | 0  | 1  | j  | j  | j  | j  | 2 D j                | 1               | 1                | (A) ← → (M(DP))<br>(X) ← (X)EXOR(j)<br>j = 0 to 15                  |
|                                       | XAMD j   | 1                | 0  | 1  | 1  | 1  | 1  | j  | j  | j  | j  | 2 F j                | 1               | 1                | (A) ← → (M(DP))<br>(X) ← (X)EXOR(j)<br>j = 0 to 15<br>(Y) ← (Y) – 1 |
|                                       | XAMI j   | 1                | 0  | 1  | 1  | 1  | 0  | j  | j  | j  | j  | 2 E j                | 1               | 1                | (A) ← → (M(DP))<br>(X) ← (X)EXOR(j)<br>j = 0 to 15<br>(Y) ← (Y) + 1 |
|                                       | TMA j    | 1                | 0  | 1  | 0  | 1  | 1  | j  | j  | j  | j  | 2 B j                | 1               | 1                | (M(DP)) ← (A)<br>(X) ← (X)EXOR(j)<br>j = 0 to 15                    |

| Skip condition         | Carry flag CY | Detailed description  |
|------------------------|---------------|---|
| –                      | –             | Transfers the contents of register B to register A.   |
| –                      | –             | Transfers the contents of register A to register B.   |
| –                      | –             | Transfers the contents of register Y to register A.   |
| –                      | –             | Transfers the contents of register A to register Y.   |
| –                      | –             | Transfers the contents of registers A and B to register E.  |
| –                      | –             | Transfers the contents of register E to registers A and B.  |
| –                      | –             | Transfers the contents of register A to register D.   |
| –                      | –             | Transfers the contents of register D to register A.   |
| –                      | –             | Transfers the contents of register Z to register A.   |
| –                      | –             | Transfers the contents of register X to register A.   |
| –                      | –             | Transfers the contents of stack pointer (SP) to register A.   |
| Continuous description | –             | Loads the value x in the immediate field to register X, and the value y in the immediate field to register Y. When the LXY instructions are continuously coded and executed, only the first LXY instruction is executed and other LXY instructions coded continuously are skipped.  |
| –                      | –             | Loads the value z in the immediate field to register Z.   |
| (Y) = 0                | –             | Adds 1 to the contents of register Y. As a result of addition, when the contents of register Y is 0, the next instruction is skipped.   |
| (Y) = 15               | –             | Subtracts 1 from the contents of register Y. As a result of subtraction, when the contents of register Y is 15, the next instruction is skipped.  |
| –                      | –             | After transferring the contents of M(DP) to register A, an exclusive OR operation is performed between register X and the value j in the immediate field, and stores the result in register X.  |
| –                      | –             | After exchanging the contents of M(DP) with the contents of register A, an exclusive OR operation is performed between register X and the value j in the immediate field, and stores the result in register X.  |
| (Y) = 15               | –             | After exchanging the contents of M(DP) with the contents of register A, an exclusive OR operation is performed between register X and the value j in the immediate field, and stores the result in register X. Subtracts 1 from the contents of register Y. As a result of subtraction, when the contents of register Y is 15, the next instruction is skipped. |
| (Y) = 0                | –             | After exchanging the contents of M(DP) with the contents of register A, an exclusive OR operation is performed between register X and the value j in the immediate field, and stores the result in register X. Adds 1 to the contents of register Y. As a result of addition, when the contents of register Y is 0, the next instruction is skipped.            |
| –                      | –             | After transferring the contents of register A to M(DP), an exclusive OR operation is performed between register X and the value j in the immediate field, and stores the result in register X.  |



# MACHINE INSTRUCTIONS (continued)

| Parameter<br><br>Type of instructions | Mnemonic | Instruction code |    |    |    |    |    |    |    |    |    |                      | Number of words | Number of cycles | Function   |
|---------------------------------------|----------|------------------|----|----|----|----|----|----|----|----|----|----------------------|-----------------|------------------|--|
|                                       |          | D9               | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hexadecimal notation |                 |                  |  |
| Arithmetic operation                  | LA n     | 0                | 0  | 0  | 1  | 1  | 1  | n  | n  | n  | n  | 0 7 n                | 1               | 1                | (A) ← n<br>n = 0 to 15   |
|                                       | TABP p   | 0                | 0  | 1  | 0  | p5 | p4 | p3 | p2 | p1 | p0 | 0 8 p<br>+p          | 1               | 3                | (SP) ← (SP) + 1<br>(SK(SP)) ← (PC)<br>(PCH) ← p<br>(PCL) ← (DR2–DR0, A3–A0)<br>(B) ← (ROM(PC))7–4<br>(A) ← (ROM(PC))3–0<br>(PC) ← (SK(SP))<br>(SP) ← (SP) – 1 (Note) |
|                                       | AM       | 0                | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 0 0 A                | 1               | 1                | (A) ← (A) + (M(DP))  |
|                                       | AMC      | 0                | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 1  | 0 0 B                | 1               | 1                | (A) ← (A) + (M(DP)) +(CY)<br>(CY) ← Carry  |
|                                       | A n      | 0                | 0  | 0  | 1  | 1  | 0  | n  | n  | n  | n  | 0 6 n                | 1               | 1                | (A) ← (A) + n<br>n = 0 to 15   |
|                                       | AND      | 0                | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 0 1 8                | 1               | 1                | (A) ← (A) AND (M(DP))  |
|                                       | OR       | 0                | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 0 1 9                | 1               | 1                | (A) ← (A) OR (M(DP))   |
|                                       | SC       | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 0 0 7                | 1               | 1                | (CY) ← 1   |
|                                       | RC       | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0 0 6                | 1               | 1                | (CY) ← 0   |
|                                       | SZC      | 0                | 0  | 0  | 0  | 1  | 0  | 1  | 1  | 1  | 1  | 0 2 F                | 1               | 1                | (CY) = 0 ?   |
|                                       | CMA      | 0                | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 0 1 C                | 1               | 1                | (A) ← (A̅)   |
|                                       | RAR      | 0                | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 1  | 0 1 D                | 1               | 1                | <div><div>→CY→</div><div>A3A2A1A0</div><div>←</div></div>  |
| Bit operation                         | SB j     | 0                | 0  | 0  | 1  | 0  | 1  | 1  | 1  | j  | j  | 0 5 C<br>+j          | 1               | 1                | (Mj(DP)) ← 1<br>j = 0 to 3   |
|                                       | RB j     | 0                | 0  | 0  | 1  | 0  | 0  | 1  | 1  | j  | j  | 0 4 C<br>+j          | 1               | 1                | (Mj(DP)) ← 0<br>j = 0 to 3   |
|                                       | SZB j    | 0                | 0  | 0  | 0  | 1  | 0  | 0  | 0  | j  | j  | 0 2 j                | 1               | 1                | (Mj(DP)) = 0 ?<br>j = 0 to 3   |
| Comparison operation                  | SEAM     | 0                | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 1  | 0  | 0 2 6                | 1               | 1                | (A) = (M(DP)) ?  |
|                                       | SEA n    | 0                | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 0 2 5                | 2               | 2                | (A) = n ?<br>n = 0 to 15   |
|                                       |          | 0                | 0  | 0  | 1  | 1  | 1  | n  | n  | n  | n  | 0 7 n                |                 |                  |  |

Note : p is 0 to 15 for M34513M2, p is 0 to 31 for M34513M4/E4, p is 0 to 47 for M34513M6 and M34514M6, and p is 0 to 63 for M34513M8/E8 and M34514M8/E8.

| Skip condition             | Carry flag CY | Detailed description  |
|----------------------------|---------------|---|
| Continuous description     | –             | Loads the value n in the immediate field to register A.<br>When the LA instructions are continuously coded and executed, only the first LA instruction is executed and other LA instructions coded continuously are skipped.  |
| –                          | –             | Transfers bits 7 to 4 to register B and bits 3 to 0 to register A. These bits 7 to 0 are the ROM pattern in address (DR2 DR1 DR0 A3 A2 A1 A0) <sub>2</sub> specified by registers A and D in page p.<br>When this instruction is executed, 1 stage of stack register is used. |
| –                          | –             | Adds the contents of M(DP) to register A. Stores the result in register A. The contents of carry flag CY remains unchanged.   |
| –                          | 0/1           | Adds the contents of M(DP) and carry flag CY to register A. Stores the result in register A and carry flag CY.  |
| Overflow = 0               | –             | Adds the value n in the immediate field to register A.<br>The contents of carry flag CY remains unchanged.<br>Skips the next instruction when there is no overflow as the result of operation.  |
| –                          | –             | Takes the AND operation between the contents of register A and the contents of M(DP), and stores the result in register A.  |
| –                          | –             | Takes the OR operation between the contents of register A and the contents of M(DP), and stores the result in register A.   |
| –                          | 1             | Sets (1) to carry flag CY.  |
| –                          | 0             | Clears (0) to carry flag CY.  |
| (CY) = 0                   | –             | Skips the next instruction when the contents of carry flag CY is "0."   |
| –                          | –             | Stores the one's complement for register A's contents in register A.  |
| –                          | 0/1           | Rotates 1 bit of the contents of register A including the contents of carry flag CY to the right.   |
| –                          | –             | Sets (1) the contents of bit j (bit specified by the value j in the immediate field) of M(DP).  |
| –                          | –             | Clears (0) the contents of bit j (bit specified by the value j in the immediate field) of M(DP).  |
| (Mj(DP)) = 0<br>j = 0 to 3 | –             | Skips the next instruction when the contents of bit j (bit specified by the value j in the immediate field) of M(DP) is "0."  |
| (A) = (M(DP))              | –             | Skips the next instruction when the contents of register A is equal to the contents of M(DP).   |
| (A) = n                    | –             | Skips the next instruction when the contents of register A is equal to the value n in the immediate field.  |

MACHINE INSTRUCTIONS (continued)

| Parameter<br><br>Type of instructions | Mnemonic | Instruction code |    |    |    |    |    |    |    |    |    |                      | Number of words | Number of cycles | Function   |
|---------------------------------------|----------|------------------|----|----|----|----|----|----|----|----|----|----------------------|-----------------|------------------|--|
|                                       |          | D9               | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hexadecimal notation |                 |                  |  |
| Branch operation                      | B a      | 0                | 1  | 1  | a6 | a5 | a4 | a3 | a2 | a1 | a0 | 1 8 a +a             | 1               | 1                | (PCL) ← a6–a0  |
|                                       | BL p, a  | 0                | 0  | 1  | 1  | 1  | p4 | p3 | p2 | p1 | p0 | 0 E p +p             | 2               | 2                | (PCH) ← p<br>(PCL) ← a6–a0<br>(Note)   |
|                                       |          | 1                | 0  | p5 | a6 | a5 | a4 | a3 | a2 | a1 | a0 | 2 p a +a             |                 |                  |  |
|                                       | BLA p    | 0                | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0 1 0                | 2               | 2                | (PCH) ← p<br>(PCL) ← (DR2–DR0, A3–A0)<br>(Note)                                      |
|                                       |          | 1                | 0  | p5 | p4 | 0  | 0  | p3 | p2 | p1 | p0 | 2 p p                |                 |                  |  |
| Subroutine operation                  | BM a     | 0                | 1  | 0  | a6 | a5 | a4 | a3 | a2 | a1 | a0 | 1 a a                | 1               | 1                | (SP) ← (SP) + 1<br>(SK(SP)) ← (PC)<br>(PCH) ← 2<br>(PCL) ← a6–a0                     |
|                                       | BML p, a | 0                | 0  | 1  | 1  | 0  | p4 | p3 | p2 | p1 | p0 | 0 C p +p             | 2               | 2                | (SP) ← (SP) + 1<br>(SK(SP)) ← (PC)<br>(PCH) ← p<br>(PCL) ← a6–a0<br>(Note)           |
|                                       |          | 1                | 0  | p5 | a6 | a5 | a4 | a3 | a2 | a1 | a0 | 2 p a +a             |                 |                  |  |
|                                       | BMLA p   | 0                | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 0 3 0                | 2               | 2                | (SP) ← (SP) + 1<br>(SK(SP)) ← (PC)<br>(PCH) ← p<br>(PCL) ← (DR2–DR0,A3–A0)<br>(Note) |
|                                       |          | 1                | 0  | p5 | p4 | 0  | 0  | p3 | p2 | p1 | p0 | 2 p p                |                 |                  |  |
| Return operation                      | RTI      | 0                | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 1  | 0  | 0 4 6                | 1               | 1                | (PC) ← (SK(SP))<br>(SP) ← (SP) – 1   |
|                                       | RT       | 0                | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 0  | 0  | 0 4 4                | 1               | 2                | (PC) ← (SK(SP))<br>(SP) ← (SP) – 1   |
|                                       | RTS      | 0                | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 0  | 1  | 0 4 5                | 1               | 2                | (PC) ← (SK(SP))<br>(SP) ← (SP) – 1   |
| Interrupt operation                   | DI       | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0 0 4                | 1               | 1                | (INTE) ← 0   |
|                                       | EI       | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0 0 5                | 1               | 1                | (INTE) ← 1   |
|                                       | SNZ0     | 0                | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 0  | 0 3 8                | 1               | 1                | (EXF0) = 1 ?<br>After skipping<br>(EXF0) ← 0   |
|                                       | SNZ1     | 0                | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 1  | 0 3 9                | 1               | 1                | (EXF1) = 1 ?<br>After skipping<br>(EXF1) ← 0   |

Note : p is 0 to 15 for M34513M2, p is 0 to 31 for M34513M4/E4, p is 0 to 47 for M34513M6 and M34514M6, and p is 0 to 63 for M34513M8/E8 and M34514M8/E8.

| Skip condition      | Carry flag CY | Detailed description  |
|---------------------|---------------|---|
| –                   | –             | Branch within a page : Branches to address a in the identical page.   |
| –                   | –             | Branch out of a page : Branches to address a in page p.   |
| –                   | –             | Branch out of a page : Branches to address (DR2 DR1 DR0 A3 A2 A1 A0) <sub>2</sub> specified by registers D and A in page p.   |
| –                   | –             | Call the subroutine in page 2 : Calls the subroutine at address a in page 2.  |
| –                   | –             | Call the subroutine : Calls the subroutine at address a in page p.  |
| –                   | –             | Call the subroutine : Calls the subroutine at address (DR2 DR1 DR0 A3 A2 A1 A0) <sub>2</sub> specified by registers D and A in page p.  |
| –                   | –             | Returns from interrupt service routine to main routine.<br>Returns each value of data pointer (X, Y, Z), carry flag, skip status, NOP mode status by the continuous description of the LA/LXY instruction, register A and register B to the states just before interrupt. |
| –                   | –             | Returns from subroutine to the routine called the subroutine.   |
| Skip at uncondition | –             | Returns from subroutine to the routine called the subroutine, and skips the next instruction at uncondition.  |
| –                   | –             | Clears (0) to the interrupt enable flag INTE, and disables the interrupt.   |
| –                   | –             | Sets (1) to the interrupt enable flag INTE, and enables the interrupt.  |
| (EXF0) = 1          | –             | Skips the next instruction when the contents of EXF0 flag is "1."<br>After skipping, clears (0) to the EXF0 flag.   |
| (EXF1) = 1          | –             | Skips the next instruction when the contents of EXF1 flag is "1."<br>After skipping, clears (0) to the EXF1 flag.   |

**MACHINE INSTRUCTIONS (continued)**

| Parameter<br><br>Type of instructions | Mnemonic | Instruction code |    |    |    |    |    |    |    |    |    |                      | Number of words | Number of cycles | Function   |
|---------------------------------------|----------|------------------|----|----|----|----|----|----|----|----|----|----------------------|-----------------|------------------|--|
|                                       |          | D9               | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hexadecimal notation |                 |                  |  |
| Interrupt operation                   | SNZI0    | 0                | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 1  | 0  | 0 3 A                | 1               | 1                | I12 = 1 : (INT0) = “H” ?<br><br>I12 = 0 : (INT0) = “L” ? |
|                                       | SNZI1    | 0                | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 0 3 B                | 1               | 1                | I22 = 1 : (INT1) = “H” ?<br><br>I22 = 0 : (INT1) = “L” ? |
|                                       | TAV1     | 0                | 0  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 0  | 0 5 4                | 1               | 1                | (A) ← (V1)   |
|                                       | TV1A     | 0                | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 0 3 F                | 1               | 1                | (V1) ← (A)   |
|                                       | TAV2     | 0                | 0  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 0 5 5                | 1               | 1                | (A) ← (V2)   |
|                                       | TV2A     | 0                | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 0 3 E                | 1               | 1                | (V2) ← (A)   |
|                                       | TAI1     | 1                | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 1  | 2 5 3                | 1               | 1                | (A) ← (I1)   |
|                                       | TI1A     | 1                | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 1  | 1  | 2 1 7                | 1               | 1                | (I1) ← (A)   |
|                                       | TAI2     | 1                | 0  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 0  | 2 5 4                | 1               | 1                | (A) ← (I2)   |
|                                       | TI2A     | 1                | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 2 1 8                | 1               | 1                | (I2) ← (A)   |
| Timer operation                       | TAW1     | 1                | 0  | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 1  | 2 4 B                | 1               | 1                | (A) ← (W1)   |
|                                       | TW1A     | 1                | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 2 0 E                | 1               | 1                | (W1) ← (A)   |
|                                       | TAW2     | 1                | 0  | 0  | 1  | 0  | 0  | 1  | 1  | 0  | 0  | 2 4 C                | 1               | 1                | (A) ← (W2)   |
|                                       | TW2A     | 1                | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 2 0 F                | 1               | 1                | (W2) ← (A)   |
|                                       | TAW3     | 1                | 0  | 0  | 1  | 0  | 0  | 1  | 1  | 0  | 1  | 2 4 D                | 1               | 1                | (A) ← (W3)   |
|                                       | TW3A     | 1                | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 2 1 0                | 1               | 1                | (W3) ← (A)   |
|                                       | TAW4     | 1                | 0  | 0  | 1  | 0  | 0  | 1  | 1  | 1  | 0  | 2 4 E                | 1               | 1                | (A) ← (W4)   |
|                                       | TW4A     | 1                | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 2 1 1                | 1               | 1                | (W4) ← (A)   |
|                                       | TAW6     | 1                | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 0  | 0  | 2 5 0                | 1               | 1                | (A) ← (W6)   |
|                                       | TW6A     | 1                | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 1  | 2 1 3                | 1               | 1                | (W6) ← (A)   |

| Skip condition                   | Carry flag CY | Detailed description   |
|----------------------------------|---------------|--|
| (INT0) = "H"<br>However, I12 = 1 | –             | When bit 2 (I12) of register I1 is "1" : Skips the next instruction when the level of INT0 pin is "H." |
| (INT0) = "L"<br>However, I12 = 0 | –             | When bit 2 (I12) of register I1 is "0" : Skips the next instruction when the level of INT0 pin is "L." |
| (INT1) = "H"<br>However, I22 = 1 | –             | When bit 2 (I22) of register I2 is "1" : Skips the next instruction when the level of INT1 pin is "H." |
| (INT1) = "L"<br>However, I22 = 0 | –             | When bit 2 (I22) of register I2 is "0" : Skips the next instruction when the level of INT1 pin is "L." |
| –                                | –             | Transfers the contents of interrupt control register V1 to register A.                                 |
| –                                | –             | Transfers the contents of register A to interrupt control register V1.                                 |
| –                                | –             | Transfers the contents of interrupt control register V2 to register A.                                 |
| –                                | –             | Transfers the contents of register A to interrupt control register V2.                                 |
| –                                | –             | Transfers the contents of interrupt control register I1 to register A.                                 |
| –                                | –             | Transfers the contents of register A to interrupt control register I1.                                 |
| –                                | –             | Transfers the contents of interrupt control register I2 to register A.                                 |
| –                                | –             | Transfers the contents of register A to interrupt control register I2.                                 |
| –                                | –             | Transfers the contents of timer control register W1 to register A.                                     |
| –                                | –             | Transfers the contents of register A to timer control register W1.                                     |
| –                                | –             | Transfers the contents of timer control register W2 to register A.                                     |
| –                                | –             | Transfers the contents of register A to timer control register W2.                                     |
| –                                | –             | Transfers the contents of timer control register W3 to register A.                                     |
| –                                | –             | Transfers the contents of register A to timer control register W3.                                     |
| –                                | –             | Transfers the contents of timer control register W4 to register A.                                     |
| –                                | –             | Transfers the contents of register A to timer control register W4.                                     |
| –                                | –             | Transfers the contents of timer control register W6 to register A.                                     |
| –                                | –             | Transfers the contents of register A to timer control register W6.                                     |

## MACHINE INSTRUCTIONS (continued)

| Parameter<br><br>Type of instructions | Mnemonic | Instruction code |    |    |    |    |    |    |    |    |    |                      | Number of words | Number of cycles | Function   |
|---------------------------------------|----------|------------------|----|----|----|----|----|----|----|----|----|----------------------|-----------------|------------------|--|
|                                       |          | D9               | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hexadecimal notation |                 |                  |  |
| Timer operation                       | TAB1     | 1                | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 0  | 0  | 2 7 0                | 1               | 1                | (B) ← (T17–T14)<br>(A) ← (T13–T10)                                       |
|                                       | T1AB     | 1                | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 2 3 0                | 1               | 1                | (R17–R14) ← (B)<br>(T17–T14) ← (B)<br>(R13–R10) ← (A)<br>(T13–T10) ← (A) |
|                                       | TAB2     | 1                | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 0  | 1  | 2 7 1                | 1               | 1                | (B) ← (T27–T24)<br>(A) ← (T23–T20)                                       |
|                                       | T2AB     | 1                | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 1  | 2 3 1                | 1               | 1                | (R27–R24) ← (B)<br>(T27–T24) ← (B)<br>(R23–R20) ← (A)<br>(T23–T20) ← (A) |
|                                       | TAB3     | 1                | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 1  | 0  | 2 7 2                | 1               | 1                | (B) ← (T37–T34)<br>(A) ← (T33–T30)                                       |
|                                       | T3AB     | 1                | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 0  | 2 3 2                | 1               | 1                | (R37–R34) ← (B)<br>(T37–T34) ← (B)<br>(R33–R30) ← (A)<br>(T33–T30) ← (A) |
|                                       | TAB4     | 1                | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 1  | 1  | 2 7 3                | 1               | 1                | (B) ← (T47–T44)<br>(A) ← (T43–T40)                                       |
|                                       | T4AB     | 1                | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 1  | 2 3 3                | 1               | 1                | (R47–R44) ← (B)<br>(T47–T44) ← (B)<br>(R43–R40) ← (A)<br>(T43–T40) ← (A) |
|                                       | TR1AB    | 1                | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 2 3 F                | 1               | 1                | (R17–R14) ← (B)<br>(R13–R10) ← (A)                                       |
|                                       | TR3AB    | 1                | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 2 3 B                | 1               | 1                | (R37–R34) ← (B)<br>(R33–R30) ← (A)                                       |
|                                       | SNZT1    | 1                | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 2 8 0                | 1               | 1                | (T1F) = 1 ?<br>After skipping<br>(T1F) ← 0                               |
|                                       | SNZT2    | 1                | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 2 8 1                | 1               | 1                | (T2F) = 1 ?<br>After skipping<br>(T2F) ← 0                               |
|                                       | SNZT3    | 1                | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 2 8 2                | 1               | 1                | (T3F) = 1 ?<br>After skipping<br>(T3F) ← 0                               |
|                                       | SNZT4    | 1                | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 2 8 3                | 1               | 1                | (T4F) = 1 ?<br>After skipping<br>(T4F) ← 0                               |

| Skip condition | Carry flag CY | Detailed description  |
|----------------|---------------|---|
| –              | –             | Transfers the contents of timer 1 to registers A and B.   |
| –              | –             | Transfers the contents of registers A and B to timer 1 and timer 1 reload register.                         |
| –              | –             | Transfers the contents of timer 2 to registers A and B.   |
| –              | –             | Transfers the contents of registers A and B to timer 2 and timer 2 reload register.                         |
| –              | –             | Transfers the contents of timer 3 to registers A and B.   |
| –              | –             | Transfers the contents of registers A and B to timer 3 and timer 3 reload register.                         |
| –              | –             | Transfers the contents of timer 4 to registers A and B.   |
| –              | –             | Transfers the contents of registers A and B to timer 4 and timer 4 reload register.                         |
| –              | –             | Transfers the contents of registers A and B to timer 1 reload register.                                     |
| –              | –             | Transfers the contents of registers A and B to timer 3 reload register.                                     |
| (T1F) = 1      | –             | Skips the next instruction when the contents of T1F flag is "1."<br>After skipping, clears (0) to T1F flag. |
| (T2F) = 1      | –             | Skips the next instruction when the contents of T2F flag is "1."<br>After skipping, clears (0) to T2F flag. |
| (T3F) = 1      | –             | Skips the next instruction when the contents of T3F flag is "1."<br>After skipping, clears (0) to T3F flag. |
| (T4F) = 1      | –             | Skips the next instruction when the contents of T4F flag is "1."<br>After skipping, clears (0) to T4F flag. |



## MACHINE INSTRUCTIONS (continued)

| Parameter<br><br>Type of instructions | Mnemonic | Instruction code |    |    |    |    |    |    |    |    |    |                      | Number of words | Number of cycles | Function                        |
|---------------------------------------|----------|------------------|----|----|----|----|----|----|----|----|----|----------------------|-----------------|------------------|---------------------------------|
|                                       |          | D9               | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hexadecimal notation |                 |                  |                                 |
| Input/Output operation                | IAP0     | 1                | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 2 6 0                | 1               | 1                | (A) ← (P0)                      |
|                                       | OP0A     | 1                | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 2 2 0                | 1               | 1                | (P0) ← (A)                      |
|                                       | IAP1     | 1                | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 1  | 2 6 1                | 1               | 1                | (A) ← (P1)                      |
|                                       | OP1A     | 1                | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 1  | 2 2 1                | 1               | 1                | (P1) ← (A)                      |
|                                       | IAP2     | 1                | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 1  | 0  | 2 6 2                | 1               | 1                | (A2–A0) ← (P22–P20)<br>(A3) ← 0 |
|                                       | IAP3     | 1                | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 1  | 1  | 2 6 3                | 1               | 1                | (A) ← (P3)                      |
|                                       | OP3A     | 1                | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 1  | 2 2 3                | 1               | 1                | (P3) ← (A)                      |
|                                       | IAP4*    | 1                | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 0  | 0  | 2 6 4                | 1               | 1                | (A) ← (P4)                      |
|                                       | OP4A*    | 1                | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 0  | 0  | 2 2 4                | 1               | 1                | (P4) ← (A)                      |
|                                       | IAP5*    | 1                | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 0  | 1  | 2 6 5                | 1               | 1                | (A) ← (P5)                      |
|                                       | OP5A*    | 1                | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 2 2 5                | 1               | 1                | (P5) ← (A)                      |
|                                       | CLD      | 0                | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 0 1 1                | 1               | 1                | (D) ← 1                         |
|                                       | RD       | 0                | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 0 1 4                | 1               | 1                | (D(Y)) ← 0<br>(Y) = 0 to 7      |
|                                       | SD       | 0                | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 1  | 0 1 5                | 1               | 1                | (D(Y)) ← 1<br>(Y) = 0 to 7      |
|                                       | SZD      | 0                | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 0  | 0  | 0 2 4                | 2               | 2                | (D(Y)) = 0 ?<br>(Y) = 0 to 7    |
|                                       |          | 0                | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0 2 B                |                 |                  |                                 |
|                                       | TK0A     | 1                | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 1  | 2 1 B                | 1               | 1                | (K0) ← (A)                      |
|                                       | TAK0     | 1                | 0  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 2 5 6                | 1               | 1                | (A) ← (K0)                      |
|                                       | TPU0A    | 1                | 0  | 0  | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 2 2 D                | 1               | 1                | (PU0) ← (A)                     |
|                                       | TAPU0    | 1                | 0  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 1  | 2 5 7                | 1               | 1                | (A) ← (PU0)                     |
|                                       | TFR0A*   | 1                | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 0  | 2 2 8                | 1               | 1                | (FR0) ← (A)                     |

\*: The 4513 Group does not have these instructions.

| Skip condition             | Carry flag CY | Detailed description  |
|----------------------------|---------------|---|
| –                          | –             | Transfers the input of port P0 to register A.                                   |
| –                          | –             | Outputs the contents of register A to port P0.                                  |
| –                          | –             | Transfers the input of port P1 to register A.                                   |
| –                          | –             | Outputs the contents of register A to port P1.                                  |
| –                          | –             | Transfers the input of port P2 to register A.                                   |
| –                          | –             | Transfers the input of port P3 to register A.                                   |
| –                          | –             | Outputs the contents of register A to port P3.                                  |
| –                          | –             | Transfers the input of port P4 to register A.                                   |
| –                          | –             | Outputs the contents of register A to port P4.                                  |
| –                          | –             | Transfers the input of port P5 to register A.                                   |
| –                          | –             | Outputs the contents of register A to port P5.                                  |
| –                          | –             | Sets (1) to port D.   |
| –                          | –             | Clears (0) to a bit of port D specified by register Y.                          |
| –                          | –             | Sets (1) to a bit of port D specified by register Y.                            |
| (D(Y)) = 0<br>(Y) = 0 to 7 | –             | Skips the next instruction when a bit of port D specified by register Y is "0." |
| –                          | –             | Transfers the contents of register A to key-on wakeup control register K0.      |
| –                          | –             | Transfers the contents of key-on wakeup control register K0 to register A.      |
| –                          | –             | Transfers the contents of register A to pull-up control register PU0.           |
| –                          | –             | Transfers the contents of pull-up control register PU0 to register A.           |
| –                          | –             | Transfers the contents of register A to direction register FR0.                 |

## MACHINE INSTRUCTIONS (continued)

| Parameter<br>Type of instructions | Mnemonic | Instruction code |    |    |    |    |    |    |    |    |    | Hexadecimal notation | Number of words | Number of cycles | Function   |
|-----------------------------------|----------|------------------|----|----|----|----|----|----|----|----|----|----------------------|-----------------|------------------|--|
|                                   |          | D9               | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |                      |                 |                  |  |
| Serial I/O control operation      | TABSI    | 1                | 0  | 0  | 1  | 1  | 1  | 1  | 0  | 0  | 0  | 2 7 8                | 1               | 1                | (A) ← (SI3–SI0)<br>(B) ← (SI7–SI4)   |
|                                   | TSIAB    | 1                | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 0  | 2 3 8                | 1               | 1                | (SI3–SI0) ← (A)<br>(SI7–SI4) ← (B)   |
|                                   | TAJ1     | 1                | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 1  | 0  | 2 4 2                | 1               | 1                | (A) ← (J1)   |
|                                   | TJ1A     | 1                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 2 0 2                | 1               | 1                | (J1) ← (A)   |
|                                   | SST      | 1                | 0  | 1  | 0  | 0  | 1  | 1  | 1  | 1  | 0  | 2 9 E                | 1               | 1                | (SIOF) ← 0<br>Serial I/O starting  |
|                                   | SNZSI    | 1                | 0  | 1  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 2 8 8                | 1               | 1                | (SIOF) = 1 ?<br>After skipping<br>(SIOF) ← 0   |
| A-D conversion operation          | TABAD    | 1                | 0  | 0  | 1  | 1  | 1  | 1  | 0  | 0  | 1  | 2 7 9                | 1               | 1                | (A) ← (AD5–AD2)<br>(B) ← (AD9–AD6)<br>However, in the comparator mode,<br>(A) ← (AD3–AD0)<br>(B) ← (AD7–AD4) |
|                                   | TALA     | 1                | 0  | 0  | 1  | 0  | 0  | 1  | 0  | 0  | 1  | 2 4 9                | 1               | 1                | (A) ← (AD1, AD0, 0, 0)   |
|                                   | TADAB    | 1                | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 1  | 2 3 9                | 1               | 1                | (AD3–AD0) ← (A)<br>(AD7–AD4) ← (B)   |
|                                   | TAQ1     | 1                | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 0  | 0  | 2 4 4                | 1               | 1                | (A) ← (Q1)   |
|                                   | TQ1A     | 1                | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 2 0 4                | 1               | 1                | (Q1) ← (A)   |
|                                   | ADST     | 1                | 0  | 1  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 2 9 F                | 1               | 1                | (ADF) ← 0<br>A-D conversion starting   |
|                                   | SNZAD    | 1                | 0  | 1  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 2 8 7                | 1               | 1                | (ADF) = 1 ?<br>After skipping<br>(ADF) ← 0   |
|                                   | TAQ2     | 1                | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 0  | 1  | 2 4 5                | 1               | 1                | (A) ← (Q2)   |
|                                   | TQ2A     | 1                | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 2 0 5                | 1               | 1                | (Q2) ← (A)   |
| Other operation                   | NOP      | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 0 0                | 1               | 1                | (PC) ← (PC) + 1  |
|                                   | POF      | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0 0 2                | 1               | 1                | RAM back-up  |
|                                   | EPOF     | 0                | 0  | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 1  | 0 5 B                | 1               | 1                | POF instruction valid  |
|                                   | SNZP     | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0 0 3                | 1               | 1                | (P) = 1 ?  |
|                                   | WRST     | 1                | 0  | 1  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 2 A 0                | 1               | 1                | (WDF1) ← 0<br>(WEF) ← 1  |
|                                   | TAMR     | 1                | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 0  | 2 5 2                | 1               | 1                | (A) ← (MR)   |
|                                   | TMRA     | 1                | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 1  | 0  | 2 1 6                | 1               | 1                | (MR) ← (A)   |
|                                   | TAQ3     | 1                | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 1  | 0  | 2 4 6                | 1               | 1                | (A) ← (Q3)   |
|                                   | TQ3A     | 1                | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 2 0 6                | 1               | 1                | (Q33, Q32) ← (A3, A2)<br>(Q31) ← (CMP1 comparison result)<br>(Q30) ← (CMP0 comparison result)                |

| Skip condition  | Carry flag CY  | Detailed description  |
|---|--|---|
| <ul style="list-style-type: none"> <li>–</li> <li>–</li> <li>–</li> <li>–</li> <li>–</li> </ul> <p>(SIOF) = 1</p>                               | <ul style="list-style-type: none"> <li>–</li> <li>–</li> <li>–</li> <li>–</li> <li>–</li> </ul>                                  | <p>Transfers the contents of serial I/O register SI to registers A and B.</p> <p>Transfers the contents of registers A and B to serial I/O register SI.</p> <p>Transfers the contents of serial I/O mode register J1 to register A.</p> <p>Transfers the contents of register A to serial I/O mode register J1.</p> <p>Clears (0) to SIOF flag and starts serial I/O.</p> <p>Skips the next instruction when the contents of SIOF flag is "1."<br/>After skipping, clears (0) to SIOF flag.</p>   |
| <ul style="list-style-type: none"> <li>–</li> <li>–</li> <li>–</li> <li>–</li> <li>–</li> <li>–</li> <li>–</li> </ul> <p>(ADF) = 1</p>          | <ul style="list-style-type: none"> <li>–</li> <li>–</li> <li>–</li> <li>–</li> <li>–</li> <li>–</li> <li>–</li> </ul>            | <p>Transfers the high-order 8 bits of the contents of register AD to registers A and B.</p> <p>Transfers the low-order 2 bits of the contents of register AD to the high-order 2 bits of the contents of register A. Simultaneously, the low-order 2 bits of the contents of the register A is "0."</p> <p>Transfers the contents of registers A and B to the comparator register at the comparator mode.</p> <p>Transfers the contents of the A-D control register Q1 to register A.</p> <p>Transfers the contents of register A to the A-D control register Q1.</p> <p>Clears the ADF flag, and the A-D conversion at the A-D conversion mode or the comparator operation at the comparator mode is started.</p> <p>Skips the next instruction when the contents of ADF flag is "1".<br/>After skipping, clears (0) the contents of ADF flag.</p> <p>Transfers the contents of the A-D control register Q2 to register A.</p> <p>Transfers the contents of register A to the A-D control register Q2.</p> |
| <ul style="list-style-type: none"> <li>–</li> <li>–</li> <li>–</li> <li>–</li> <li>–</li> <li>–</li> <li>–</li> <li>–</li> </ul> <p>(P) = 1</p> | <ul style="list-style-type: none"> <li>–</li> <li>–</li> <li>–</li> <li>–</li> <li>–</li> <li>–</li> <li>–</li> <li>–</li> </ul> | <p>No operation</p> <p>Puts the system in RAM back-up state by executing the POF instruction after executing the EPOF instruction.</p> <p>Makes the immediate POF instruction valid by executing the EPOF instruction.</p> <p>Skips the next instruction when P flag is "1". After skipping, P flag remains unchanged.</p> <p>Operates the watchdog timer and initializes the watchdog timer flag WDF1.</p> <p>Transfers the contents of the clock control register MR to register A.</p> <p>Transfers the contents of register A to the clock control register MR.</p> <p>Transfers the contents of the voltage comparator control register Q3 to register A.</p> <p>Transfers the contents of the high-order 2 bits of register A to the high-order 2 bits of voltage comparator control register Q3, and the comparison result of the voltage comparator is transferred to the low-order 2 bits of the register Q3.</p>  |

# CONTROL REGISTERS

| Interrupt control register V1 |   | at reset : 00002 |   | at RAM back-up : 00002          |  | R/W |
|-------------------------------|---|------------------|---|---------------------------------|--|-----|
| V13                           | Timer 2 interrupt enable bit  | 0                | Interrupt disabled (SNZT2 instruction is valid)   |                                 |  |     |
|                               |   | 1                | Interrupt enabled (SNZT2 instruction is invalid)  |                                 |  |     |
| V12                           | Timer 1 interrupt enable bit  | 0                | Interrupt disabled (SNZT1 instruction is valid)   |                                 |  |     |
|                               |   | 1                | Interrupt enabled (SNZT1 instruction is invalid)  |                                 |  |     |
| V11                           | External 1 interrupt enable bit   | 0                | Interrupt disabled (SNZ1 instruction is valid)  |                                 |  |     |
|                               |   | 1                | Interrupt enabled (SNZ1 instruction is invalid)   |                                 |  |     |
| V10                           | External 0 interrupt enable bit   | 0                | Interrupt disabled (SNZ0 instruction is valid)  |                                 |  |     |
|                               |   | 1                | Interrupt enabled (SNZ0 instruction is invalid)   |                                 |  |     |
| Interrupt control register V2 |   | at reset : 00002 |   | at RAM back-up : 00002          |  | R/W |
| V23                           | Serial I/O interrupt enable bit   | 0                | Interrupt disabled (SNZSI instruction is valid)   |                                 |  |     |
|                               |   | 1                | Interrupt enabled (SNZSI instruction is invalid)  |                                 |  |     |
| V22                           | A-D interrupt enable bit  | 0                | Interrupt disabled (SNZAD instruction is valid)   |                                 |  |     |
|                               |   | 1                | Interrupt enabled (SNZAD instruction is invalid)  |                                 |  |     |
| V21                           | Timer 4 interrupt enable bit  | 0                | Interrupt disabled (SNZT4 instruction is valid)   |                                 |  |     |
|                               |   | 1                | Interrupt enabled (SNZT4 instruction is invalid)  |                                 |  |     |
| V20                           | Timer 3 interrupt enable bit  | 0                | Interrupt disabled (SNZT3 instruction is valid)   |                                 |  |     |
|                               |   | 1                | Interrupt enabled (SNZT3 instruction is invalid)  |                                 |  |     |
| Interrupt control register I1 |   | at reset : 00002 |   | at RAM back-up : state retained |  | R/W |
| I13                           | Not used  | 0                | This bit has no function, but read/write is enabled.  |                                 |  |     |
|                               |   | 1                |   |                                 |  |     |
| I12                           | Interrupt valid waveform for INT0 pin/<br>return level selection bit (Note 2) | 0                | Falling waveform (“L” level of INT0 pin is recognized with the SNZI0 instruction)/“L” level |                                 |  |     |
|                               |   | 1                | Rising waveform (“H” level of INT0 pin is recognized with the SNZI0 instruction)/“H” level  |                                 |  |     |
| I11                           | INT0 pin edge detection circuit control bit                                   | 0                | One-sided edge detected   |                                 |  |     |
|                               |   | 1                | Both edges detected   |                                 |  |     |
| I10                           | INT0 pin<br>timer 1 control enable bit  | 0                | Disabled  |                                 |  |     |
|                               |   | 1                | Enabled   |                                 |  |     |
| Interrupt control register I2 |   | at reset : 00002 |   | at RAM back-up : state retained |  | R/W |
| I23                           | Not used  | 0                | This bit has no function, but read/write is enabled.  |                                 |  |     |
|                               |   | 1                |   |                                 |  |     |
| I22                           | Interrupt valid waveform for INT1 pin/<br>return level selection bit (Note 3) | 0                | Falling waveform (“L” level of INT1 pin is recognized with the SNZI1 instruction)/“L” level |                                 |  |     |
|                               |   | 1                | Rising waveform (“H” level of INT1 pin is recognized with the SNZI1 instruction)/“H” level  |                                 |  |     |
| I21                           | INT1 pin edge detection circuit control bit                                   | 0                | One-sided edge detected   |                                 |  |     |
|                               |   | 1                | Both edges detected   |                                 |  |     |
| I20                           | INT1 pin<br>timer 3 control enable bit  | 0                | Disabled  |                                 |  |     |
|                               |   | 1                | Enabled   |                                 |  |     |

Notes 1: "R" represents read enabled, and "W" represents write enabled.

2: When the contents of I12 is changed, the external interrupt request flag EXF0 may be set. Accordingly, clear EXF0 flag with the SNZ0 instruction.

3: When the contents of I22 is changed, the external interrupt request flag EXF1 may be set. Accordingly, clear EXF1 flag with the SNZ1 instruction.

| Timer control register W1 |   | at reset : 00002 |   | at RAM back-up : 00002          |  | R/W |
|---------------------------|---|------------------|---|---------------------------------|--|-----|
| W13                       | Prescaler control bit                               | 0                | Stop (state initialized)                                      |                                 |  |     |
|                           |   | 1                | Operating   |                                 |  |     |
| W12                       | Prescaler dividing ratio selection bit              | 0                | Instruction clock divided by 4                                |                                 |  |     |
|                           |   | 1                | Instruction clock divided by 16                               |                                 |  |     |
| W11                       | Timer 1 control bit                                 | 0                | Stop (state retained)   |                                 |  |     |
|                           |   | 1                | Operating   |                                 |  |     |
| W10                       | Timer 1 count start synchronous circuit control bit | 0                | Count start synchronous circuit not selected                  |                                 |  |     |
|                           |   | 1                | Count start synchronous circuit selected                      |                                 |  |     |
| Timer control register W2 |   | at reset : 00002 |   | at RAM back-up : state retained |  | R/W |
| W23                       | Timer 2 control bit                                 | 0                | Stop (state retained)   |                                 |  |     |
|                           |   | 1                | Operating   |                                 |  |     |
| W22                       | Not used  | 0                | This bit has no function, but read/write is enabled.          |                                 |  |     |
|                           |   | 1                |   |                                 |  |     |
| W21                       | Timer 2 count source selection bits                 | W21              | W20   | Count source                    |  |     |
|                           |   | 0                | 0   | Timer 1 underflow signal        |  |     |
| 0                         |   | 1                | Prescaler output  |                                 |  |     |
| W20                       |   | 1                | 0   | CNTR0 input                     |  |     |
|                           | 1   | 1                | 16 bit timer (WDT) underflow signal                           |                                 |  |     |
| Timer control register W3 |   | at reset : 00002 |   | at RAM back-up : state retained |  | R/W |
| W33                       | Timer 3 control bit                                 | 0                | Stop (state retained)   |                                 |  |     |
|                           |   | 1                | Operating   |                                 |  |     |
| W32                       | Timer 3 count start synchronous circuit control bit | 0                | Count start synchronous circuit not selected                  |                                 |  |     |
|                           |   | 1                | Count start synchronous circuit selected                      |                                 |  |     |
| W31                       | Timer 3 count source selection bits                 | W31              | W30   | Count source                    |  |     |
|                           |   | 0                | 0   | Timer 2 underflow signal        |  |     |
| 0                         |   | 1                | Prescaler output  |                                 |  |     |
| W30                       |   | 1                | 0   | Not available                   |  |     |
|                           | 1   | 1                | Not available   |                                 |  |     |
| Timer control register W4 |   | at reset : 00002 |   | at RAM back-up : state retained |  | R/W |
| W43                       | Timer 4 control bit                                 | 0                | Stop (state retained)   |                                 |  |     |
|                           |   | 1                | Operating   |                                 |  |     |
| W42                       | Not used  | 0                | This bit has no function, but read/write is enabled.          |                                 |  |     |
|                           |   | 1                |   |                                 |  |     |
| W41                       | Timer 4 count source selection bits                 | W41              | W40   | Count source                    |  |     |
|                           |   | 0                | 0   | Timer 3 underflow signal        |  |     |
| 0                         |   | 1                | Prescaler output  |                                 |  |     |
| W40                       |   | 1                | 0   | CNTR1 input                     |  |     |
|                           | 1   | 1                | Not available   |                                 |  |     |
| Timer control register W6 |   | at reset : 00002 |   | at RAM back-up : state retained |  | R/W |
| W63                       | CNTR1 output control bit                            | 0                | Timer 3 underflow signal output divided by 2                  |                                 |  |     |
|                           |   | 1                | CNTR1 output control by timer 4 underflow signal divided by 2 |                                 |  |     |
| W62                       | D7/CNTR1 function selection bit                     | 0                | D7(I/O)/CNTR1 input   |                                 |  |     |
|                           |   | 1                | CNTR1 (I/O)/D7(input)   |                                 |  |     |
| W61                       | CNTR0 output control bit                            | 0                | Timer 1 underflow signal output divided by 2                  |                                 |  |     |
|                           |   | 1                | CNTR0 output control by timer 2 underflow signal divided by 2 |                                 |  |     |
| W60                       | D6/CNTR0 output control bit                         | 0                | D6(I/O)/CNTR0 input   |                                 |  |     |
|                           |   | 1                | CNTR0 (I/O)/D6(input)   |                                 |  |     |

Note: "R" represents read enabled, and "W" represents write enabled.

| Serial I/O mode register J1             |  | at reset : 00002 |  | at RAM back-up : state retained | R/W                                     |
|---|--|------------------|--|---------------------------------|---|
| J13                                     | Not used   | 0                | This bit has no function, but read/write is enabled.               |                                 |   |
|   |  | 1                |  |                                 |   |
| J12                                     | Serial I/O internal clock dividing ratio selection bit                         | 0                | Instruction clock signal divided by 8                              |                                 |   |
|   |  | 1                | Instruction clock signal divided by 4                              |                                 |   |
| J11                                     | Serial I/O port selection bit  | 0                | Input ports P20, P21, P22 selected                                 |                                 |   |
|   |  | 1                | Serial I/O ports SCK, SOUT, SIN/input ports P20, P21, P22 selected |                                 |   |
| J10                                     | Serial I/O synchronous clock selection bit                                     | 0                | External clock   |                                 |   |
|   |  | 1                | Internal clock (instruction clock divided by 4 or 8)               |                                 |   |
| A-D control register Q1                 |  | at reset : 00002 |  | at RAM back-up : state retained | R/W                                     |
| Q13                                     | Note used  | 0                | This bit has no function, but read/write is enabled.               |                                 |   |
|   |  | 1                |  |                                 |   |
| Q12                                     | Analog input pin selection bits (Note 2)                                       | Q12              | Q11  | Q10                             | Selected pins                           |
|   |  | 0                | 0  | 0                               | AIN0                                    |
|   |  | 0                | 0  | 1                               | AIN1                                    |
|   |  | 0                | 1  | 0                               | AIN2                                    |
| Q11                                     |  | 0                | 1  | 1                               | AIN3                                    |
|   |  | 1                | 0  | 0                               | AIN4 (Not available for the 4513 Group) |
|   |  | 1                | 0  | 1                               | AIN5 (Not available for the 4513 Group) |
| Q10                                     |  | 1                | 1  | 0                               | AIN6 (Not available for the 4513 Group) |
|   |  | 1                | 1  | 1                               | AIN7 (Not available for the 4513 Group) |
| A-D control register Q2                 |  | at reset : 00002 |  | at RAM back-up : state retained | R/W                                     |
| Q23                                     | A-D operation mode selection bit   | 0                | A-D conversion mode  |                                 |   |
|   |  | 1                | Comparator mode  |                                 |   |
| Q22                                     | P43/AIN7 and P42/AIN6 pin function selection bit (Not used for the 4513 Group) | 0                | P43, P42 (read/write enabled for the 4513 Group)                   |                                 |   |
|   |  | 1                | AIN7, AIN6/P43, P42 (read/write enabled for the 4513 Group)        |                                 |   |
| Q21                                     | P41/AIN5 pin function selection bit (Not used for the 4513 Group)              | 0                | P41 (read/write enabled for the 4513 Group)                        |                                 |   |
|   |  | 1                | AIN5/P41 (read/write enabled for the 4513 Group)                   |                                 |   |
| Q20                                     | P40/AIN4 pin function selection bit (Not used for the 4513 Group)              | 0                | P40 (read/write enabled for the 4513 Group)                        |                                 |   |
|   |  | 1                | AIN4/P40 (read/write enabled for the 4513 Group)                   |                                 |   |
| Comparator control register Q3 (Note 3) |  | at reset : 00002 |  | at RAM back-up : state retained | R/W                                     |
| Q33                                     | Voltage comparator (CMP1) control bit  | 0                | Voltage comparator (CMP1) invalid                                  |                                 |   |
|   |  | 1                | Voltage comparator (CMP1) valid                                    |                                 |   |
| Q32                                     | Voltage comparator (CMP0) control bit  | 0                | Voltage comparator (CMP0) invalid                                  |                                 |   |
|   |  | 1                | Voltage comparator (CMP0) valid                                    |                                 |   |
| Q31                                     | CMP1 comparison result store bit   | 0                | CMP1- > CMP1+  |                                 |   |
|   |  | 1                | CMP1- < CMP1+  |                                 |   |
| Q30                                     | CMP0 comparison result store bit   | 0                | CMP0- > CMP0+  |                                 |   |
|   |  | 1                | CMP0- < CMP0+  |                                 |   |
| Clock control register MR               |  | at reset : 10002 |  | at RAM back-up : 10002          | R/W                                     |
| MR3                                     | System clock selection bit   | 0                | f(XIN) (high-speed mode)   |                                 |   |
|   |  | 1                | f(XIN)/2 (middle-speed mode)                                       |                                 |   |
| MR2                                     | Not used   | 0                | This bit has no function, but read/write is enabled.               |                                 |   |
|   |  | 1                |  |                                 |   |
| MR1                                     | Not used   | 0                | This bit has no function, but read/write is enabled.               |                                 |   |
|   |  | 1                |  |                                 |   |
| MR0                                     | Not used   | 0                | This bit has no function, but read/write is enabled.               |                                 |   |
|   |  | 1                |  |                                 |   |

Notes 1: "R" represents read enabled, "W" represents write enabled.

2: Select AIN4–AIN7 with register Q1 after setting register Q2.

3: Bits 0 and 1 of register Q3 can be only read.

| Key-on wakeup control register K0 |   | at reset : 00002 |                        | at RAM back-up : state retained | R/W |
|-----------------------------------|---|------------------|------------------------|---------------------------------|-----|
| K03                               | Pins P12 and P13 key-on wakeup control bit      | 0                | Key-on wakeup not used |                                 |     |
|                                   |   | 1                | Key-on wakeup used     |                                 |     |
| K02                               | Pins P10 and P11 key-on wakeup control bit      | 0                | Key-on wakeup not used |                                 |     |
|                                   |   | 1                | Key-on wakeup used     |                                 |     |
| K01                               | Pins P02 and P03 key-on wakeup control bit      | 0                | Key-on wakeup not used |                                 |     |
|                                   |   | 1                | Key-on wakeup used     |                                 |     |
| K00                               | Pins P00 and P01 key-on wakeup control bit      | 0                | Key-on wakeup not used |                                 |     |
|                                   |   | 1                | Key-on wakeup used     |                                 |     |
| Pull-up control register PU0      |   | at reset : 00002 |                        | at RAM back-up : state retained | R/W |
| PU03                              | Pins P12 and P13 pull-up transistor control bit | 0                | Pull-up transistor OFF |                                 |     |
|                                   |   | 1                | Pull-up transistor ON  |                                 |     |
| PU02                              | Pins P10 and P11 pull-up transistor control bit | 0                | Pull-up transistor OFF |                                 |     |
|                                   |   | 1                | Pull-up transistor ON  |                                 |     |
| PU01                              | Pins P02 and P03 pull-up transistor control bit | 0                | Pull-up transistor OFF |                                 |     |
|                                   |   | 1                | Pull-up transistor ON  |                                 |     |
| PU00                              | Pins P00 and P01 pull-up transistor control bit | 0                | Pull-up transistor OFF |                                 |     |
|                                   |   | 1                | Pull-up transistor ON  |                                 |     |
| Direction register FR0 (Note 2)   |   | at reset : 00002 |                        | at RAM back-up : state retained | W   |
| FR03                              | Port P53 input/output control bit               | 0                | Port P53 input         |                                 |     |
|                                   |   | 1                | Port P53 output        |                                 |     |
| FR02                              | Port P52 input/output control bit               | 0                | Port P52 input         |                                 |     |
|                                   |   | 1                | Port P52 output        |                                 |     |
| FR01                              | Port P51 input/output control bit               | 0                | Port P51 input         |                                 |     |
|                                   |   | 1                | Port P51 output        |                                 |     |
| FR00                              | Port P50 input/output control bit               | 0                | Port P50 input         |                                 |     |
|                                   |   | 1                | Port P50 output        |                                 |     |

Notes 1: "R" represents read enabled, and "W" represents write enabled.

2: The 4513 Group does not have the direction register FR0.



## BUILT-IN PROM VERSION

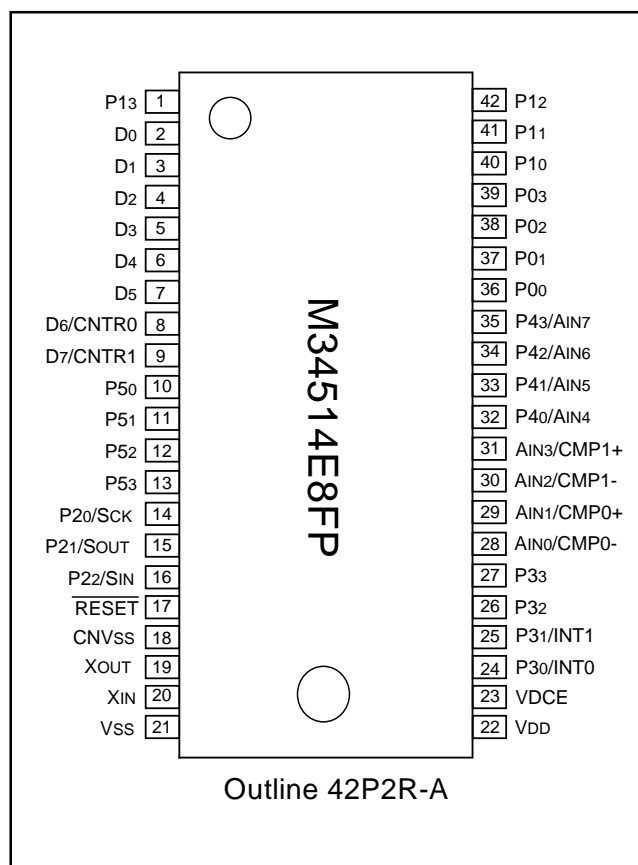
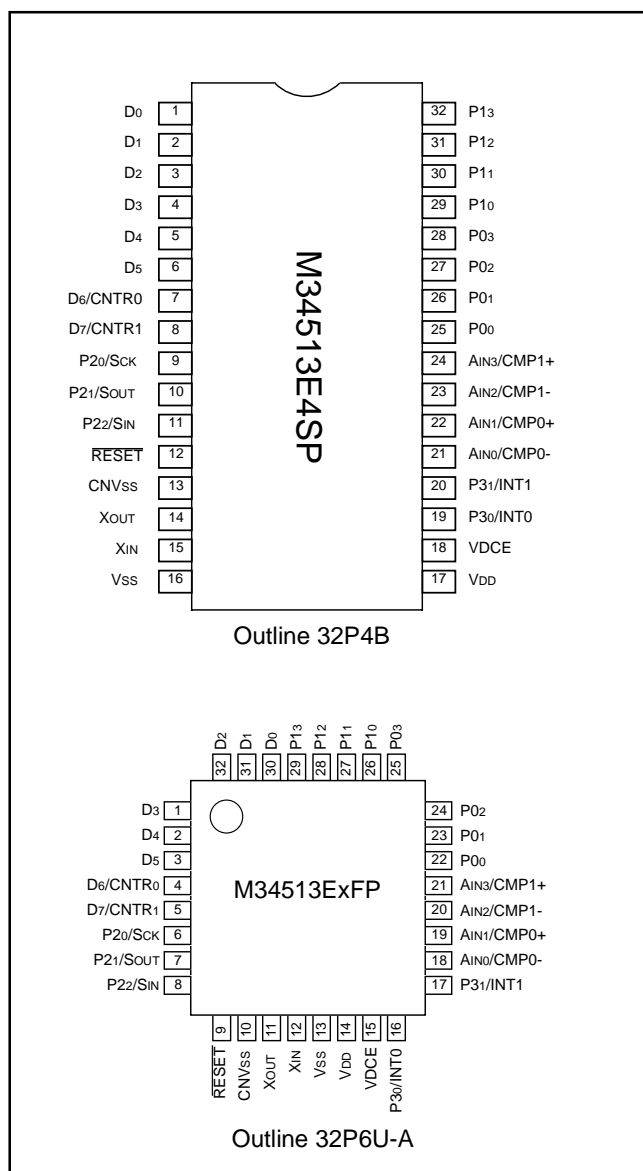
In addition to the mask ROM versions, the 4513/4514 Group has programmable ROM version software compatible with mask ROM. The built-in PROM of One Time PROM version can be written to and not be erased.

The built-in PROM versions have functions similar to those of the mask ROM versions, but they have PROM mode that enables writing to built-in PROM.

Table 25 shows the product of built-in PROM version. Figure 49 and 50 show the pin configurations of built-in PROM versions.

**Table 25 Product of built-in PROM version**

| Product       | PROM size<br>(X 10 bits) | RAM size<br>(X 4 bits) | Package               | ROM type                                    |
|---------------|--------------------------|------------------------|-----------------------|---|
| M34513E4SP/FP | 4096 words               | 256 words              | SP: 32P4B FP: 32P6U-A | One Time PROM version<br>[shipped in blank] |
| M34513E8FP    | 8192 words               | 384 words              | 32P6B-A               |   |
| M34514E8FP    | 8192 words               | 384 words              | 42P2R-A               |   |



**Fig. 50 Pin configuration of built-in PROM version of 4514 Group**

**Fig. 49 Pin configuration of built-in PROM version of 4513 Group**

## (1) PROM mode

The built-in PROM version has a PROM mode in addition to a normal operation mode. The PROM mode is used to write to and read from the built-in PROM.

In the PROM mode, the programming adapter can be used with a general-purpose PROM programmer to write to or read from the built-in PROM as if it were M5M27C256K. Programming adapters are listed in Table 26. Contact addresses at the end of this sheet for the appropriate PROM programmer.

- Writing and reading of built-in PROM

Programming voltage is 12.5 V. Write the program in the PROM of the built-in PROM version as shown in Figure 51.

## (2) Notes on handling

- ① A high-voltage is used for writing. Take care that overvoltage is not applied. Take care especially at turning on the power.
- ② For the One Time PROM version shipped in blank, Mitsubishi Electric corp. does not perform PROM writing test and screening in the assembly process and following processes. In order to improve reliability after writing, performing writing and test according to the flow shown in Figure 52 before using is recommended (Products shipped in blank: PROM contents is not written in factory when shipped).

Table 26 Programming adapters

| Microcomputer          | Programming adapter |
|------------------------|---------------------|
| M34513E4SP             | PCA7442SP           |
| M34513E4FP, M34513E8FP | PCA7442FP           |
| M34514E8FP             | PCA7441             |

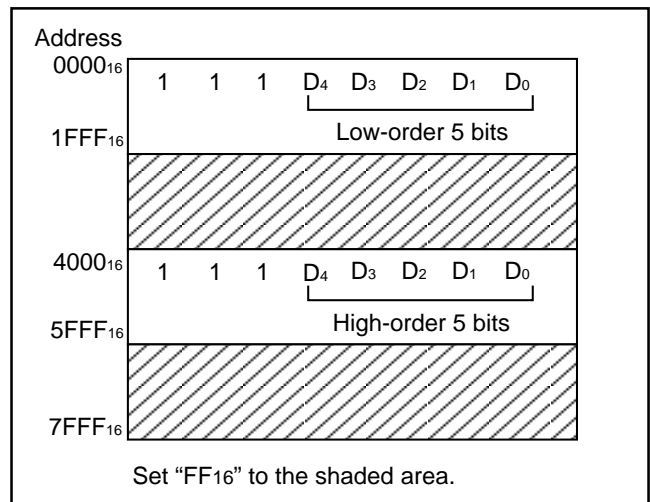


Fig. 51 PROM memory map

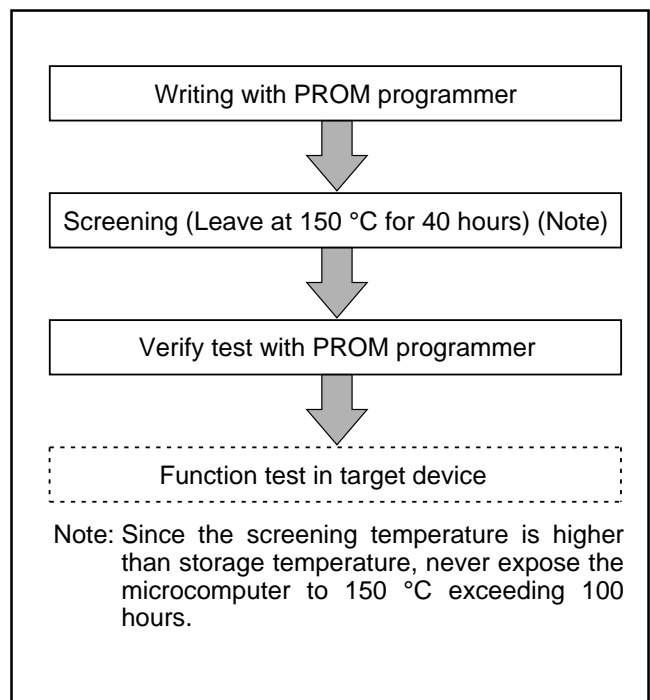


Fig. 52 Flow of writing and test of the product shipped in blank

**ABSOLUTE MAXIMUM RATINGS**

| Symbol          | Parameter   | Conditions                          |                | Ratings                      | Unit |
|-----------------|---|-------------------------------------|----------------|------------------------------|------|
| V <sub>DD</sub> | Supply voltage  |                                     |                | −0.3 to 7.0                  | V    |
| V <sub>I</sub>  | Input voltage P0, P1, P2, P3, P4, P5, $\overline{\text{RESET}}$ , XIN, VDCE |                                     |                | −0.3 to V <sub>DD</sub> +0.3 | V    |
| V <sub>I</sub>  | Input voltage D0–D7   |                                     |                | −0.3 to 13                   | V    |
| V <sub>I</sub>  | Input voltage AIN0–AIN7   |                                     |                | −0.3 to V <sub>DD</sub> +0.3 | V    |
| V <sub>O</sub>  | Output voltage P0, P1, P3, P4, P5, $\overline{\text{RESET}}$                | Output transistors in cut-off state |                | −0.3 to V <sub>DD</sub> +0.3 | V    |
| V <sub>O</sub>  | Output voltage D0–D7  |                                     |                | −0.3 to 13                   | V    |
| V <sub>O</sub>  | Output voltage XOUT   |                                     |                | −0.3 to V <sub>DD</sub> +0.3 | V    |
| P <sub>d</sub>  | Power dissipation   | Ta = 25 °C                          | Package: 42P2R | 300                          | mW   |
|                 |   |                                     | Package: 32P6U | 300                          |      |
|                 |   |                                     | Package: 32P4B | 1100                         |      |
| Topr            | Operating temperature range   |                                     |                | −20 to 85                    | °C   |
| Tstg            | Storage temperature range   |                                     |                | −40 to 125                   | °C   |

# RECOMMENDED OPERATING CONDITIONS 1

(Mask ROM version: Ta = -20 °C to 85 °C, VDD = 2.0 V to 5.5 V, unless otherwise noted)

(One Time PROM version: Ta = -20 °C to 85 °C, VDD = 2.5 V to 5.5 V, unless otherwise noted)

| Symbol    | Parameter                                    | Conditions                               |                               | Limits  |      |         | Unit |
|-----------|--|--|-------------------------------|---------|------|---------|------|
|           |  |  |                               | Min.    | Typ. | Max.    |      |
| VDD       | Supply voltage                               | Mask ROM version                         | $f(XIN) \leq 4.2 \text{ MHz}$ | 2.5     |      | 5.5     | V    |
|           |  | Middle-speed mode                        | $f(XIN) \leq 3.0 \text{ MHz}$ | 2.0     |      | 5.5     |      |
|           |  | Mask ROM version                         | $f(XIN) \leq 4.2 \text{ MHz}$ | 4.0     |      | 5.5     |      |
|           |  | High-speed mode                          | $f(XIN) \leq 2.0 \text{ MHz}$ | 2.5     |      | 5.5     |      |
|           |  |  | $f(XIN) \leq 1.5 \text{ MHz}$ | 2.0     |      | 5.5     |      |
|           |  | One Time PROM version                    | $f(XIN) \leq 4.2 \text{ MHz}$ | 2.5     |      | 5.5     |      |
|           |  | Middle-speed mode                        |                               |         |      |         |      |
|           |  | One Time PROM version                    | $f(XIN) \leq 4.2 \text{ MHz}$ | 4.0     |      | 5.5     |      |
|           |  | High-speed mode                          | $f(XIN) \leq 2.0 \text{ MHz}$ | 2.5     |      | 5.5     |      |
| VRAM      | RAM back-up voltage<br>(at RAM back-up mode) | Mask ROM version                         |                               | 1.8     |      |         | V    |
|           |  | One Time PROM version                    |                               | 2.0     |      |         |      |
| VSS       | Supply voltage                               |  |                               |         | 0    |         | V    |
| VIH       | "H" level input voltage                      | P0, P1, P2, P3, P4, P5, XIN, VDCE        |                               | 0.8VDD  |      | VDD     | V    |
| VIH       | "H" level input voltage                      | D0-D7                                    |                               | 0.8VDD  |      | 12      | V    |
| VIH       | "H" level input voltage                      | RESET                                    |                               | 0.85VDD |      | VDD     | V    |
| VIH       | "H" level input voltage                      | CNTR0, CNTR1, SIN, SCK, INT0, INT1       |                               | 0.85VDD |      | VDD     | V    |
| VIL       | "L" level input voltage                      | P0, P1, P2, P3, P4, P5, D0-D7, XIN, VDCE |                               | 0       |      | 0.2VDD  | V    |
| VIL       | "L" level input voltage                      | RESET                                    |                               | 0       |      | 0.3VDD  | V    |
| VIL       | "L" level input voltage                      | CNTR0, CNTR1, SIN, SCK, INT0, INT1       |                               | 0       |      | 0.15VDD | V    |
| IOH(peak) | "H" level peak output current                | P5                                       | VDD = 5.0 V                   | -20     |      |         | mA   |
|           |  |  | VDD = 3.0 V                   | -10     |      |         |      |
| IOH(avg)  | "H" level average output current             | P5 (Note)                                | VDD = 5.0 V                   | -10     |      |         | mA   |
|           |  |  | VDD = 3.0 V                   | -5      |      |         |      |
| IOL(peak) | "L" level peak output current                | P3, RESET                                | VDD = 5.0 V                   |         |      | 10      | mA   |
|           |  |  | VDD = 3.0 V                   |         |      | 4       |      |
| IOL(peak) | "L" level peak output current                | D6, D7                                   | VDD = 5.0 V                   |         |      | 40      | mA   |
|           |  |  | VDD = 3.0 V                   |         |      | 30      |      |
| IOL(peak) | "L" level peak output current                | D0-D5                                    | VDD = 5.0 V                   |         |      | 24      | mA   |
|           |  |  | VDD = 3.0 V                   |         |      | 12      |      |
| IOL(peak) | "L" level peak output current                | P0, P1, P4, P5, SCK,<br>SOUT             | VDD = 5.0 V                   |         |      | 24      | mA   |
|           |  |  | VDD = 3.0 V                   |         |      | 12      |      |
| IOL(avg)  | "L" level average output current             | P3, RESET (Note)                         | VDD = 5.0 V                   |         |      | 5       | mA   |
|           |  |  | VDD = 3.0 V                   |         |      | 2       |      |
| IOL(avg)  | "L" level average output current             | D6, D7 (Note)                            | VDD = 5.0 V                   |         |      | 30      | mA   |
|           |  |  | VDD = 3.0 V                   |         |      | 15      |      |
| IOL(avg)  | "L" level average output current             | D0-D5 (Note)                             | VDD = 5.0 V                   |         |      | 15      | mA   |
|           |  |  | VDD = 3.0 V                   |         |      | 7       |      |
| IOL(avg)  | "L" level average output current             | P0, P1, P4, P5, SCK,<br>SOUT (Note)      | VDD = 5.0 V                   |         |      | 12      | mA   |
|           |  |  | VDD = 3.0 V                   |         |      | 6       |      |
| ΣIOH(avg) | "H" level total average current              | P5                                       |                               | -30     |      |         | mA   |
| ΣIOL(avg) | "L" level total average current              | P5, D, RESET, SCK, SOUT                  |                               |         |      | 80      |      |
|           |  | P0, P1, P3, P4                           |                               |         |      | 80      |      |

Note: The average output current (IOH, IOL) is the average value during 100 ms.

**RECOMMENDED OPERATING CONDITIONS 2**

(Mask ROM version: Ta = -20 °C to 85 °C, VDD = 2.0 V to 5.5 V, unless otherwise noted)

(One Time PROM version: Ta = -20 °C to 85 °C, VDD = 2.5 V to 5.5 V, unless otherwise noted)

| Symbol   | Parameter   | Conditions            |                      | Limits |      |      | Unit    |
|----------|---|-----------------------|----------------------|--------|------|------|---------|
|          |   |                       |                      | Min.   | Typ. | Max. |         |
| f(XIN)   | Oscillation frequency<br>(with a ceramic resonator)           | Mask ROM version      | VDD = 2.5 V to 5.5 V |        |      | 4.2  | MHz     |
|          |   | Middle-speed mode     | VDD = 2.0 V to 5.5 V |        |      | 3.0  |         |
|          |   | One Time PROM version | VDD = 2.5 V to 5.5 V |        |      | 4.2  |         |
|          |   | Middle-speed mode     | VDD = 2.5 V to 5.5 V |        |      | 4.2  |         |
|          |   | Mask ROM version      | VDD = 4.0 V to 5.5 V |        |      | 4.2  |         |
|          |   | High-speed mode       | VDD = 2.5 V to 5.5 V |        |      | 2.0  |         |
|          |   |                       | VDD = 2.0 V to 5.5 V |        |      | 1.5  |         |
|          |   | One Time PROM version | VDD = 4.0 V to 5.5 V |        |      | 4.2  |         |
| f(XIN)   | Oscillation frequency<br>(with external clock input)          | Mask ROM version      | VDD = 2.0 V to 5.5 V |        |      | 3.0  | MHz     |
|          |   | Middle-speed mode     | VDD = 2.0 V to 5.5 V |        |      | 3.0  |         |
|          |   | One Time PROM version | VDD = 2.5 V to 5.5 V |        |      | 3.0  |         |
|          |   | Middle-speed mode     | VDD = 2.5 V to 5.5 V |        |      | 3.0  |         |
|          |   | Mask ROM version      | VDD = 4.0 V to 5.5 V |        |      | 3.0  |         |
|          |   | High-speed mode       | VDD = 2.5 V to 5.5 V |        |      | 1.0  |         |
|          |   |                       | VDD = 2.0 V to 5.5 V |        |      | 0.8  |         |
|          |   | One Time PROM version | VDD = 4.0 V to 5.5 V |        |      | 3.0  |         |
| tw(SCK)  | Serial I/O external clock period<br>("H" and "L" pulse width) | Mask ROM version      | VDD = 4.0 V to 5.5 V | 1.5    |      |      | $\mu$ s |
|          |   | Middle-speed mode     | VDD = 2.5 V to 5.5 V | 3.0    |      |      |         |
|          |   |                       | VDD = 2.0 V to 5.5 V | 4.0    |      |      |         |
|          |   | One Time PROM version | VDD = 4.0 V to 5.5 V | 1.5    |      |      | $\mu$ s |
|          |   | Middle-speed mode     | VDD = 2.5 V to 5.5 V | 3.0    |      |      |         |
|          |   |                       | VDD = 2.5 V to 5.5 V | 3.0    |      |      |         |
|          |   | Mask ROM version      | VDD = 4.0 V to 5.5 V | 750    |      |      | ns      |
|          |   | High-speed mode       | VDD = 2.5 V to 5.5 V | 1.5    |      |      | $\mu$ s |
|          |   |                       | VDD = 2.0 V to 5.5 V | 2.0    |      |      | $\mu$ s |
|          |   | One Time PROM version | VDD = 4.0 V to 5.5 V | 750    |      |      | ns      |
| tw(CNTR) | Timer external input period<br>("H" and "L" pulse width)      | Mask ROM version      | VDD = 4.0 V to 5.5 V | 1.5    |      |      | $\mu$ s |
|          |   | Middle-speed mode     | VDD = 2.5 V to 5.5 V | 3.0    |      |      |         |
|          |   |                       | VDD = 2.0 V to 5.5 V | 4.0    |      |      |         |
|          |   | One Time PROM version | VDD = 4.0 V to 5.5 V | 1.5    |      |      | $\mu$ s |
|          |   | Middle-speed mode     | VDD = 2.5 V to 5.5 V | 3.0    |      |      |         |
|          |   |                       | VDD = 2.5 V to 5.5 V | 3.0    |      |      |         |
|          |   | Mask ROM version      | VDD = 4.0 V to 5.5 V | 750    |      |      | ns      |
|          |   | High-speed mode       | VDD = 2.5 V to 5.5 V | 1.5    |      |      | $\mu$ s |
|          |   |                       | VDD = 2.0 V to 5.5 V | 2.0    |      |      | $\mu$ s |
|          |   | One Time PROM version | VDD = 4.0 V to 5.5 V | 750    |      |      | ns      |
|          |   | High-speed mode       | VDD = 2.5 V to 5.5 V | 1.5    |      |      | $\mu$ s |

# ELECTRICAL CHARACTERISTICS

(Mask ROM version: Ta = -20 °C to 85 °C, VDD = 2.0 V to 5.5 V, unless otherwise noted)

(One Time PROM version: Ta = -20 °C to 85 °C, VDD = 2.5 V to 5.5 V, unless otherwise noted)

| Symbol    | Parameter   |   | Test conditions   |                  | Limits |      |      | Unit |
|-----------|---|---|-------------------|------------------|--------|------|------|------|
|           |   |   |                   |                  | Min.   | Typ. | Max. |      |
| VOH       | “H” level output voltage P5   | VDD = 5 V   | IOH = −10 mA      | 3                |        |      | V    |      |
|           |   | VDD = 3 V   | IOH = −5 mA       | 2                |        |      |      |      |
| VOL       | “L” level output voltage P0, P1, P4, P5   | VDD = 5 V   | IOL = 12 mA       |                  |        | 2    | V    |      |
|           |   | VDD = 3 V   | IOL = 6 mA        |                  |        | 0.9  |      |      |
| VOL       | “L” level output voltage P3, $\overline{\text{RESET}}$                              | VDD = 5 V   | IOL = 5 mA        |                  |        | 2    | V    |      |
|           |   | VDD = 3 V   | IOL = 2 mA        |                  |        | 0.9  |      |      |
| VOL       | “L” level output voltage D6, D7   | VDD = 5 V   | IOL = 30 mA       |                  |        | 2    | V    |      |
|           |   |   | IOL = 10 mA       |                  |        | 0.9  |      |      |
|           |   | VDD = 3 V   | IOL = 15 mA       |                  |        | 2    | V    |      |
|           |   |   | IOL = 5 mA        |                  |        | 0.9  |      |      |
| VOL       | “L” level output voltage D0–D5  | VDD = 5 V   | IOL = 15 mA       |                  |        | 2    | V    |      |
|           |   | VDD = 3 V   | IOL = 3 mA        |                  |        | 0.9  |      |      |
| IIH       | “H” level input current<br>P0, P1, P2, P3, P4, P5, $\overline{\text{RESET}}$ , VDCE | VI = VDD, port P4 selected,<br>port P5: input state                               |                   |                  |        |      | 1    | μA   |
| IIH       | “H” level input current D0–D7   | VI = 12 V   |                   |                  |        |      | 1    | μA   |
| IIL       | “L” level input current<br>P0, P1, P2, P3, P4, P5, $\overline{\text{RESET}}$ , VDCE | VI = 0 V No pull-up of ports P0 and P1,<br>port P4 selected, port P5: input state |                   |                  | −1     |      |      | μA   |
| IIL       | “L” level input current D0–D7   | VI = 0 V  |                   |                  | −1     |      |      | μA   |
| IDD       | Supply current  | at active mode  | VDD = 5 V         | f(XIN) = 4.0 MHz |        | 1.8  | 5.5  | mA   |
|           |   |   | Middle-speed mode | f(XIN) = 400 kHz |        | 0.5  | 1.5  |      |
|           |   |   | VDD = 3 V         | f(XIN) = 4.0 MHz |        | 0.9  | 2.7  |      |
|           |   |   | Middle-speed mode | f(XIN) = 400 kHz |        | 0.2  | 0.6  |      |
|           |   |   | VDD = 5 V         | f(XIN) = 4.0 MHz |        | 3.0  | 9.0  |      |
|           |   |   | High-speed mode   | f(XIN) = 400 kHz |        | 0.6  | 1.8  |      |
|           |   |   | VDD = 3 V         | f(XIN) = 2.0 MHz |        | 0.9  | 2.7  |      |
|           |   |   | High-speed mode   | f(XIN) = 400 kHz |        | 0.3  | 0.9  |      |
|           |   | at RAM back-up mode   | Ta = 25 °C        |                  |        | 0.1  | 1    | μA   |
|           |   |   | VDD = 5 V         |                  |        |      | 10   |      |
|           |   |   | VDD = 3 V         |                  |        |      | 6    |      |
| RPU       | Pull-up resistor value  | VDD = 5 V   | VI = 0 V          | 20               | 50     | 125  | kΩ   |      |
|           |   | VDD = 3 V   |                   | 40               | 100    | 250  |      |      |
| VT+ − VT− | Hysteresis INT0, INT1, CNTR0, CNTR1, SIN, SCK                                       | VDD = 5 V   |                   |                  |        | 0.3  |      | V    |
|           |   | VDD = 3 V   |                   |                  |        | 0.3  |      |      |
| VT+ − VT− | Hysteresis $\overline{\text{RESET}}$  | VDD = 5 V   |                   |                  |        | 1.5  |      | V    |
|           |   | VDD = 3 V   |                   |                  |        | 0.6  |      |      |

## A-D CONVERTER RECOMMENDED OPERATING CONDITIONS

(Comparator mode included, Ta = -20 °C to 85 °C, unless otherwise noted)

| Symbol | Parameter             | Conditions                     | Limits |      |      | Unit |
|--------|-----------------------|--------------------------------|--------|------|------|------|
|        |                       |                                | Min.   | Typ. | Max. |      |
| VDD    | Supply voltage        |                                | 2.7    |      | 5.5  | V    |
| VIA    | Analog input voltage  |                                | 0      |      | VDD  | V    |
| f(XIN) | Oscillation frequency | Middle-speed mode, VDD ≥ 2.7 V | 0.8    |      |      | MHz  |
|        |                       | High-speed mode, VDD ≥ 2.7 V   | 0.4    |      |      | MHz  |

## A-D CONVERTER CHARACTERISTICS

(Ta = -20 °C to 85 °C, unless otherwise noted)

| Symbol | Parameter                        | Test conditions                            | Limits |      |      | Unit |
|--------|----------------------------------|--|--------|------|------|------|
|        |                                  |  | Min.   | Typ. | Max. |      |
| —      | Resolution                       |  |        |      | 10   | bits |
| —      | Linearity error                  | Ta = 25 °C, VDD = 2.7 V to 5.5 V           |        |      | ±2   | LSB  |
|        |                                  | Ta = -25 °C to 85 °C, VDD = 3.0 V to 5.5 V |        |      |      |      |
| —      | Differential non-linearity error | Ta = 25 °C, VDD = 2.7 V to 5.5 V           |        |      | ±0.9 | LSB  |
|        |                                  | Ta = -25 °C to 85 °C, VDD = 3.0 V to 5.5 V |        |      |      |      |
| VOT    | Zero transition voltage          | VDD = 5.12 V                               | 0      | 5    | 20   | mV   |
|        |                                  | VDD = 3.072 V                              | 0      | 3    | 15   |      |
| VFST   | Full-scale transition voltage    | VDD = 5.12 V                               | 5105   | 5115 | 5125 | mV   |
|        |                                  | VDD = 3.072 V                              | 3060   | 3069 | 3075 |      |
| IADD   | A-D operating current            | VDD = 5.0 V f(XIN) = 0.4 MHz to 4.0 MHz    |        | 0.7  | 2.0  | mA   |
|        |                                  | VDD = 3.0 V f(XIN) = 0.4 MHz to 2.0 MHz    |        | 0.2  | 0.4  |      |
| TCONV  | A-D conversion time              | f(XIN) = 4.0 MHz, Middle-speed mode        |        |      | 93.0 | μs   |
|        |                                  | f(XIN) = 4.0 MHz, High-speed mode          |        |      | 46.5 |      |
| —      | Comparator resolution            | Comparator mode                            |        |      | 8    | bits |
| —      | Comparator error (Note)          | VDD = 5.12 V                               |        |      | ±20  | mV   |
|        |                                  | VDD = 3.072 V                              |        |      | ±15  |      |
| —      | Comparator comparison time       | f(XIN) = 4.0 MHz, Middle-speed mode        |        |      | 12   | μs   |
|        |                                  | f(XIN) = 4.0 MHz, High-speed mode          |        |      | 6    |      |

Note: As for the error from the ideal value in the comparator mode, when the contents of the comparator register is n, the logic value of the comparison voltage Vref which is generated by the built-in DA converter can be obtained by the following formula.

— Logic value of comparison voltage Vref —

$$V_{ref} = \frac{V_{DD}}{256} \times n$$

n = Value of register AD (n = 0 to 255)

## VOLTAGE DROP DETECTION CIRCUIT CHARACTERISTICS

(Ta = -20 °C to 85 °C, unless otherwise noted)

| Symbol | Parameter   | Test conditions | Limits |      |      | Unit |
|--------|---|-----------------|--------|------|------|------|
|        |   |                 | Min.   | Typ. | Max. |      |
| VRST   | Detection voltage                                   |                 | 2.7    |      | 4.1  | V    |
|        |   | Ta = 25 °C      | 3.3    | 3.5  | 3.7  |      |
| IRST   | Operation current of voltage drop detection circuit | VDD = 5.0 V     |        | 50   | 100  | μA   |

# VOLTAGE COMPARATOR RECOMMENDED OPERATING CONDITIONS

(Ta = -20 °C to 85 °C, unless otherwise noted)

| Symbol | Parameter                        | Conditions           | Limits |      |        | Unit |
|--------|----------------------------------|----------------------|--------|------|--------|------|
|        |                                  |                      | Min.   | Typ. | Max.   |      |
| VDD    | Supply voltage                   |                      | 3.0    |      | 5.5    | V    |
| VINCMP | Voltage comparator input voltage | VDD = 3.0 V to 5.5 V | 0.3VDD |      | 0.7VDD | V    |
| tCMP   | Voltage comparator response time | VDD = 3.0 V to 5.5 V |        |      | 20     | μs   |

# VOLTAGE COMPARATOR CHARACTERISTICS

(Ta = -20 °C to 85 °C, VDD = 3.0 V to 5.5 V, unless otherwise noted)

| Symbol | Parameter                            | Test conditions  | Limits |      |      | Unit |
|--------|--------------------------------------|--|--------|------|------|------|
|        |                                      |  | Min.   | Typ. | Max. |      |
| –      | Comparison decision voltage error    | CMP0- > CMP0+, CMP0- < CMP0+<br>CMP1- > CMP1+, CMP1- < CMP1+ |        | 20   | 100  | mV   |
| ICMP   | Voltage comparator operation current | VDD = 5.0 V  |        | 15   | 50   | μA   |

# BASIC TIMING DIAGRAM

|                                       |                         | Machine cycle |  | Mi |  | Mi+1 |  |
|---------------------------------------|-------------------------|---------------|--|----|--|------|--|
| Parameter                             | Pin name                |               |  |    |  |      |  |
| Clock                                 | XIN                     |               |  |    |  |      |  |
|                                       | System clock = f(XIN)   |               |  |    |  |      |  |
|                                       | XIN                     |               |  |    |  |      |  |
|                                       | System clock = f(XIN)/2 |               |  |    |  |      |  |
| Port D output                         | D0–D7                   |               |  |    |  |      |  |
| Port D input                          | D0–D7                   |               |  |    |  |      |  |
| Ports P0, P1, P3,<br>P4, P5 output    | P00–P03                 |               |  |    |  |      |  |
|                                       | P10–P13                 |               |  |    |  |      |  |
|                                       | P30–P33                 |               |  |    |  |      |  |
|                                       | P40–P43                 |               |  |    |  |      |  |
|                                       | P50–P53                 |               |  |    |  |      |  |
| Ports P0, P1, P2, P3,<br>P4, P5 input | P00–P03                 |               |  |    |  |      |  |
|                                       | P10–P13                 |               |  |    |  |      |  |
|                                       | P20–P22                 |               |  |    |  |      |  |
|                                       | P30–P33                 |               |  |    |  |      |  |
|                                       | P40–P43                 |               |  |    |  |      |  |
| Interrupt input                       | P50–P53                 |               |  |    |  |      |  |
|                                       | INT0,INT1               |               |  |    |  |      |  |



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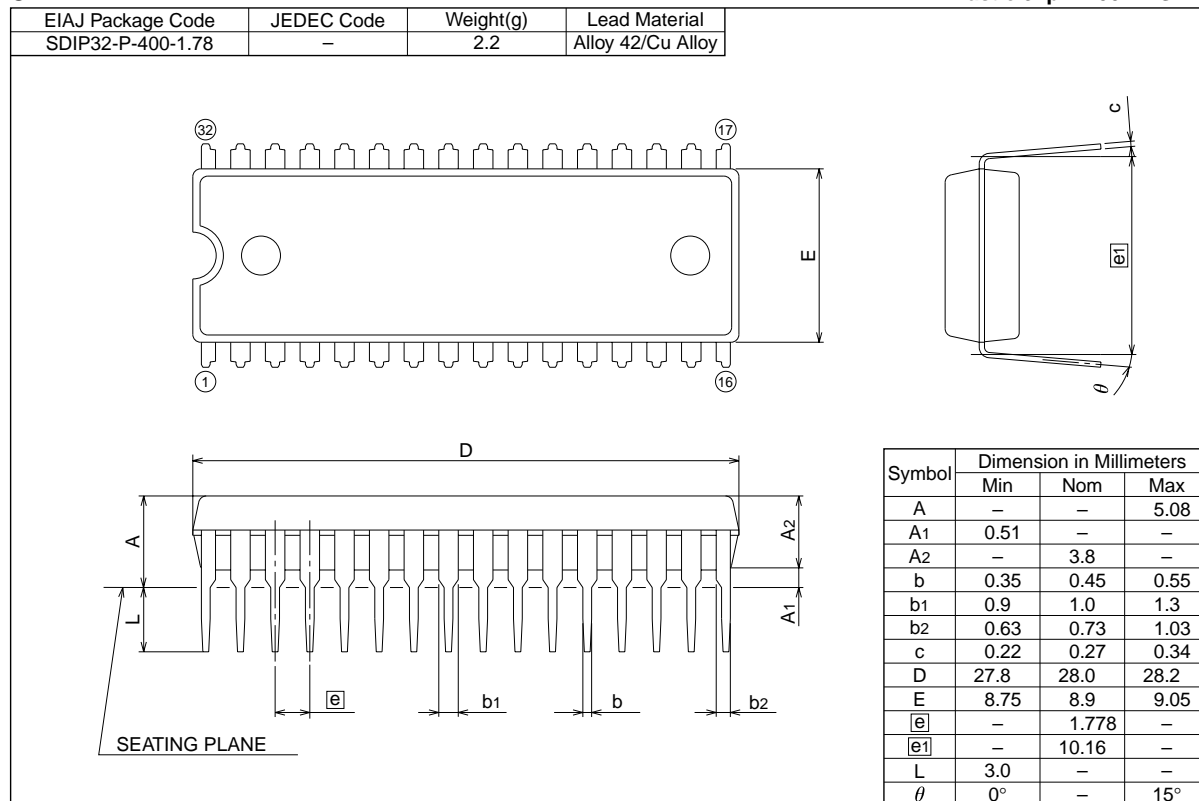
SINGLE-CHIP 4-BIT CMOS MICROCOMPUTER

## PACKAGE OUTLINE

### 32P4B

(MMP)

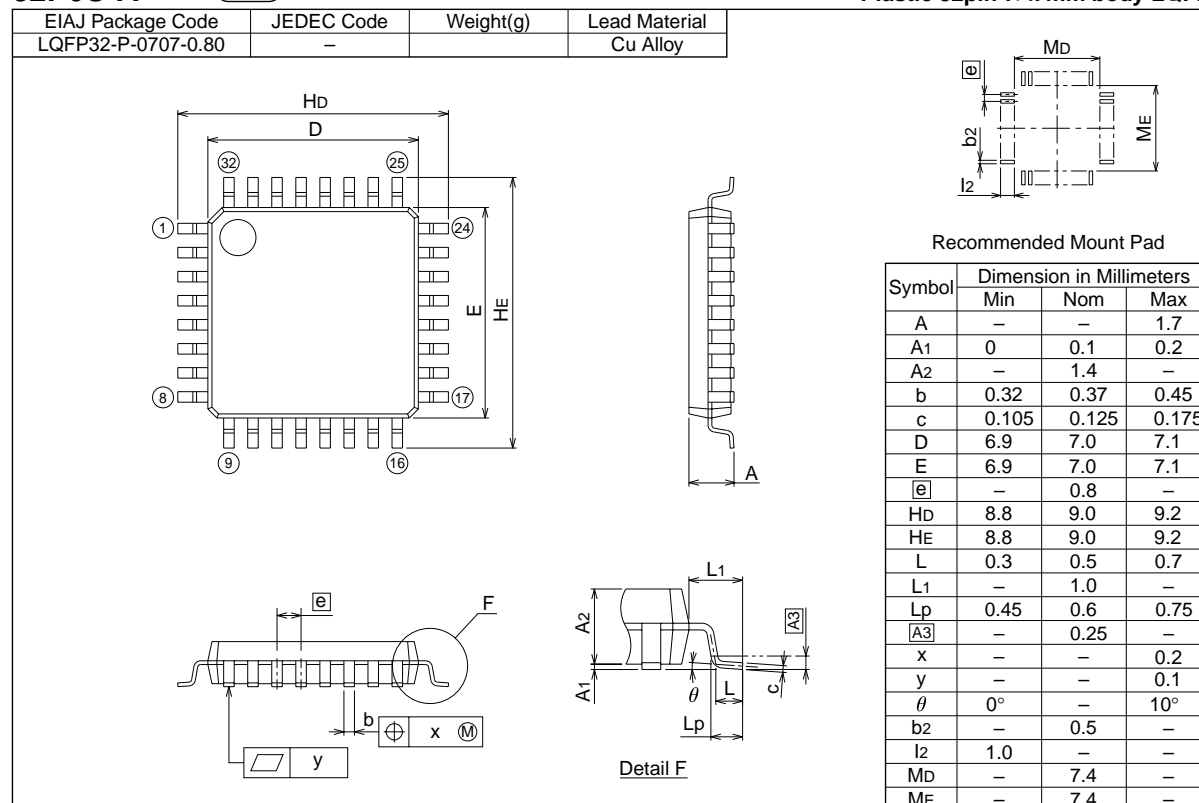
Plastic 32pin 400mil SDIP



### 32P6U-A

(MMP)

Plastic 32pin 7X7mm body LQFP

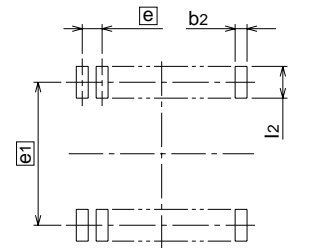
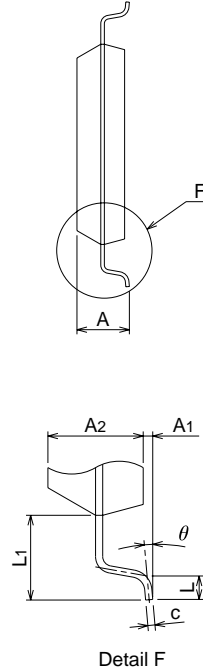
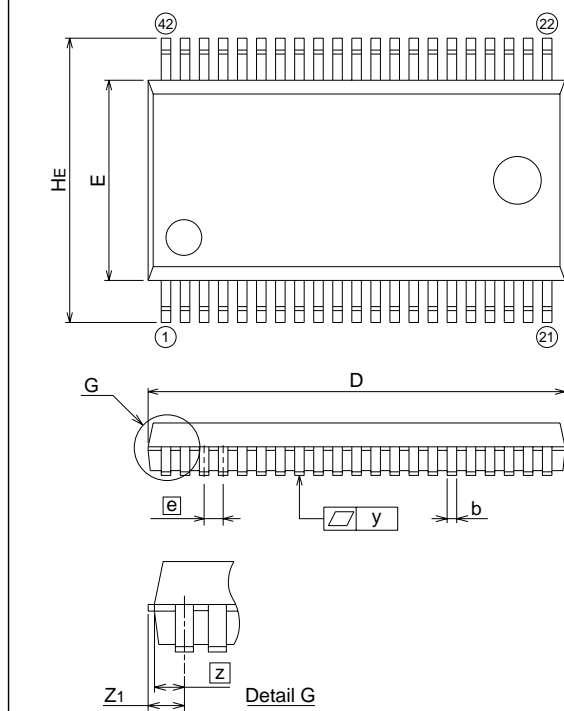


## 42P2R-A

(MMP)

## Plastic 42pin 450mil SSOP

| EIAJ Package Code | JEDEC Code | Weight(g) | Lead Material     |
|-------------------|------------|-----------|-------------------|
| SSOP42-P-450-0.80 | —          | 0.63      | Alloy 42/Cu Alloy |



Recommended Mount Pad

| Symbol | Dimension in Millimeters |       |       |
|--------|--------------------------|-------|-------|
|        | Min                      | Nom   | Max   |
| A      | —                        | —     | 2.4   |
| A1     | 0.05                     | —     | —     |
| A2     | —                        | 2.0   | —     |
| b      | 0.35                     | 0.4   | 0.5   |
| c      | 0.13                     | 0.15  | 0.2   |
| D      | 17.3                     | 17.5  | 17.7  |
| E      | 8.2                      | 8.4   | 8.6   |
| e      | —                        | 0.8   | —     |
| HE     | 11.63                    | 11.93 | 12.23 |
| L      | 0.3                      | 0.5   | 0.7   |
| L1     | —                        | 1.765 | —     |
| z      | —                        | 0.75  | —     |
| Z1     | —                        | —     | 0.9   |
| y      | —                        | —     | 0.15  |
| theta  | 0°                       | —     | 10°   |
| b2     | —                        | 0.5   | —     |
| e1     | —                        | 11.43 | —     |
| l2     | 1.27                     | —     | —     |

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# REVISION DESCRIPTION LIST

# 4513/4514 GROUP DATA SHEET

| Rev.<br>No. | Revision Description   | Rev.<br>date |
|-------------|--|--------------|
| 1.0         | First Edition  | 980807       |
| 1.1         | <p>Page 1: APPLICATION revised, Table "Under development" eliminated.</p> <p>Pages 10 to 14: PORT BLOCK DIAGRAMS revised.</p> <p>Page 24: Fig. 17 revised.</p> <p>Page 28: Table 9 Timer 1 structure and Timer 3 structure revised.</p> <p>Page 29: Fig. 19 revised.</p> <p>Page 32: (10) Count start synchronous circuit (timer 1 and 3) revised.</p> <p>Page 38: Table 13 Slave (reception); line 6; received → transmitted</p> <p>Page 39: Fig. 26 AIN8 → AIN4, AIN9 → AIN5, AIN10 → AIN6, AIN11 → AIN7</p> <p>Page 56: ROM ORDERING METHOD revised.</p> <p>Mask ROM Order Confirmation Form, Mark Specification Form eliminated.</p> <p>As for Mask ROM Order Confirmation Form and Mark Specification Form, refer to<br/> <a href="http://www.infocom.maec.co.jp/rom/efram/romtopf.htm">http://www.infocom.maec.co.jp/rom/efram/romtopf.htm</a></p> <p>32P6B-A package is changed to 32P6U-A package.</p> <p>Pages 94 and 95: All packages renewed.</p> | 010724       |
|             |  |              |