

PROTECTION PRODUCTS - RailClamp®

Description

RailClamp® TVS arrays are ultra low capacitance ESD protection devices designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).

RClamp®0551P has a maximum capacitance of 0.50pF. This allows it to be used on circuits operating in excess of 5GHz without appreciable signal attenuation. They exceed the ESD immunity requirements of IEC 61000-4-2, Level 4.

RClamp0551P is in a 2-pin SLP1006P2 package measuring 1.0 x 0.6 x 0.5mm. Leads are spaced at a pitch of 0.65mm and feature a lead-free finish. Each device will protect one high-speed line operating at 5 volts. It gives the designer the flexibility to protect single lines in applications where arrays are not practical. The combination of small size, low capacitance, and high ESD surge capability makes them ideal for use in applications such as cellular phones and digital video interfaces.

Features

- ◆ Transient protection for data lines to
IEC 61000-4-2 (ESD) ±17kV (air), ±17kV (contact)
IEC 61000-4-4 (EFT) 40A (tp = 5/50ns)
Cable Discharge Event (CDE)
- ◆ Ultra-small package (1.0 x 0.6 x 0.5mm)
- ◆ Protects one data or I/O line
- ◆ Low capacitance: **0.50pF**
- ◆ Dynamic Resistance: 1.3 Ohms Typical
- ◆ Low ESD clamping voltage
- ◆ Operating voltage: 5V
- ◆ Solid-state silicon-avalanche technology

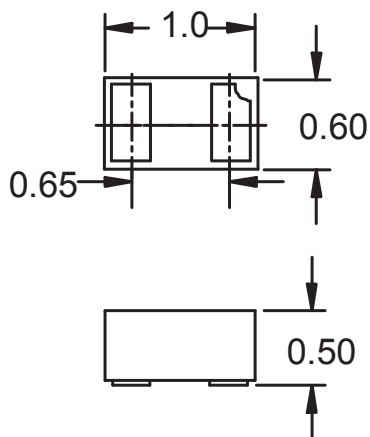
Mechanical Characteristics

- ◆ SLP1006P2 package
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking: Marking code
- ◆ Packaging: Tape and Reel
- ◆ Lead Finish: NiPdAu
- ◆ Pb-Free, Halogen Free, RoHS/WEEE Compliant

Applications

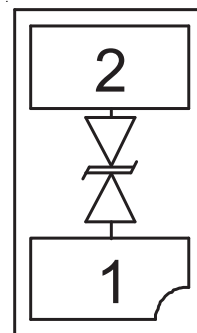
- ◆ USB 2.0
- ◆ V-By-One
- ◆ Display Port
- ◆ MHL / MDDI
- ◆ LVDS Interfaces
- ◆ eSATA Interfaces

Dimensions



Nominal Dimensions (mm)

Schematic & Pin Configuration



SLP1006P2 (Bottom View)

PROTECTION PRODUCTS
Absolute Maximum Rating

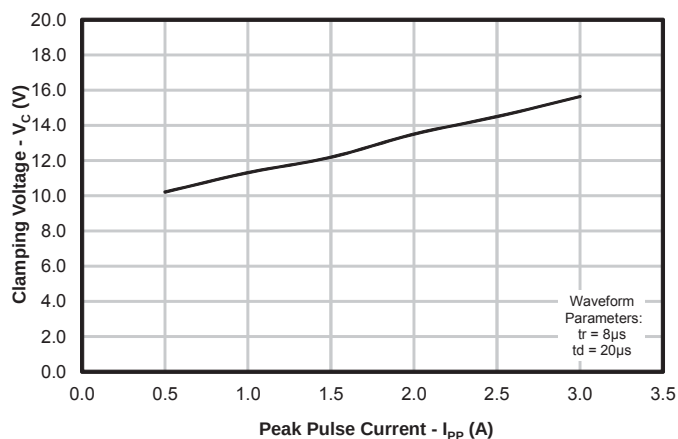
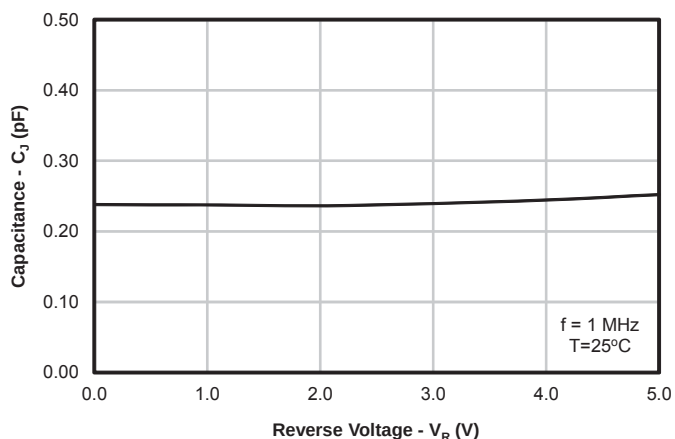
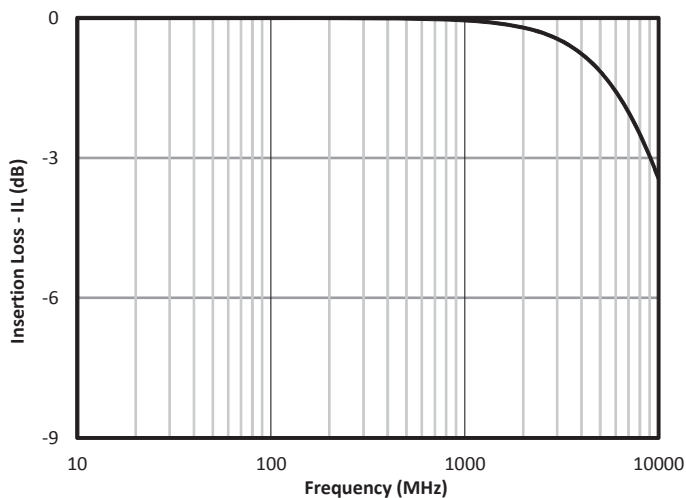
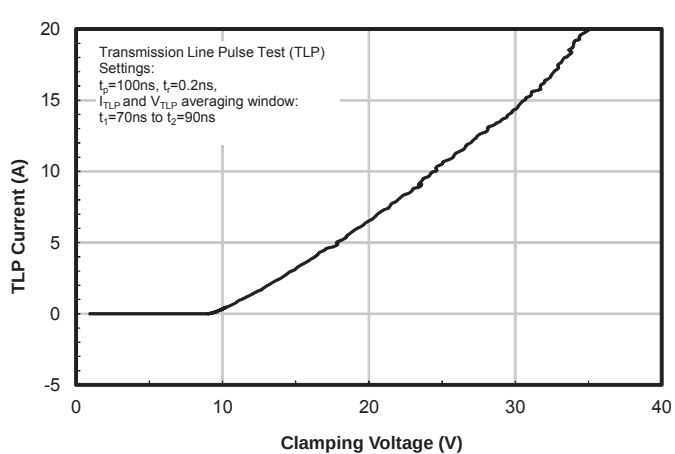
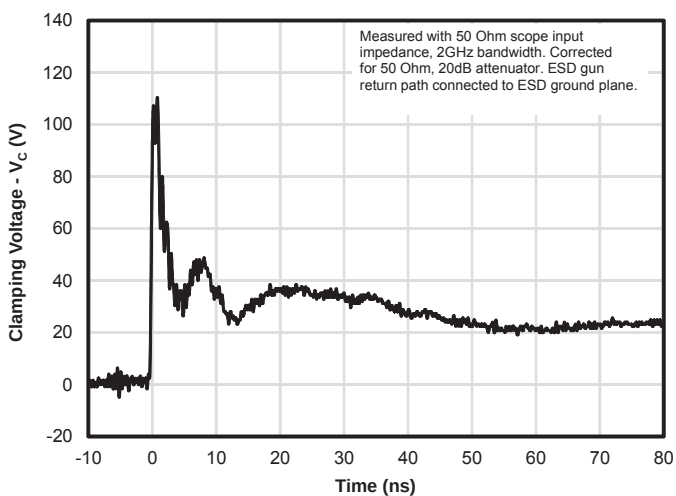
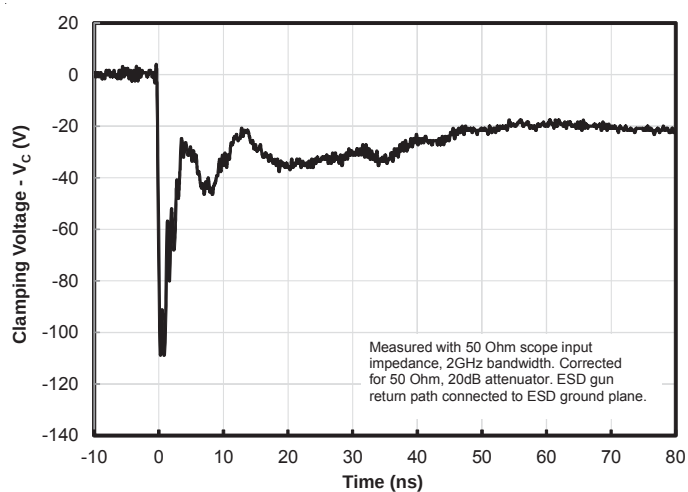
Rating	Symbol	Value	Units
Peak Pulse Power ($t_p = 8/20\mu s$)	P_{pk}	60	Watts
Maximum Peak Pulse Current ($t_p = 8/20\mu s$)	I_{pp}	3	Amps
ESD per IEC 61000-4-2 (Air) ¹ ESD per IEC 61000-4-2 (Contact) ¹	V_{ESD}	+/- 17 +/- 17	kV
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				5	V
Breakdown Voltage	V_{BR}	$I_{BR} = 1mA$	6	9.3	11	V
Reverse Leakage Current	I_R	$V_{RWM} = 5V$		0.01	0.100	μA
Clamping Voltage	V_C	$I_{pp} = 1A, t_p = 8/20\mu s$		12.5	15	V
Clamping Voltage	V_C	$I_{pp} = 3A, t_p = 8/20\mu s$		15.5	20	V
ESD Clamping Voltage ²	V_C	$I_{pp} = 4A,$ $t_{lp} = 0.2/100ns$		16.5		V
ESD Clamping Voltage ²	V_C	$I_{pp} = 16A,$ $t_{lp} = 0.2/100ns$		32		V
Dynamic Resistance ^{2, 3}	R_{DYN}	$t_{lp} = 0.2 / 100ns$		1.3		Ohms
Junction Capacitance	C_J	$V_R = 0V, f = 1MHz$		0.25	0.50	pF

Notes

- 1)ESD gun return path connected to ESD ground reference plane.
- 2)Transmission Line Pulse Test (TLP) Settings: $t_p = 100ns$, $t_r = 0.2ns$, I_{TLP} and V_{TLP} averaging window: $t_1 = 70ns$ to $t_2 = 90ns$.
- 3) Dynamic resistance calculated from $I_{pp} = 4A$ to $I_{pp} = 16A$
- 4) Device is electrically symmetrical

PROTECTION PRODUCTS
Typical Characteristics
Clamping Voltage vs. Peak Pulse Current

Capacitance vs. Reverse Voltage

Typical Insertion Loss (S21)

TLP Characteristic

ESD Clamping (+8kV Contact per IEC 61000-4-2)

ESD Clamping (-8kV Contact per IEC 61000-4-2)


PROTECTION PRODUCTS**Applications Information****Device Connection Options**

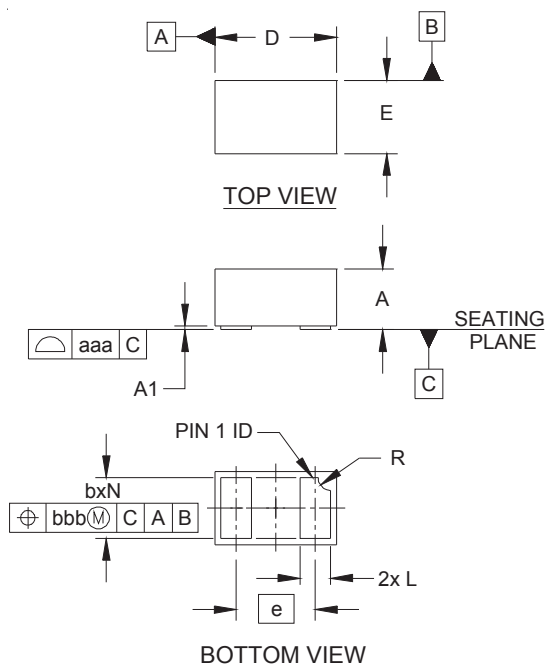
These low capacitance TVS diodes are designed to provide common mode protection for one high-speed line or differential protection for one line pair. The device is bidirectional and may be used on lines where the signal polarity is positive and negative.

Circuit Board Layout Recommendations for Suppression of ESD.

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

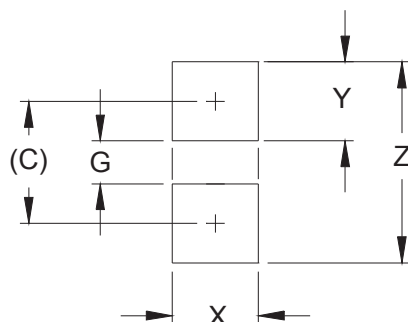
Equivalent Circuit Diagram

PROTECTION PRODUCTS
Outline Drawing - SLP1006P2


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.016	.020	.022	0.40	0.50	0.55
A1	.000	.001	.002	0.00	0.03	0.05
b	.018	.020	.022	0.45	0.50	0.55
D	.035	.039	.043	0.90	1.00	1.10
E	.020	.024	.028	0.50	0.60	0.70
e	.026 BSC			0.65 BSC		
L	.008	.010	.012	0.20	0.25	0.30
R	.002	.004	.006	0.05	0.10	0.15
N	2			2		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Land Pattern - SLP1006P2


DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.033)	(0.85)
G	.012	0.30
X	.024	0.60
Y	.022	0.55
Z	.055	1.40

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Codes



Notes:

- 1) Device is electrically symmetrical
- 2) Marking will also include line matrix date code

Notes:

RailClamp and RClamp are trademarks of Semtech Corporation

Carrier Tape Specification



Device Orientation in Tape

Contact Information

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