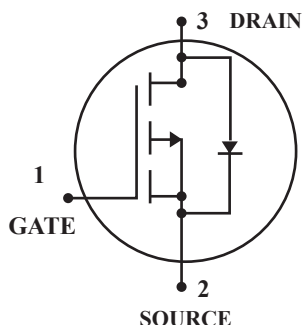


P-Channel Enhancement Mode Power MOSFET

 Lead(Pb)-Free



DRAIN CURRENT

-3.7 AMPERES

DRAIN SOURCE VOLTAGE

-30 VOLTAGE

Features:

*Super High Dense Cell Design For Low $R_{DS(ON)}$

$$R_{DS(ON)} < 75m\Omega @ V_{GS} = -10V$$

*Rugged and Reliable

*Simple Drive Requirement

*SOT-23 Package



SOT-23

Maximum Ratings(T_A=25℃ Unless Otherwise Specified)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DS}	-30	V
Gate-Source Voltage	V _{GS}	±20	
Continuous Drain Current ³ , (T _A =25°C) 			

Device Marking

WTC2309=2309

Electrical Characteristics ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Static

Drain-Source Breakdown Voltage $V_{GS}=0, I_D=-250\mu\text{A}$	$V_{(BR)DSS}$	-30	-	-	V
Gate-Source Threshold Voltage $V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	$V_{GS(Th)}$	-1.0	-	-3.0	
Gate-Source Leakage Current $V_{GS} = \pm 20\text{V}$	I_{GSS}	-	-	± 100	nA
Drain- Source Leakage Current($T_j=25^\circ\text{C}$) $V_{DS}=-30\text{V}, V_{GS}=0$	I_{DSS}	-	-	-1	μA
Drain- Source Leakage Current($T_j=55^\circ\text{C}$) $V_{DS}=-24\text{V}, V_{GS}=0$		-	-	-25	
Drain-Source On-Resistance ² $V_{GS}=-10\text{V}, I_D=-3.0\text{A}$ $V_{GS}=-4.5\text{V}, I_D=-2.6\text{A}$	$R_{DS(on)}$	- -	- -	75 120	$\text{m}\Omega$
Forward Transconductance $V_{DS}=-10\text{V}, I_D=-3\text{A}$	g_{fs}	-	5.0	-	S

Dynamic

Input Capacitance $V_{GS}=0\text{V}, V_{DS}=-25\text{V}, f=1.0\text{MHz}$	C_{iss}	-	412	660	pF
Output Capacitance $V_{GS}=0\text{V}, V_{DS}=-25\text{V}, f=1.0\text{MHz}$	C_{oss}	-	91	-	
Reverse Transfer Capacitance $V_{GS}=0\text{V}, V_{DS}=-25\text{V}, f=1.0\text{MHz}$	C_{rss}	-	62	-	

Switching

Turn-on Delay Time ² $V_{DS}=-15V, V_{GS}=-10V, I_D=-1A, R_D=15\Omega, R_G=3.3\Omega$	$t_{d(on)}$	-	8	-	ns
Rise Time $V_{DS}=-15V, V_{GS}=-10V, I_D=-1A, R_D=15\Omega, R_G=3.3\Omega$	t_r	-	5	-	
Turn-off Delay Time $V_{DS}=-15V, V_{GS}=-10V, I_D=-1A, R_D=15\Omega, R_G=3.3\Omega$	$t_{d(off)}$	-	20	-	
Fall Time $V_{DS}=-15V, V_{GS}=-10V, I_D=-1A, R_D=15\Omega, R_G=3.3\Omega$	t_f	-	7	-	
Total Gate Charge ² $V_{DS}=-24V, V_{GS}=-4.5V, I_D=-3A$	Q_g	-	5	8	nC
Gate-Source Charge $V_{DS}=-24V, V_{GS}=-4.5V, I_D=-3A$	Q_{gs}	-	1	-	
Gate-Drain Charge $V_{DS}=-24V, V_{GS}=-4.5V, I_D=-3A$	Q_{gd}	-	3	-	

Source-Drain Diode Characteristics

Forward On Voltage ² $V_{GS}=0V, I_S=-1.2A$	V_{SD}	-	-	-1.2	V
Reverse Recovery Time ² $V_{GS}=0V, I_S=-3.0A, dl/dt=100A/\mu s$	T_{rr}	-	20	-	ns
Reverse Recovery Charge $V_{GS}=0V, I_S=-3.0A, dl/dt=100A/\mu s$	Q_{rr}	-	15	-	nC

Note: 1. Pulse width limited by Max, junction temperature.

2. pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

3. Surface mounted on 1 in² copper pad of FR4 board; 270°C/W when mounted on min, copper pad.

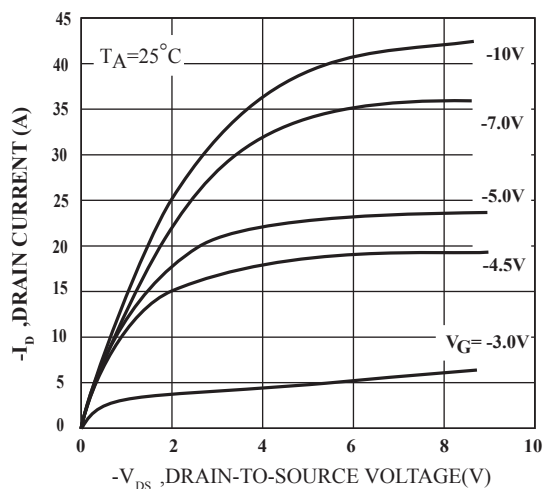


FIG.1 Typical Output Characteristics

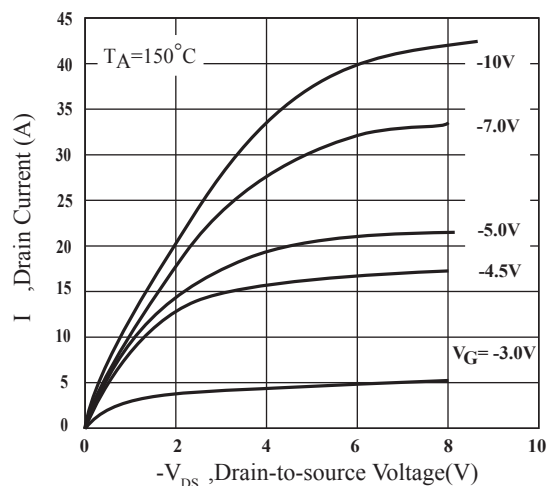


Fig.2 Typical Output Characteristics

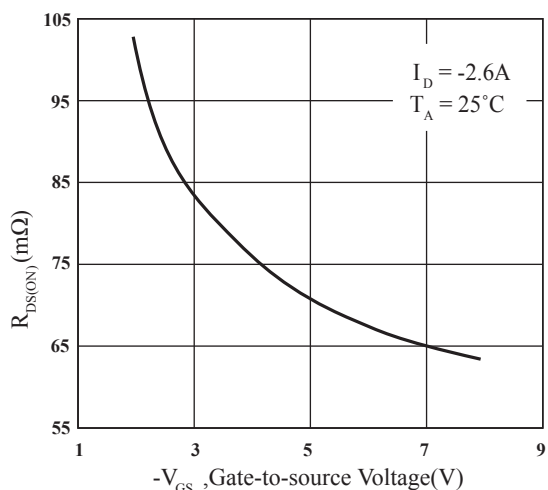


Fig.3 On-Resistance v.s. Gate Voltage

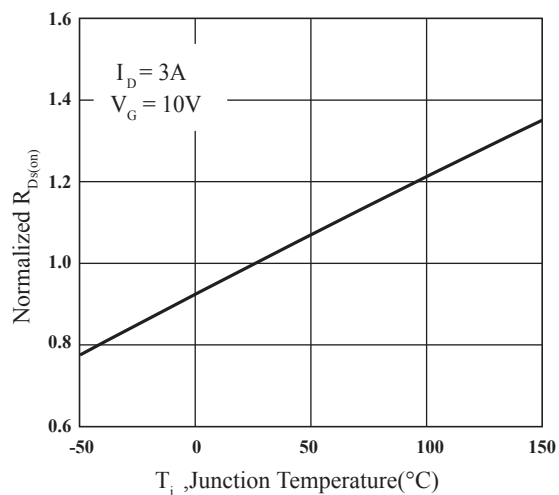


Fig.4 Normalized On-Resistance

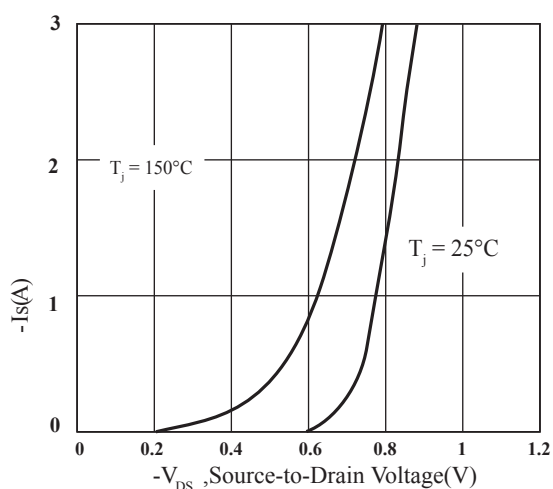


Fig.5 Forward Characteristics of Reverse Diode

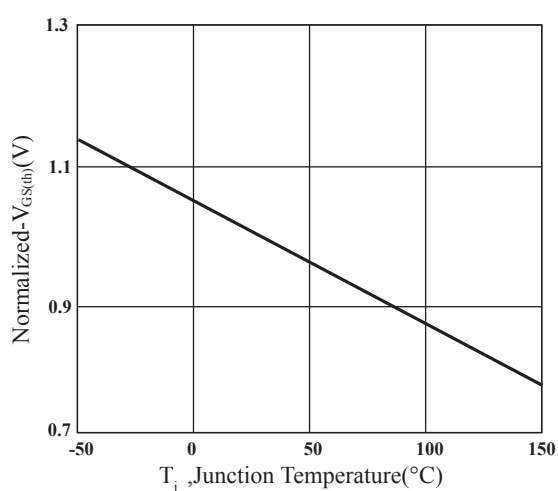


Fig.6 Gate Threshold Voltage v.s. Junction Temperature

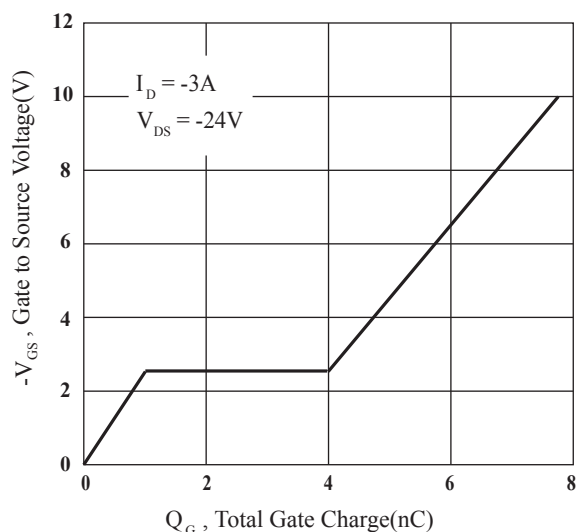


Fig 7. Gate Charge Characteristics

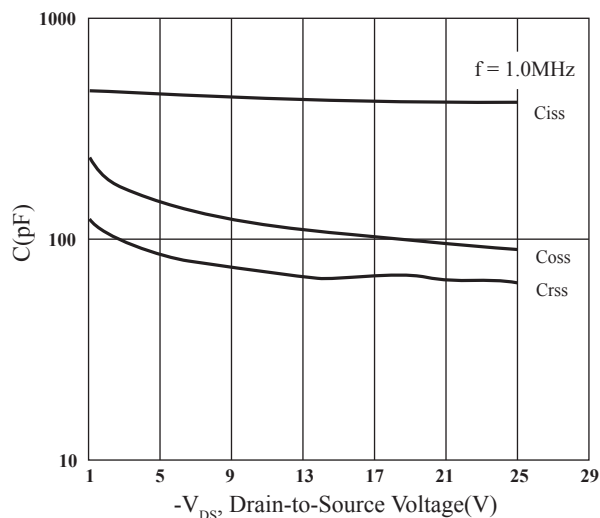


Fig 8. Typical Capacitance Characteristics

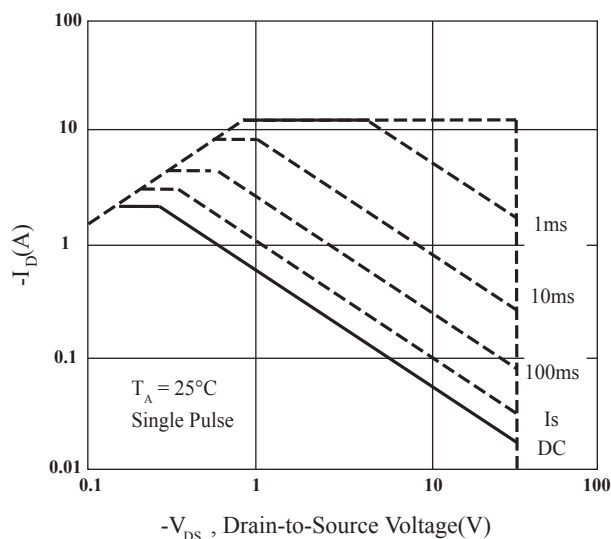


Fig 9. Maximum Safe Operation Area

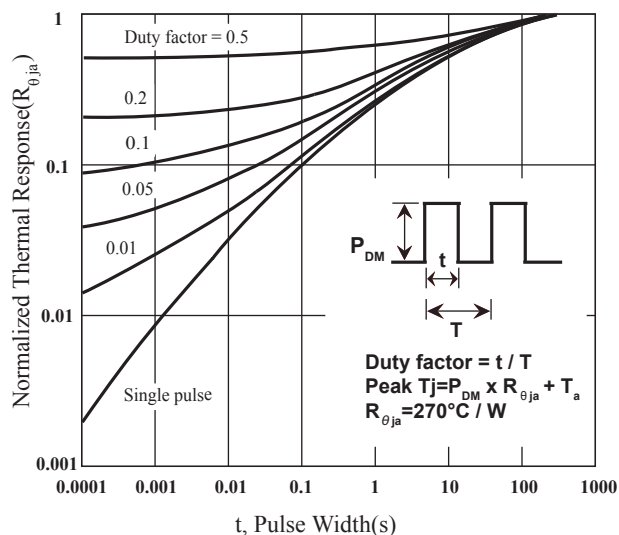


Fig 10. Effective Transient Thermal Impedance

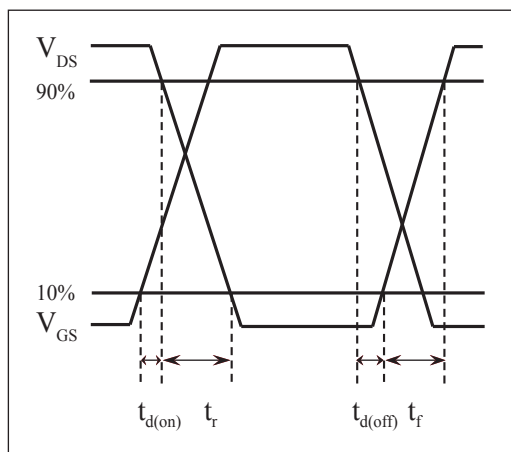


Fig.11 Switching Time Waveform

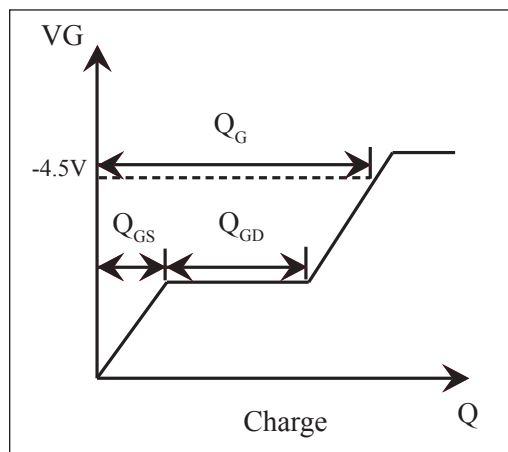
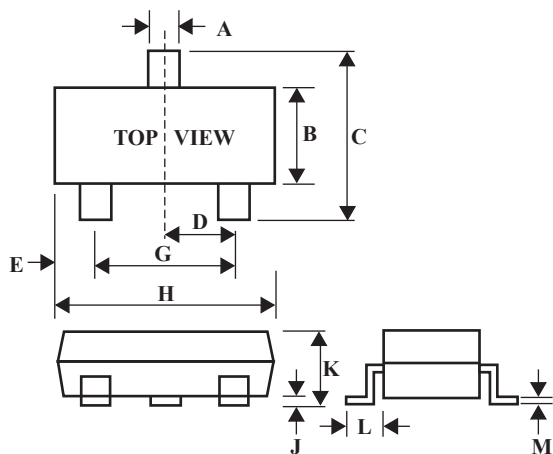


Fig.12 Gate Charge Waveform

SOT-23 Outline Dimension



SOT-23		
Dim	Min	Max
A	0.35	0.51
B	1.19	1.40
C	2.10	3.00
D	0.85	1.05
E	0.46	1.00
G	1.70	2.10
H	2.70	3.10
J	0.01	0.13
K	0.89	1.10
L	0.30	0.61
M	0.076	0.25