# NXP

**Freescale Semiconductor**
Product Brief

# MC9S12P Family

## Low-Cost 16-Bit Microcontroller Family
Covers MC9S12P128, MC9S12P96, MC9S12P64, and MC9S12P32

The MC9S12P family is an optimized, automotive, 16-bit microcontroller product line focused on low-cost, high-performance, and low pin-count. This family is intended to bridge between high-end 8-bit microcontrollers and high-performance 16-bit microcontrollers, such as the MC9S12XS family. The MC9S12P family is targeted at generic automotive applications requiring CAN or LIN/J2602 communication. Typical examples of these applications include body controllers, occupant detection, door modules, seat controllers, RKE receivers, smart actuators, lighting modules, and smart junction boxes.

The MC9S12P family uses many of the same features found on the MC9S12XS family, including error correction code (ECC) on flash memory, a separate data-flash module for diagnostic or data storage, a fast analog-to-digital converter (ATD) and a frequency modulated phase locked loop (IPLL) that improves the EMC performance.

## Contents

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The MC9S12P family will deliver all the advantages and efficiencies of a 16-bit MCU while retaining the low cost, power consumption, EMC, and code-size efficiency advantages currently enjoyed by users of Freescale's existing 8-bit and 16-bit MCU families. Like the MC9S12XS family, the MC9S12P family will run 16-bit wide accesses without wait states for all peripherals and memories. The MC9S12P family will be available in 80-pin QFP, 64-pin LQFP, and 48-pin QFN package options and aims to maximize pin compatibility with the MC9S12XS family. In addition to the I/O ports available in each module, further I/O ports are available with interrupt capability allowing wake-up from stop or wait modes.

# 1     Application Example

The MC9S12P family MCUs are general-purpose devices suitable for a range of application, including:

- Body controllers
- Occupant detection
- Door modules
- Seat controllers
- RKE receivers
- Smart actuators
- Lighting modules
- Smart junction boxes
- Intelligent watchdog

## 1.1     Door Control

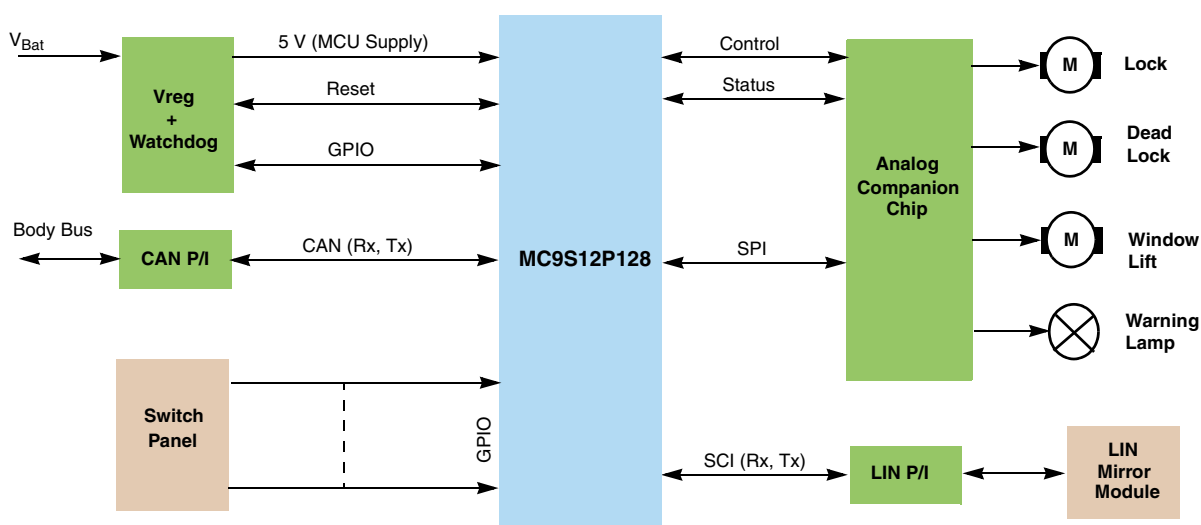Figure 1 outlines a typical door application build around the MC9S12P128 microcontroller.



**Figure 1. Door Application Using MC9S12P128**

# 2 Features

This section describes the key features of the MC9S12P family.

## 2.1 MC9S12P Family Comparison

Table 1 provides a summary of different members of the MC9S12P family and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this microcontroller family.

**Table 1. MC9S12P Family**

| Feature | MC9S12P32 | MC9S12P64 | MC9S12P96 | MC9S12P128 |
|---|---|---|---|---|
| CPU | HCS12 | | | |
| Flash memory (ECC) | 32 Kbytes | 64 Kbytes | 96 Kbytes | 128 Kbytes |
| Data flash (ECC) | 4 Kbytes | | | |
| RAM | 2 Kbytes | 4 Kbytes | 6 Kbytes | |
| MSCAN | 1 | | | |
| SCI | 1 | | | |
| SPI | 1 | | | |
| Timer | 8 ch x 16-bit | | | |
| PWM | 6 ch x 8-bit | | | |
| ADC | 8 ch x 12-bit | | | |
| Frequency modulated PLL | Yes | | | |
| External oscillator (4 – 16 MHz Pierce with loop control) | Yes | | | |
| Internal 1 MHz RC oscillator | Yes | | | |
| Supply voltage | 3.15 V – 5.5 V | | | |
| Execution speed | Static – 32 MHz | | | |
| Package | 64 LQFP, 48 QFN | | 80 QFP, 64 LQFP, 48 QFN | |

## 2.2 Block Diagram

Figure 2 shows a high-level block diagram of the MC9S12P family.
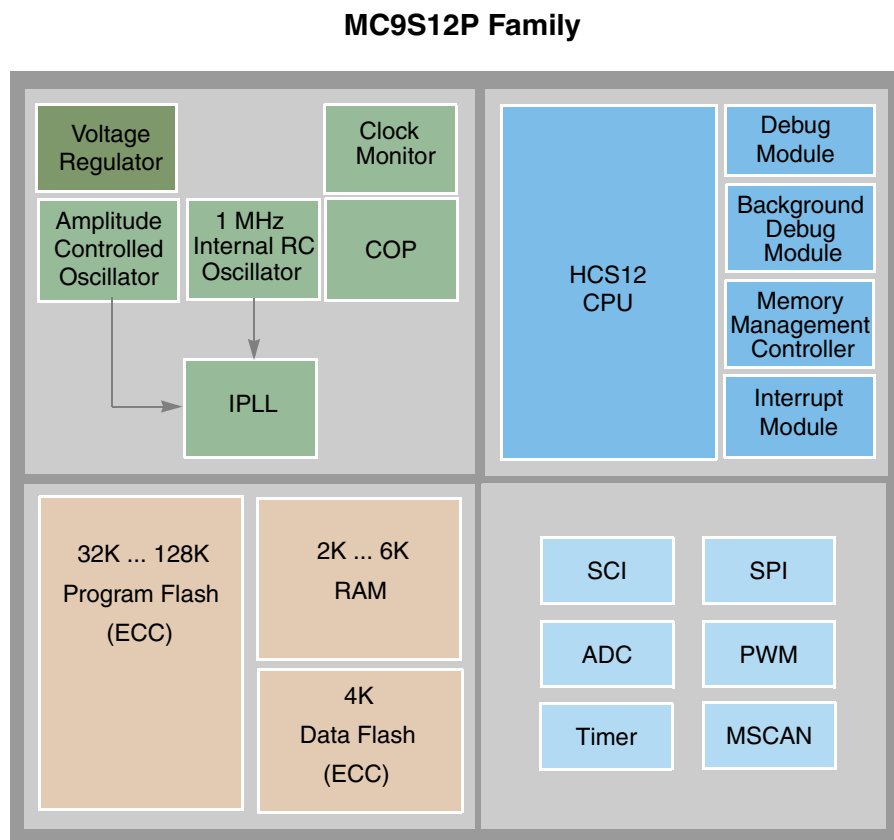
**MC9S12P Family**



Figure 2. MC9S12P Family Block Diagram

## 2.3 Critical Performance Parameters

The critical performance parameters of the MC9S12P feature:

- Operating voltage of 3.15 V to 5.5 V
- Operating temperature ($T_A$) of –40°C to 125°C
- Junction temperature ($T_J$) of up to 150°C
- Bus frequency ($f_{Bus}$) up to 32 MHz
- Packaging:
  — 80-pin QFP, 0.65 mm pitch, 14 mm x 14 mm outline
  — 64-pin LQFP, 0.5 mm pitch, 10 mm x 10 mm outline
  — 48-pin QFN, 0.65 mm pitch, 7 mm x 7 mm outline

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Table 2 describes the MC9S12P family design targets for supply currents.

**Table 2. Current Consumption Target[1]**

| Mode | Condition[2] | Typical[3] | Max[4] |
|---|---|---|---|
| **Run**<br>$f_{osc}$ = 4 MHz, $f_{Bus}$ = 32 MHz,<br>all modules enabled | 25°C, 32 MHz | 25 mA | TBD |
| **Wait**<br>$f_{osc}$ = 4 MHz, $f_{Bus}$ = 32 MHz,<br>all peripherals enabled | 25°C | 20 mA | TBD |
| **Wait**<br>$f_{osc}$ = 4 MHz, $f_{Bus}$ = 8 MHz,<br>all peripherals enabled | 25°C | 5 mA | TBD |
| **Wait**<br>RTI enabled, all peripherals<br>disabled, PLL off | 25°C | 3 mA | TBD |
| **Stop** | –40°C | 20 μA | TBD |
| | 25°C | 25 μA | TBD |
| | 85°C | 150 μA | TBD |
| | 105°C | 300 μA | TBD |
| | 125°C | 450 μA | TBD |

NOTES:
[1] Values to be targeted by design, all values are currently estimates until silicon is available and characterization is performed
[2] All temperatures are based on an ambient air temperature
[3] Target typical current consumption for the mode observed on typical operating conditions and configuration for typical process devices
[4] Target maximum current consumption for mode observed under typical operating conditions and configuration across full process variation of manufactured devices

## 2.3.1    Low Power Operation

The MC9S12P has two dynamic-power modes (run and wait) and one static low-power mode (stop).

- Dynamic power mode: run
  — Run mode is the main full performance operating mode with the entire device clocked. The user can configure the device operating speed through selection of the clock source and the phase locked loop (PLL) frequency. To save power, unused peripherals must not be enabled.

- Dynamic power mode: wait
  — This mode is entered when the CPU executes the WAI instruction. In this mode the CPU will not execute instructions. The internal CPU clock is switched off. All peripherals can be active in system wait mode. For further power consumption the peripherals can individually turn off their local clocks. Asserting $\overline{RESET}$, $\overline{XIRQ}$, $\overline{IRQ}$, or any other interrupt that is not masked ends system wait mode.

- Static power mode: stop
  - The oscillator is stopped in this mode. By default, all clocks are switched off and all counters and dividers remain frozen. The autonomous periodic interrupt (API) and ATD modules may be enabled to self wake the device. A fast wakeup mode is available to allow the device to wake from full stop mode immediately on the internal RC oscillator without starting the oscillator clock.

## 2.4    Chip-Level Features

On-chip modules available within the family include the following features:

- HCS12 CPU core
- Up to 128 Kbyte on-chip flash with ECC
- 4 Kbyte data flash with ECC
- Up to 6 Kbyte on-chip SRAM
- Phase locked loop (IPLL) frequency multiplier with internal filter
- 4–16 MHz amplitude controlled Pierce oscillator
- 1 MHz internal RC oscillator
- Timer module (TIM) supporting input/output channels that provide a range of 16-bit input capture, output compare, counter, and pulse accumulator functions
- Pulse width modulation (PWM) module with 6 x 8-bit channels
- 8-channel, 12-bit resolution successive approximation analog-to-digital converter (ATD)
- One serial peripheral interface (SPI) module
- One serial communication interface (SCI) module supporting LIN communications
- One multi-scalable controller area network (MSCAN) module (supporting CAN protocol 2.0A/B)
- On-chip voltage regulator (VREG) for regulation of input supply and all internal voltages
- Autonomous periodic interrupt (API)

## 2.5    Module Features

The following sections provide more details of the modules implemented on the MC9S12P family.

### 2.5.1    HCS12 16-Bit Central Processor Unit (CPU)

The HCS12 CPU is a high-speed, 16-bit processing unit that has a programming model identical to that of the industry standard M68HC11 central processor unit (CPU).

- Full 16-bit data paths supports efficient arithmetic operation and high-speed math execution
- Supports instructions with odd byte counts, including many single-byte instructions. This allows much more efficient use of ROM space.
- Extensive set of indexed addressing capabilities, including:
  - Using the stack pointer as an indexing register in all indexed operations
  - Using the program counter as an indexing register in all but auto increment/decrement mode

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    — Accumulator offsets using A, B, or D accumulators

    — Automatic index predecrement, preincrement, postdecrement, and postincrement (by –8 to +8)

### 2.5.2 On-Chip Flash with ECC

On-chip flash memory on the MC9S12P on the features the following:

- Up to 128 Kbyte of program flash memory
  - 32 data bits plus 7 syndrome ECC (error correction code) bits allow single bit fault correction and double fault detection
  - Erase sector size 512 bytes
  - Automated program and erase algorithm
  - User margin level setting for reads
  - Protection scheme to prevent accidental program or erase
- 4 Kbyte data flash space
  - 16 data bits plus 6 syndrome ECC (error correction code) bits allow single bit fault correction and double fault detection
  - Erase sector size 256 bytes
  - Automated program and erase algorithm
  - User margin level setting for reads

### 2.5.3 On-Chip SRAM

- Up to 6 Kbytes of general-purpose RAM

### 2.5.4 Main External Oscillator (XOSC)

- Loop control Pierce oscillator using a 4 MHz to 16 MHz crystal
  - Current gain control on amplitude output
  - Signal with low harmonic distortion
  - Low power
  - Good noise immunity
  - Eliminates need for external current limiting resistor
  - Transconductance sized for optimum start-up margin for typical crystals

### 2.5.5 Internal RC Oscillator (IRC)

- Trimmable internal reference clock.
  - Frequency: 1 MHz
  - Untrimmed accuracy over full temperature range: ±14%

— Trimmed accuracy over –40°C to +125°C ambient temperature range: ±2.0%

— Trimmed accuracy over –40°C to +85°C ambient temperature range: ±1.5%

### 2.5.6 Internal Phase-Locked Loop (IPLL)

- Phase-locked-loop clock frequency multiplier
  - No external components required
  - Reference divider and multiplier allow large variety of clock rates
  - Automatic bandwidth control mode for low-jitter operation
  - Automatic frequency lock detector
  - Configurable option to spread spectrum for reduced EMC radiation (frequency modulation)
  - Reference clock sources:
    - External 4–16 MHz resonator/crystal (XOSC)
    - Internal 1 MHz RC oscillator (IRC)

### 2.5.7 Clocks and Reset Generator (CRG)

- COP (computer operating properly) watchdog
- Real time interrupt (RTI)
- Clock monitor (CM)
- Fast wake from stop in self-clock mode for power saving and immediate program execution
- System reset generation

### 2.5.8 System Integrity Support

- Power-on reset (POR)
- Illegal address detection with reset
- Low-voltage detection with interrupt or reset
- Computer operating properly (COP) watchdog
  - Configurable as window COP for enhanced failure detection
  - Can be initialized out of reset using option bits located in flash memory
- Clock monitor supervising the correct function of the oscillator

### 2.5.9 Timer (TIM)

- 8 x 16-bit channels for input capture or output compare
- 16-bit free-running counter with 7-bit precision prescaler
- 1 x 16-bit pulse accumulator

## 2.5.10    Pulse Width Modulation Module (PWM)

- Up to 6 channel x 8-bit or 3 channel x 16-bit pulse width modulator
  — Programmable period and duty cycle per channel
  — Center-aligned or left-aligned outputs
  — Programmable clock select logic with a wide range of frequencies

## 2.5.11    Controller Area Network Module (MSCAN)

- 1 Mbit per second, CAN 2.0 A, B software compatible
  — Standard and extended data frames
  — 0–8 bytes data length
  — Programmable bit rate up to 1 Mbps
- Five receive buffers with FIFO storage scheme
- Three transmit buffers with internal prioritization
- Flexible identifier acceptance filter programmable as:
  — 2 x 32-bit
  — 4 x 16-bit
  — 8 x 8-bit
- Wakeup with integrated low pass filter option
- Loop back for self test
- Listen-only mode to monitor CAN bus
- Bus-off recovery by software intervention or automatically
- 16-bit time stamp of transmitted/received messages

## 2.5.12    Serial Communication Interface Module (SCI)

- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 13-bit baud rate selection
- Programmable character length
- Programmable polarity for transmitter and receiver
- Active edge receive wakeup
- Break detect and transmit collision detect supporting LIN

## 2.5.13 Serial Peripheral Interface Module (SPI)

- Configurable 8- or 16-bit data size
- Full-duplex or single-wire bidirectional
- Double-buffered transmit and receive
- Master or slave mode
- MSB-first or LSB-first shifting
- Serial clock phase and polarity options

## 2.5.14 Analog-to-Digital Converter Module (ATD)

- 8-channel, 12-bit analog-to-digital converter
  - 8-/10-/12-bit resolution
  - 3 μs, 10-bit single conversion time
  - Left or right justified result data
  - External and internal conversion trigger capability
  - Internal oscillator for conversion in stop modes
  - Wakeup from low power modes on analog comparison > or <= match
  - Continuous conversion mode
  - Multiple channel scans
- Pins can also be used as digital I/O

## 2.5.15 On-Chip Voltage Regulator (VREG)

- Linear voltage regulator with bandgap reference
- Low-voltage detect (LVD) with low-voltage interrupt (LVI)
- Power-on reset (POR) circuit
- Low-voltage reset (LVR)

## 2.5.16 Background Debug (BDM)

- Background debug module (BDM) with single-wire interface
  - Non-intrusive memory access commands
  - Supports in-circuit programming of on-chip nonvolatile memory

## 2.5.17 Debugger (DBG)

- Three comparators A, B, and C to monitor CPU buses
  - A compares full address bus and 16-bit data bus with mask register
  - B and C compare address bus only
  - Three modes: simple address/data match, inside address range, or outside address range

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- 64 x 20-bit circular trace buffer to capture change-of-flow addresses or address and data of every access
- Tag-type or force-type hardware breakpoint requests
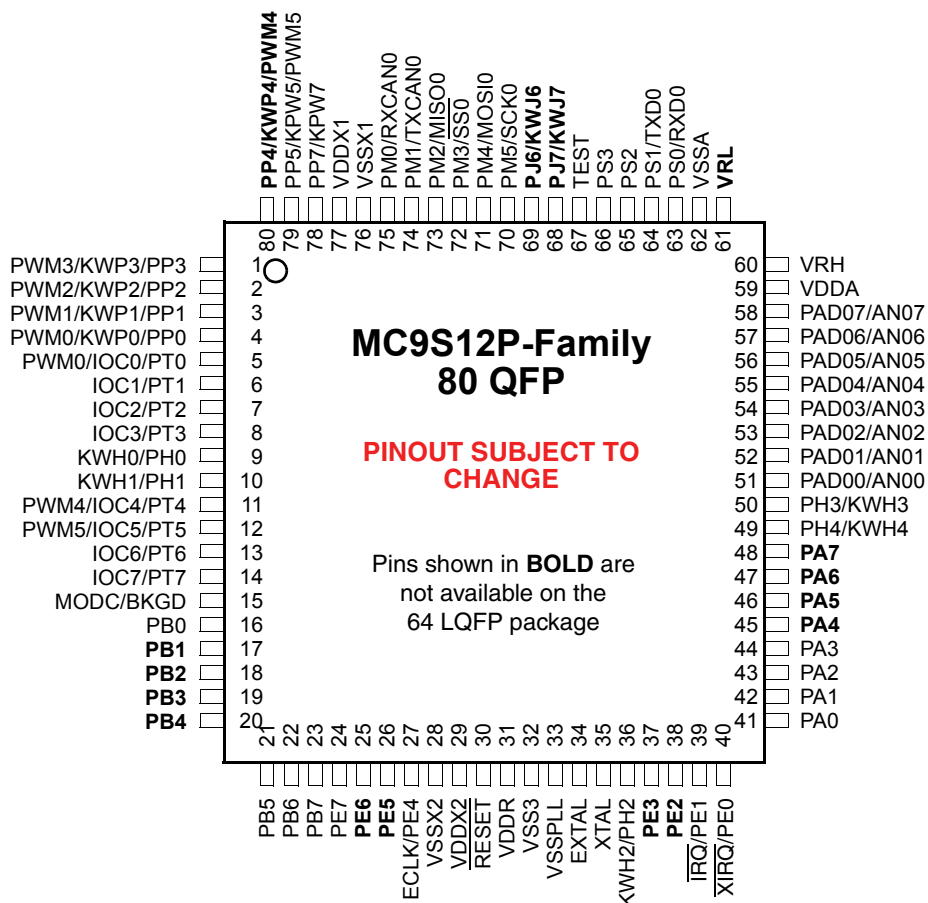
# 3 Pinouts



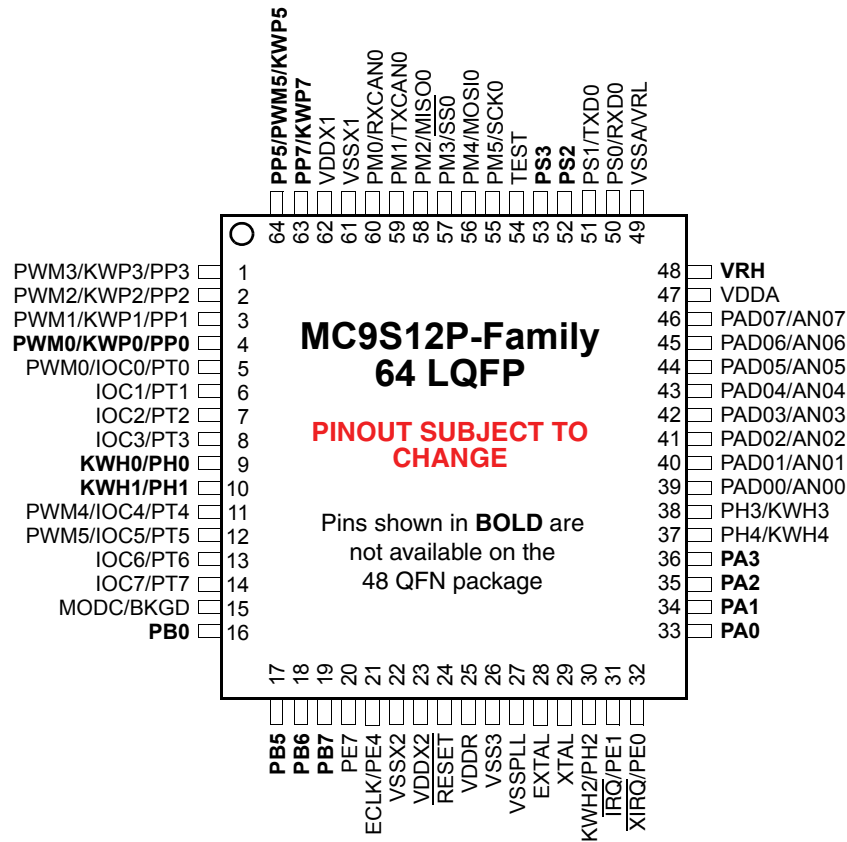**Figure 3. MC9S12P-Family Pin Assignment: 80 QFP Package**

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**Figure 4. MC9S12P-Family Pin Assignment: 64 LQFP Package**

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**Figure 5. MC9S12P-Family Pin Assignment: 48 QFN Package**

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# 4 Developer Environment

The MC9S12P family of MCUs is supported by tools similar to those of other Freescale HCS12 products. The HCS12 MCU family offers a widespread and established network of tools and software vendors.

This development support will be available:

- Automotive evaluation boards (EVB) featuring CAN and LIN interfaces, and more
- Compilers
- Debuggers

This software support will be available:

- CAN and LIN drivers

# 5 Document Revision History

Identifies content changes compared to the previously released version.

**Table 3. Revision History**

| Revision | Location(s) | Substantive Change(s) |
|:---:|---|---|
| 0 | D.Beattie - FSL EKB 12-Feb-07 | 1st draft for review |
| 1 | D.Beattie - FSL EKB 27-Feb-07 | Corrected DBG module features<br>Added Typical Idd estimations<br>Updated RAM sizes<br>Changed block diagram format. |
| 2 | D.Beattie - FSL EKB 02-Mar-07 | Removed 80QFP option for P32<br>1.5% IRC trimmed accuracy (-40 to +85C) |
| 3 | D.Beattie - FSL EKB 05-Apr-07 | Added Pinout diagrams for 80 QFP, 64 LQFP and 48 QFN package options<br>Corrected DBG comparators from 4 to 3 |
| 4 | D.Beattie - FSL EKB 05-Apr-07 | Removed PIT from block diagram |

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