CEL

BIPOLAR ANALOG INTEGRATED CIRCUIT
UPC2763TB

3 V, SUPER MINIMOLD
MEDIUM POWER SI MMIC AMPLIFIER

FEATURES

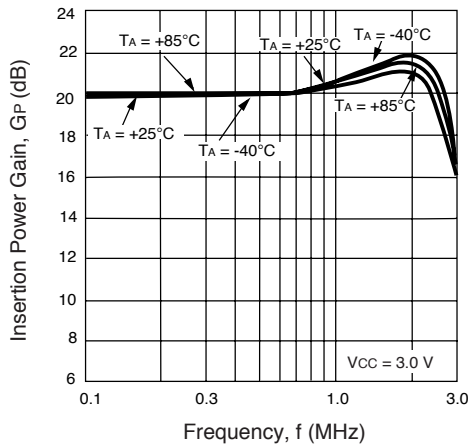
- **HIGH OUTPUT POWER:** P_{SAT} = +11 dBm at 900 MHz
- **LOW VOLTAGE:** 3.0 V TYP, 2.7 V MIN
- **WIDE BANDWIDTH:** 2.7 GHz at -3 dB
- **HIGH GAIN:** 20 dB at 1.9 GHz
- **SUPER SMALL PACKAGE:** SOT-363 package
- **TAPE AND REEL PACKAGING OPTION AVAILABLE**

DESCRIPTION

The UPC2763TB is a Silicon Monolithic integrated circuit which is manufactured using the NESAT™ III process. The NESAT™ III process produces transistors with f_T approaching 20 GHz. The UPC2763TB is pin compatible and has comparable performance to the larger UPC2763T, so it is suitable for use as a replacement to help reduce system size. The IC is housed in a 6 pin super minimold or SOT-363 package. Operating on a 3 volt supply this IC is ideally suited for handheld, portable designs.

Stringent quality assurance and test procedures ensure the highest reliability and performance.

GAIN vs. FREQUENCY AND TEMPERATURE



ELECTRICAL CHARACTERISTICS (T_A = 25°C, Z_L = Z_S = 50 Ω, V_{CC} = 3.0 V)

PART NUMBER PACKAGE OUTLINE			UPC2763TB S06		
SYMBOLS	**PARAMETERS AND CONDITIONS**	**UNITS**	**MIN**	**TYP**	**MAX**
I_{CC}	Circuit Current (no signal)	mA		27	35
G_S	Small Signal Gain, f = 900 MHz f = 1900 MHz	dB dB	18 18	20 21	23 24
f_U	Upper Limit Operating Frequency (The gain at fu is 3 dB down from the gain at 0.1 GHz)	GHz	2.3	2.7	
P_{1dB}	Output Power at 1 dB Compression Point, f = 900 MHz f = 1900 MHz	dBm dBm	+7 +4	+9.5 +6.5	
P_{SAT}	Saturated Output Power, f = 900 MHz f = 1900 MHz	dBm dBm		11 8	
NF	Noise Figure, f = 900 MHz f = 1900 MHz	dB dB		5.5 5.5	7.0 7.5
RL_{IN}	Input Return Loss, f = 900 MHz f = 1900 MHz	dB dB	8 8	11 11	
RL_{OUT}	Output Return Loss, f = 900 MHz f = 1900 MHz	dB dB	5 6	7 9	
ISOL	Isolation, f = 900 MHz f = 1900 MHz	dB dB	25 24	30 29	
OIP_3	SSB Output Third Order Intercept Point f = 900, 902 MHz P_{OUT} = +4 dBm f = 1900, 1902 MHz	dBm dBm		+17 +11	
P_{ADJ}	Adjacent Channel Power, Δf = ±50 KHz f = 900 MHz, π/4 QPSK wave[1], Δf = ±100 KHz P_O = +4 dBm	dBc dBc		-61 -62	

Note:
1. π/4 QPSK modulated wave input, data rate 42 kbps.

ABSOLUTE MAXIMUM RATINGS[1] (T_A = 25°C)

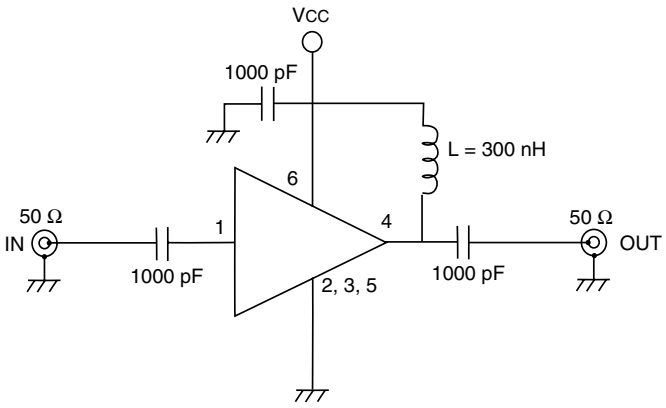
SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{CC}	Supply Voltage	V	3.6
I_{CC}	Total Supply Current	mA	70
P_{IN}	Input Power	dBm	+10
P_T	Total Power Dissipation[2]	mW	200
T_{OP}	Operating Temperature	°C	-40 to +85
T_{STG}	Storage Temperature	°C	-55 to +150

Notes:
1. Operation in excess of any one of these parameters may result in permanent damage.
2. Mounted on a 50 x 50 x 1.6 mm epoxy glass PWB (T_A = 85°C).

RECOMMENDED OPERATING CONDITIONS

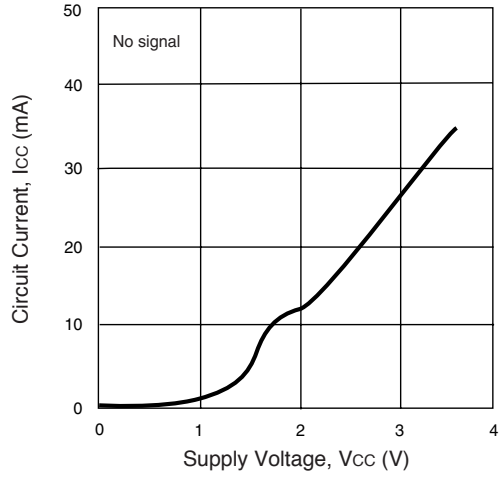
SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V_{CC}	Supply Voltage	V	2.7	3	3.3
T_{OP}	Operating Temperature	°C	-40	25	85

TEST CIRCUIT

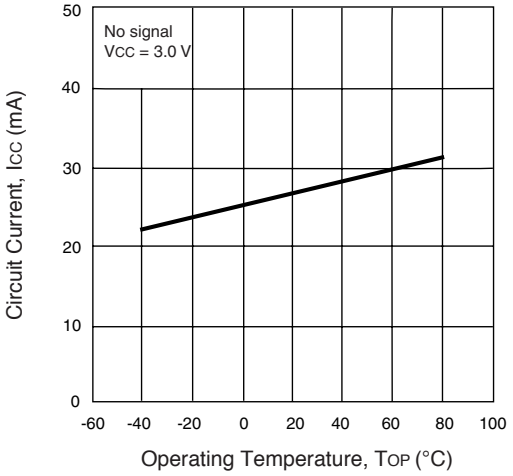


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

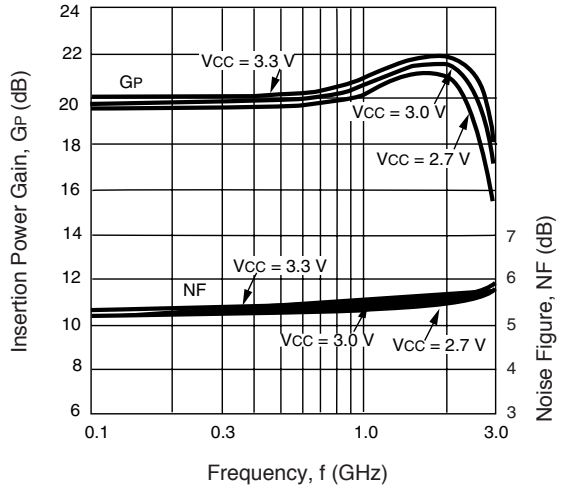
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



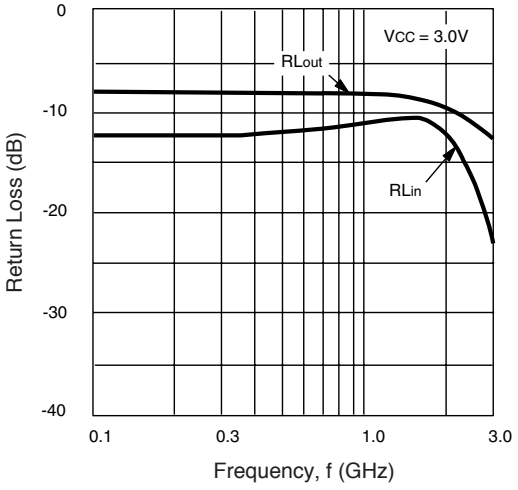
CIRCUIT CURRENT vs. OPERATING TEMPERATURE



NOISE FIGURE AND INSERTION POWER GAIN vs. FREQUENCY AND VOLTAGE

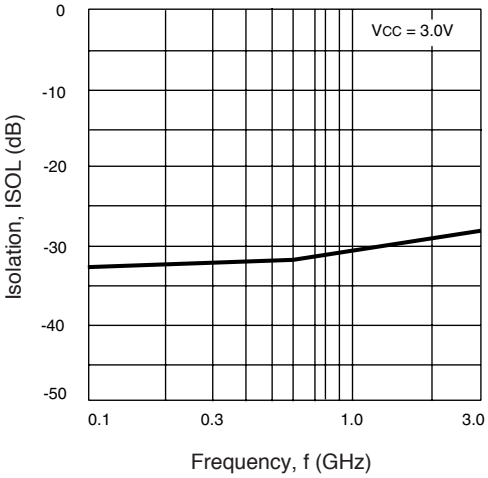


INPUT AND OUTPUT RETURN LOSS vs. FREQUENCY

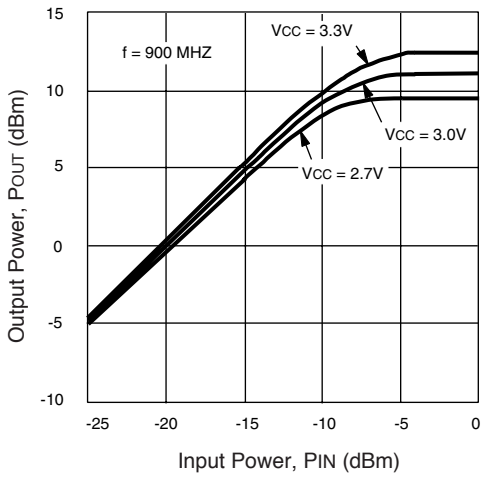


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

ISOLATION vs. FREQUENCY



OUTPUT POWER vs. INPUT POWER AND VOLTAGE



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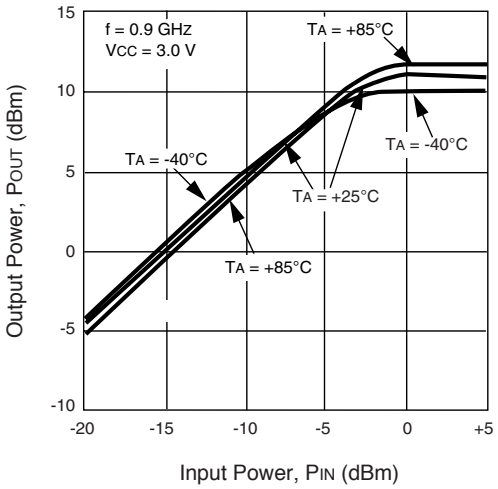

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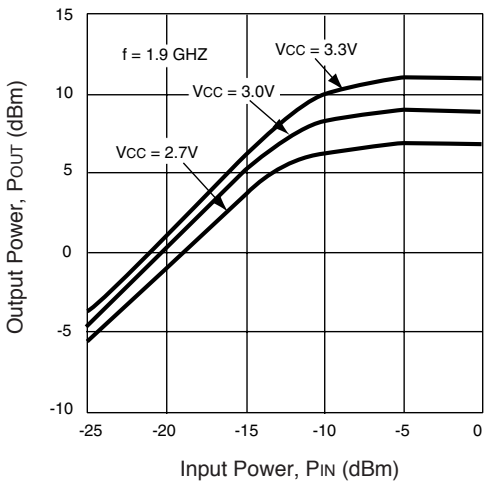

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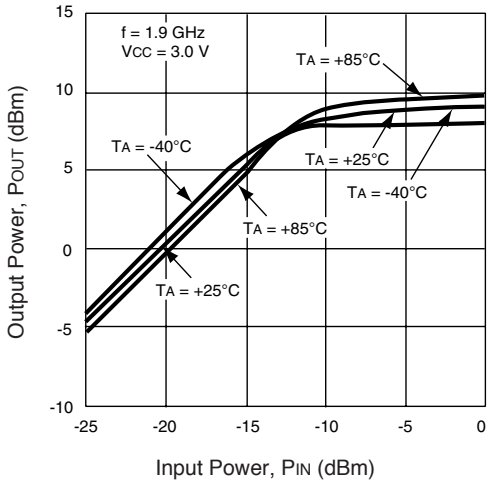
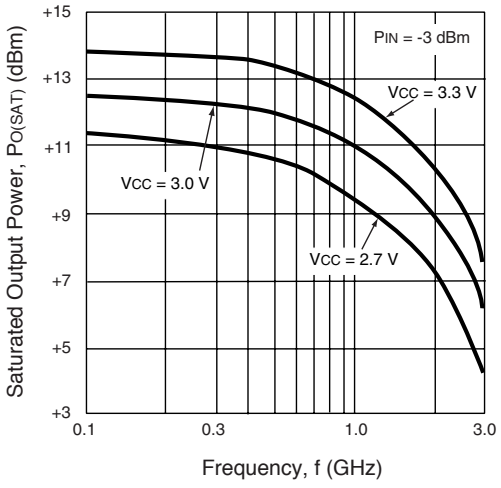
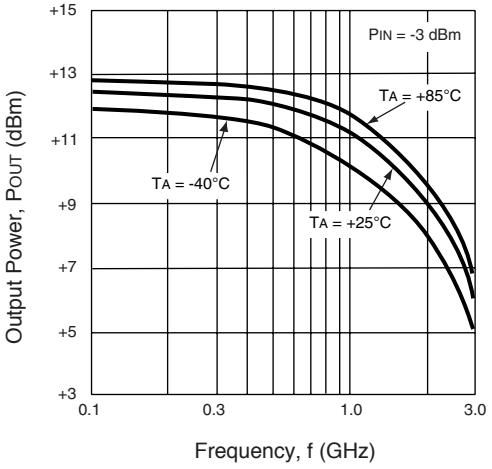


SATURATED OUTPUT POWER vs. FREQUENCY AND VOLTAGE

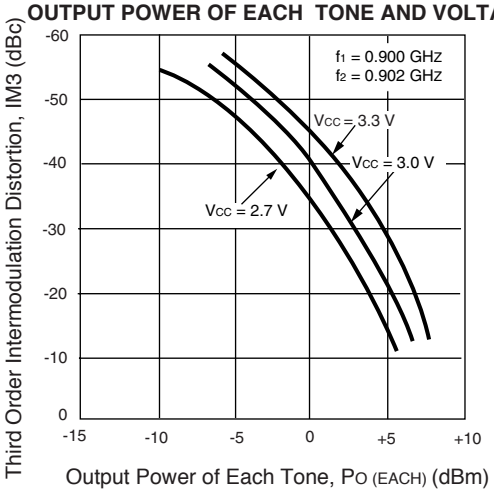


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

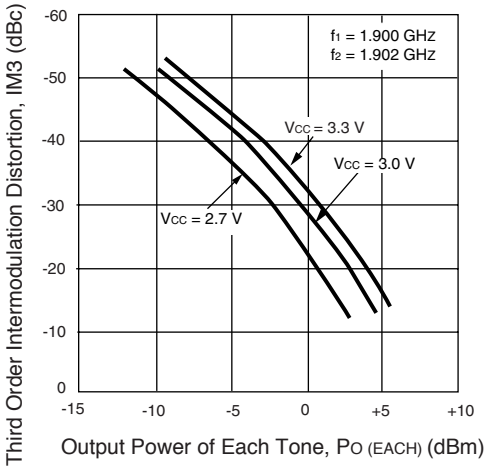
SATURATED OUTPUT POWER vs. FREQUENCYAND TEMPERATURE



THIRD ORDER INTERMODULATION DISTORTION vs. OUTPUT POWER OF EACH TONE AND VOLTAGE

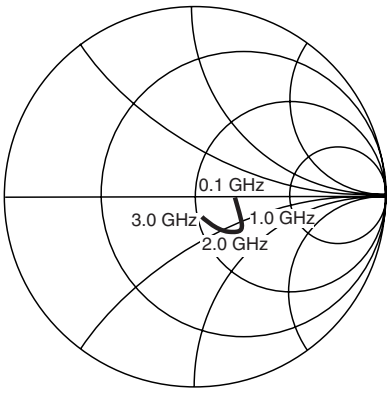


THIRD ORDER INTERMODULATION DISTORTION vs. OUTPUT POWER OF EACH TONE AND VOLTAGE

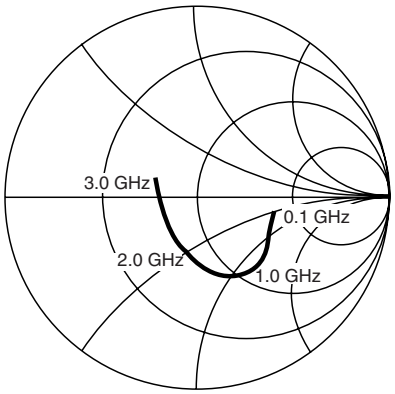


TYPICAL SCATTERING PARAMETERS (T_A = +25°C, V_{CC} = V_{OUT} = 3.0 V)

S11



S22

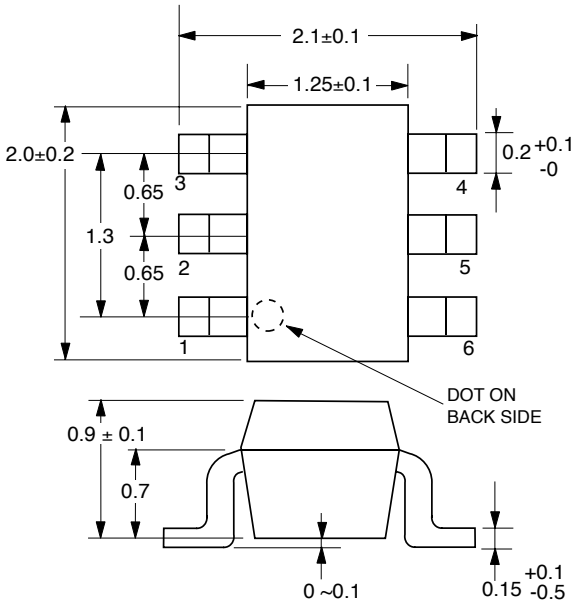


V_{CC} = V_{OUT} = 3.0 V, I_{CC} = 28 mA

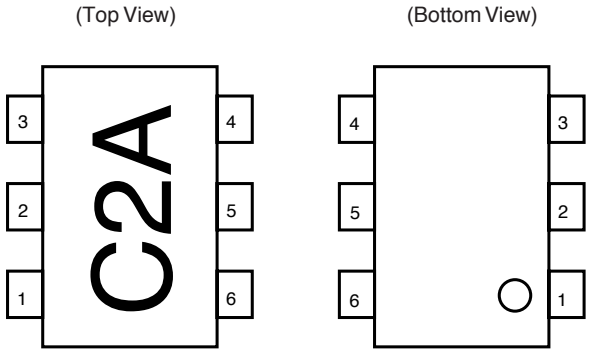
FREQUENCY	S_{11}		S_{21}		S_{12}		S_{22}		K
GHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	
0.1	0.231	-1.4	10.210	-3.8	0.023	2.4	0.406	-4.1	1.68
0.2	0.242	-0.2	10.305	-8.5	0.023	7.8	0.412	-7.5	1.66
0.3	0.250	2.7	10.464	-12.9	0.024	9.3	0.407	-9.9	1.58
0.4	0.425	2.8	10.655	-18.2	0.024	13.4	0.407	-13.9	1.55
0.5	0.242	2.0	10.863	-22.8	0.026	16.1	0.405	-17.6	1.44
0.6	0.241	-2.2	11.093	-28.1	0.027	19.9	0.414	-21.6	1.37
0.7	0.263	-5.3	11.544	-33.2	0.028	22.3	0.419	-24.6	1.25
0.8	0.291	-5.6	11.843	-39.0	0.029	22.5	0.424	-27.7	1.16
0.9	0.316	-5.1	12.291	-45.1	0.029	23.9	0.424	-31.9	1.09
1.0	0.322	-4.0	12.676	-52.4	0.030	25.6	0.425	-37.1	1.02
1.1	0.318	-5.4	13.066	-59.8	0.031	24.1	0.438	-42.5	0.96
1.2	0.309	-9.0	13.311	-67.3	0.031	27.0	0.442	-47.8	0.96
1.3	0.322	-14.2	13.661	-75.8	0.033	28.8	0.441	-51.2	0.90
1.4	0.344	-20.6	13.845	-83.9	0.033	28.5	0.434	-56.0	0.87
1.5	0.371	-23.7	13.824	-93.0	0.035	30.1	0.435	-62.2	0.82
1.6	0.380	-27.5	13.890	-101.5	0.035	28.1	0.439	-68.9	0.80
1.7	0.388	-30.6	13.634	-110.5	0.036	29.2	0.439	-74.6	0.78
1.8	0.378	-36.4	13.236	-119.6	0.035	29.9	0.428	-81.3	0.84
1.9	0.378	-42.1	12.724	-127.9	0.035	30.9	0.411	-87.0	0.89
2.0	0.375	-46.6	12.290	-136.1	0.035	32.9	0.393	-93.4	0.94
2.1	0.369	-50.5	11.707	-144.0	0.035	33.0	0.385	-99.6	0.99
2.2	0.351	-53.8	11.130	-151.7	0.036	35.7	0.373	-104.9	1.06
2.3	0.331	-59.8	10.524	-159.1	0.036	36.8	0.359	-110.3	1.13
2.4	0.306	-66.4	9.824	-165.9	0.034	38.7	0.336	-117.5	1.31
2.5	0.300	-73.1	9.152	-172.3	0.035	40.1	0.321	-123.3	1.41
2.6	0.294	-75.8	8.583	-178.2	0.034	43.8	0.306	-129.4	1.55
2.7	0.290	-77.1	8.029	176.2	0.035	46.3	0.299	-133.9	1.58
2.8	0.270	-77.7	7.610	170.6	0.037	47.7	0.288	-138.6	1.63
2.9	0.248	-78.7	7.240	166.1	0.039	51.1	0.270	-143.6	1.67
3.0	0.219	-82.3	6.827	161.2	0.039	53.6	0.253	-150.1	1.79
3.1	0.198	-88.7	6.516	156.9	0.040	55.1	0.244	-156.2	1.88

OUTLINE DIMENSIONS (Units in mm)

PACKAGE OUTLINE S06

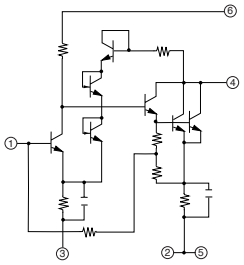


LEAD CONNECTIONS



1. INPUT
2. GND
3. GND
4. OUTPUT
5. GND
6. V_{CC}

PIN DESCRIPTIONS

Pin No.	Pin Name	Applied Voltage (V)	Description	Internal Equivalent Circuit
1	Input	–	Signal input pin. An internal matching circuit, configured with resistors, enables 50 Ω connection over a wide bandwidth. A multi-feedback circuit is designed to cancel the deviations of h_{FE} and resistance. This pin must be coupled to the signal source with a blocking capacitor.	
4	Output	2.7 to 3.3	Signal output pin. Connect an inductor between this pin and V_{CC} to supply current to the internal output transistors.	
6	V_{CC}		Power supply pin. This pin should be externally equipped with a bypass capacitor to minimize ground impedance.	
2 3 5	GND	0	Ground pins. These pins should be connected to system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. All the ground pins must be connected together with wide ground pattern to minimize impedance difference.	

ORDERING INFORMATION

PART NUMBER	QTY
UPC2763TB-E3-A	3K/Reel

Note:
Embossed Tape, 8 mm wide. Pins 1, 2 and 3 face perforated side of tape.