DATA SHEET

PCK210

Low voltage dual 1:5 differential ECL/PECL clock driver

Product data
Supersedes data of 2002 Dec 13

2004 Apr 23

Philips
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Low voltage dual 1:5 differential ECL/PECL clock driver

PCK210

FEATURES

- 85 ps part-to-part skew typical
- 20 ps output-to-output skew typical
- Differential design
- V_{BB} output
- Voltage and temperature compensated outputs
- Low voltage V_{EE} range of –2.25 V to –3.8 V
- 75 kΩ input pull-down resistors
- Form, fit, and function compatible with MC100EP210

DESCRIPTION

The PCK210 is a low skew 1-to-5 dual differential driver, designed with clock distribution in mind. The input signals can be either differential or single-ended if the V_{BB} output is used. The signal is fanned out to 5 identical differential outputs.

The PCK210 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate-to-gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent t_{PD} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met, it is necessary that both sides of the differential output are terminated into 50 Ω, even if only one side is being used. In most applications, all ten differential pairs will be used, and therefore terminated. In the case where fewer than ten pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20 ps) of the output(s) being used, which, while not being catastrophic to most designs, will mean a loss of skew margin.

The PCK210, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the PCK210 to be used for high performance clock distribution in +3.3 V or +2.5 V systems. Designers can take advantage of the PCK210's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies.

The PCK210 may be driven single-endedly utilizing the V_{BB} bias output with the $\overline{CLKA}$ or $\overline{CLKB}$ input. If a single-ended signal is to be used, the V_{BB} pin should be connected to the $\overline{CLKA}$ or $\overline{CLKB}$ input and bypassed to ground via a 0.01 µF capacitor. The V_{BB} output can only source/sink 0.3 mA, therefore, it should be used as a switching reference for the PCK210 only. Part-to-part skew specifications are not guaranteed when driving the PCK210 single-endedly.

PINNING

Pin configurations

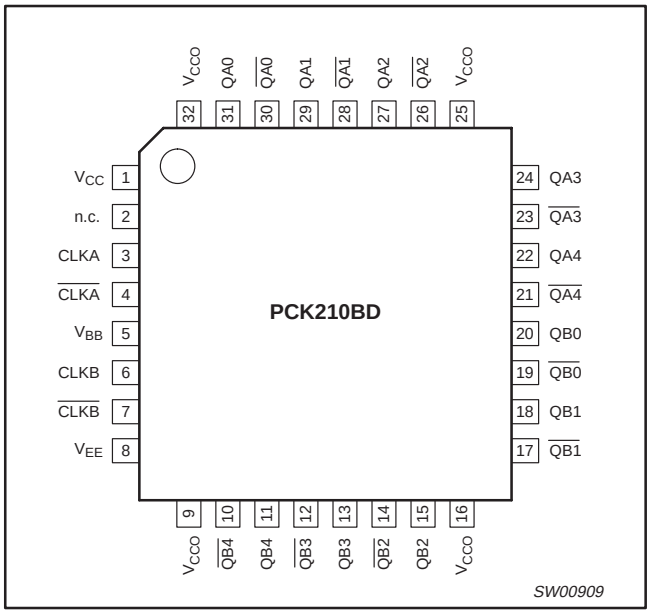


Figure 1. LQFP32 pin configuration

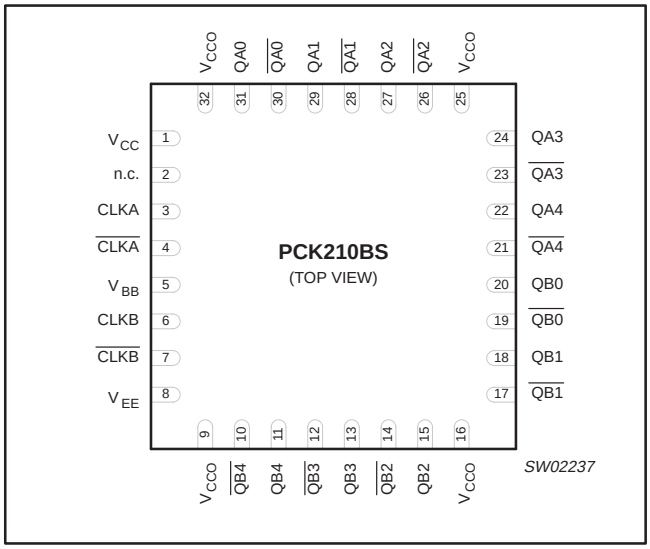


Figure 2. HVQFN32 pin configuration

ORDERING INFORMATION

Type number	Package			Temperature range
	Name	Description	Version	
PCK210BD	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1	–40 °C to +85 °C
PCK210BS	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-1	–40 °C to +85 °C

Pin description

SYMBOL	PIN	DESCRIPTION
V_{CC}	1	Supply voltage
n.c.	2	not connected
CLKA, $\overline{CLKA}$	3, 4	Differential input pair
V_{BB}	5	V_{BB} output
CLKB, $\overline{CLKB}$	6, 7	Differential input pair
V_{EE}	8	Ground
V_{CCO}	9, 16, 25, 32	Output drive power supply voltage
QA0–QA4, QB0–QB4	31, 29, 27, 24, 22, 20, 18, 15, 13, 11	Differential outputs
$\overline{QA0}$–$\overline{QA4}$, $\overline{QB0}$–$\overline{QB4}$	30, 28, 26, 23, 21, 19, 17, 14, 12, 10	Differential outputs

LOGIC SYMBOL

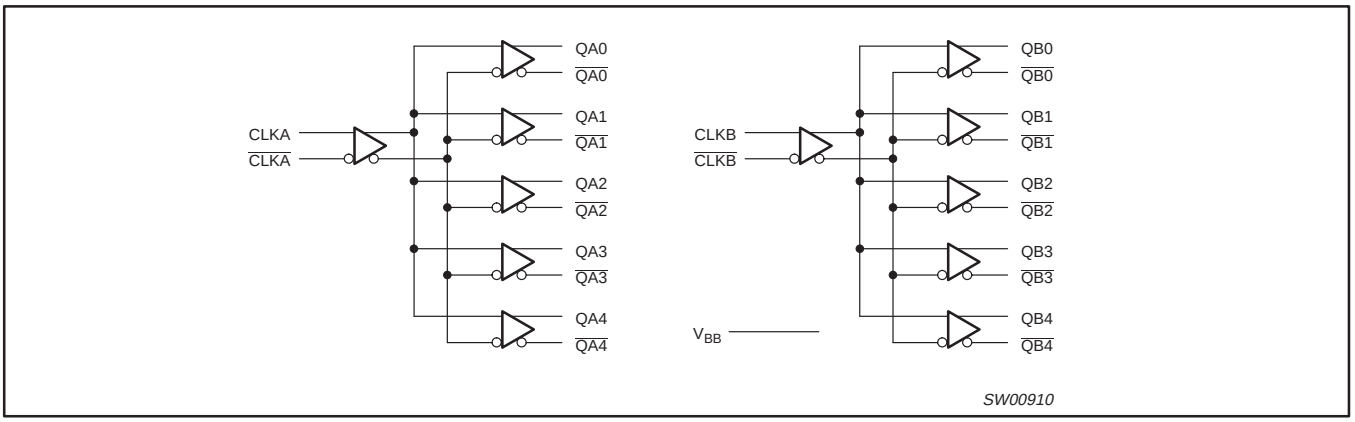


Figure 3. Logic symbol

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	–0.3	+4.6	V
V_I	Input voltage	–0.3	V_{CC} + 0.3	V
I_{IN}	Input current	–	±20	mA
T_{stg}	Storage temperature range	–40	+125	°C
ESD_{HBM}	Electrostatic discharge (Human Body Model; 1.5 kΩ, 100 pF)	–	>1750	V
ESD_{MM}	Electrostatic discharge (Machine Model; 0 kΩ, 100 pF)	–	>200	V
ESD_{CDM}	Electrostatic discharge (Charge Device Model)	–	>1000	V

NOTE:

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage		2.25	3.8	V
V_{IR}	Receiver input voltage		V_{EE}	V_{CC}	V
V_{DIFF}	Input differential voltage[1]	$V_{(CLKinN)–V(CLKin)}$	—	1.00	V
T_{amb}	Operating ambient temperature range in free air		–40	+85	°C

NOTE:

1. To idle an unused differential clock input, connect one input terminal (e.g. CLK1) to V_{BB} and leave its complimentary input terminal (e.g. $\overline{CLK1}$) open-circuit, in which case $\overline{CLK1}$ will default LOW by its internal pull-down reistor. Inputs should not be shorted to ground or V_{CC}.

THERMAL CHARACTERISTICS

Proper thermal management is critical for reliable system operation. This is especially true for high fan-out and high drive capability products.

DC ELECTRICAL CHARACTERISTICS

V_{supply}: $V_{CC} = V_{CCO} = 0.0$ V; $V_{EE} = -2.25$ V to -3.80 V.

SYMBOL	PARAMETER	CONDITIONS	–40 °C		+25 °C		+85 °C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
I_{EE}	Internal supply current	Absolute value of current	20	80	20	85	30	90	mA
I_{CC}	Output and internal supply current	All outputs terminated 50 Ω to $V_{CC} - 2.0$ V	270	390	270	395	270	405	mA
I_{IN}	Input current	Includes pull-up/pull-down resistors	–	150	–	150	–	150	µA
V_{BB}	Internally generated bias voltage	for $V_{EE} = -2.25$ V to -3.8 V	–1.38	–1.16	–1.38	–1.16	–1.38	–1.16	V
V_{PP}	Input amplitude	Difference of input $\approx V_{IH} - V_{IL}$ (Note 1)	0.5	1.3	0.5	1.3	0.5	1.3	V
V_{CMR}	Common mode voltage	Crosspoint of input $\approx$ average (V_{IH}, V_{IL})	V_{EE} + 1.0	–0.3	V_{EE} + 1.0	–0.3	V_{EE} + 1.0	–0.3	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -30$ mA	–1.30	–0.95	–	–	–1.20	–0.85	V
V_{OL}	LOW-level output voltage	$I_{OL} = -5$ mA	–1.85	–1.40	–	–	–1.90	–1.50	V
V_{OUTpp}	Differential output swing		350	–	–	–	500	–	mV

DC ELECTRICAL CHARACTERISTICS

V_{supply}: $V_{CC} = V_{CCO} = 2.25$ V to 3.80 V; $V_{EE} = 0.0$ V.

SYMBOL	PARAMETER	CONDITIONS	–40 °C		+25 °C		+85 °C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
I_{EE}	Internal supply current	Absolute value of current	20	80	20	85	30	90	mA
I_{CC}	Output and internal supply current	All outputs terminated 50 Ω to $V_{CC} - 2.0$ V	270	390	270	395	270	405	mA
I_{IN}	Input current	Includes pull-up/ pull-down resistors	–	150	–	150	–	150	µA
V_{BB}	Internally generated bias voltage	$V_{CC} = 2.25$ V to 3.8 V	$V_{CC} - 1.38$	$V_{CC} - 1.16$	$V_{CC} - 1.38$	$V_{CC} - 1.16$	$V_{CC} - 1.38$	$V_{CC} - 1.16$	V
V_{PP}	Input amplitude	Difference of input $\approx V_{IH} - V_{IL}$ (Note 1)	0.5	1.3	0.5	1.3	0.5	1.3	V
V_{CMR}	Common mode voltage	Crosspoint of input $\approx$ average (V_{IH}, V_{IL})	1	$V_{CC} - 0.3$	1	$V_{CC} - 0.3$	1	$V_{CC} - 0.3$	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -30$ mA	$V_{CC} - 1.30$	$V_{CC} - 0.95$	–	–	$V_{CC} - 1.20$	$V_{CC} - 0.85$	V
V_{OL}	LOW-level output voltage	$I_{OL} = -5$ mA	$V_{CC} - 1.85$	$V_{CC} - 1.40$	–	–	$V_{CC} - 1.90$	$V_{CC} - 1.50$	V
V_{OUTpp}	Differential output swing		350	–	–	–	500	–	mV

NOTE:
1. V_{PP} minimum and maximum required to maintain AC specifications. Actual device function will tolerate minimum V_{PP} of 100 mV.

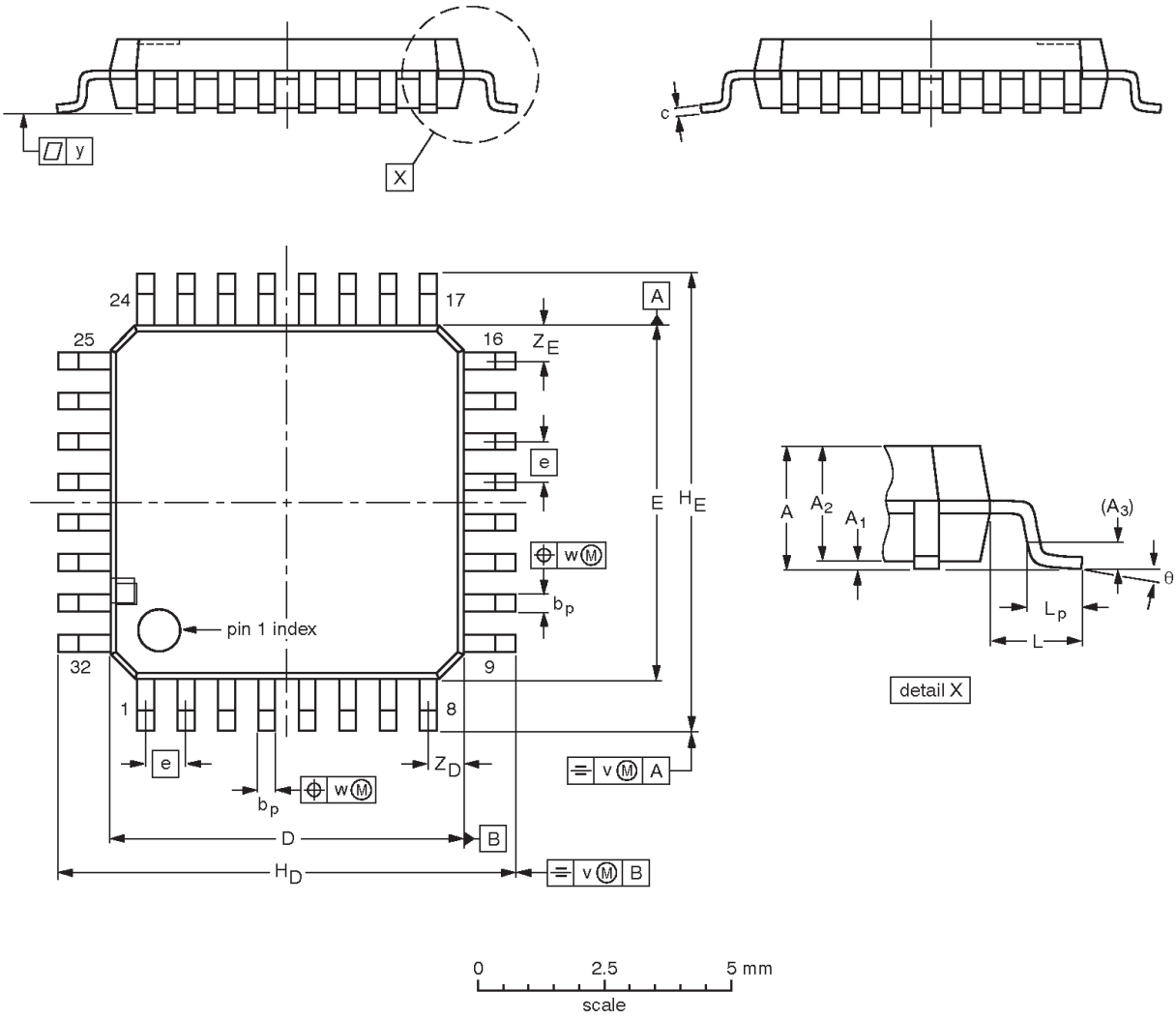
AC CHARACTERISTICS — PECL input

V_{supply}: $V_{CC} = V_{CCO}$ = 2.25 V to 3.80 V; V_{EE} = 0.0 V *–OR–* $V_{CC} = V_{CCO}$ = 0.0 V; V_{EE} = –2.25 V to –3.80 V.

SYMBOL	PARAMETER	CONDITIONS	–40 °C			+25 °C			+85 °C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Differential propagation delay CLK,$\overline{CLK}$ to all Q0,$\overline{Q0}$ through Q4,$\overline{Q4}$	Nominal (single input condition) V_{PP} = 0.650 V, $V_{CMR} = V_{CC} – 0.800$ V Applies to 500 MHz reference. (Note 1)	270	–	420	300	–	450	380	–	530	ps
$t_{SK(part)}$	Part-to-part skew	Single input condition (Note 1)	–	–	110	–	–	110	–	–	110	ps
$t_{SK(output)}$	Output-to-output skew for given part	Single input condition (Note 1)	–	15	50	–	15	50	–	15	50	ps
t_{PD}	Differential propagation delay CLK,$\overline{CLK}$ to all Q0,$\overline{Q0}$ through Q4,$\overline{Q4}$	All input conditions (Note 1)	220	–	520	250	–	550	320	–	620	ps
$t_{SK(part)}$	Part-to-part skew	(Note 1)	–	–	160	–	–	160	–	–	160	ps
$t_{SK(output)}$	Output-to-output skew for given part	(Note 1)	–	15	50	–	15	50	–	15	50	ps
t_{jitter}	Cyle-to-cycle jitter		–	–	1	–	–	1	–	–	1	ns
f_{MAX}	Maximum frequency	Functional to 1.5 GHz Timing specifications apply up to 1.0 GHz	–	–	1500	–	–	1500	–	–	1500	MHz
t_r, t_f	Output rise and fall times (20%, 80%)	(Note 1)	100	–	320	100	–	320	100	–	320	ps

NOTE:
1. For operation with 2.5 V supply, the output termination is 50 Ω to V_{EE}.
   For operation at 3.3 V supply, the output termination is 50 Ω to V_{CC} – 2 V.

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm SOT358-1



DIMENSIONS (mm are the original dimensions)

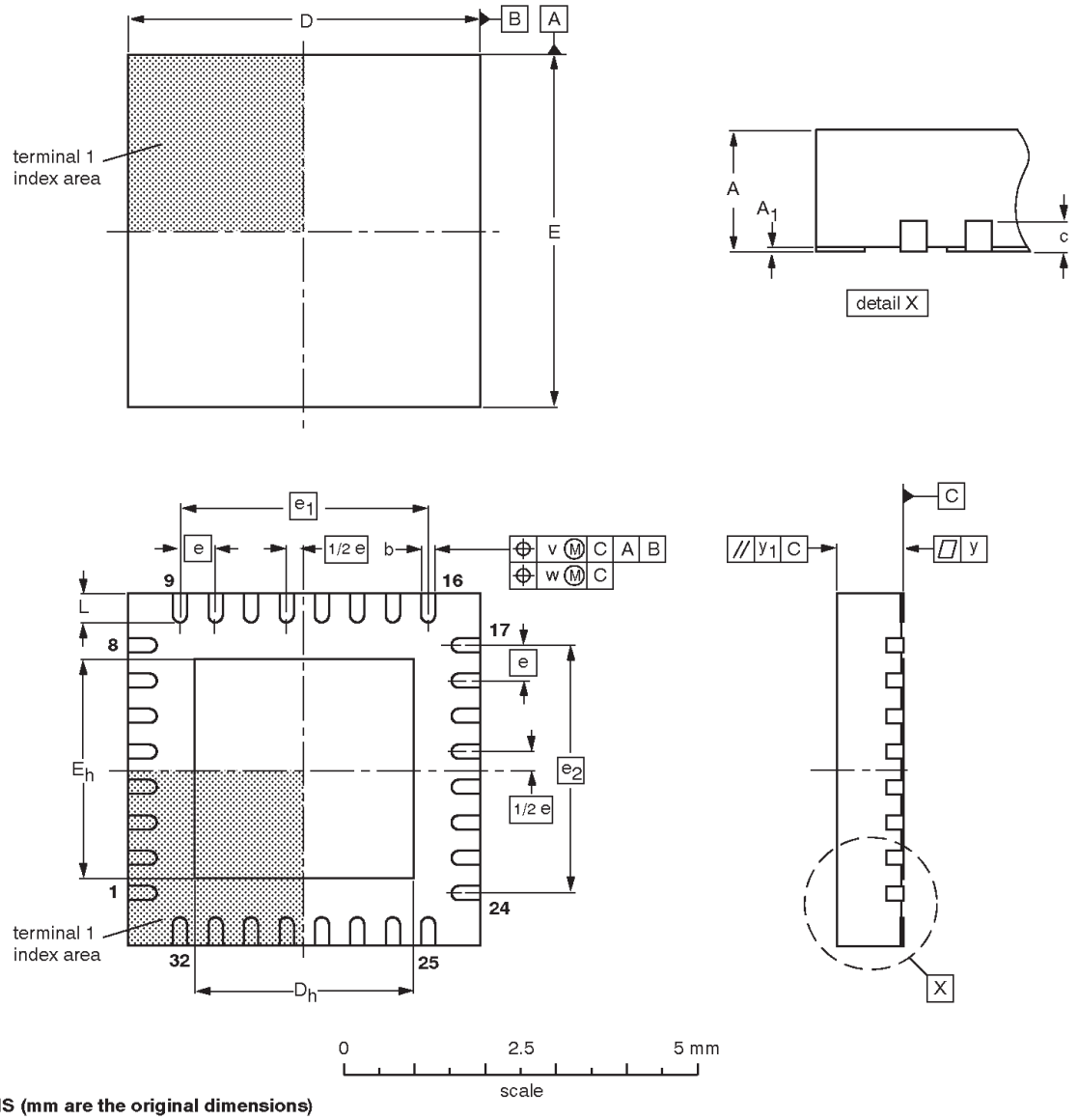
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT358 -1	136E03	MS-026				~~00-01-19~~ 03-02-25

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

REVISION HISTORY

Rev	Date	Description
_3	20040423	**Product data (9397 750 13083). Supersedes data of 2002 Dec 13 (9397 750 10866).** Modifications: ● Add Part type PCK210BS, HVQFN32 package option (SOT617-1). ● Change temperature range in Ordering information table on page 2 from “–40 to +70 °C” to “–40 °C to +85 °C”.
_2	20021213	**Product data (9397 750 10866); ECN 853-2336 29225 of 22 November 2002.** ● NOTE: date shown on cover (2002 Nov 13) is incorrect. It should be “2002 Dec 13” as shown on all other pages and this Revision history table.
_1	20020411	**Product data (9397 750 09657); ECN 853-2336 27995 of 11 April 2002.**

Low voltage dual 1:5 differential ECL/PECL clock driver

PCK210

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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