FAIRCHILD
A Schlumberger Company

μA96172 • μA96174 Quad Differential Line Drivers

Linear Division Interface Products

Description

The μA96172 and μA96174 are high speed quad differential line drivers designed to meet EIA Standard RS-485. The devices have three-state outputs and are optimized for balanced multipoint data bus transmission at rates up to 10 Mbps. The drivers have wide positive and negative common mode range for multipoint applications in noisy environments. Positive and negative current-limiting is provided which protects the drivers from line fault conditions over a +12 V to −7.0 V common mode range. A thermal shutdown feature is also provided and occurs at junction temperature of approximately 160°C. The μA96172 features an active high and active low Enable, common to all four drivers. The μA96174 features separate active high Enables for each driver pair. Compatible RS-485 receivers, transceivers, and repeaters are also offered by Fairchild and are designed to provide optimum bus performance. The respective device types are μA96173/96175, μA96176, and μA96177/96178.

- **Meets EIA Standard RS-485 And RS-422A**
- **Monotonic Differential Output Switching**
- **Transmission Rate To 10 Mbs**
- **Three-State Outputs**
- **Designed For Multipoint Bus Transmission**
- **Common Mode Output Voltage Range: −7.0 V To +12 V**
- **Operates From Single +5.0 V Supply**
- **Thermal Shutdown Protection**
- **μA96172/96174 Are Lead And Function Compatible with the SN75172/75174 or the AM26LS31/MC3487 respectively**

Function Table (Each Driver) μA96172

Input	Enables		Outputs	
A	E	$\overline{E}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

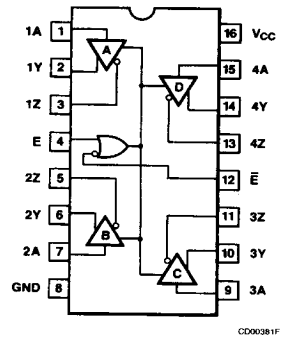
Function Table (Each Driver) μA96174

Input	Enable	Outputs	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

Connection Diagram 16-Lead DIP (Top View)

μA96172



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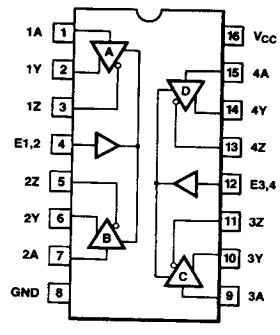

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Order Information

Device Code	Package Code	Package Description
μA96172DC	7B	Ceramic DIP
μA96172PC	9B	Molded DIP
μA96174DC	7B	Ceramic DIP
μA96174PC	9B	Molded DIP

Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Supply Voltage[3]	7.0 V
Enable Input Voltage	5.5 V

Notes
1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.
3. All voltages are with respect to network ground terminal.

Recommended Operating Conditions

Symbol	Characteristic	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{OC}	Common Mode Output Voltage	−7.0[1]		+12.0	V
I_{OH}	Output Current HIGH			−60	mA
I_{OL}	Output Current LOW			60	mA
T_A	Operating Temperature	0	25	70	°C

Note
1. The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

μA96172, μA96174

Electrical Characteristics Over recommended temperature and supply voltage ranges, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit
V_{IH}	Input Voltage HIGH		2.0			V
V_{IL}	Input Voltage LOW				0.8	V
V_{OH}	Output Voltage HIGH	I_{OH} = −20mA		3.1		V
V_{OL}	Output Voltage LOW	I_{OL} = 20mA		0.8		V
V_{IC}	Input Clamp Voltage	I_I = −18 mA			−1.5	V
$\lvert V_{OD1} \rvert$	Differential Output Voltage	I_O = 0 mA			6.0	V
$\lvert V_{OD2} \rvert$	Differential Output Voltage	R_L = 54 Ω, Fig. 1a R_L = 100 Ω, Fig. 1b	1.5 2.0	2.0 2.3		V V
$\Delta\lvert V_{OD} \rvert$	Change in Magnitude of Differential Output Voltage[2]	R_L = 54 Ω or 100 Ω, Fig. 1b			±0.2	V

μA96172, μA96174 (Cont.)
Electrical Characteristics Over recommended temperature and supply voltage ranges, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Typ[1]	Max	Unit
V_{OC}	Common Mode Output Voltage[3]					3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage[2]					±0.2	V
I_O	Output Current with Power off	V_{CC} = 0 V, V_O = −7.0 V to 12 V				±100	μA
I_{OZ}	High Impedance State Output Current	V_O = −7.0 V to 12 V			±50	±200	μA
I_{IH}	Input Current HIGH	V_I = 2.7 V				20	μA
I_{IL}	Input Current LOW	V_I = 0.5 V				−100	μA
I_{OS}	Short Circuit Output Current	V_O = −7.0 V				−250	mA
		V_O = 0 V				−150	
		V_O = V_{CC}				150	
		V_O = 12 V				250	
I_{CC}	Supply Current (all drivers)	No load	Outputs Enabled		50	70	mA
			Outputs Disabled		50	60	

Switching Characteristics V_{CC} = 5.0 V, T_A = 25°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{DD}	Differential Output Delay Time	R_L = 60 Ω, Fig. 2		15	25	ns
t_{TD}	Differential Output Transition Time			15	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27 Ω, Fig. 3		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			12	20	ns
t_{PZH}	Output Enable Time to High Level	R_L = 110 Ω, Fig. 4		30	45	ns
t_{PZL}	Output Enable Time to Low Level	R_L = 110 Ω, Fig. 5		30	45	ns
t_{PHZ}	Output Disable Time from High Level	R_L = 110 Ω, Fig. 4		25	35	ns
t_{PLZ}	Output Disable Time from Low Level	R_L = 110 Ω, Fig. 5		30	45	ns

Notes
1. All typical values are V_{CC} = 5.0 V and T_A = 25°C.
2. $\Delta\ |V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
3. In EIA Standard RS-422A and RS-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltages, V_{OS}.

Parameter Measurement Information

Figure 1a Differential Output Voltage with Varying Common Mode Voltage

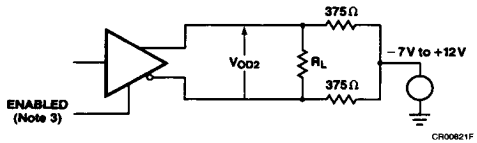


Figure 1b Differential and Common Mode Output Voltage

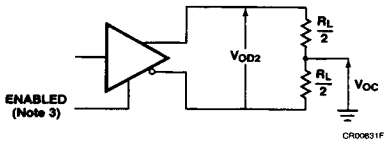
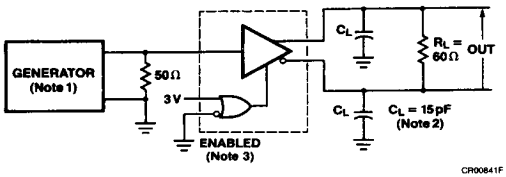


Figure 2 Differential Output Delay and Transition Times



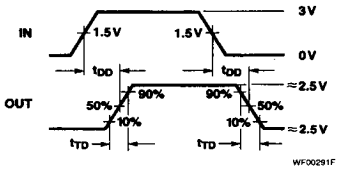
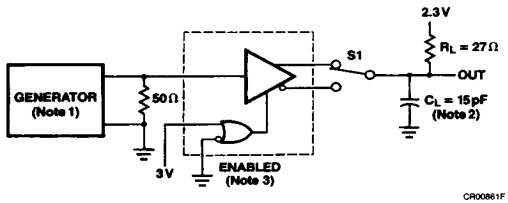


Figure 3 Propagation Delay Times



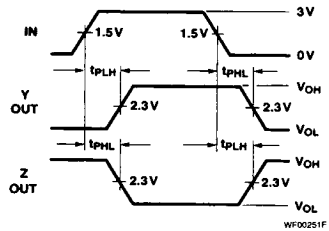
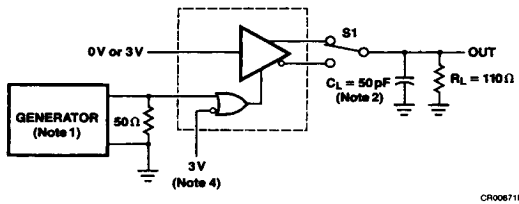
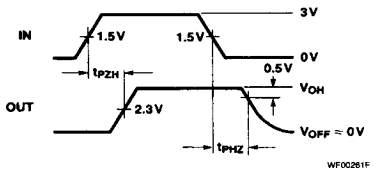


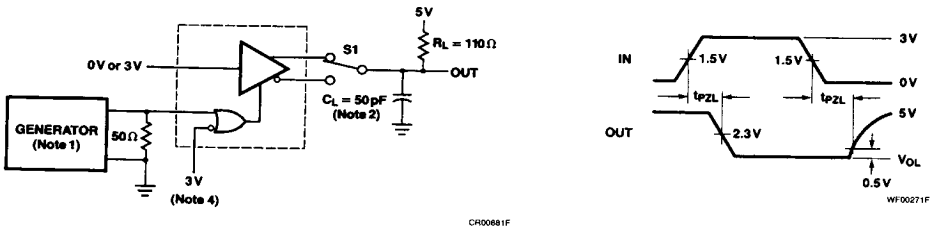
Figure 4 t_{PZH} and t_{PHZ}





Parameter Measurement Information (Cont.)

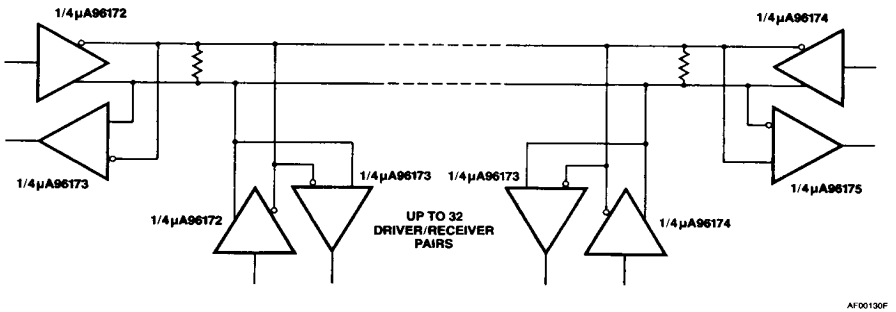
Figure 5 t_{PZL} and t_{PLZ}



Notes

1. The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, duty cycle = 50%, $t_r \leqslant 5.0$ ns, $t_f \leqslant 5.0$ ns, $Z_O = 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. μA96172 with active high and active low Enables is shown here. μA96174 has active high Enable only.
4. To test the active low Enable $\overline{E}$ of μA96172, ground E and apply an inverted waveform to $\overline{E}$. μA96174 has active high Enable only.

Typical Application



Note

The line length should be terminated at both ends in its characteristic impedance.
Stub lengths off the main line should be kept as short as possible.