



+48V Quad Hot-Swap Controllers For Power-Over-LAN

General Description

The MAX5913A/MAX5914A are quadruple hot-swap controllers. The MAX5913A/MAX5914A independently control four external n-channel switches to hot-swap system loads from a single V_{CC} supply line. The devices allow the safe insertion and removal of power devices from live network ports. The operating supply voltage range is between +35V and +72V. The devices are intended for applications in Power-Over-Media-Dependent Interface (MDI), but are not limited to such usage.

The MAX5913A/MAX5914A feature an internal undervoltage lockout (UVLO) function that prevents the FET from turning on, if V_{CC} does not exceed the default value of +32V. The devices also feature a +12V relay driver with 100mA current drive capable of driving low-voltage +3.3V relays. The MAX5913A features an active-low relay driver that sinks current when the relay output is enabled. The MAX5914A features an active-high relay driver output that sources 1mA to drive an external FET relay driver when the relay output is enabled. Control circuitry ensures the relays and the FETs are off until V_{CC} reaches the UVLO threshold. The MAX5913A/MAX5914A use an external sense resistor to enable all the internal current-sense functions.

The MAX5913A/MAX5914A feature a programmable analog current-limit circuit. If the switch remains in current limit for more than a programmable time, the n-channel FET latches off and the supply can be restarted either by autoretry or by an external command after the preset off-time has elapsed.

The MAX5913A/MAX5914A are available in a 44-pin MQFP package and are specified for the extended -40°C to +85°C operating temperature range.

Applications

- Power-Over-LAN
- Power-Over-MDI
- IP Phone Switches/Routers
- Telecom Line Cards
- Network Switches/Routers
- Midspan Power-Over-MDI

Typical Operating Circuit appears at end of data sheet.

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Features

- ♦ Wide Operating Input Voltage Range: +35V to +72V
- ♦ IEEE® 802.3af Compatible
- ♦ Four Independent Power Switch Controllers
- ♦ Open-Circuit Detector
- ♦ On-Board Charge Pumps to Drive External n-Channel FETs
- ♦ Current Sense with External Resistor
- ♦ Foldback Current Limiting
- ♦ +32V Input Undervoltage Lockout
- ♦ On-Chip +12V, 100mA Voltage Relay Drivers

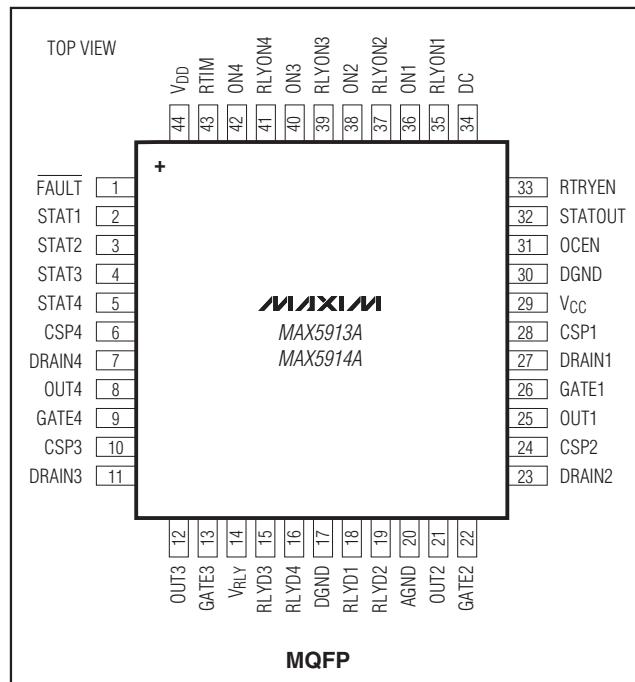
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5913AEMH+	-40°C to +85°C	44 MQFP
MAX5913AEMH+T	-40°C to +85°C	44 MQFP
MAX5914AEMH+	-40°C to +85°C	44 MQFP
MAX5914AEMH+T	-40°C to +85°C	44 MQFP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

V _{CC} to AGND or DGND	-0.6V to +76V
DRAIN ₊ , OUT ₊ to AGND or DGND	-0.6V to (V _{CC} +0.3V)
CSP ₊ to V _{CC}	-0.3V to +0.3V
GATE ₊ to OUT ₊	-0.3V to +13V
V _{RLY} to DGND	-0.3V to +18V
RLYD ₊ to DGND	-0.3V to (V _{RLY} + 0.3V)
ON ₊ , RLYON ₊ , OCEN, RTRYEN, STATOUT, DC to DGND	-0.3V to +12V
FAULT to DGND	-0.3V to +12V
STAT ₊ , RTIM to DGND	-0.3V to (V _{DD} + 0.3V)

V _{DD} to DGND	-0.3V to +7V
DGND to AGND	-5V to +5V
Current into RLYD ₊	-50mA to +150mA
Current into Any Other Pin	±50mA
Continuous Power Dissipation (T _A = +70°C)	
44-Pin MQFP (derate 12.7mW/°C above +70°C)	1.013W
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{CSP} = +48V, V_{AGND} = V_{DGND} = 0V, V_{DD} = +3.3V, V_{RLY} = +12V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = V_{CSP} = +48V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Analog Supply Voltage	V _{CC}	Measured with respect to AGND	35	72	72	V
Analog Supply Current	I _S	V _{CC} = V _{CSP} = 72V	2.7	4	4	mA
		I _S = I _{CC} + I _{CSP}	TA = -40°C to 0°C	5	5	
Digital Supply Voltage	V _{DD}	Measured with respect to DGND	2.5	3.3	3.7	V
Digital Supply Current	I _{DD}	All logic outputs high, RTIM unconnected	1.1	3	3	mA
Analog Supply Undervoltage Lockout	V _{UVLO}	V _{CC} rising, circuits enabled	29	32	35	V
UVLO Hysteresis	V _{UVLO,H}		3	3	3	V
UVLO Deglitch Delay	t _{D,UVLO}	V _{ON} = 3.3V, V _{RLYON} = 3.3V (Figure 1)	12.8	25.6	38.4	ms
Relay Driver Supply	V _{RLY}	Measured with respect to DGND		14	14	V
Ground Potential Difference	V _{GG}	Voltage difference between DGND and AGND	-4	4	4	V
FEEDBACK INPUT AND CURRENT SENSE						
OUT Sense Bias Current	I _{FP}	V _{OUT} = V _{CC}		2	2	µA
Initial Feedback Voltage	V _{FB_S}	Voltage under which the foldback circuit starts reducing the current-limit value (Note 1)		18	18	V
Current-Limit Threshold Voltage	V _{SC}	Maximum ΔV across R _{SENSE} at V _{OUT} > V _{FB_S}	125	142.5	160	mV
Foldback Voltage	V _{FBLK}	Maximum ΔV across R _{SENSE} at V _{OUT} = 0V	42	48	54	mV
Fast Discharge Threshold	V _{FC}		360	420	480	mV
Switch-On Threshold	V _{SWON}	Maximum V _{CC} - V _{OUT} at which the switch is defined as fully on, V _{OUT} increasing	1.2	1.5	1.8	V
Switch-On Comparator Hysteresis	V _{SWON_H}			160	160	mV
MOSFET DRIVERS						
Gate Overdrive Voltage	V _{GS}	V _{GATE} - V _{CC} when switch is fully on 0°C to +85°C	7	9	11	V
		TA = -40°C to 0°C	7	9	12	
Gate Charge Current	I _{GATE}	V _{GATE} = 0V	7	10	13	µA

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MAX5913A/MAX5914A

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = V_{CSP_} = +48V$, $V_{AGND} = V_{DGND} = 0V$, $V_{DD} = +3.3V$, $V_{RLY} = +12V$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = V_{CSP_} = +48V$ and $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gate Discharge Current	I _{GATE,DIS}	During current regulation	8			µA
		V _{ON} = 0V	1			mA
		(V _{CSP_} - V _{DRAIN_}) > V _{FC}	15			mA
Source-Gate Clamp Voltage	V _{SGZ}	V _{OUT_} = 0V, force 30mA into GATE __ , measure V _{GATE} - V _{OUT}	14	16.5	18	V
OPEN-CIRCUIT DETECTOR						
Open-Circuit Current-Threshold Voltage	V _{OCD}	Minimum ΔV across R _{SENSE} to detect an open circuit	1.5	3	4.5	mV
Delay to Open-Circuit Detect	t _{OC}	(Figure 2)	450	900	1350	ms
Deglitch Delay	t _{LPFD}	(V _{CSP_} - V _{DRAIN_}) < V _{OCD} (Figure 2)	106	204	302	ms
RELAY DRIVERS						
Maximum Low Voltage (MAX5913A)	V _{RLOW}	RLYON = high, I _{RLYD_} = 100mA		0.5		V
Relay Pullup Current (MAX5914A)	I _{RPUP}	RLYON = high, V _{RLYD_} = 0V	0.3	0.8	1.3	mA
Clamp Diode Voltage	V _{RCLAMP}	Force 100mA into RLYD, measure V _{RLYD} - V _{RLY}		2		V
Relay Output Leakage		RLYON __ = low, V _{RLYD_} = V _{RLY}	1			µA
TIMING						
Short-Circuit and Startup Timer (Note 2)	t _O	On time for continuous overcurrent conditions	R _{RTIM} = 2kΩ	4.8	6.4	8.0
			R _{RTIM} = 40kΩ	76	128	180
			R _{RTIM} = ∞	3.2	6.4	9.6
Auto-Retry Duty Cycle		DC = logic low		1		%
		DC = logic high		2		
		DC = unconnected		4		
Port Turn-On Delay	t _{ON_DEL}	V _{ON} = 3.3V (Figure 3)	12.8	25.6	38.4	ms
Relay Turn-Off Delay	t _{OFF_DEL}	After RLYON __ goes low (Figure 3)	1.6	3.2	4.8	ms
DIGITAL INTERFACE						
DC Pin Input-Voltage High	V _{IH_DC}	2.5V ≤ V _{DD} ≤ 3.7V	0.7 × V _{DD}			V
DC Pin Input-Voltage Low	V _{IL_DC}	2.5V ≤ V _{DD} ≤ 3.7V		0.3 × V _{DD}		V
DC Pin Input Impedance	R _{IN_DC}		1			kΩ
Logic Input High	V _{IH}	2.5V ≤ V _{DD} ≤ 3.7V	0.8 × V _{DD}			V
Logic Input Low	V _{IL}	2.5V ≤ V _{DD} ≤ 3.7V		0.3 × V _{DD}		V
Logic Input Leakage			1			µA
FAULT Output-Voltage Low	V _{FL}	I _{SINK} = 4mA		0.4		V
FAULT High Input Leakage				1		µA
Logic Output-Voltage High	V _{OH}	STAT __ outputs sourcing 0.5mA	V _{DD} - 0.4			mV
Logic Output-Voltage Low	V _{OL}	STAT __ outputs sinking 0.5mA		0.4		V

Note 1: See *Typical Operating Characteristics* for Current-Limit Foldback, and refer to *Current Sensing and Regulation* section.

Note 2: The resistor at RTIM can range from 2kΩ to 40kΩ.

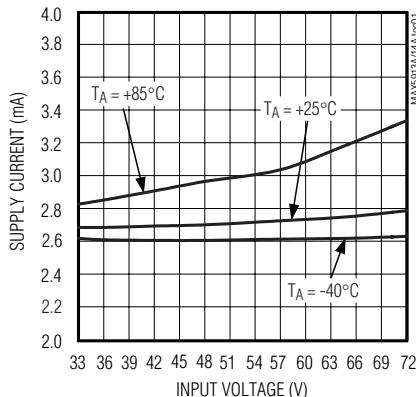
Note 3: Limits are 100% tested at $T_A = +25^\circ C$ and $T_A = +85^\circ C$. Limits at $-40^\circ C$ are guaranteed by design and characterization, but are not production tested.

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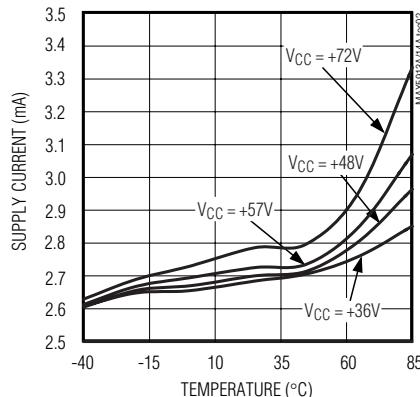
Typical Operating Characteristics

($V_{CSP_} = V_{CC} = +48V$, $V_{DD} = +3.3V$, $V_{RLY} = +12V$, $V_{AGND} = V_{DGND} = 0V$, $RTIM$ = open, $T_A = +25^{\circ}C$, unless otherwise specified.)

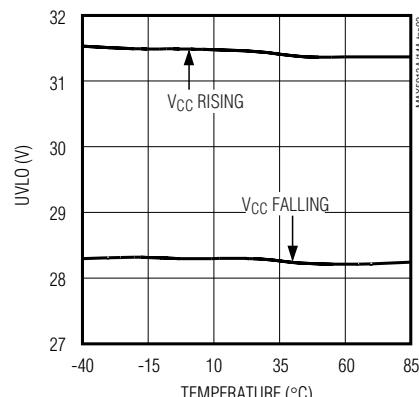
SUPPLY CURRENT vs. INPUT VOLTAGE



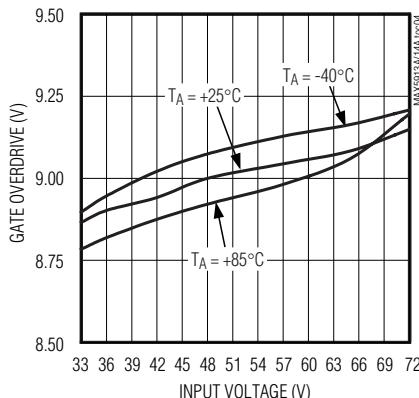
SUPPLY CURRENT vs. TEMPERATURE



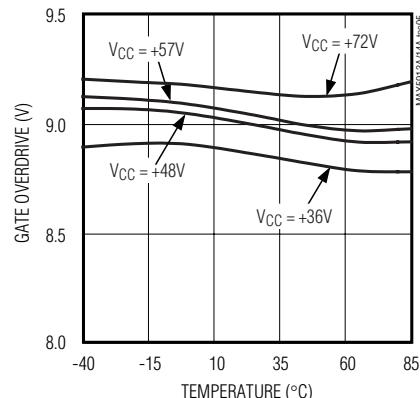
UNDERVOLTAGE LOCKOUT vs. TEMPERATURE



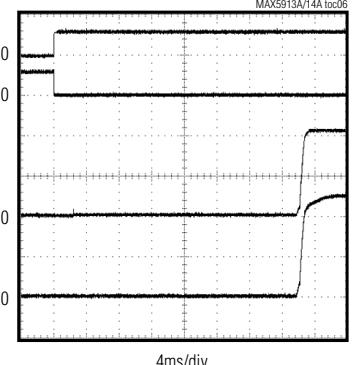
GATE OVERDRIVE VOLTAGE vs. INPUT VOLTAGE



GATE OVERDRIVE VOLTAGE vs. TEMPERATURE



STARTUP WAVEFORMS



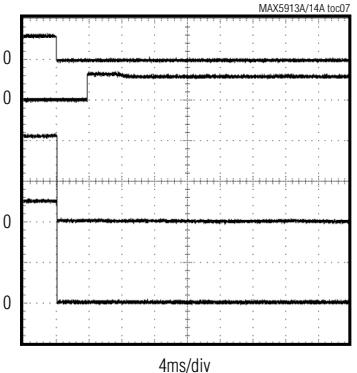
A: $V_{ON} = V_{RLYON}$, 5V/div

B: V_{RLYD} , 20V/div

C: V_{OUT} , 20V/div

D: V_{GATE} , 20V/div

TURN-OFF WAVEFORMS



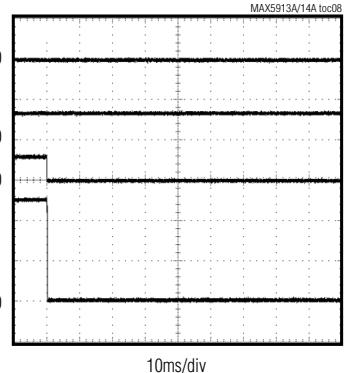
A: $V_{ON} = V_{RLYON}$, 5V/div

B: V_{RLYD} , 20V/div

C: V_{OUT} , 20V/div

D: V_{GATE} , 20V/div

GATE TURN-OFF WAVEFORM



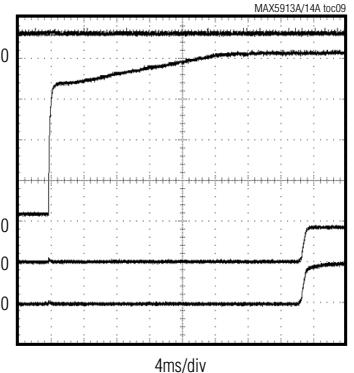
A: V_{RLYD} , 20V/div

B: V_{RLYON} , 5V/div

C: V_{ON} , 5V/div

D: V_{GATE} , 20V/div

UVLO TURN-ON DELAY



A: $V_{ON} = V_{DD}$

B: V_{CC} , 10V/div

C: V_{OUT} , 50V/div

D: V_{GATE} , 50V/div

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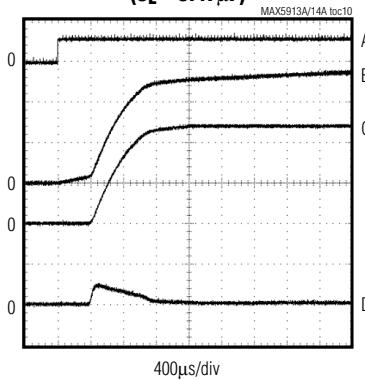
MAX5913A/MAX5914A

Typical Operating Characteristics (continued)

($V_{CSP_} = V_{CC} = +48V$, $V_{DD} = +3.3V$, $V_{RLY} = +12V$, $V_{AGND} = V_{DGND} = 0V$, $RTIM$ = open, $T_A = +25^\circ C$, unless otherwise specified.)

TURN-ON INTO CAPACITIVE LOAD

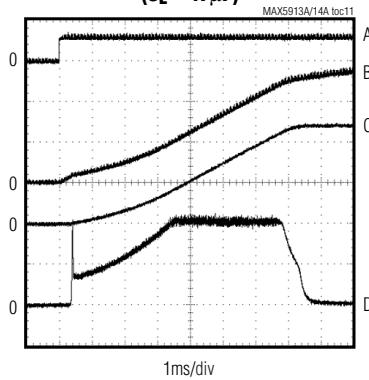
($C_L = 0.47\mu F$)



RLYON = V_{DD}
A: V_{ON} , 5V/div
B: V_{GATE} , 20V/div
C: V_{OUT} , 20V/div
D: I_{OUT} , 100mA/div

TURN-ON INTO CAPACITIVE LOAD

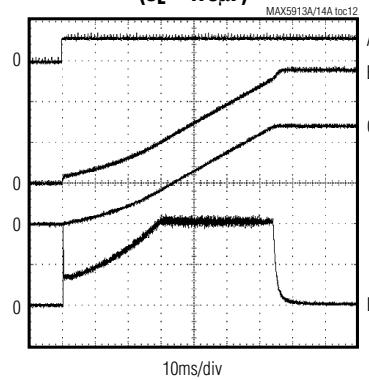
($C_L = 47\mu F$)



RLYON = V_{DD} , $R_{RTIM} = 2k\Omega$
A: V_{ON} , 5V/div
B: V_{GATE} , 20V/div
C: V_{OUT} , 20V/div
D: I_{OUT} , 200mA/div

TURN-ON INTO CAPACITIVE LOAD

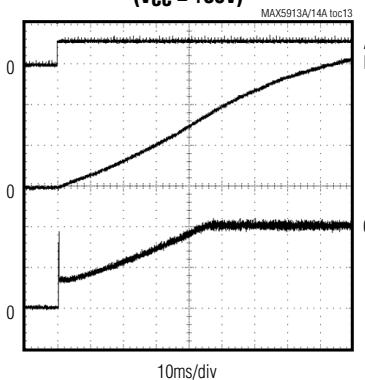
($C_L = 470\mu F$)



RLYON = V_{DD} , $R_{RTIM} = 40k\Omega$
A: V_{ON} , 5V/div
B: V_{GATE} , 20V/div
C: V_{OUT} , 20V/div
D: I_{OUT} , 200mA/div

CURRENT-LIMIT FOLDBACK

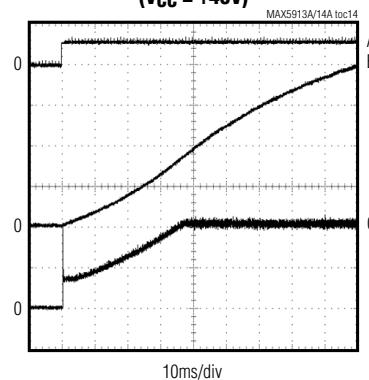
($V_{CC} = +36V$)



RLYON = V_{DD} , $R_L = 100\Omega$, $R_{RTIM} = 40k\Omega$, $C_{LOAD} = 470\mu F$
A: V_{ON} , 5V/div
B: V_{OUT} , 10V/div
C: I_{OUT} , 200mA/div

CURRENT-LIMIT FOLDBACK

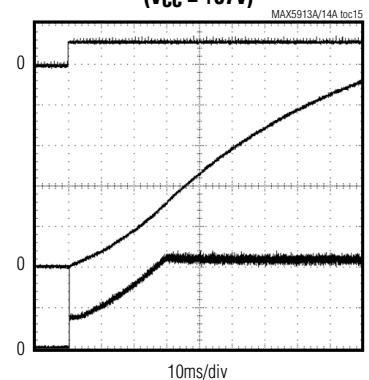
($V_{CC} = +48V$)



RLYON = V_{DD} , $R_L = 139\Omega$, $R_{RTIM} = 40k\Omega$, $C_{LOAD} = 470\mu F$
A: V_{ON} , 5V/div
B: V_{OUT} , 10V/div
C: I_{OUT} , 200mA/div

CURRENT-LIMIT FOLDBACK

($V_{CC} = +57V$)

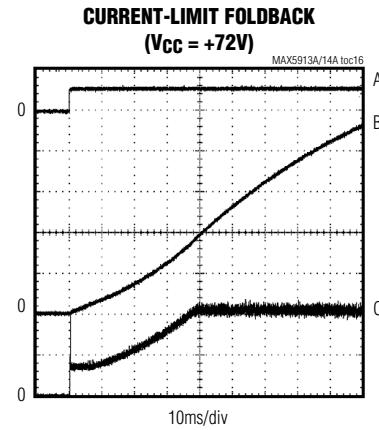


RLYON = V_{DD} , $R_L = 162\Omega$, $R_{RTIM} = 40k\Omega$, $C_{LOAD} = 470\mu F$
A: V_{ON} , 5V/div
B: V_{OUT} , 10V/div
C: I_{OUT} , 200mA/div

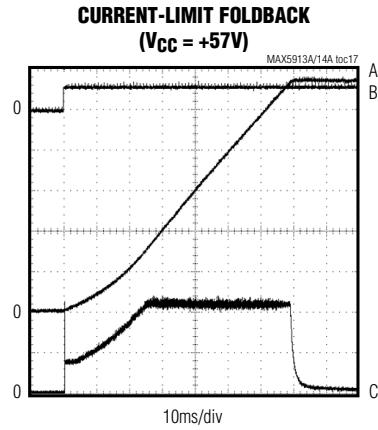
+48V Quad Hot-Swap Controllers For Power-Over-LAN

Typical Operating Characteristics (continued)

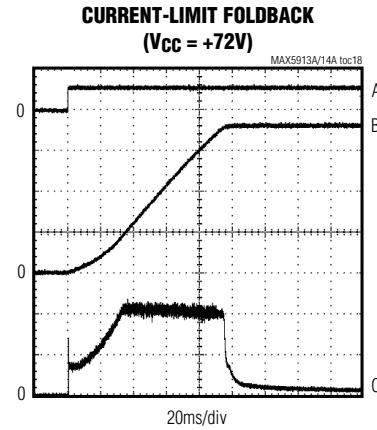
($V_{CSP_} = V_{CC} = +48V$, $V_{DD} = +3.3V$, $V_{RLY} = +12V$, $V_{AGND} = V_{DGND} = 0V$, $R_{RTIM} = \text{open}$, $T_A = +25^\circ\text{C}$, unless otherwise specified.)



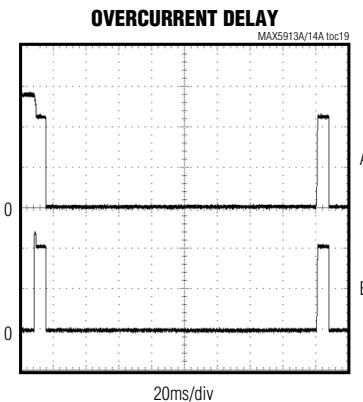
$R_{LYON} = V_{DD}$, $R_L = 200\Omega$, $R_{RTIM} = 40k\Omega$
A: V_{ON} , 5V/div
B: V_{OUT} , 10V/div
C: I_{OUT} , 200mA/div



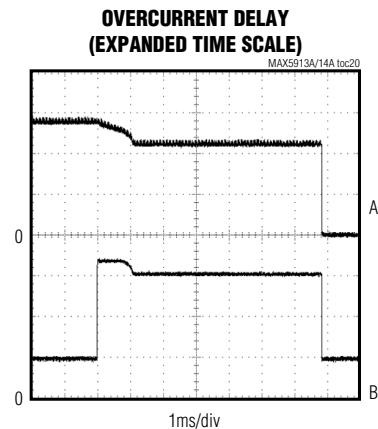
$R_{LYON} = V_{DD}$, $R_L = \text{OPEN}$,
 $R_{RTIM} = 40k\Omega$, $C_{LOAD} = 470\mu\text{F}$
A: V_{ON} , 5V/div
B: V_{OUT} , 10V/div
C: I_{OUT} , 200mA/div



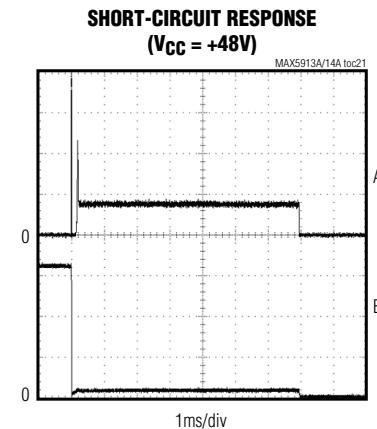
$R_{LYON} = V_{DD}$, $R_L = \text{OPEN}$, $R_{RTIM} = 40k\Omega$, $C_{LOAD} = 470\mu\text{F}$
A: V_{ON} , 5V/div
B: V_{OUT} , 20V/div
C: I_{OUT} , 200mA/div



$R_{TRYEN} = V_{DD}$, $R_{LYON} = \text{ON} = V_{DD}$, $DC = 4\%$,
 $R_{RTIM} = 2k\Omega$, $R_L = 100\Omega$
A: V_{OUT} , 20V/div
B: I_{OUT} , 200mA/div



$R_{TRYEN} = V_{DD}$, $R_{LYON} = \text{ON} = V_{DD}$,
 $DC = \text{DON'T CARE}$, $R_{RTIM} = 2k\Omega$, $R_L = 100\Omega$
A: V_{OUT} , 20V/div
B: I_{OUT} , 200mA/div



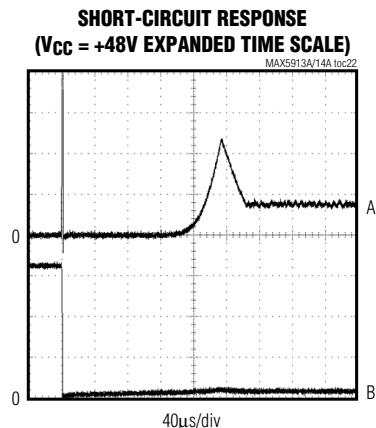
$ON = R_{LYON} = V_{DD}$, $R_L = 1\Omega$, $R_{RTIM} = 2k\Omega$
A: I_{OUT} , 200mA/div
B: V_{OUT} , 20V/div

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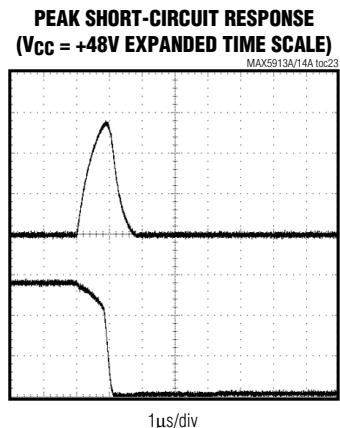
MAX5913A/MAX5914A

Typical Operating Characteristics (continued)

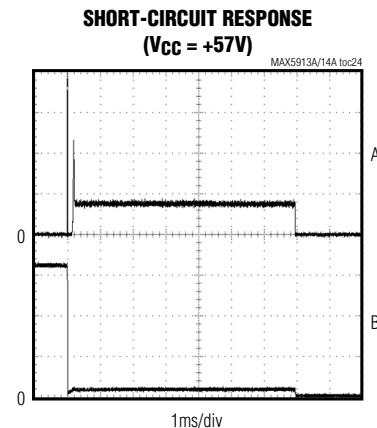
($V_{CSP_} = V_{CC} = +48V$, $V_{DD} = +3.3V$, $V_{RLY} = +12V$, $V_{AGND} = V_{DGND} = 0V$, $RTIM$ = open, $T_A = +25^\circ C$, unless otherwise specified.)



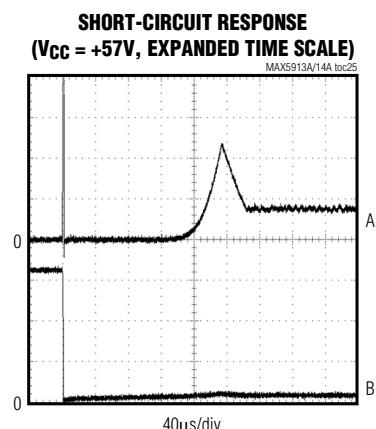
ON = RLYON = V_{DD} , $R_L = 1\Omega$, $R_{RTIM} = 2k\Omega$
A: I_{OUT} , 200mA/div
B: V_{GATE} , 20V/div



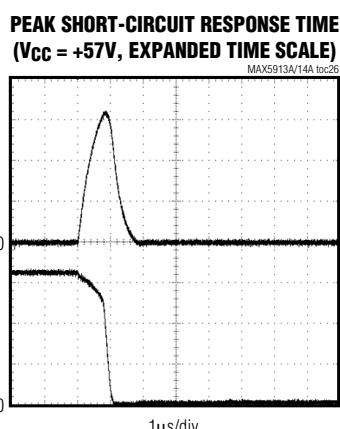
ON = RLYON = V_{DD} , $R_L = 1\Omega$, $R_{RTIM} = 2k\Omega$
A: I_{OUT} , 5A/div
B: V_{GATE} , 20V/div



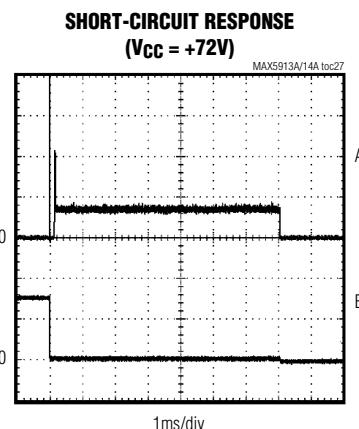
ON = RLYON = V_{DD}
A: I_{OUT} , 200mA/div
B: V_{GATE} , 20V/div



ON = RLYON = V_{DD} , $R_L = 1\Omega$, $R_{RTIM} = 2k\Omega$
A: I_{OUT} , 200mA/div
B: V_{GATE} , 20V/div



ON = RLYON = V_{DD} , $R_L = 1\Omega$, $R_{RTIM} = 2k\Omega$
A: I_{OUT} , 5A/div
B: V_{GATE} , 20V/div

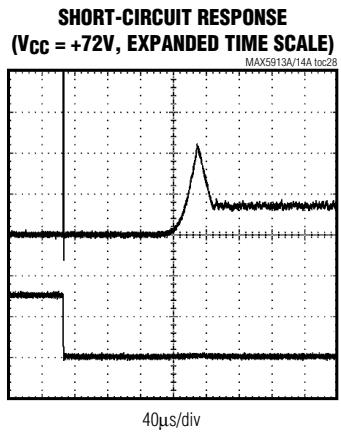


ON = RLYON = V_{DD}
A: I_{OUT} , 200mA/div
B: V_{GATE} , 50V/div

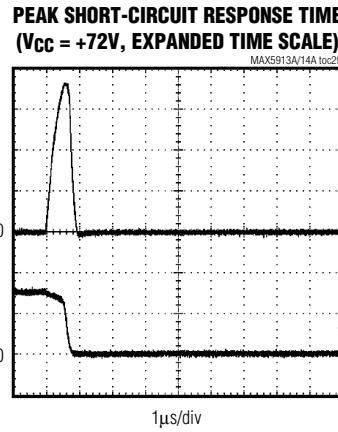
+48V Quad Hot-Swap Controllers For Power-Over-LAN

Typical Operating Characteristics (continued)

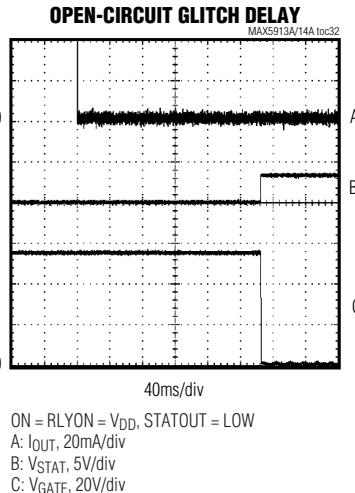
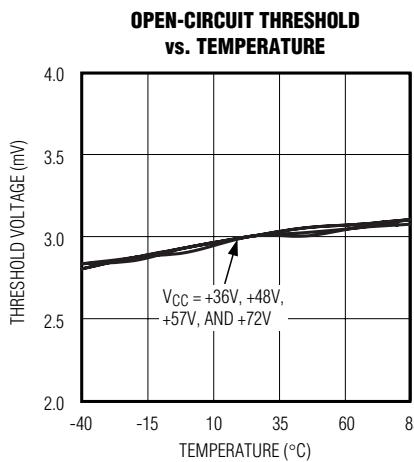
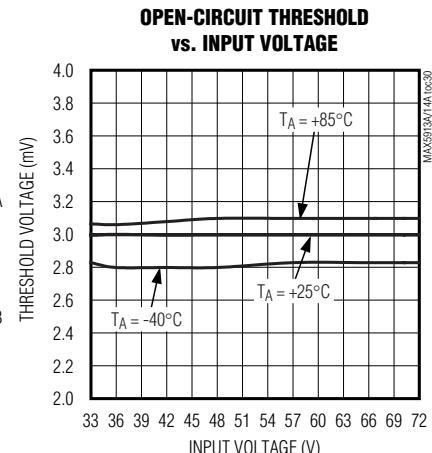
($V_{CSP_} = V_{CC} = +48V$, $V_{DD} = +3.3V$, $V_{RLY} = +12V$, $V_{AGND} = V_{DGND} = 0V$, $RTIM$ = open, $T_A = +25^\circ C$, unless otherwise specified.)



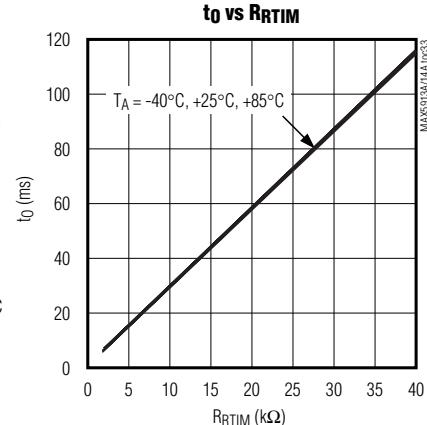
ON = RLYON = V_{DD} , $R_L = 1\Omega$, $R_{RTIM} = 2k\Omega$
 A: I_{OUT} , 200mA/div
 B: V_{GATE} , 50V/div



ON = RLYON = V_{DD} , $R_L = 1\Omega$, $R_{RTIM} = 2k\Omega$
 A: I_{OUT} , 5A/div
 B: V_{GATE} , 50V/div



ON = RLYON = V_{DD} , STATOUT = LOW
 A: I_{OUT} , 20mA/div
 B: V_{STAT} , 5V/div
 C: V_{GATE} , 20V/div

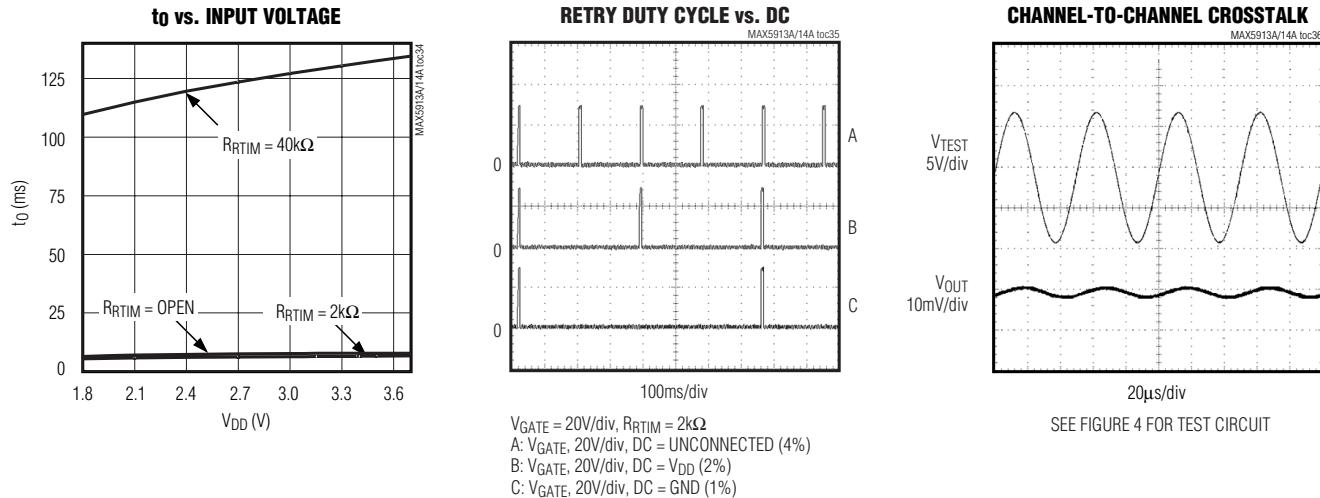


+48V Quad Hot-Swap Controllers For Power-Over-LAN

Typical Operating Characteristics (continued)

($V_{CSP_} = V_{CC} = +48V$, $V_{DD} = +3.3V$, $V_{RLY} = +12V$, $V_{AGND} = V_{DGND} = 0V$, $RTIM$ = open, $T_A = +25^\circ C$, unless otherwise specified.)

MAX5913A/MAX5914A



Pin Description

PIN	NAME	FUNCTION
1	FAULT	Active-Low Fault Output. FAULT is an open-drain output that goes low when a fault is detected on any of the four channels. FAULT is low when an OC (open circuit) is detected, or when the MAX5913A/MAX5914A is in auto-retry caused by an overcurrent condition. When RTRYEN is low, and the channel switch is latched off due to an overcurrent condition, FAULT remains low until ON_ is driven low.
2, 3, 4, 5	STAT1, STAT2, STAT3, STAT4	Status Outputs. STAT_ are push-pull outputs. Depending on the STATOUT pin status, STAT_flags either the Power-OK_ or Port-OC_ status. Power-OK_high indicates: a) ON_input is high. b) The switch port is fully on and startup is completed ($V_{CSP_} - V_{OUT_}$) < V_{SWON} . c) Input voltage is above V_{UVLO} . d) Switch is not in current limit. Power-OK_low indicates a fault with any of the above conditions. Port-OC_output high indicates that the switch is latched off because the switch current is less than the open-current threshold, Port-OC is low otherwise.
6, 10, 24, 28	CSP4, CSP3, CSP2, CSP1	Current-Sense Positive Input. Connect to VCC and place a current-sense resistor from CSP_ to DRAIN_. Use a Kelvin sense trace from a current-sense resistor to CSP_(see Figure 7).
7, 11, 23, 27	DRAIN4, DRAIN3, DRAIN2, DRAIN1	MOSFET Drain Current-Sense Negative Input. Connect to drain of power MOSFET and connect a current-sense resistor from CSP_ to DRAIN_. Use Kelvin sense trace from current-sense resistor to DRAIN_(see Figure 7).

+48V Quad Hot-Swap Controllers For Power-Over-LAN

Pin Description (continued)

PIN	NAME	FUNCTION
8, 12, 21, 25	OUT4, OUT3, OUT2, OUT1	MOSFET Source Output Voltage Sense. Connect to a power MOSFET source through a 100Ω series resistor.
9, 13, 22, 26	GATE4, GATE3, GATE2, GATE1	MOSFET Gate Driver Output. The MAX5913A/MAX5914A regulate the gate-drive voltage to $(V_{CC} + 9V)$ to fully turn on the power n-channel MOSFET. GATE __ sources $10\mu A$ during startup to slowly turn on the MOSFET switch. GATE __ sinks $1mA$ to turn off the MOSFET switch.
14	V _{RLY}	Relay Supply-Voltage Input. Referenced to DGND.
15, 16, 18, 19	RLYD3, RLYD4, RLYD1, RLYD2	Relay-Drive Output. For the MAX5913A, RLYD __ sinks $100mA$ when the relay driver is enabled. For the MAX5914A, RLYD __ sources $1mA$ when the relay driver is enabled.
17, 30	DGND	Digital Ground. All logic voltages are referred to DGND. The voltage difference between DGND and AGND can be up to $\pm 4V$.
20	AGND	Analog Ground. All analog voltages are referred to AGND.
29	V _{CC}	Analog Power Supply. Connect V _{CC} to $+35V$ to $+72V$ power supply. UVLO circuitry turns off the MOSFET switch and relay for $V_{CC} < V_{UVLO}$. Bypass V _{CC} to AGND with a $1\mu F$ capacitor.
31	OCEN	Open-Circuit Detector Enable Input. Drive OCEN high to enable open-circuit detector, or drive low to disable. When enabled, the open-circuit detector waits for a 900ms delay after Power-OK conditions are met before enabling the open-circuit detector function.
32	STATOUT	Status Output Multiplexer (MUX) Control Input. Controls the signal MUX into the STAT __ outputs. Drive STATOUT high to route Power-OK __ status to STAT __ outputs, or drive STATOUT low to route Port-OC __ status to STAT __ outputs.
33	RTRYEN	Auto-Retry Enable Input. Drive RTRYEN high to enable auto-retry. Drive RTRYEN low to enable switch latch-off mode. When switch is latched off, a high-to-low transition on the ON __ control input clears the latch.
34	DC	Duty-Cycle Programming Input. DC sets the minimum off-time after an overcurrent condition latches off the switch. When RTRYEN is high, DC sets the auto-retry duty cycle. Drive DC low for 1% duty cycle, drive DC high for 2%, or leave DC unconnected for 4% duty cycle.
35, 37, 39, 41	RLYON1, RLYON2, RLYON3, RLYON4	Relay-Driver Control Input. Drive RLYON __ high to enable RLYD __ , drive RLYON __ low to turn off the MOSFET switch for the channel and disable RLYD __ .
36, 38, 40, 42	ON1, ON2, ON3, ON4	MOSFET Switch Control Input. Drive ON __ high to enable GATE __ to turn on the MOSFET switch. RLYON __ must be high to enable the switch. Drive ON __ low to disable the switch. Pulling ON __ low also resets the latch when RTRYEN is low or if the switch is latched off due to open-circuit detection.
43	RTIM	Timing Oscillator Frequency Set Input. Connect a $2k\Omega$ to $40k\Omega$ resistor from RTIM to DGND to set the maximum continuous overcurrent time, t _O . Leave RTIM unconnected to set default 6.4ms t _O .
44	V _{DD}	Digital Power Supply. Bypass V _{DD} to DGND with a $1\mu F$ capacitor.

+48V Quad Hot-Swap Controllers For Power-Over-LAN

Detailed Description

The MAX5913A/MAX5914A quadruple hot-swap controllers provide Power-Over-MDI, also known as Power-Over-LAN systems (Figure 5). The MAX5913A/MAX5914A enable control of four external n-channel MOSFET switches from a single VCC ranging from +35V to +72V, with timing control and current-limiting functions built in.

The MAX5913A/MAX5914A features include undervoltage lockout (UVLO), 100mA relay drivers, dual-level current sense, foldback current limit, programmable overcurrent time and auto-retry periods, internal charge pumps to drive external MOSFET and soft-start, port status output indicating power-OK (POK) or open-circuit conditions (Figure 6).

Switch and Relay Control Inputs

The MAX5913A/MAX5914A ON_ inputs turn on the corresponding MOSFET switch. Driving ON_ high turns on the switch if the corresponding RLYON is driven high, and VCC > VUVLO for more than 25.6ms. Driving RLYON_ high immediately turns on the corresponding relay, and activates the 25.6ms delay after which the corresponding ON_ input is active. Driving RLYON_ low immediately turns off the switch and activates a 3.2ms delay, after which the relay is turned off. These internal delays safely allow driving ON_ and RLYON_ simultaneously. The relay is turned on while the switch is off so that there is no voltage across the relay contacts. The relay is turned off while the switch is off so that there is no current flowing when the relay contacts are opened (see Figure 3).

Input Voltage and UVLO

The MAX5913A/MAX5914A operate from a +35V to +72V supply voltage. VCC powers the MAX5913A/MAX5914A analog circuitry and is monitored continuously during startup and normal operation. The MAX5913A/MAX5914A keep all MOSFET switches and relay drivers securely off before VCC rises above VUVLO. The MAX5913A/MAX5914A turn off all MOSFET switches and relay drivers after VCC falls below VUVLO - VUVLO,H.

Startup

When the turn-on condition is met (see the *Input Voltage and UVLO* and *Switch and Relay Control Inputs* sections), the MAX5913A/MAX5914A slowly turn on the external MOSFET switch by charging its gate using a constant current source, IGATE (10µA typ). The gate voltage slope is determined by the total gate capacitance CGATE connected to this node. Since the output voltage follows the gate voltage, thus the output rises with a slope determined by:

$$\frac{\Delta V_{OUT}}{\Delta t} = \frac{I_{GATE}}{C_{GATE}}$$

If a capacitor load is connected to the output, the total current through the FET is:

$$I = I_{GATE} \frac{C_L}{C_{GATE}} + I_L$$

where CL is the load capacitance and IL is the current required by any load connected to the output during the startup phase.

If the current through the FET reaches the programmed current-limit value:

$$I_{MAX} = \frac{V_{SC}}{R_{SENSE}}$$

the internal current-limit circuitry activates and regulates this FET current to be a value, ILIM, that depends on VOUT (IFLBK) (Figure 8). See the *Current Sensing and Regulation* section. In this case, the maximum rate of change of the output is determined by:

$$\frac{\Delta V_{OUT}}{\Delta t} = \frac{I_{LIM} - I_L}{C_L}$$

The formula shows the necessity for ILIM to be larger than IL in order to allow the output voltage to rise. The foldback function is active as long as the circuit is in overcurrent condition. Should the overcurrent condition persist for a period longer than the maximum time tO, the switch is latched off and GATE_ is discharged to ground with a 1mA pulldown current.

If auto-retry is enabled, the switch turns on again after a waiting period, tOFF, which is determined by the programmed duty cycle.

After the startup, the internal charge pumps provide (VCC + 9V) typical gate overdrive to fully turn on the switch. When the switch is fully on (voltage drop across the switch is \leq 1.5V), and the switch is not in current limit, the POK signal is asserted.

Current Sensing and Regulation

The MAX5913A/MAX5914A control port current with using two voltage comparators (dual-level detection) that sense the voltage drop across an external current-sense resistor. Connect CSP_ to VCC and connect a current-sense resistor between CSP_ and DRAIN_. Kelvin sensing should be used as shown in Figure 7.

MAX5913A/MAX5914A

+48V Quad Hot-Swap Controllers For Power-Over-LAN

Test Circuits and Timing Diagrams

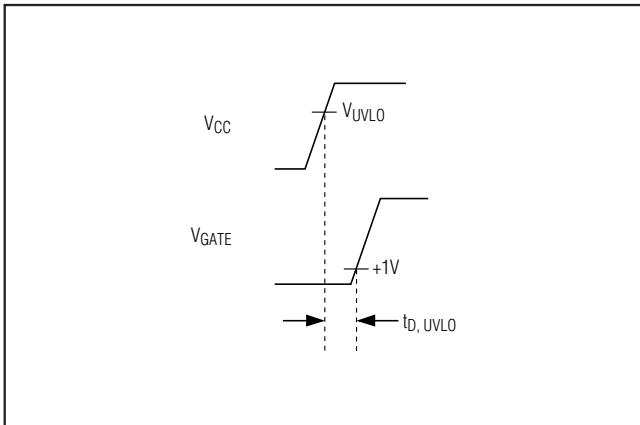


Figure 1. UVLO Deglitch Delay

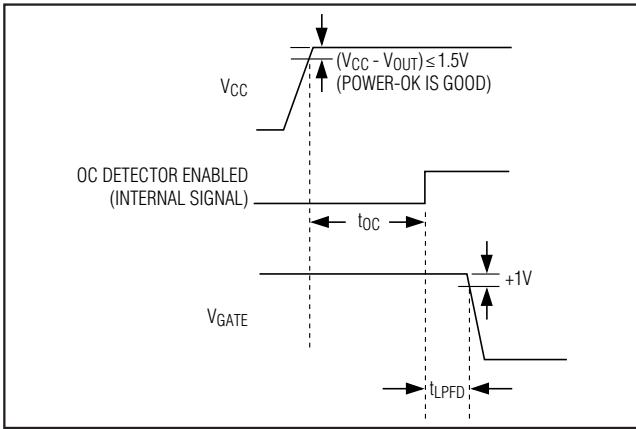


Figure 2. Open-Circuit Detector Deglitch Delay

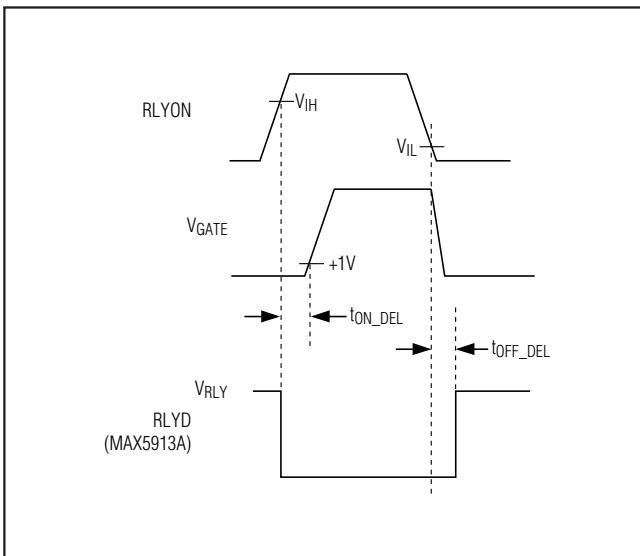


Figure 3. Port Turn-On Delay, Relay Turn-Off Delay

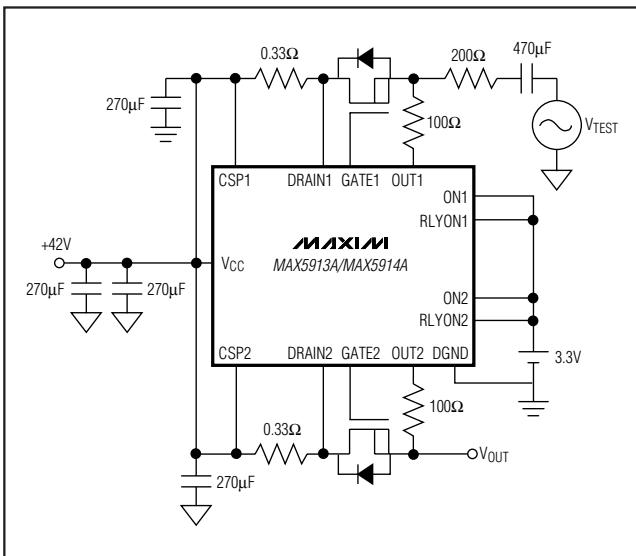


Figure 4. Channel-to-Channel Crosstalk Test Circuit

The first comparator compares the sensed voltage against the V_{SC} threshold (typically 142.5mV). Choose a sense resistor as follows:

$$R_{SENSE} = V_{SC} / I_{MAX}$$

where I_{MAX} is the maximum current allowed through the switch.

When I_{MAX} is reached, foldback current-limit circuitry regulates the current limit as a function of V_{OUT} (Figure 8). As V_{OUT} approaches zero, the maximum voltage drop

across the sense resistor is lowered to a minimum value of 48mV (typ). This foldback feature helps reduce the power dissipation in the external power FET during output overload and output short-circuit conditions. If a load with very low activation voltage is permanently connected to the output, make the minimum limit current sufficiently larger than the load current. If the load current indeed exceeds the foldback-limit value, the MAX5913A/MAX5914A are not able to power up the switch.

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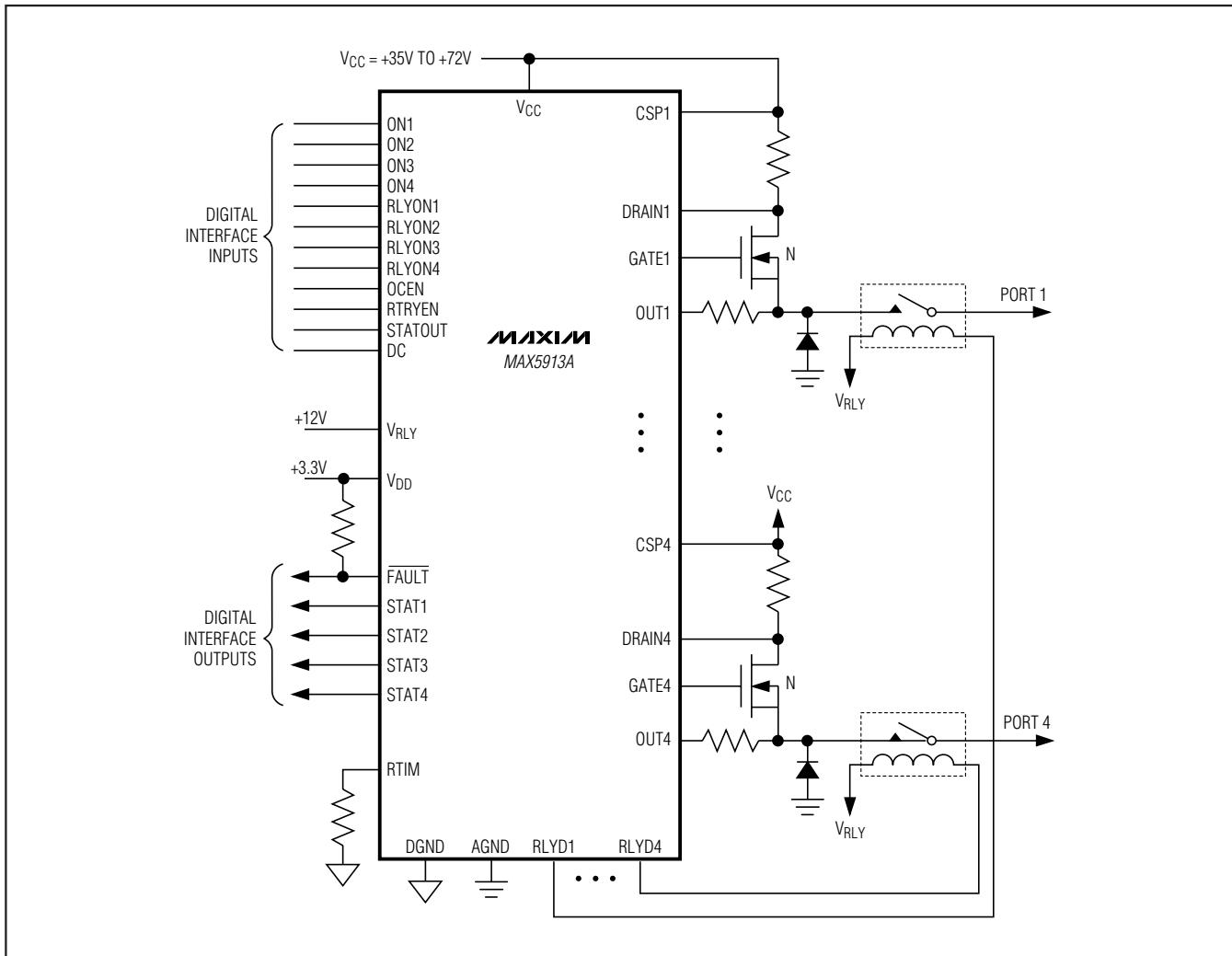


Figure 5. Typical Application Circuit

A second comparator with a detection threshold of 3VSC activates a fast 15mA pulldown of the gate. The purpose of this comparator is to rapidly discharge the gate when a momentary current peak overstresses the external FET, helping the regulation to act more rapidly.

The sense resistor is also used to detect an open-circuit or low-current condition with a typical threshold of 3mV.

Open-Circuit Detection

The MAX5913A/MAX5914A detect when a port has low current or is open circuit, and turn off the switch to that port. After the switch is turned on and the POK conditions are met, the open-circuit detector is enabled after

a 900ms delay. The open-circuit voltage threshold is set at 3mV across the current-sense resistor. Drive OCEN high to enable open-circuit detectors for all four ports. Drive OCEN low to disable the detectors. Each port has an open-circuit flag that can be read from STAT_ outputs when the STATOUT is low. STAT_ output high indicates that the switch is latched off due to an open-circuit condition on that port. To reset the latch pull ON low and then high to restart (Table 1).

Output Voltage Sense and Power-OK

The MAX5913A/MAX5914A sense the output voltage of the port at the source of the external MOSFET switch.

+48V Quad Hot-Swap Controllers For Power-Over-LAN

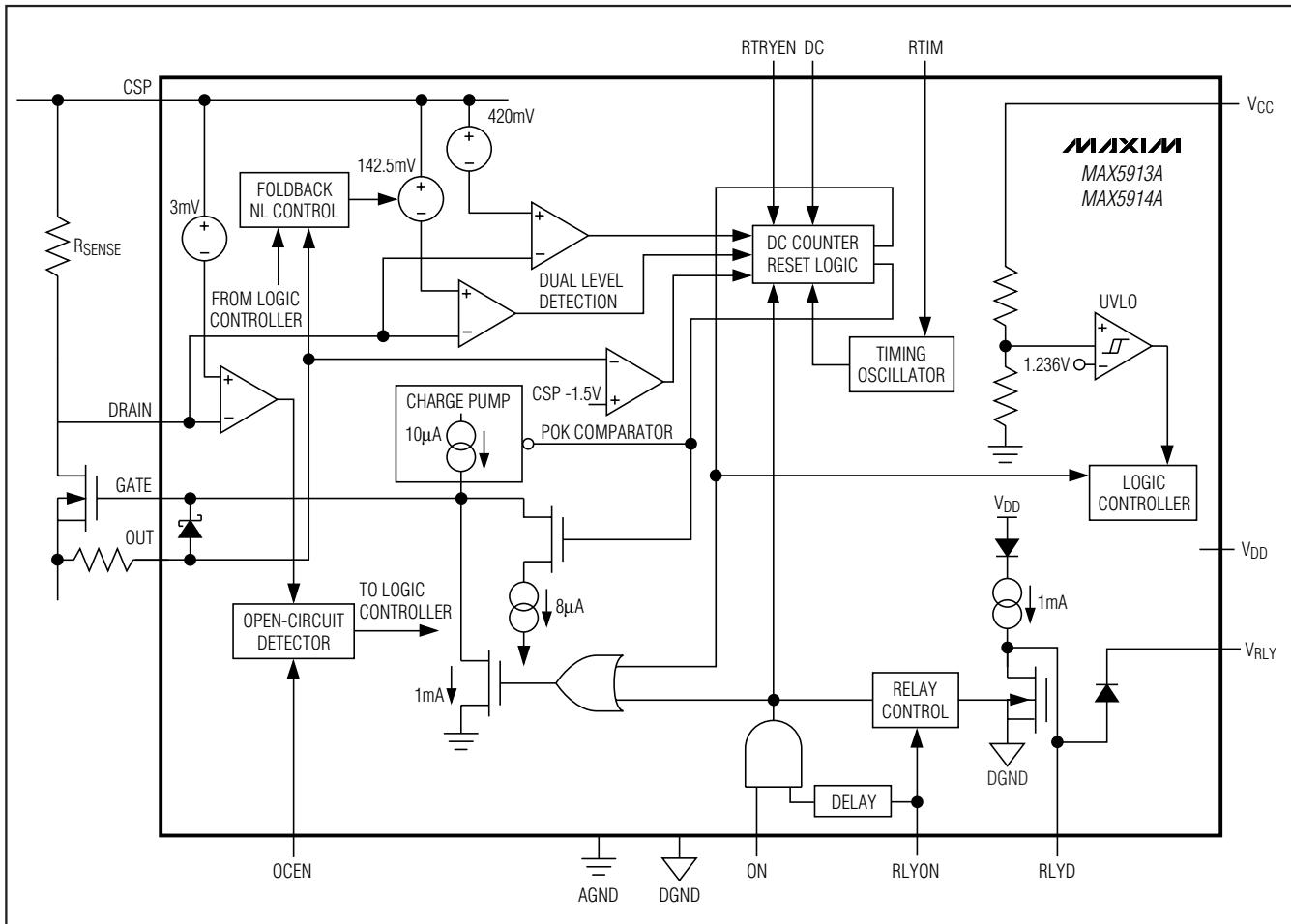


Figure 6. Functional Diagram

Internally the circuit compares the output voltage with V_{CC} to determine when the FET is completely on. A POK condition is met when:

$$(V_{CC} - V_{OUT}) \leq 1.5V$$

The internal circuit monitors V_{OUT} to determine the value of the foldback current when the circuit goes into current-limit conditions. The value of the current limit decreases as the output voltage decreases in order to limit the power dissipation of the FET. The nonlinear relationship between V_{OUT} and I_{LIM} is depicted in Figure 8.

The foldback circuit is active whenever the MAX5913A/MAX5914A are in current-limit mode after an overcurrent condition has been detected.

Connect a catch diode to analog ground and a 100Ω resistor in series with OUT_- to limit the current during negative inductive kicks that can bring OUT_- below the ground potential (Figure 5).

Relay Drivers

The MAX5913A/MAX5914A include on-chip relay drivers, $RYLD_-$, capable of sinking 100mA. When $RLYON_-$ goes high, the MAX5913A/MAX5914A immediately enable the relay driver, and the corresponding ON_- switch control input is delayed 25.6ms to allow the relay to close under a zero-voltage condition. When $RLYON_-$ goes low, the MAX5913A/MAX5914A immediately turn off the corresponding switch, and then turn off the relay driver after a 3.2ms delay, ensuring the relay contacts open under a zero-current condition. The polarity of the MAX5913A

+48V Quad Hot-Swap Controllers For Power-Over-LAN

RLYD_{_} is opposite to that of the MAX5914A. For the MAX5913A, upon the assertion of the RLYON_{_} input, RLYD_{_} sinks 100mA to DGND. For the MAX5914A, when RLYON_{_} is high, an internal 1mA current source pulls up RLYD_{_} to VDD. A 100mA catch diode is internally connected between RLYD_{_} and VRLY to protect the MAX5913A/MAX5914A from inductive kicks from the relay coil. VRLY must be connected to the high-side relay supply voltage.

Programmable Timing, RTIM

An external resistor from RTIM to DGND sets the frequency of the internal oscillator upon which t₀ and the auto-retry times are based.

Use 2kΩ to 40kΩ resistors for RRTIM.

$$t_0 = (RRTIM / 2k\Omega) (6.4ms)$$

If RTIM is unconnected, an internal resistor sets t₀ to a nominal 6.4ms.

Auto-Retry and Programmable Duty Cycle

The MAX5913A/MAX5914A feature auto-retry with adjustable duty cycle. Driving RTRYEN high enables the auto-retry function. When the switch encounters an overcurrent for a period greater than t₀, the switch is turned off, and remains off for a t_{OFF} programmed by DC, a three-level input. After the t_{OFF} period, the switch is automatically turned on again. When the port encounters a continuous overload or short-circuit condition, the switch turns on and off repeatedly with the on duty cycle of 1%, 2%, or 4% depending on the DC input state (Table 2). When RTRYEN is low, the auto-retry is disabled, and a fault condition at the switch turns the switch off and the switch remains latched off. Driving the corresponding ON control input low resets the latch. Pulling ON high to turn on the switch. However, the MAX5913A/MAX5914A always wait a minimum time, t_{OFF}, before restarting the switch.

Table 1. Status Output

PORT_CONDITION	OCEN	STATOUT	STAT __
Enabled. Switch fully on and not in current limit.	x	H	H (Power-OK __ is good)
Enabled. Switch in current limit, or V _{DS} > 1.5V.	x	H	L (Power-OK __ is not good)
Enabled. Switch current is less than OC threshold, port is latched off.	H	L	H (Port-OC __ , Port current is low or zero)
Enabled. Switch fully on and output current is greater than OC threshold.	H	L	L (Port-OC __ , Port current is good)
Disabled.	L	L	L

Logic Interface and Status Outputs

The MAX5913A/MAX5914A logic interface controls the device functionality. All the basic control functions for the four switches are separated. ON_{_} enables individual on/off control of each MOSFET (the corresponding relay must be on to turn on the switch). RLYON_{_} enables individual on/off control of each relay. STAT_{_} indicates POK or Port-OC (open circuit) status of each switch. The other logic pins are common to all four switches. A single FAULT output goes low when any of the four channels is latched off. Driving OCEN high enables the open-circuit detectors. Driving RTRYEN high enables the auto-retry function, RTRYEN low enables the switch latch-off function. DC, a three-level logic input, programs the duty cycle. The STATOUT input selects the signal multiplexed at STAT_{_} outputs (Table 1.). Driving STATOUT high routes POK status to the STAT_{_} outputs. Driving STATOUT low routes Port-OC status to the STAT_{_} outputs.

Fault Management

UVLO and Power-OK

The MAX5913A/MAX5914A monitor the V_{CC} input voltage and each switch's current and voltage to determine POK, overcurrent, or Port-OC status. When V_{CC} falls below the UVLO threshold, FAULT goes low and all four switches and relays are turned off. When the voltage across the switch is less than 1.5V, the switch is fully on, and if the switch is not in current limit or open circuit, POK status is good (high).

Open-Circuit Faults

With the open-circuit detector enabled, when any switch current falls below the open-circuit detector threshold current, the open-circuit detector turns off the switch after a 25.6ms delay, FAULT goes low, and the Port-OC flag is set for that switch. To clear the switch latched-off condition, FAULT and Port-OC flags drive the corresponding ON input low.

MAX5913A/MAX5914A

+48V Quad Hot-Swap Controllers For Power-Over-LAN

Overcurrent Faults

When an on-switch current exceeds the current-limit threshold, foldback circuitry activates and regulates the switch current. When the current limit lasts for longer than t_0 , the switch latches off. The POK status flag is set low, and the FAULT flag is set. If auto-retry is enabled, the switch remains off for a period t_{OFF} . If auto-retry is disabled, the switch remains latched off, and FAULT is low. Reset the latch and FAULT by driving corresponding ON_ low.

Applications Information

Considerations for circuit design include output capacitor requirements, current-limit requirements, setting the maximum on-time in current limit, and choosing a suitable MOSFET and on-time duty cycle in auto-retry.

Output Capacitor Requirements

The load capacitor requirements should be determined first, as this affects the required startup.

Current-Limit Requirements (Choosing RSENSE)

The current limit should be set to at least 20% higher than the expected full load current. If current limit is also used to control startup current, then set this limit high enough so that the output voltage can rise and settle before t_0 elapses (see the *Setting t₀ (Choosing RRTIM)* section).

Setting t₀ (Choosing RRTIM)

Choose the t_0 time by connecting a $2\text{k}\Omega$ to $40\text{k}\Omega$ resistor from RRTIM to DGND. The minimum 6.4ms t_0 is set with $R_{RTIM} = 2\text{k}\Omega$. The maximum 128ms t_0 is set with $R_{RTIM} = 40\text{k}\Omega$ set according to the following equation:

$$t_0 = (R_{RTIM} / 2\text{k}\Omega) (6.4\text{ms})$$

t_0 should be chosen appropriately, depending on the startup condition. There are two cases:

- 1) For startup without current limit, when:

$$I = I_{GATE} \frac{C_L}{C_{GATE}} + I_L < \frac{V_{SC}}{R_{SENSE}}$$

The startup current does not reach the maximum current-limit threshold and t_0 will not activate during startup condition. In this case, set t_0 to a small

value, but large enough to allow the switch to remain on during large output load-current transients. The smaller the t_0 , the faster the MAX5913A/MAX5914A turn off the external FET in case of output overload or short-circuit condition.

- 2) For startup with current limit, when:

$$I = I_{GATE} \left(\frac{C_L}{C_{GATE}} + I_L \right) \geq \frac{V_{SC}}{R_{SENSE}}$$

which is expected when:

$$\frac{C_L}{C_{GATE}}$$

is large, t_0 must be set to be long enough to allow the output voltage to rise and settle before t_0 elapses. In this case, t_0 must satisfy the following equation:

$$t_0 = C_L \frac{\frac{18}{2} I_{MAX} - I_L}{I_{MAX} - I_L} + C_L \frac{V_{CC} - 18\text{V}}{I_{MAX} - I_L}$$

where V_{CC} is the input voltage and given that $I_L < I_{LIM}$.

Choosing Power MOSFET

The FET must withstand a short-circuit condition where its power dissipation is $P_{DISS} = V_{CC} \times I_{LIM}$. The FET must have sufficient thermal capacitance to prevent thermal heating damage during the t_0 time.

Choose Duty Cycle (Setting DC)

The duty cycle can be adjusted to allow time for heat to dissipate between t_0 cycles, allowing use of smaller MOSFETs with lower thermal capacitance. For smaller duty cycle, a smaller FET is sufficient. See Table 2 for setting the duty cycle.

The auto-retry off-time should not be too long to keep the system wait time during retry period to a reasonable value. For example, when t_0 is set to 128ms and duty cycle is set to 1%, the retry time is $99 \times 128\text{ms} = 12.7\text{s}$.

Application Circuits

In a typical LAN system there are two ways to deliver power over the LAN cable. Power can be supplied to the unused cable pairs, or power can be supplied over the signal pairs (Figures 9 and 10).

+48V Quad Hot-Swap Controllers For Power-Over-LAN

MAX5913A/MAX5914A

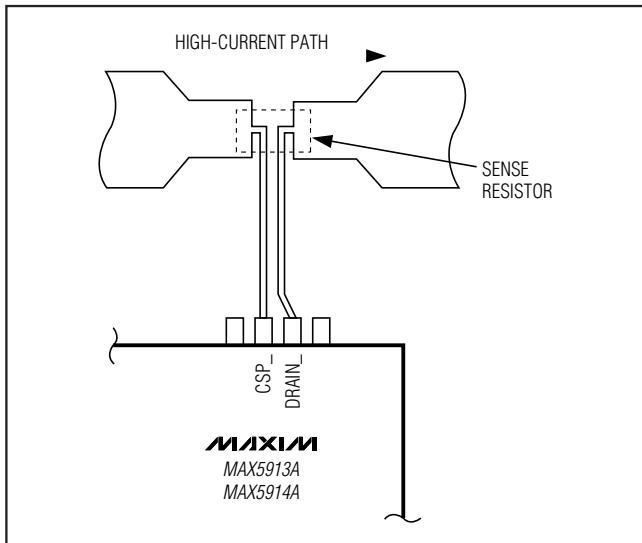


Figure 7. Recommended Layout for Kelvin-Sensing Current Through Sense Resistor

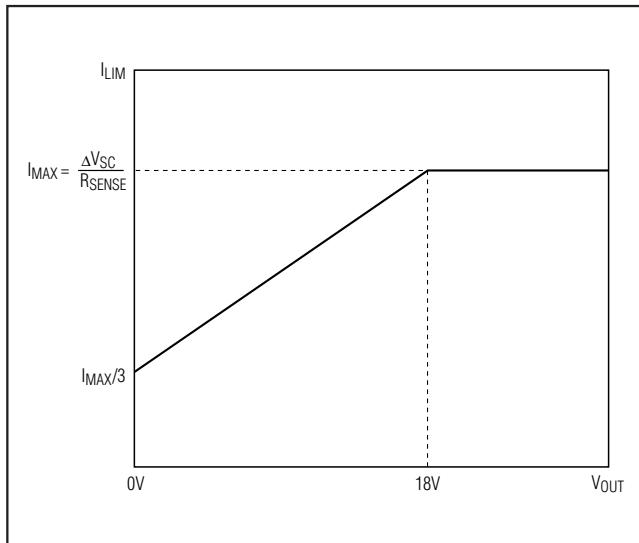
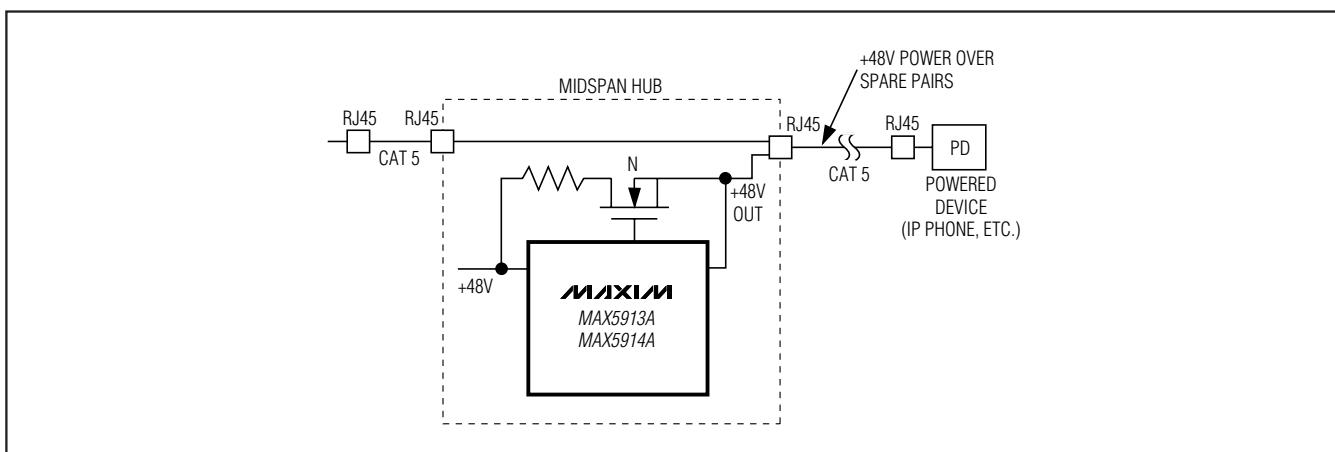
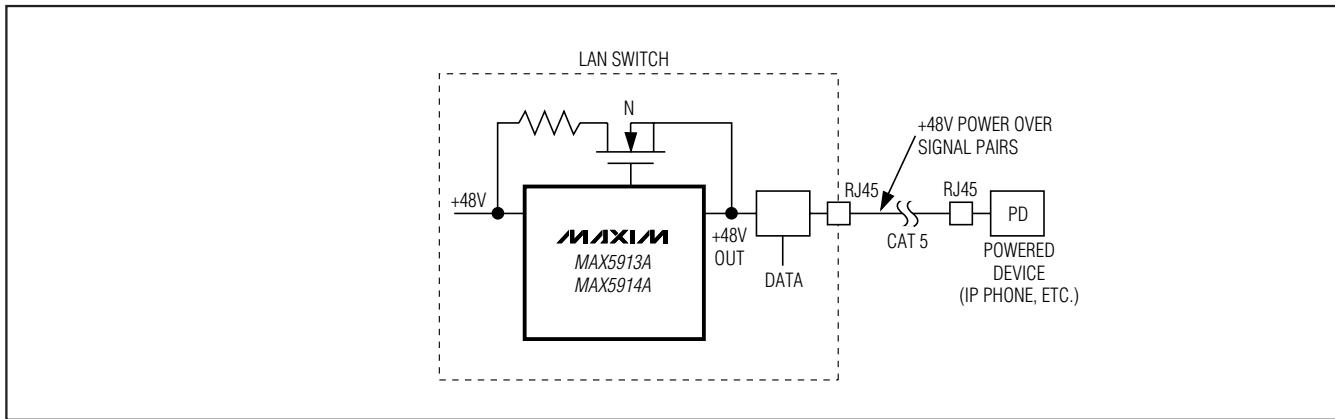


Figure 8. Foldback Current-Limit Response

Table 2. Duty Programming Cycle

DC	tOFF	DUTY CYCLE
0	$99 \times t_O$	1%
1	$49 \times t_O$	2%
Open	$24 \times t_O$	4%

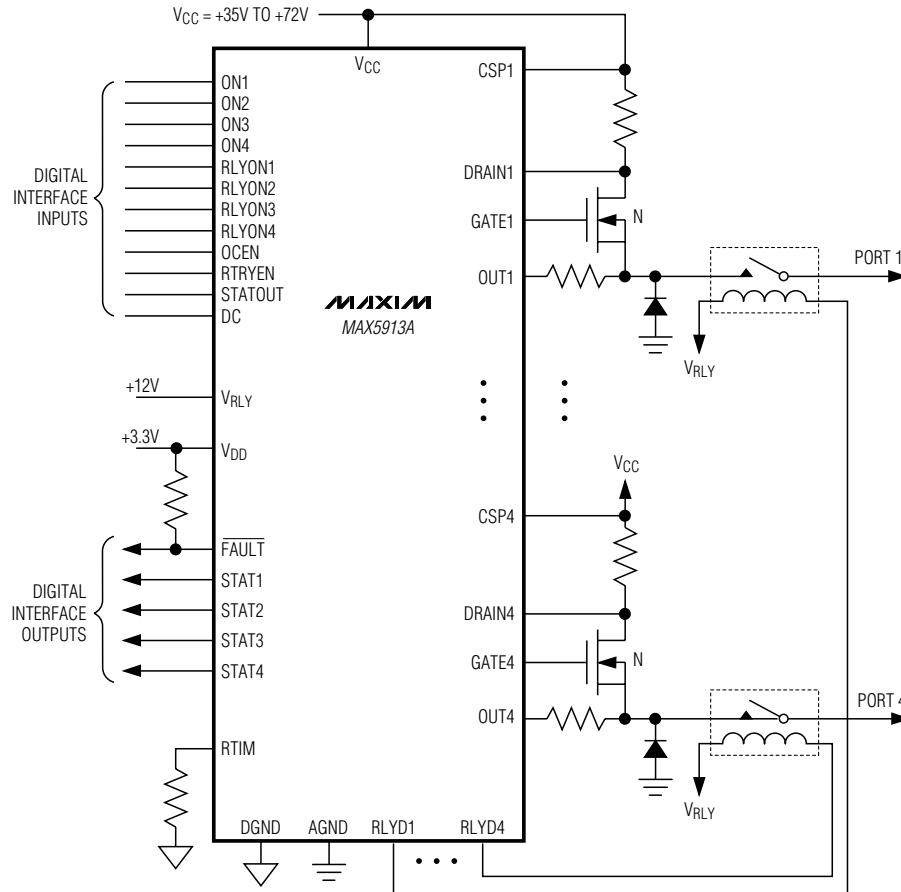
+48V Quad Hot-Swap Controllers For Power-Over-LAN



+48V Quad Hot-Swap Controllers For Power-Over-LAN

Typical Operating Circuit

MAX5913A/MAX5914A



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
44 MQFP	M44+3	21-0826	90-0169

+48V Quad Hot-Swap Controllers For Power-Over-LAN

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/04	Initial release	—
1	1/11	Released the MAX5914A. Updated the <i>Ordering Information</i> , <i>Electrical Characteristics</i> , <i>Typical Operating Characteristics</i> , <i>Pin Description</i> , and the <i>Programming Timing</i> , <i>RTIM</i> section	1–9, 15

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