



## FEATURES

- Fast access time : 12/15 ns (max.)
- Low operating power consumption :  
60 mA (typical)
- Power Supply range 3.1V to 3.6V
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Package : 32-pin 300 mil skinny PDIP  
32-pin 300 mil SOJ  
32-pin 450mil SOP  
32-pin 8mm x 20mm TSOP-1  
32-pin 8mm x 13.4mm STSOP

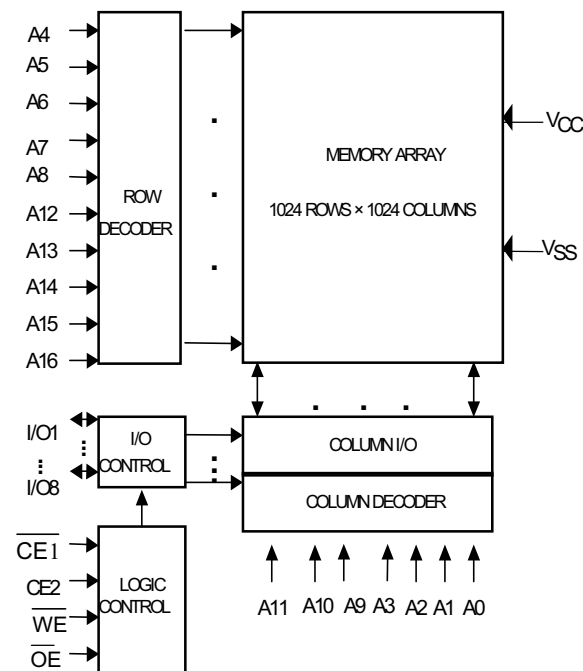
## GENERAL DESCRIPTION

The UT61L1024 is a 1,048,576-bit high-speed CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

The UT61L1024 is designed for high-speed system applications. It is particularly suited for use in high-density high-speed system applications.

The UT61L1024 operates from a single 3.3V power supply and all inputs and outputs are fully TTL compatible.

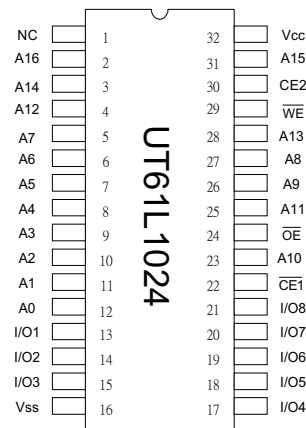
## FUNCTIONAL BLOCK DIAGRAM



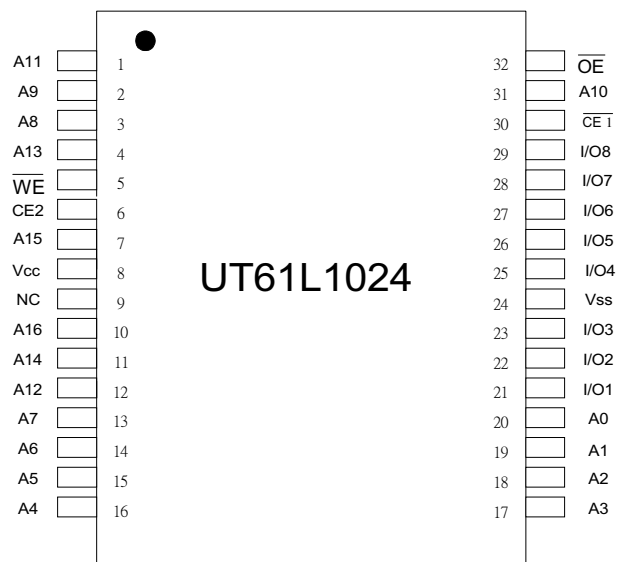
## PIN DESCRIPTION

| SYMBOL          | DESCRIPTION            |
|-----------------|------------------------|
| A0 - A16        | Address Inputs         |
| I/O1 - I/O8     | Data Inputs/Outputs    |
| CE1, CE2        | Chip enable 1,2 Inputs |
| WE              | Write Enable Input     |
| OE              | Output Enable Input    |
| V <sub>CC</sub> | Power Supply           |
| V <sub>SS</sub> | Ground                 |
| NC              | No Connection          |

## PIN CONFIGURATION



PDIP / SOJ / SOP



TSOP-I / STSOP

**ABSOLUTE MAXIMUM RATINGS\***

| PARAMETER  | SYMBOL              | RATING       | UNIT |
|--|---------------------|--------------|------|
| Terminal Voltage with Respect to V <sub>SS</sub> | V <sub>TERM</sub>   | -0.5 to +4.6 | V    |
| Operating Temperature                            | T <sub>A</sub>      | 0 to +70     | °C   |
| Storage Temperature                              | T <sub>STG</sub>    | -65 to +150  | °C   |
| Power Dissipation                                | P <sub>D</sub>      | 1            | W    |
| DC Output Current                                | I <sub>OUT</sub>    | 50           | mA   |
| Soldering Temperature (under 10 sec)             | T <sub>solder</sub> | 260          | °C   |

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

**TRUTH TABLE**

| MODE           | $\overline{CE1}$ | CE2 | $\overline{OE}$ | $\overline{WE}$ | I/O OPERATION    | SUPPLY CURRENT                     |
|----------------|------------------|-----|-----------------|-----------------|------------------|------------------------------------|
| Standby        | H                | X   | X               | X               | High - Z         | I <sub>SB</sub> , I <sub>SB1</sub> |
| Standby        | X                | L   | X               | X               | High - Z         | I <sub>SB</sub> , I <sub>SB1</sub> |
| Output Disable | L                | H   | H               | H               | High - Z         | I <sub>CC</sub>                    |
| Read           | L                | H   | L               | H               | D <sub>OUT</sub> | I <sub>CC</sub>                    |
| Write          | L                | H   | X               | L               | D <sub>IN</sub>  | I <sub>CC</sub>                    |

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

**DC ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub> = 3.1V~3.6V, T<sub>A</sub> = 0°C to 70°C)

| PARAMETER                      | SYMBOL           | TEST CONDITION  | MIN.         | MAX.                 | UNIT     |
|--------------------------------|------------------|---|--------------|----------------------|----------|
| Input High Voltage             | V <sub>IH</sub>  |   | 2.0          | V <sub>CC</sub> +0.5 | V        |
| Input Low Voltage              | V <sub>IL</sub>  |   | - 0.5        | 0.6                  | V        |
| Input Leakage Current          | I <sub>LI</sub>  | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>   | - 1          | 1                    | μA       |
| Output Leakage Current         | I <sub>LO</sub>  | V <sub>SS</sub> ≤ V <sub>I/O</sub> ≤ V <sub>CC</sub><br>$\overline{CE1} = V_{IH}$ or CE2 = V <sub>IL</sub><br>or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ | - 1          | 1                    | μA       |
| Output High Voltage            | V <sub>OH</sub>  | I <sub>OH</sub> = - 4mA   | 2.2          | -                    | V        |
| Output Low Voltage             | V <sub>OL</sub>  | I <sub>OL</sub> = 8mA   | -            | 0.4                  | V        |
| Operating Power Supply Current | I <sub>CC</sub>  | Cycle time=Min, I <sub>I/O</sub> = 0mA,<br>$\overline{CE1} = V_{IL}$ , CE2 = V <sub>IH</sub>  | - 12<br>- 15 | 100<br>90            | mA<br>mA |
| Standby Power Supply Current   | I <sub>SB</sub>  | $\overline{CE1} = V_{IH}$ or CE2 = V <sub>IL</sub>  | -            | 20                   | mA       |
|                                | I <sub>SB1</sub> | $\overline{CE1} \geq V_{CC}-0.2V$ ; or CE2 ≤ 0.2V   | -            | 3                    | mA       |



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Rev 1.4

UT61L1024

128K X 8 BIT HIGH SPEED CMOS SRAM

## CAPACITANCE ( $T_A=25^{\circ}\text{C}$ , $f=1.0\text{MHz}$ )

| PARAMETER                | SYMBOL    | MIN. | MAX. | UNIT |
|--------------------------|-----------|------|------|------|
| Input Capacitance        | $C_{IN}$  | -    | 8    | pF   |
| Input/Output Capacitance | $C_{I/O}$ | -    | 10   | pF   |

Note : These parameters are guaranteed by device characterization, but not production tested.

## AC TEST CONDITIONS

|  |  |
|--|--|
| Input Pulse Levels                       | 0V to 3.0V   |
| Input Rise and Fall Times                | 3ns  |
| Input and Output Timing Reference Levels | 1.5V   |
| Output Load                              | $C_L=30\text{pF}$ , $I_{OH}/I_{OL}=-4\text{mA}/8\text{mA}$ |

## AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 3.1\text{V} \sim 3.6\text{V}$ , $T_A = 0^{\circ}\text{C}$ to $70^{\circ}\text{C}$ )

### (1) READ CYCLE

| PARAMETER                          | SYMBOL                      | UT61L1024-12 |      | UT61L1024-15 |      | UNIT |
|------------------------------------|-----------------------------|--------------|------|--------------|------|------|
|                                    |                             | MIN.         | MAX. | MIN.         | MAX. |      |
| Read Cycle Time                    | $t_{RC}$                    | 12           | -    | 15           | -    | ns   |
| Address Access Time                | $t_{AA}$                    | -            | 12   | -            | 15   | ns   |
| Chip Enable Access Time            | $t_{ACE1^*}$ , $t_{ACE1}$   | -            | 12   | -            | 15   | ns   |
| Output Enable Access Time          | $t_{OE}$                    | -            | 6    | -            | 7    | ns   |
| Chip Enable to Output in Low Z     | $t_{CLZ1^*}$ , $t_{CLZ2^*}$ | 3            | -    | 4            | -    | ns   |
| Output Enable to Output in Low Z   | $t_{OLZ^*}$                 | 0            | -    | 0            | -    | ns   |
| Chip Disable to Output in High Z   | $t_{CHZ1^*}$ , $t_{CHZ2^*}$ | -            | 6    | -            | 7    | ns   |
| Output Disable to Output in High Z | $t_{OHZ^*}$                 | -            | 6    | -            | 7    | ns   |
| Output Hold from Address Change    | $t_{OH}$                    | 3            | -    | 3            | -    | ns   |

### (2) WRITE CYCLE

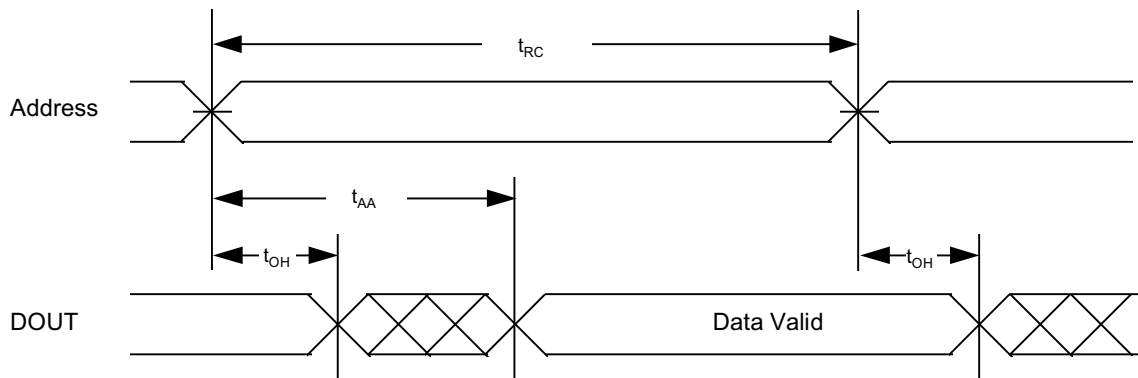
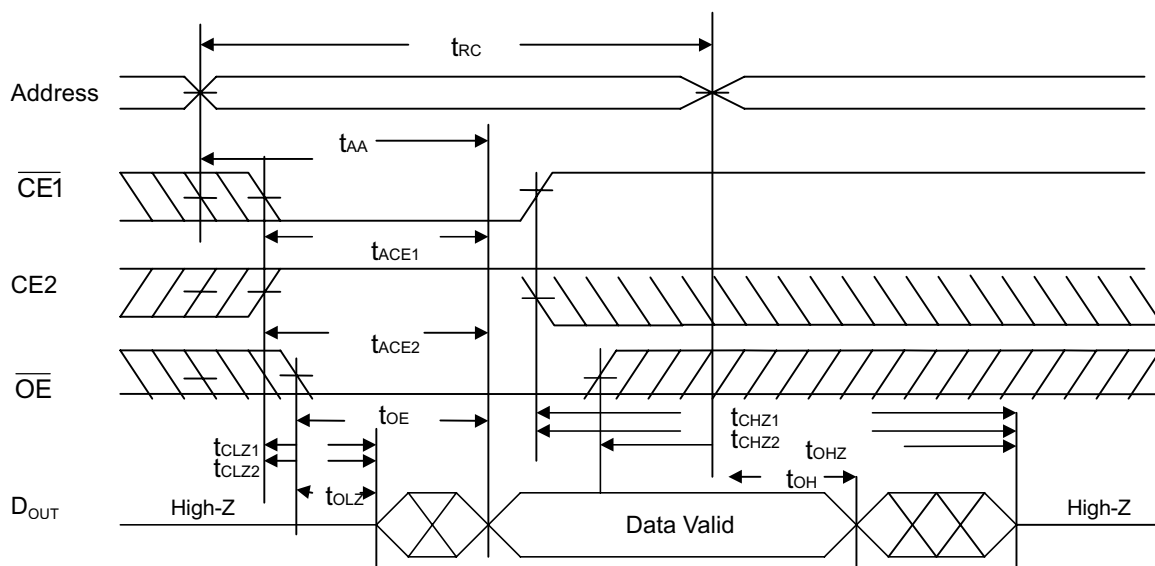
| PARAMETER                        | SYMBOL                  | UT61L1024-12 |      | UT61L1024-15 |      | UNIT |
|----------------------------------|-------------------------|--------------|------|--------------|------|------|
|                                  |                         | MIN.         | MAX. | MIN.         | MAX. |      |
| Write Cycle Time                 | $t_{WC}$                | 12           | -    | 15           | -    | ns   |
| Address Valid to End of Write    | $t_{AW}$                | 10           | -    | 12           | -    | ns   |
| Chip Enable to End of Write      | $t_{CW1^*}$ , $t_{CW2}$ | 10           | -    | 12           | -    | ns   |
| Address Set-up Time              | $t_{AS}$                | 0            | -    | 0            | -    | ns   |
| Write Pulse Width                | $t_{WP}$                | 9            | -    | 10           | -    | ns   |
| Write Recovery Time              | $t_{WR}$                | 0            | -    | 0            | -    | ns   |
| Data to Write Time Overlap       | $t_{DW}$                | 7            | -    | 8            | -    | ns   |
| Data Hold from End of Write Time | $t_{DH}$                | 0            | -    | 0            | -    | ns   |
| Output Active from End of Write  | $t_{OW^*}$              | 3            | -    | 4            | -    | ns   |
| Write to Output in High Z        | $t_{WHZ^*}$             | -            | 7    | -            | 8    | ns   |

\*These parameters are guaranteed by device characterization, but not production tested.



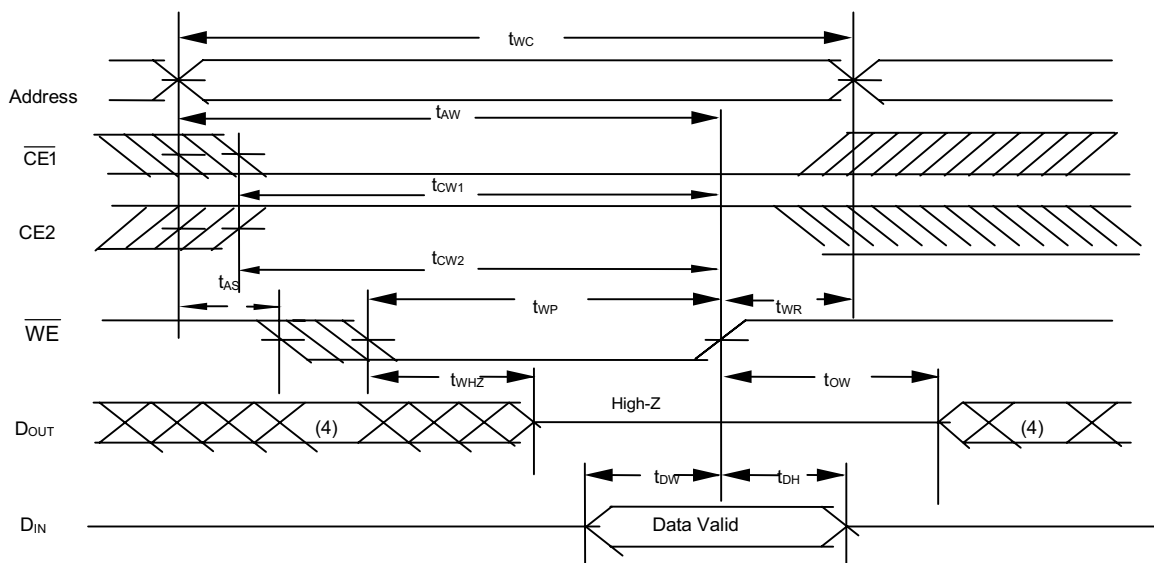
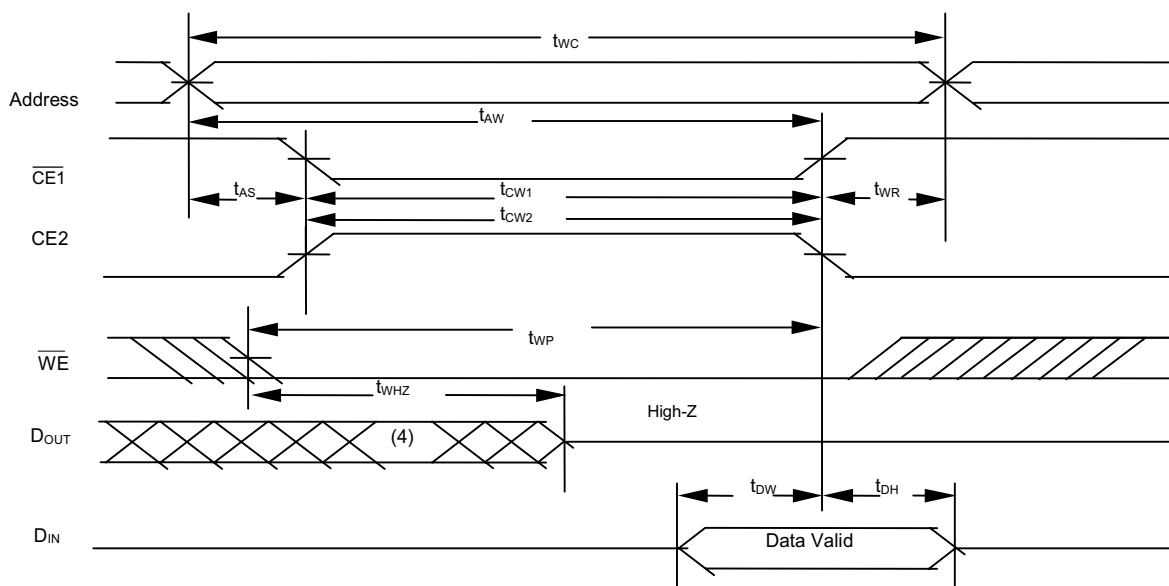
## TIMING WAVEFORMS

## READ CYCLE 1 (Address Controlled) (1,2,4)

READ CYCLE 2 ( $\overline{CE1}$ , CE2 and  $\overline{OE}$  Controlled) (1,3,5,6)

## Notes :

1.  $\overline{WE}$  is HIGH for read cycle.
2. Device is continuously selected  $\overline{CE1} = V_{IL}$  and  $CE2 = V_{IH}$ .
3. Address must be valid prior to or coincident with  $\overline{CE1}$  and CE2 transition; otherwise  $t_{AA}$  is the limiting parameter.
4.  $\overline{OE}$  is low.
5.  $t_{CLZ1}$ ,  $t_{CLZ2}$ ,  $t_{OLZ}$ ,  $t_{CHZ1}$ ,  $t_{CHZ2}$  and  $t_{OHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
6. At any given temperature and voltage condition,  $t_{CHZ1}$  is less than  $t_{CLZ1}$ ,  $t_{CHZ2}$  is less than  $t_{CLZ2}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .

**WRITE CYCLE 1** ( $\overline{\text{WE}}$  Controlled) (1,2,3,5)**WRITE CYCLE 2** ( $\overline{\text{CE1}}$  and CE2 Controlled) (1,2,5)

## Notes :

1.  $\overline{\text{WE}}$  or  $\overline{\text{CE1}}$  must be HIGH during all address transitions.
2. A write occurs during the overlap of a low  $\overline{\text{CE1}}$  and a low  $\overline{\text{WE}}$ .
3. During a  $\overline{\text{WE}}$  controlled write cycle with  $\overline{\text{OE}}$  LOW,  $t_{WP}$  must be greater than  $t_{WHZ} + t_{DW}$  to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{\text{CE1}}$  LOW transition occurs simultaneously with or after  $\overline{\text{WE}}$  LOW transition, the outputs remain in a high impedance state.
6.  $t_{OW}$  and  $t_{WHZ}$  are specified with  $C_L = 5\text{pF}$ . Transition is measured  $\pm 500\text{mV}$  from steady state.



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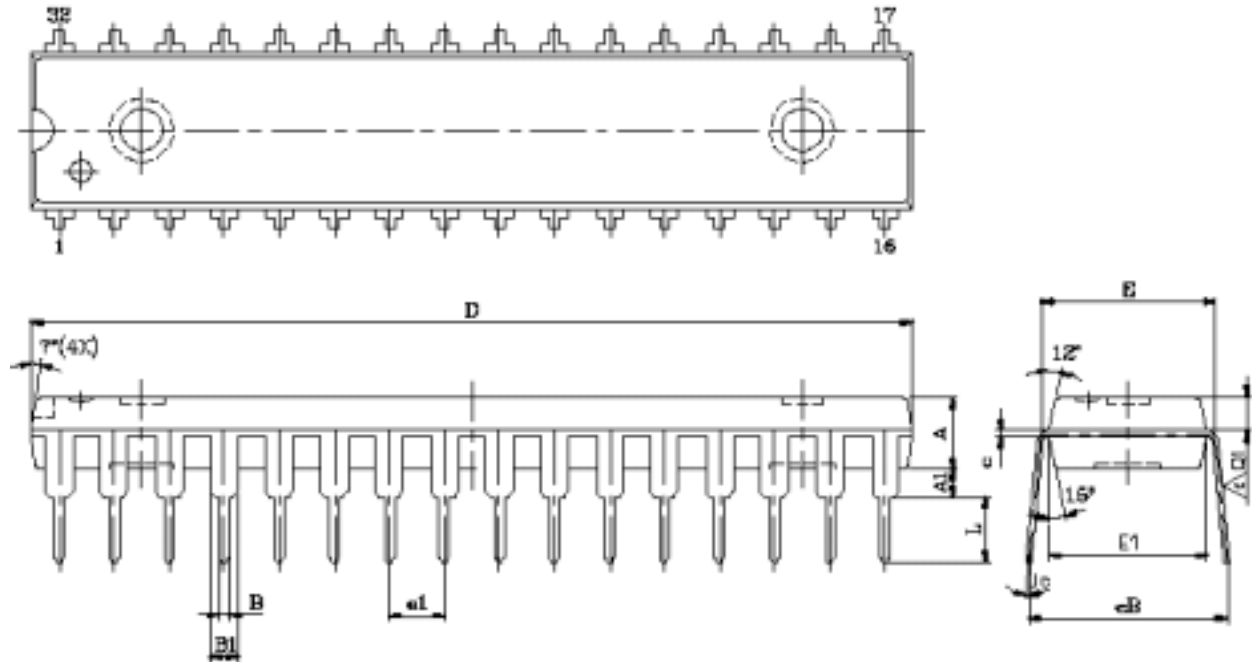
Rev 1.4

UT61L1024

128K X 8 BIT HIGH SPEED CMOS SRAM

## PACKAGE OUTLINE DIMENSION

### 32 pin PDIP 300mil Package Outline Dimension



| SYMBOL \ UNIT | INCH(BASE)              | MM(REF)                 |
|---------------|-------------------------|-------------------------|
| A             | $0.130 \pm 0.005$       | $3.302 \pm 0.127$       |
| A1            | 0.015(MIN)              | 0.381 (MIN)             |
| B             | $0.018 \pm 0.004$       | $0.457 \pm 0.102$       |
| B1            | $0.050 \pm 0.008$       | $1.270 \pm 0.203$       |
| c             | $0.010 \pm 0.004$       | $0.254 \pm 0.102$       |
| D             | $1.600 \pm 0.005$       | $40.640 \pm 0.127$      |
| E             | $0.315 \pm 0.010$       | $8.001 \pm 0.254$       |
| E1            | $0.288 \pm 0.004$       | $7.315 \pm 0.102$       |
| e1            | 0.100 TYP               | 2.540 TYP               |
| eB            | $0.350 \pm 0.020$       | $8.890 \pm 0.508$       |
| L             | 0.125 (MIN)             | 3.175 (MIN)             |
| Q1            | $0.060 \pm 0.005$       | $1.524 \pm 0.127$       |
| Jc            | $0^\circ \sim 10^\circ$ | $0^\circ \sim 10^\circ$ |





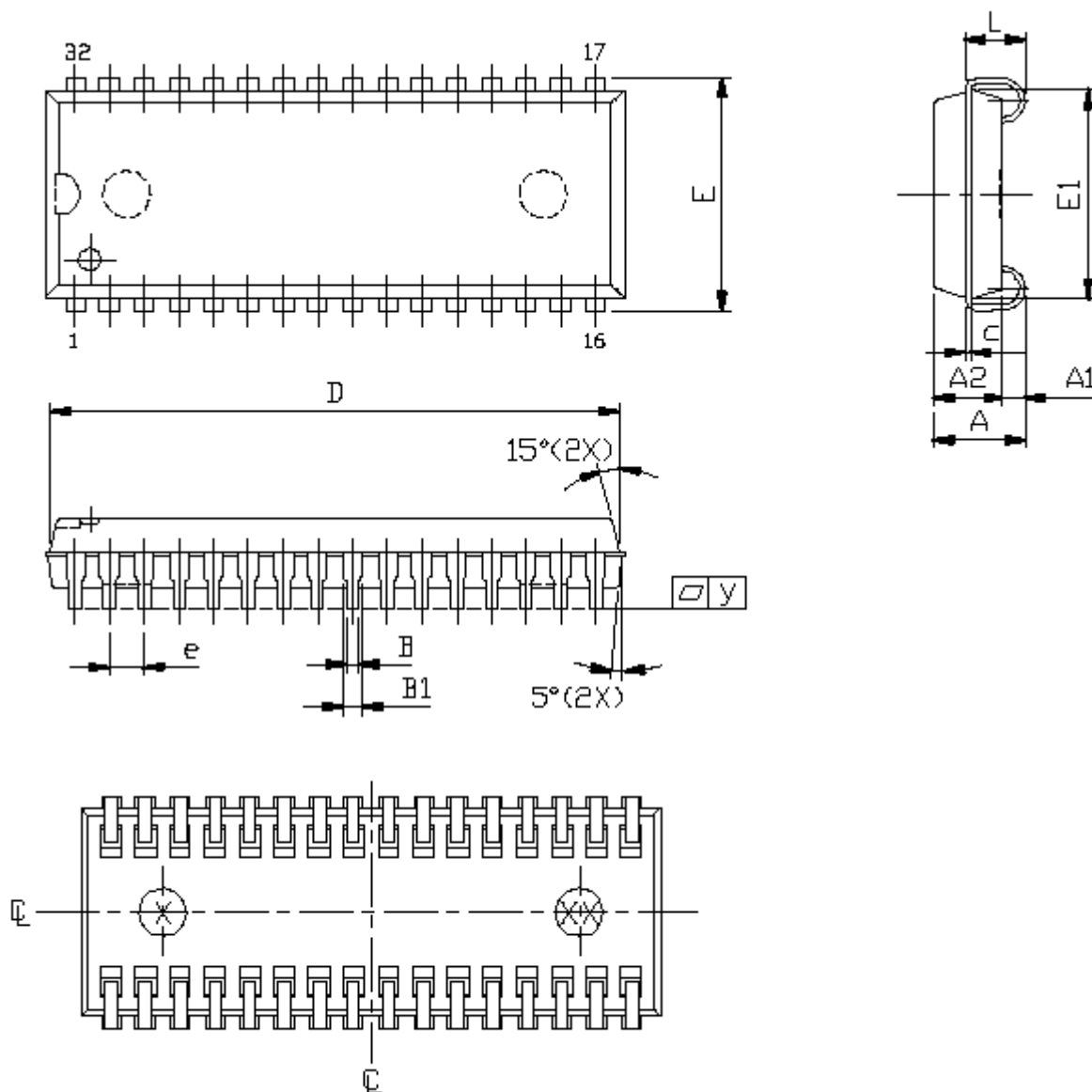
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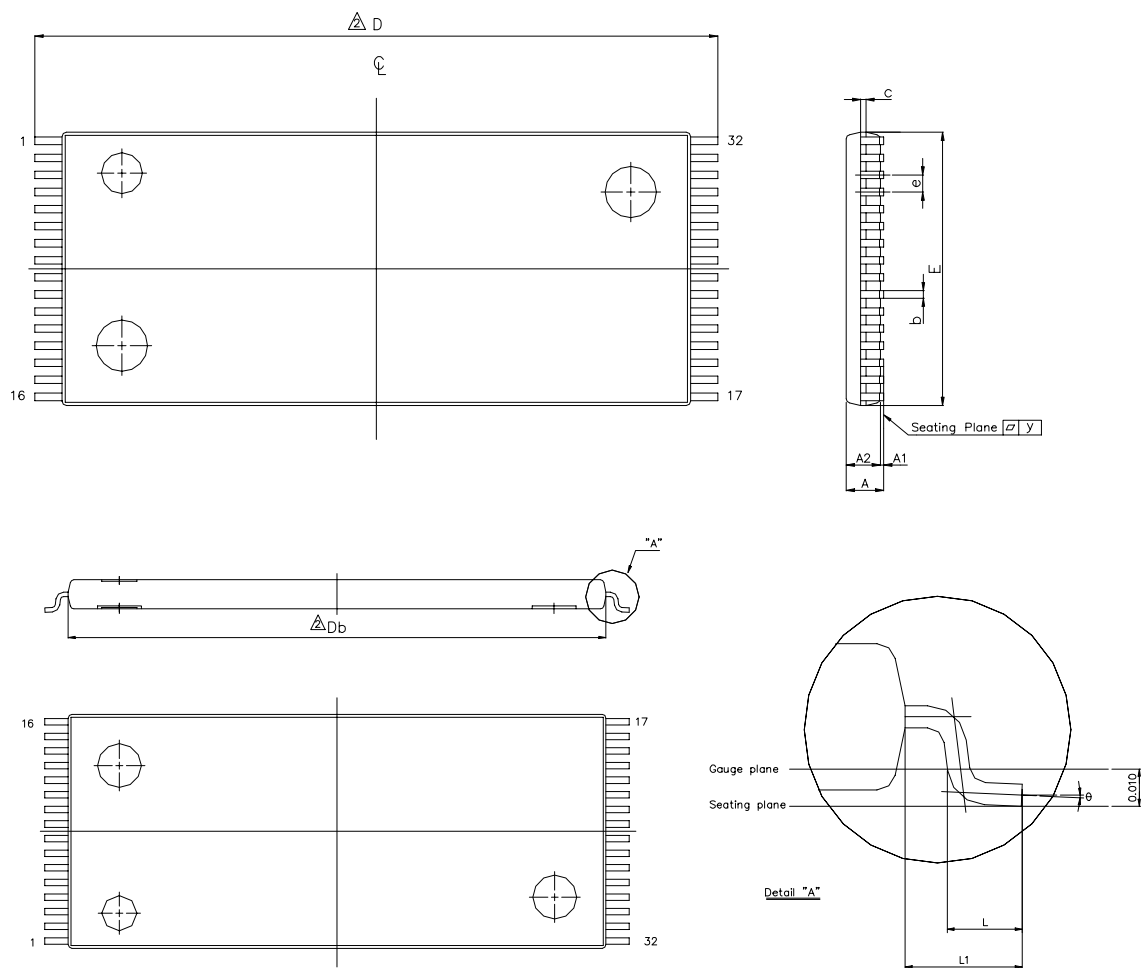
128K X 8 BIT HIGH SPEED CMOS SRAM

### 32 pin SOJ Package Outline Dimension

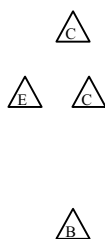


| SYMBOL | UNIT | INCH(BASE)    | MM(REF)       |
|--------|------|---------------|---------------|
| A      |      | 0.148 (MAX)   | 3.759 (MAX)   |
| A1     |      | 0.026 (MIN)   | 0.660 (MIN)   |
| A2     |      | 0.100 ± 0.005 | 2.540 ± 0.127 |
| B      |      | 0.018 (TYP)   | 0.457(TYP)    |
| B1     |      | 0.028 (TYP)   | 0.711 (TYP)   |
| C      |      | 0.010 (TYP)   | 0.254 (TYP)   |
| D      |      | 0.830 (MAX)   | 21.082 (MAX)  |
| E      |      | 0.335 (TYP)   | 8.509 (TYP)   |
| E1     |      | 0.300 ± 0.005 | 7.620 ± 0.127 |
| e      |      | 0.050 (TYP)   | 1.270 (TYP)   |
| L      |      | 0.086 ± 0.010 | 2.184 ± 0.254 |
| y      |      | 0.003 (MAX)   | 0.076 (MAX)   |

### 32 pin 8mm × 20mm TSOP-I Package Outline Dimension



| UNIT<br>SYMBOL | INCH(BASE)     | MM(REF)      |
|----------------|----------------|--------------|
| A              | 0.047 (MAX)    | 1.20 (MAX)   |
| A1             | 0.004 ± 0.002  | 0.10 ± 0.05  |
| A2             | 0.039 ± 0.002  | 1.00 ± 0.05  |
| b              | 0.008 + 0.002  | 0.20 + 0.05  |
| c              | 0.005 (TYP)    | 0.127 (TYP)  |
| D              | 0.724 ± 0.004  | 18.40 ± 0.10 |
| E              | 0.315 ± 0.004  | 8.00 ± 0.10  |
| e              | 0.020 (TYP)    | 0.50 (TYP)   |
| HD             | 0.787 ± 0.008  | 20.00 ± 0.20 |
| L              | 0.0197 ± 0.004 | 0.50 ± 0.10  |
| L1             | 0.0315 ± 0.004 | 0.08 ± 0.10  |
| y              | 0.003 (MAX)    | 0.076 (MAX)  |
| Θ              | 0°~5°          | 0°~5°        |







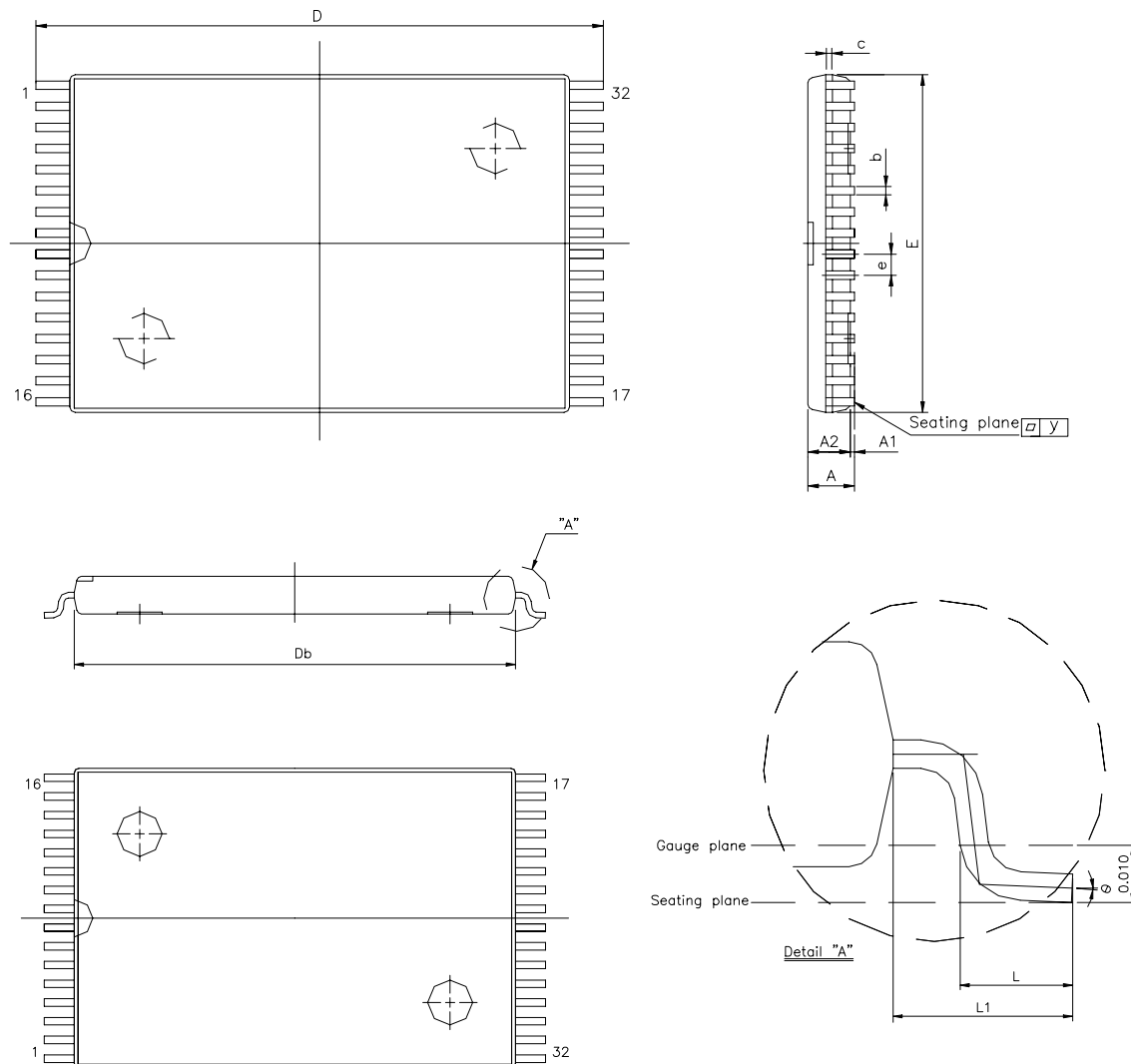
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# UT61L1024

## 128K X 8 BIT HIGH SPEED CMOS SRAM

### 32 pin 8mm x 13.4mm STSOP Package Outline Dimension



#### Note :

- 1.E dimension is not including end flash.
- 2.The total of both sides' end flash is not above 0.3mm.

| SYMBOL | UNIT | MM(REF)    | INCH(BASE)   |
|--------|------|------------|--------------|
| A      |      | 1.20(Max.) | 0.047(Max.)  |
| A1     |      | 0.1060.05  | 0.00460.002  |
| A2     |      | 1.0060.05  | 0.03960.002  |
| b      |      | 0.20(typ.) | 0.006(typ.)  |
| c      |      | 0.15(typ.) | 0.006(typ.)  |
| D      |      | 13.4060.20 | 0.52660.006  |
| Db     |      | 11.8060.10 | 0.46560.004  |
| E      |      | 8.00060.10 | 0.31560.004  |
| e      |      | 0.50(typ.) | 0.020(typ.)  |
| L      |      | 0.5060.10  | 0.02060.004  |
| L1     |      | 0.8060.10  | 0.031560.004 |
| y      |      | 0.08(Max.) | 0.003(Max.)  |
| e      |      | 08~58      | 08~58        |



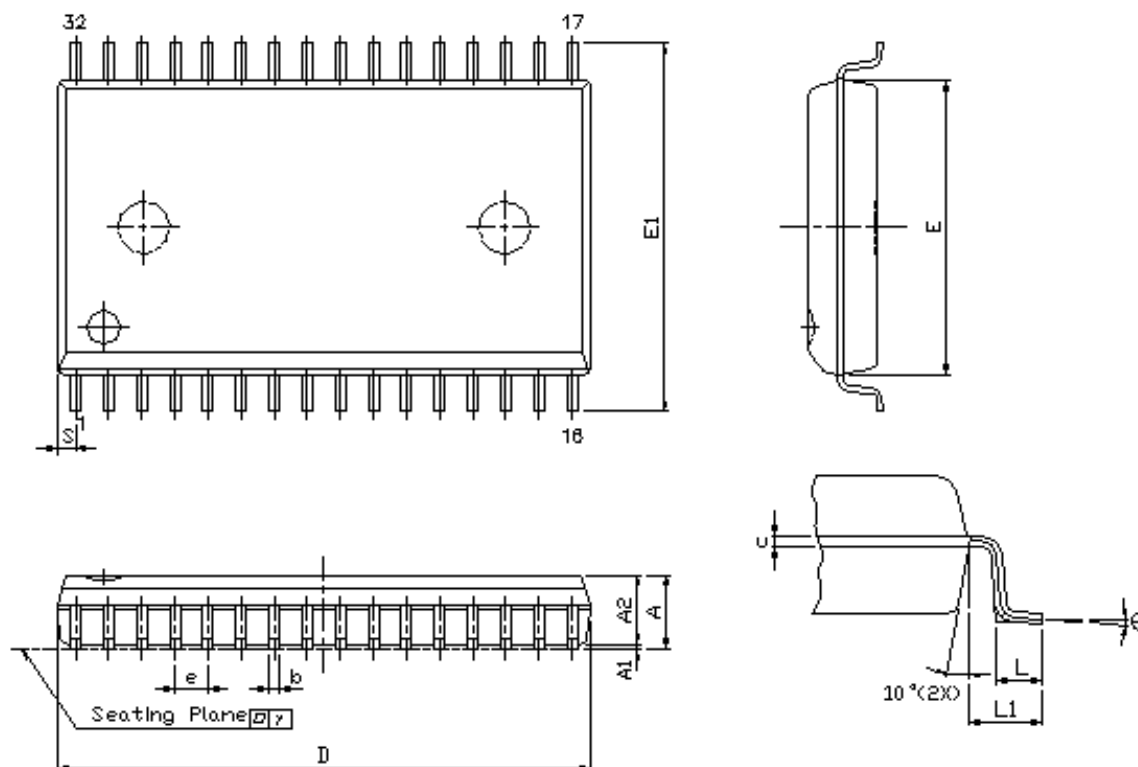
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128K X 8 BIT HIGH SPEED CMOS SRAM

32 pin 445mil SOP Package Outline Dimension



| SYMBOL | UNIT | INCH(BASE)   | MM(REF)      |
|--------|------|--------------|--------------|
| A      |      | 0.118(MAX.)  | 0.047(MAX.)  |
| A1     |      | 0.004(MIN)   | 0.00460.002  |
| A2     |      | 0.111(MAX)   | 0.03960.002  |
| b      |      | 0.016(TYP.)  | 0.006(TYP.)  |
| c      |      | 0.008(TYP.)  | 0.006(TYP.)  |
| D      |      | 0.817(MAX)   | 0.52660.006  |
| E      |      | 0.44560.005  | 0.31560.004  |
| e      |      | 0.050(TYP.)  | 0.020(TYP.)  |
| L      |      | 0.034760.008 | 0.02060.004  |
| L1     |      | 0.05560.008  | 0.031560.004 |
| S      |      | 0.026(MAX)   | 0.914(MAX)   |
| y      |      | 0.004(MAX.)  | 0.101(MAX.)  |
| Θ      |      | 08~108       | 08~108       |



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## ORDERING INFORMATION

| PART NO.       | ACCESS TIME (ns) | PACKAGE           |
|----------------|------------------|-------------------|
| UT61L1024KC-12 | 12               | 32PIN SKINNY PDIP |
| UT61L1024KC-15 | 15               | 32PIN SKINNY PDIP |
| UT61L1024JC-12 | 12               | 32PIN SOJ         |
| UT61L1024JC-15 | 15               | 32PIN SOJ         |
| UT61L1024SC-12 | 12               | 32PIN SOP         |
| UT61L1024LC-12 | 12               | 32PIN TSOP-1      |
| UT61L1024LC-15 | 15               | 32PIN TSOP-1      |
| UT61L1024LS-12 | 12               | 32PIN STSOP       |
| UT61L1024LS-15 | 15               | 32PIN STSOP       |



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## REVISION HISTORY

| REVISION | DESCRIPTION   | DATE         |
|----------|---|--------------|
| Rev. 1.0 | Original.   | Apr. 05 2000 |
| Rev. 1.1 | Add TSOP-I Package  | Aug. 29.2000 |
| Rev. 1.2 | Modify the format of power consumption  | Sep. 01.2000 |
| Rev. 1.3 | 1. $V_{OH}$ : 2.4 -> 2.2<br>2. Input Rise & Fall times : 5->3ns<br>3. The symbols CE1# ,OE# & WE# are revised as $\overline{CE1}$ , $\overline{OE}$ & $\overline{WE}$ | Jun. 18,2001 |
| Rev.1.4  | Add SOP Package.  | Jul. 6,2001  |