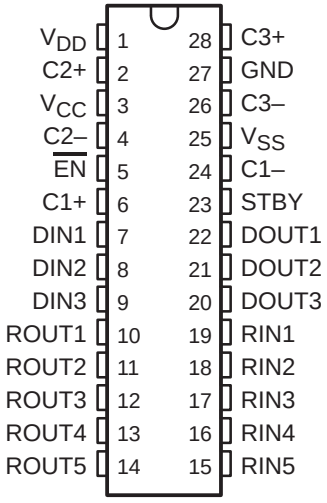
- **Single-Chip and Single-Supply Interface for IBM PC/AT™ Serial Port**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.11 Standards**
- **Operates With 3.3-V or 5-V Supplies**
- **One Receiver Remains Active During Standby (Wake-up Mode)**
- **Designed to Operate at 128 kbit/s Over a 3-m Cable**
- **Low Standby Current . . . 5 μA Max**
- **ESD Protection on RS-232 Pins Meets or Exceeds 4 kV (HBM) and 1.5 kV (HBM) on All Pins Per MIL-STD-883, Method 3015**
- **External Capacitors . . . 0.1 μF**
  (V_{CC} = 3.3 V . . . Five External Capacitors)
  (V_{CC} = 5 V . . . Four External Capacitors)
- **Accepts 5-V Logic Input With 3.3-V Supply**
- **Applications**
  - **RS-232 Interface**
  - **Battery-Powered Systems, PDAs**
  - **Notebook, Laptop, and Palmtop PCs**
  - **External Modems and Hand-Held Terminals**
- **Packaged in Shrink Small-Outline Package**

DB PACKAGE†
(TOP VIEW)



† The DB package is only available in left-ended tape and reel (order part number SN75LV4737ADBR).

description

The SN75LV4737A‡ consists of three line drivers, five line receivers, and a charge-pump circuit. It provides the electrical interface between an asynchronous communication controller and the serial-port connector, and meets the requirements of TIA/EIA-232-F. This combination of drivers and receivers matches those needed for the typical serial port used in an IBM PC/AT or compatibles. The charge pump and five small external capacitors allow operation from a single 3.3-V supply, and four capacitors allow operation from a 5-V supply.

The device has flexible control options for power management when the serial port is inactive. A common disable for all of the drivers and receivers is provided with the active-high STBY input. The active-low $\overline{EN}$ input is an enable for one receiver to implement a wake-up feature for the serial port. All the logic inputs can accept signals from controllers operating from a 5-V supply, even though the SN75LV4737A is operating from 3.3 V.

The SN75LV4737A is characterized for operation over the temperature range of 0°C to 70°C.

‡ Patent-pending design

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Function Tables

EACH DRIVER

INPUTS		OUTPUT
DIN	STBY	DOUT
X	H	Z
L	L	H
H	L	L
Open	L	L

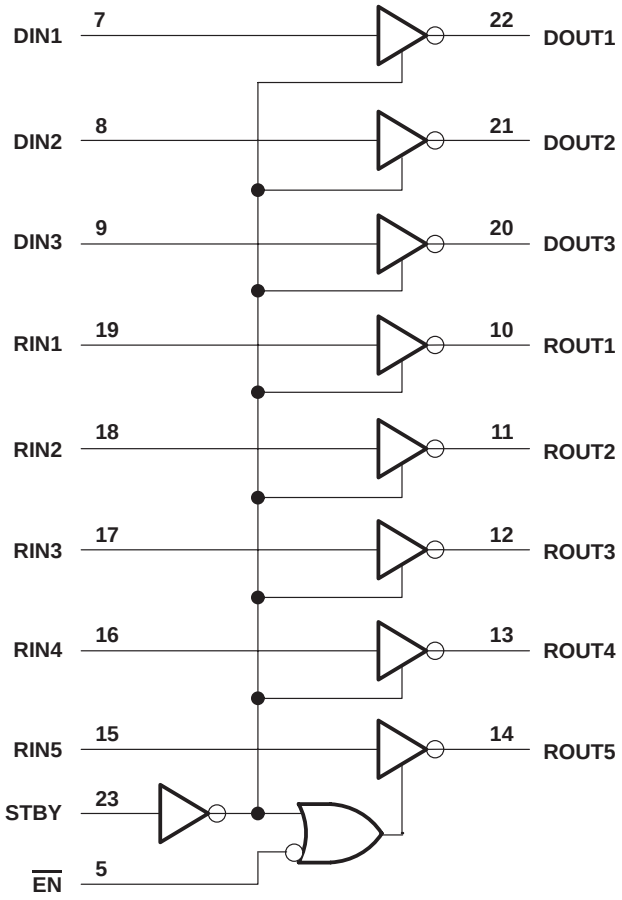
H = high level, L = low level, X = irrelevant, Z = high impedance

EACH RECEIVER

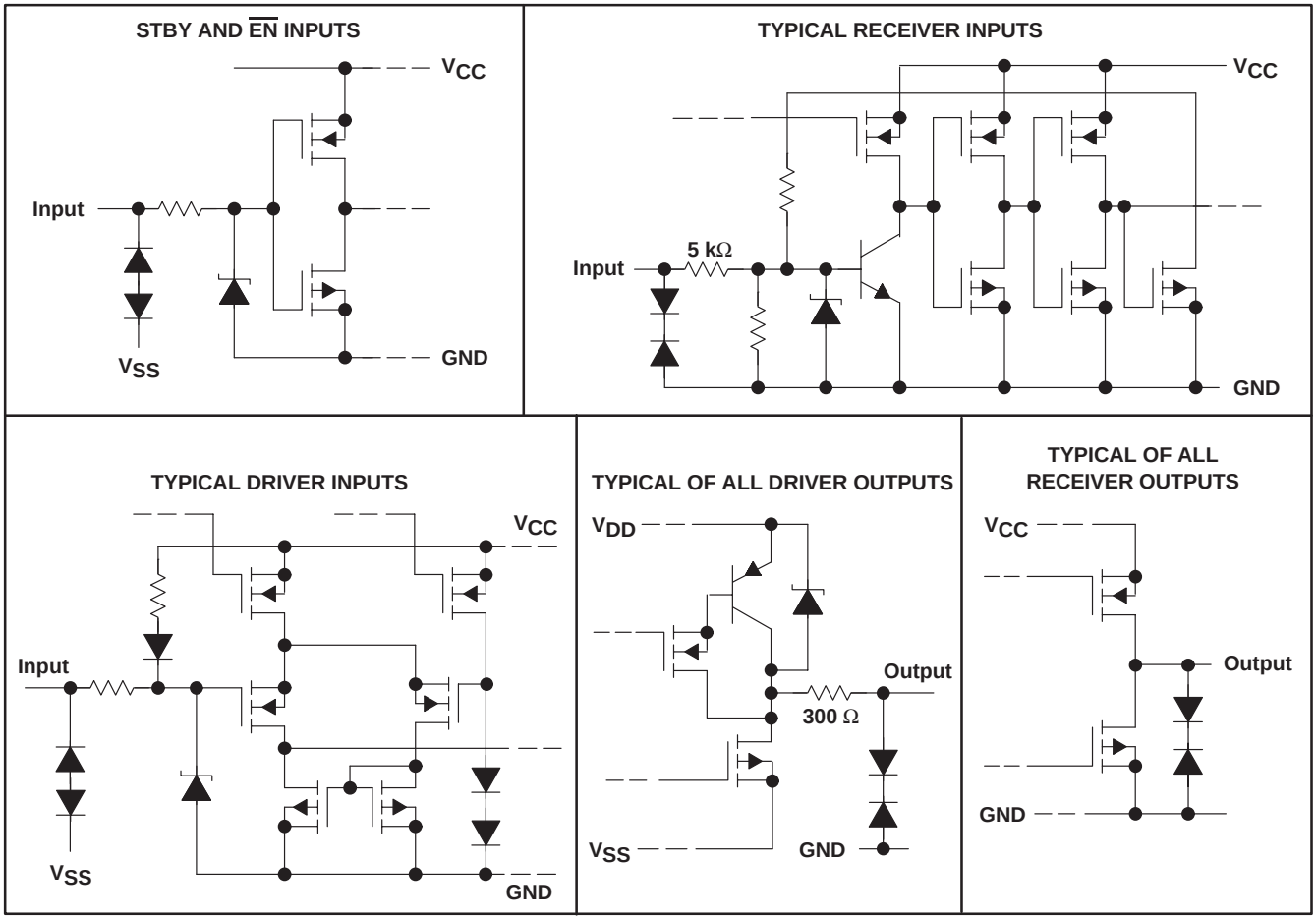
INPUTS				OUTPUTS	
STBY	$\overline{EN}$	RIN5	RIN1–RIN4	ROUT5	ROUT1–ROUT4
H	H	X	X	Z	Z
H	L	H	X	L	Z
H	L	L	X	H	Z
L	X	L	L	H	H
L	X	H	H	L	L

H = high level, L = low level, X = irrelevant, Z = high impedance

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Positive output supply voltage, V_{DD} (see Note 1)	15 V
Negative output supply voltage, V_{SS}	–15 V
Input voltage range, V_I: Driver	–3 V to 7 V
Receiver	–30 V to 30 V
Output voltage range, V_O: Driver	V_{SS} – 0.3 V to V_{DD} + 0.3 V
Receiver	–0.3 V to 7 V
Package thermal impedance, θ_{JA} (see Note 2)	62°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	V
V_{IH}	Driver high-level input voltage	DIN, $\overline{EN}$, STBY	V_{CC} = 3.3 V	2			V
		DIN	V_{CC} = 5 V	2			
		$\overline{EN}$, STBY		2.5			
V_{IL}	Driver low-level input voltage	DIN, $\overline{EN}$, STBY				0.8	V
V_I	Receiver input voltage					±30	V
	External capacitor	3.3-V operation (C1, C2, C3, C4, C5), 5-V operation (C1, C3, C4, C5), See Note 3 and Figures 6 and 7		0.1			µF
T_A	Operating free-air temperature			0		70	°C

NOTE 3: C2 is needed only for 3.3-V operation.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 6 and 7) (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC} = 3.3 V			V_{CC} = 5 V			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{DD}	Positive supply voltage	No load		8	10		7	8.7		V
V_{SS}	Negative supply voltage	No load			–9.5	–7		–8	–6	V
I_I	Input current ($\overline{EN}$, STBY)	See Notes 4 and 5				±2			±2	µA
I_{CC}	Supply current	No load, Inputs open	STBY at GND, $\overline{EN}$ at V_{CC} or GND	8.4	10	18	10	12	20.7	mA
	Supply current (standby mode) (see Note 4)		$\overline{EN}$, STBY at V_{CC}			5			5	µA
	Supply current (wake-up mode) (see Note 5)		$\overline{EN}$ at GND, STBY at V_{CC}			10			10	

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTES: 4. When standby mode is not used, STBY input must be taken low.
5. When wake-up mode is not used, $\overline{EN}$ input must be taken high.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	R_L = 3 kΩ		5.5	7		V
V_{OL}	Low-level output voltage	R_L = 3 kΩ			–6	–5	V
I_{IH}	High-level input current	$V_I = V_{CC}$				1	µA
I_{IL}	Low-level input current	V_I at GND				–10	µA
I_{OS}	Short-circuit output current (see Note 6)	V_{CC} = 3.6 V,	V_O = 0 V		±15	±40	mA
		V_{CC} = 5.5 V,	V_O = 0 V				
r_o	Output resistance	$V_{CC} = V_{DD} = V_{SS}$ = 0 V,	V_O = ±2 V	300	500		Ω

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTE 6: Short-circuit durations should be controlled to prevent exceeding the device absolute maximum power dissipation ratings, and not more than one output should be shorted at a time.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 50 pF, R_L = 3 kΩ to 7 kΩ, See Figure 1	V_{CC} = 3.3 V	100	500	850	ns
			V_{CC} = 5 V	100	500	850	
t_{PHL}	Propagation delay time, high- to low-level output		V_{CC} = 3.3 V	100	500	850	ns
			V_{CC} = 5 V	100	500	850	
t_{PZH}	Output enable time to high level	C_L = 50 pF, See Figure 2	R_L = 3 kΩ to 7 kΩ,		1	5	ms
t_{PZL}	Output enable time to low level				3	7	ms
t_{PHZ}	Output disable time from high level	C_L = 50 pF, R_L = 3 kΩ to 7 kΩ, See Figure 2	V_{CC} = 3.3 V		0.9	3	µs
			V_{CC} = 5 V		0.6	3	
t_{PLZ}	Output disable time from low level		V_{CC} = 3.3 V		0.5	3	µs
			V_{CC} = 5 V		0.3	3	
SR	Slew rate	C_L = 50 pF, See Figure 1	R_L = 3 kΩ to 7 kΩ,	4		30	V/µs
SR(tr)	Slew rate, transition region	C_L = 2500 pF, See Figure 3	R_L = 3 kΩ to 7 kΩ,	3		30	V/µs

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

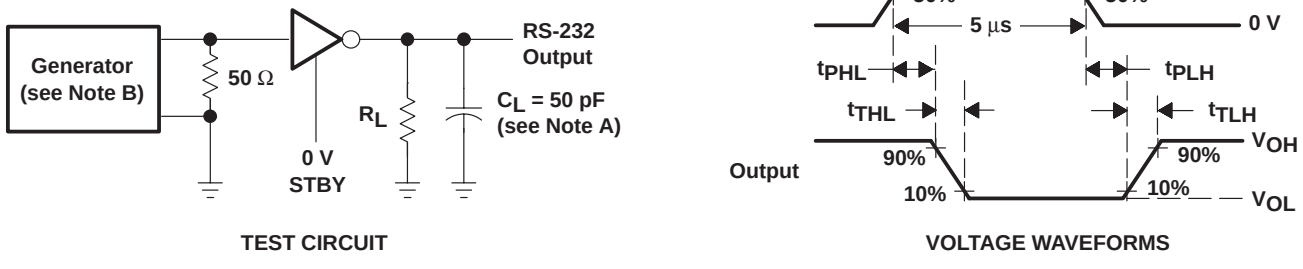
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	V_{CC} = 3.3 V	2.4	3		V
			V_{CC} = 5 V	3.5	5		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.2	0.4	V
V_{IT+}	Positive-going input threshold voltage				2.2	2.6	V
$V_{IT–}$	Negative-going input threshold voltage			0.6	1		V
V_{hys}	Input hysteresis ($V_{IT+} – V_{IT–}$)			0.5	1.2	1.8	V
r_i	Input resistance	V_I = ±3 V to ±25 V		3	5	7	kΩ

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF, R_L = 3 kΩ to GND

PARAMETER		TEST CONDITIONS	V_{CC} = 3.3 V			V_{CC} = 5 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 4	10	70	200	10	70	200	ns
t_{PHL}	Propagation delay time, high- to low-level output		10	60	200	10	55	200	ns
t_{PLH}	Propagation delay time, low- to high-level output (wake-up mode)			40	200		40	200	µs
t_{PHL}	Propagation delay time, high- to low-level output (wake-up mode)			90	500		70	500	ns
t_{PZH}	Output enable time to high level	See Figure 5		3	10		1.2	10	µs
t_{PZL}	Output enable time to low level			100	250		60	250	ns
t_{PHZ}	Output disable time from high level		100	200	600	100	150	600	ns
t_{PLZ}	Output disable time from low level			130	250		60	250	ns

PARAMETER MEASUREMENT INFORMATION

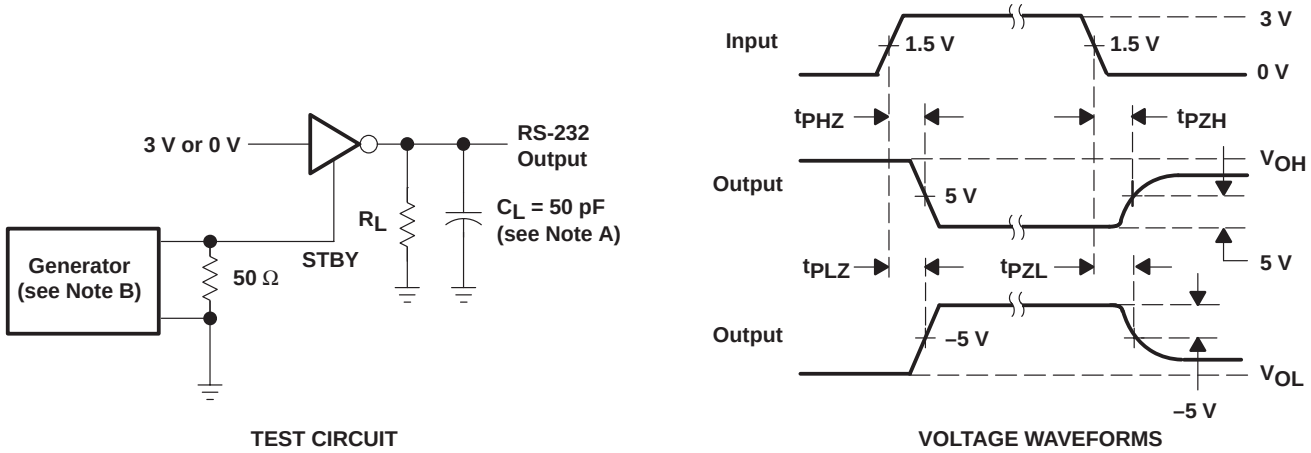


TEST CIRCUIT VOLTAGE WAVEFORMS

$$SR = \frac{0.8\ V(V_{OH} - V_{OL})}{t_{TLH}} \text{ or } \frac{0.8\ V(V_{OL} - V_{OH})}{t_{THL}}$$

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 1. Driver Propagation Delay Times and Slew Rate (5-μs Input)

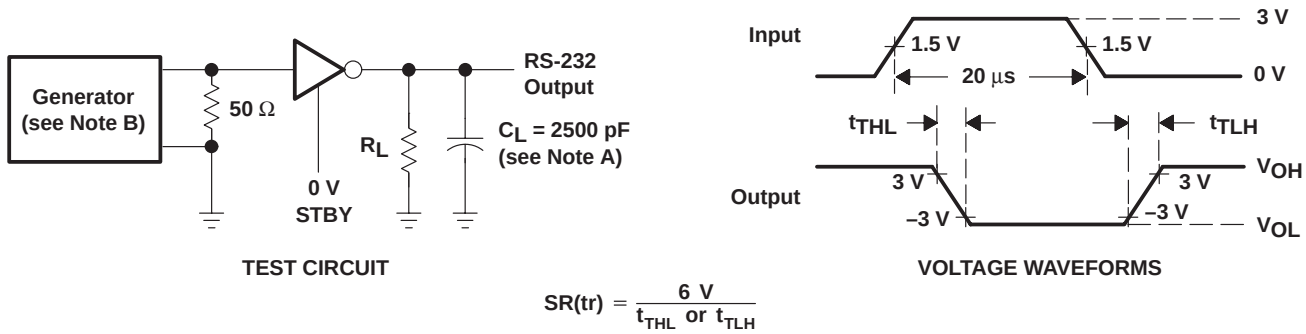


TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 2. Driver Enable and Disable Test Times

PARAMETER MEASUREMENT INFORMATION



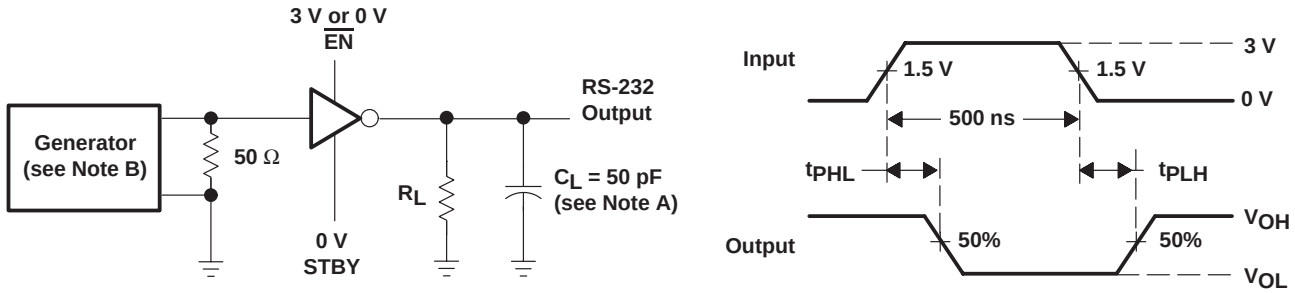
TEST CIRCUIT

VOLTAGE WAVEFORMS

$$SR(tr) = \frac{6\ V}{t_{THL}\ or\ t_{TLH}}$$

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 3. Driver Transition Times and Slew Rate (20-μs Input)



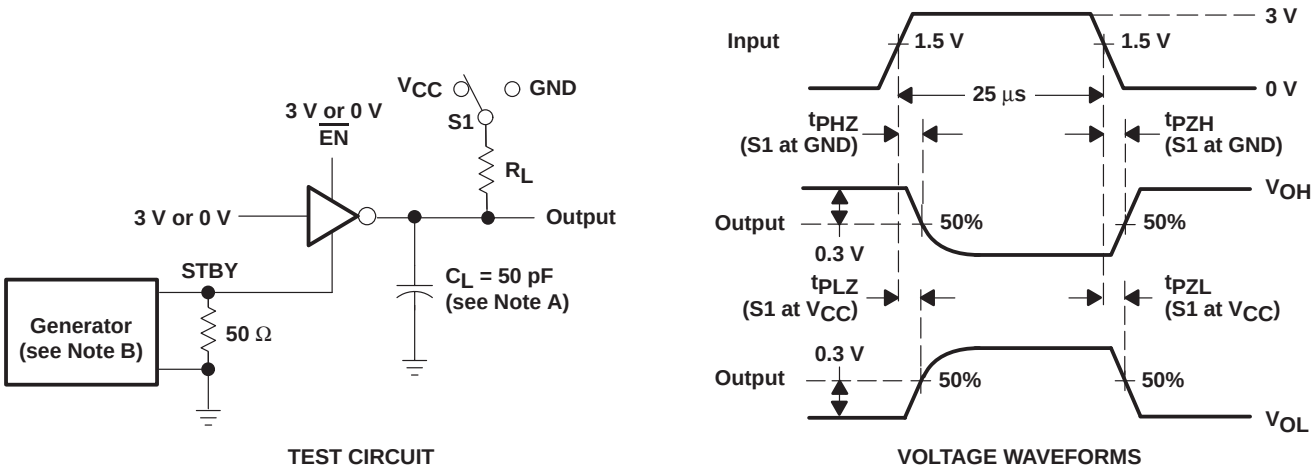
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 4. Receiver Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION

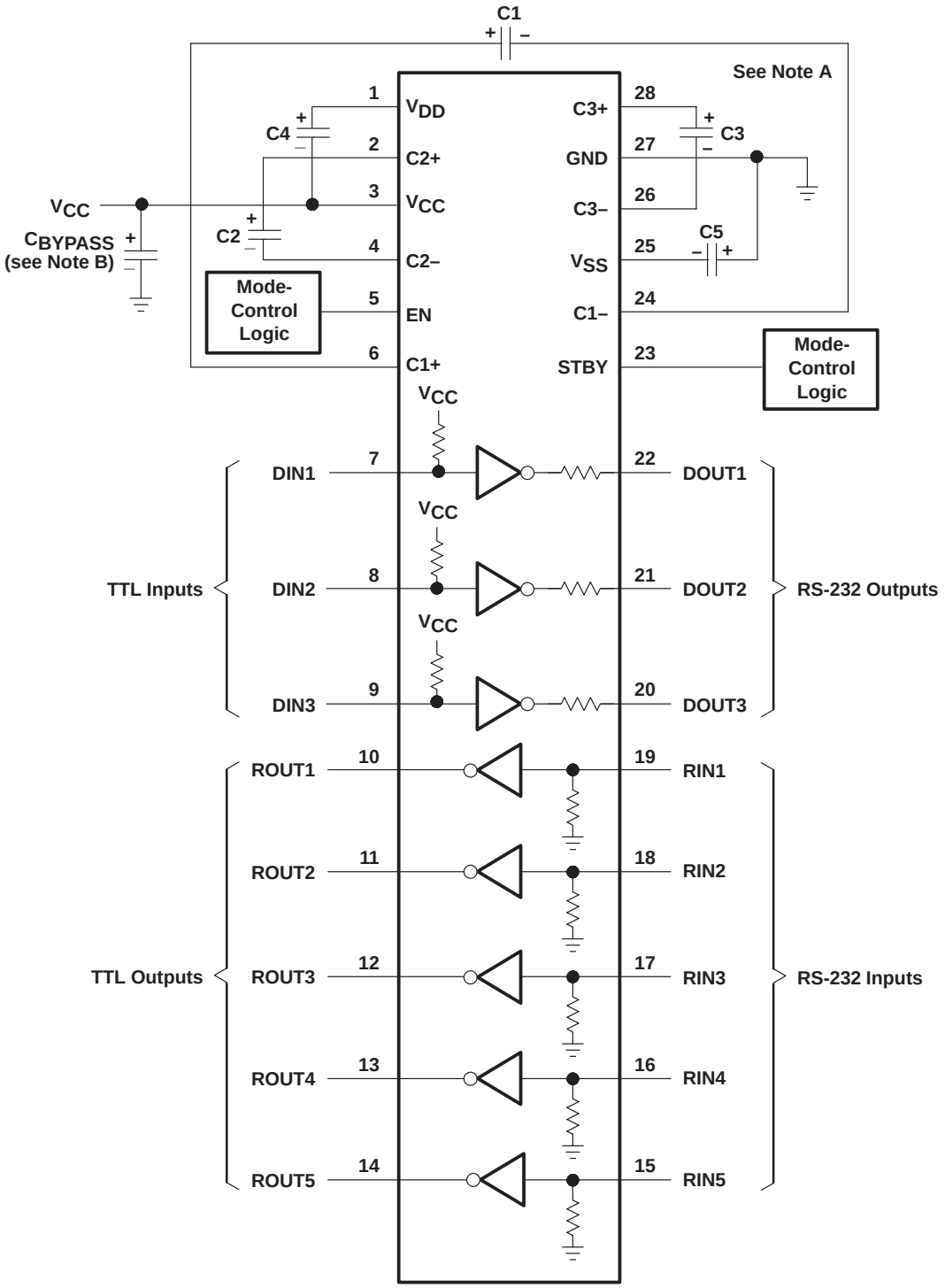


TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 5. Receiver Enable and Disable Times

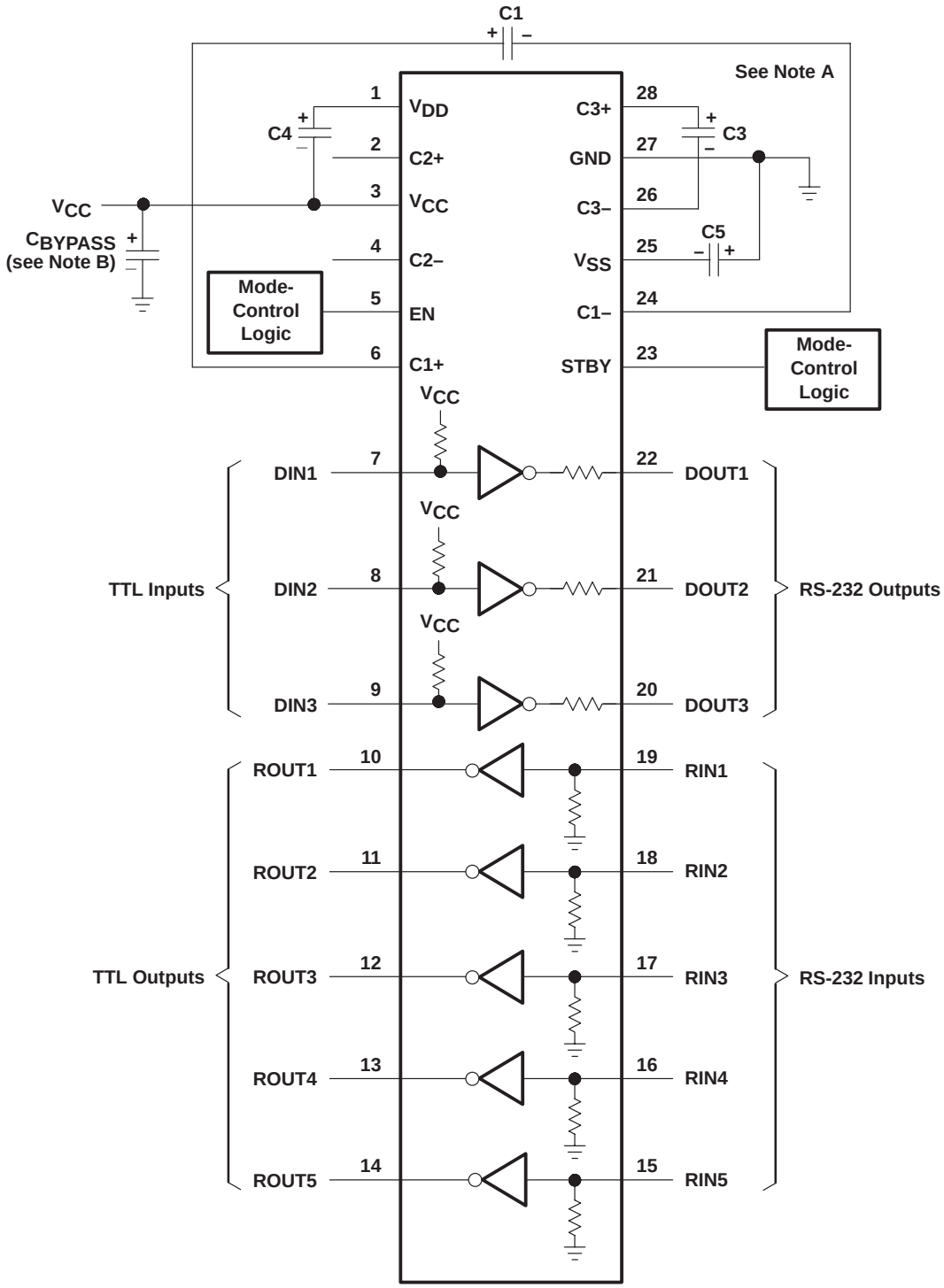
APPLICATION INFORMATION



NOTES: A. C1 = C2 = C3 = C4 = C5 = C_{BYPASS} = 0.1 μF
B. C_{BYPASS} is used as a decoupling capacitor.

Figure 6. Typical 3.3-V Operating Circuit

APPLICATION INFORMATION



NOTES: A. C2 is not used. C1 = C3 = C4 = C5 = C_{BYPASS} = 0.1 µF
B. C_{BYPASS} is used as a decoupling capacitor.

Figure 7. Typical 5-V Operating Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN75LV4737ADB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LV4737ADBE4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LV4737ADBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LV4737ADBLE	OBSOLETE	SSOP	DB	28		TBD	Call TI	Call TI
SN75LV4737ADBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LV4737ADBRE4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LV4737ADBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

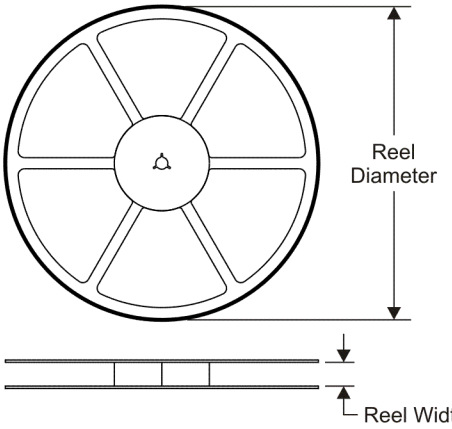
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

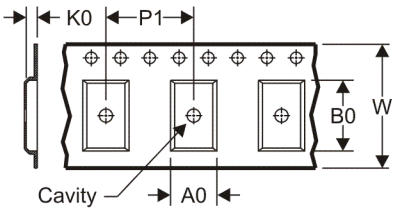
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

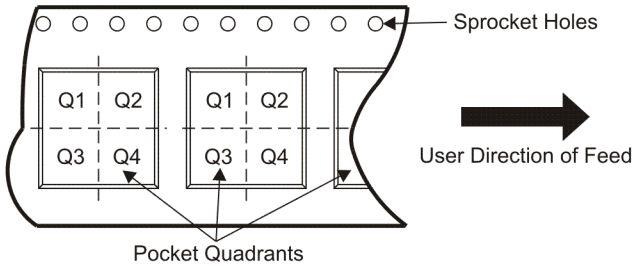


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

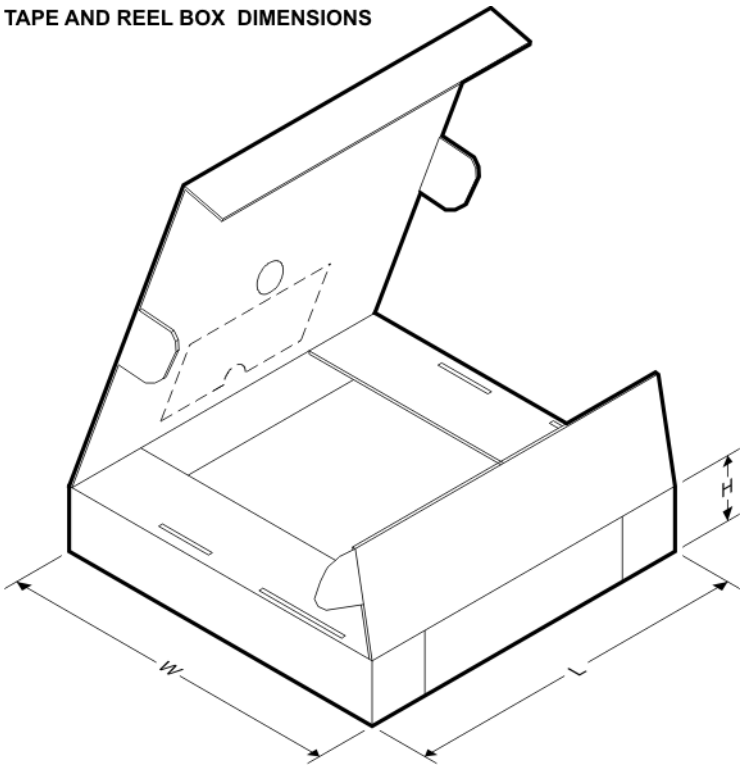
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LV4737ADBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



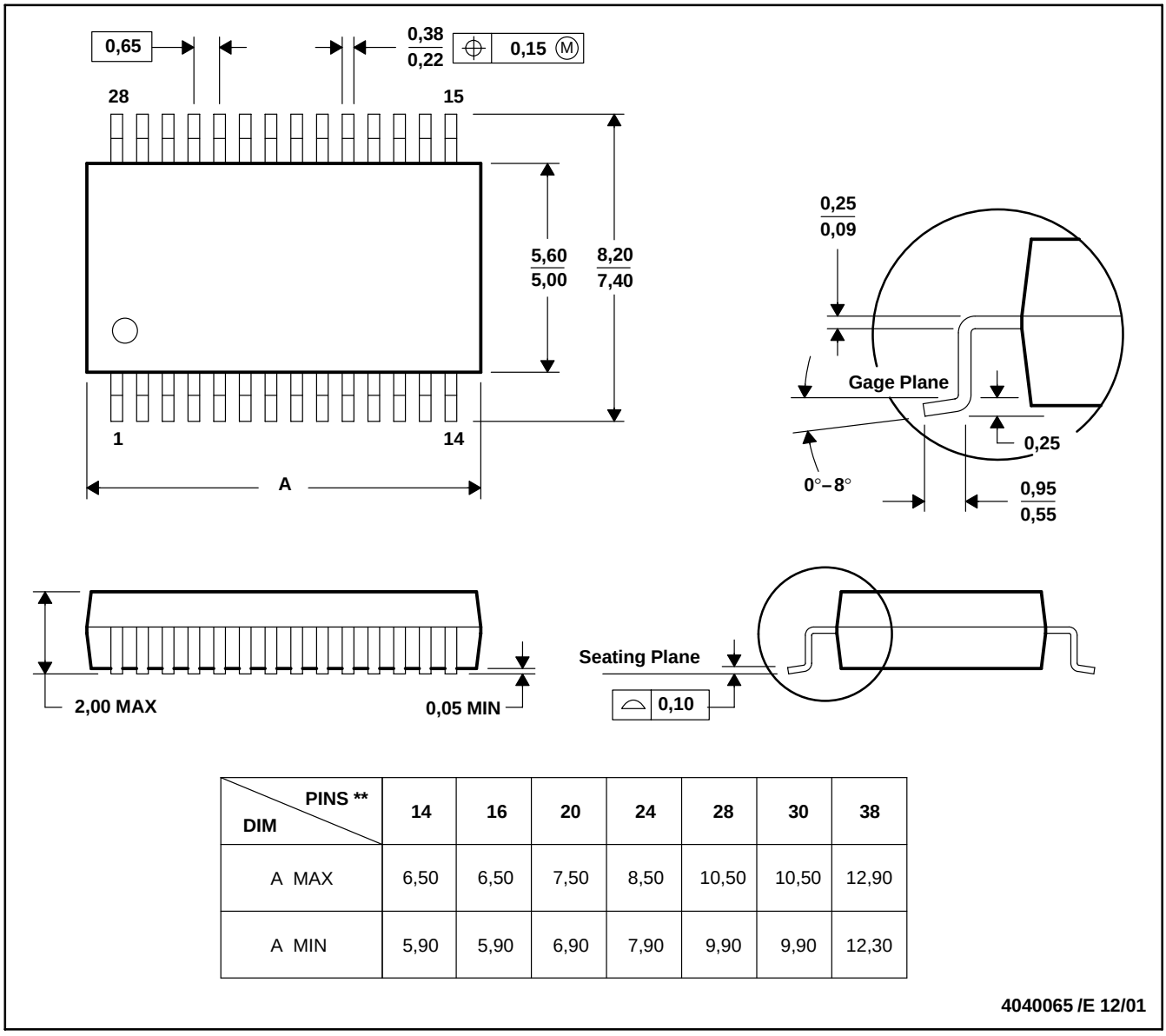
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LV4737ADBR	SSOP	DB	28	2000	346.0	346.0	33.0

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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