

High voltage fast-switching NPN power transistor

Features

- High voltage capability
- Minimum lot-to-lot spread for reliable operation
- Very high switching speed

Applications

- Electronic ballast for fluorescent lighting
- Flyback and forward single transistor low power converters

Description

The device is manufactured using high voltage multi-epitaxial planar technology for high switching speeds and medium voltage capability.

It uses a cellular emitter structure with planar edge termination to enhance switching speeds while maintaining the wide RBSOA.

The device is designed for use in lighting applications and low cost switch-mode power supplies.

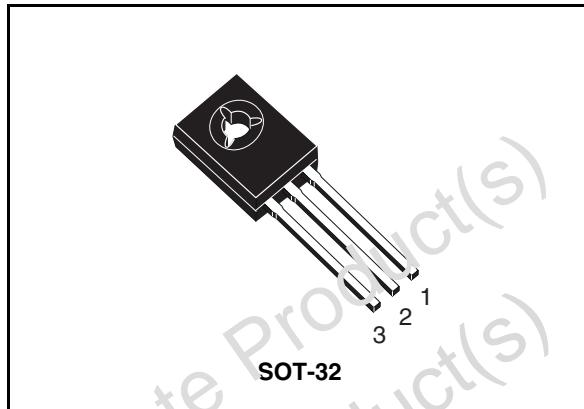


Figure 1. Internal schematic diagram

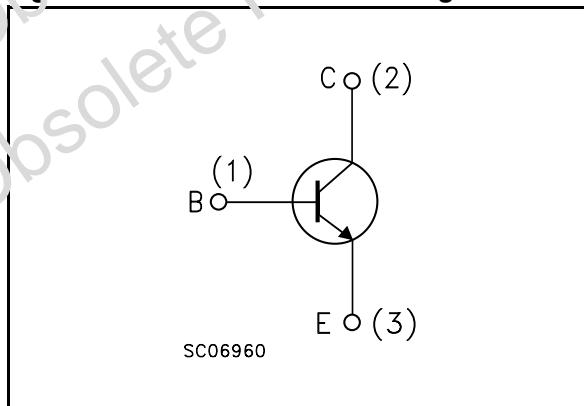


Table 1. Device summary

| Order code | Marking | Package | Packaging |
|------------|---------|---------|-----------|
| BULT118 | BULT118 | SOT-32 | Tube |

1 Electrical ratings

Table 2. Absolute maximum rating

| Symbol | Parameter | Value | Unit |
|-----------|--|------------|------|
| V_{CES} | Collector-emitter voltage ($V_{BE} = 0$) | 700 | V |
| V_{CEO} | Collector-emitter voltage ($I_B = 0$) | 400 | V |
| V_{EBO} | Emitter-base voltage ($I_C = 0$) | 9 | V |
| I_C | Collector current | 2 | A |
| I_{CM} | Collector peak current ($t_P < 5$ ms) | 4 | A |
| I_B | Base current | 1 | A |
| I_{BM} | Base peak current ($t_P < 5$ ms) | 2 | A |
| P_{tot} | Total dissipation at $T_c = 25$ °C | 45 | W |
| T_{stg} | Storage temperature | -65 to 150 | °C |
| T_J | Max. operating junction temperature | 150 | °C |

2 Electrical characteristics

($T_{case} = 25^\circ\text{C}$ unless otherwise specified)

Table 3. Electrical characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------------|--|--|---------------|--------------------|-------------------|---|
| I_{CES} | Collector cut-off current ($V_{BE} = 0$) | $V_{CE} = 700 \text{ V}$ $V_{CE} = 700 \text{ V} \quad T_C = 125^\circ\text{C}$ | | | 100 500 | μA μA |
| I_{CEO} | Collector-emitter leakage current | $V_{CE} = 400 \text{ V}$ | | | 250 | μA |
| V_{EBO} | Emitter-base voltage | $I_E = 10 \text{ mA}$ | 9 | | | V |
| $V_{CEO(sus)}^{(1)}$ | Collector-emitter sustaining voltage ($I_B = 0$) | $I_C = 10 \text{ mA}$ | 400 | | | V |
| $V_{CE(sat)}^{(1)}$ | Collector-emitter saturation voltage | $I_C = 0.5 \text{ A} \quad I_B = 0.1 \text{ A}$ $I_C = 1 \text{ A} \quad I_B = 0.2 \text{ A}$ $I_C = 2 \text{ A} \quad I_B = 0.4 \text{ A}$ | | | 0.5 1 1.5 | V |
| $V_{BE(sat)}^{(1)}$ | Base-emitter saturation voltage | $I_C = 0.5 \text{ A} \quad I_B = 0.1 \text{ A}$ $I_C = 1 \text{ A} \quad I_B = 0.2 \text{ A}$ $I_C = 2 \text{ A} \quad I_B = 0.4 \text{ A}$ | | | 1 1.2 1.3 | V |
| $h_{FE}^{(1)}$ | DC current gain | $I_C = 10 \text{ mA} \quad V_{CE} = 5 \text{ V}$ $I_C = 0.5 \text{ A} \quad V_{CE} = 5 \text{ V}$ $I_C = 2 \text{ A} \quad V_{CE} = 5 \text{ V}$ | 10 10 8 | | 50 | |
| t_s t_r t_f | Resistive load Rise time Storage time Fall time | $I_C = 1 \text{ A} \quad V_{CC} = 125 \text{ V}$ $I_{B1} = -I_{B2} = 0.2 \text{ A}$ | | 0.4 3.2 0.25 | 0.7 4.5 0.4 | μs μs μs |
| t_s t_f | Inductive load Storage time Fall time | $I_C = 1 \text{ A} \quad I_{B1} = 0.2 \text{ A}$ $V_{BE(off)} = -5 \text{ V} \quad L = 50 \text{ mH}$ $V_{Clamp} = 300 \text{ V}$ | | 0.8 0.16 | | μs μs |

1. Pulsed duration = 300 μs , duty cycle $\leq 1.5\%$

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

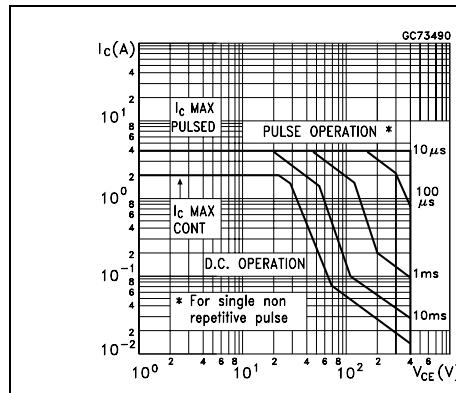


Figure 3. Derating curve

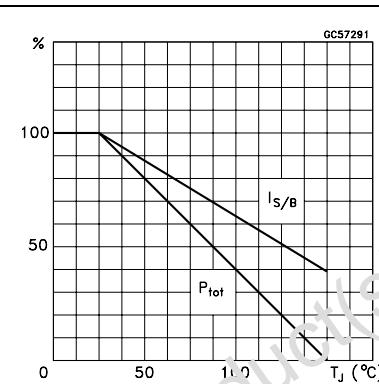


Figure 4. DC current gain

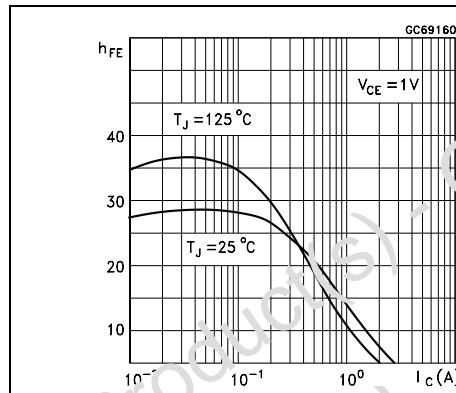


Figure 5. DC current gain

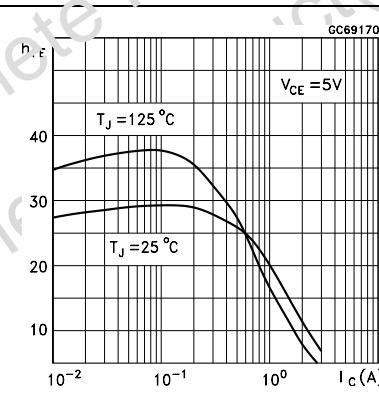


Figure 6. Collector-emitter saturation voltage

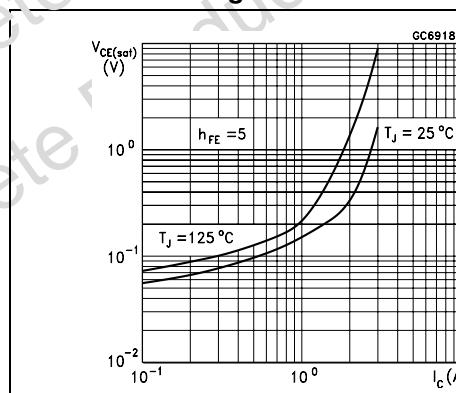


Figure 7. Base-emitter saturation voltage

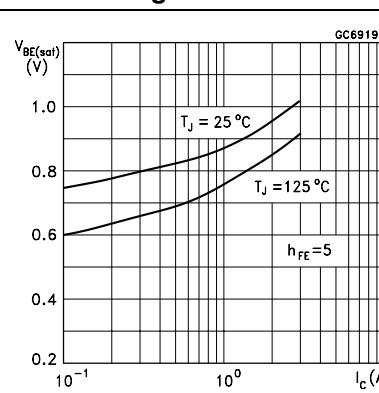


Figure 8. Inductive load fall time

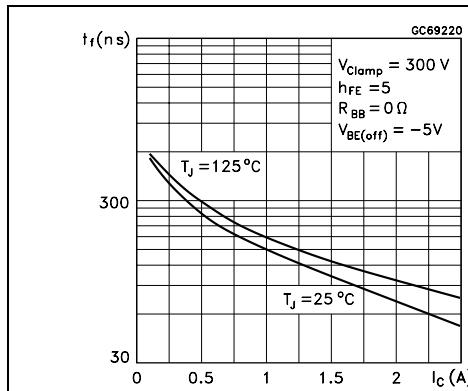


Figure 9. Inductive load storage time

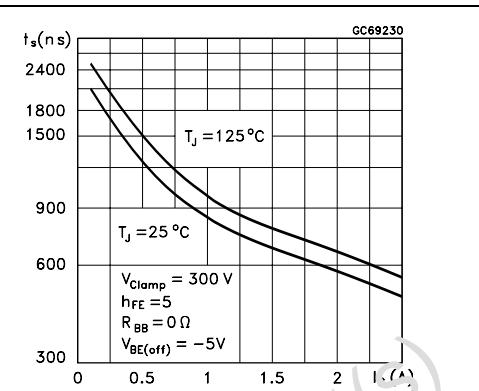


Figure 10. Resistive load fall time

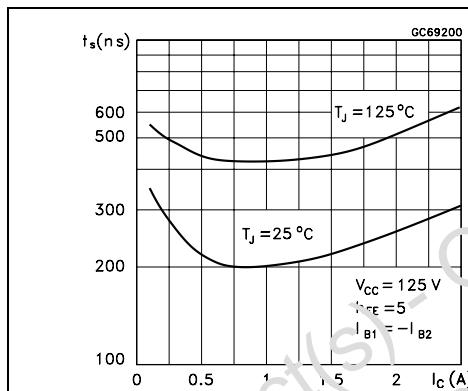


Figure 11. Resistive load storage time

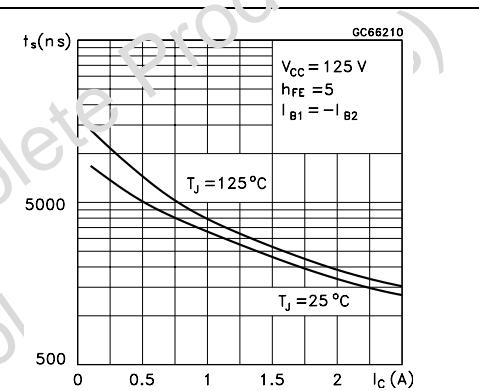
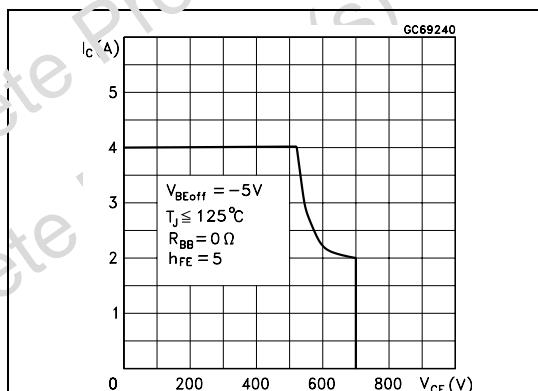


Figure 12. Reverse biased SOA



2.2 Test circuits

Figure 13. Resistive load switching test circuit

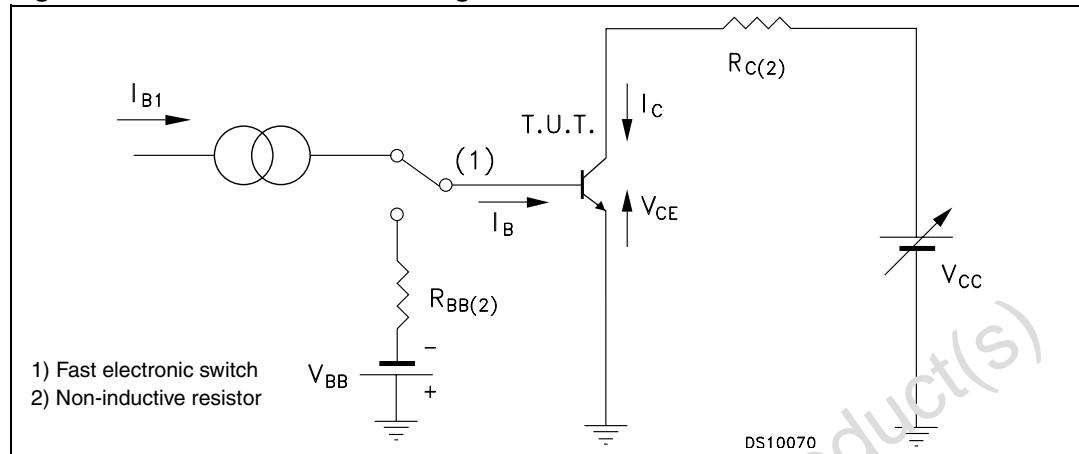
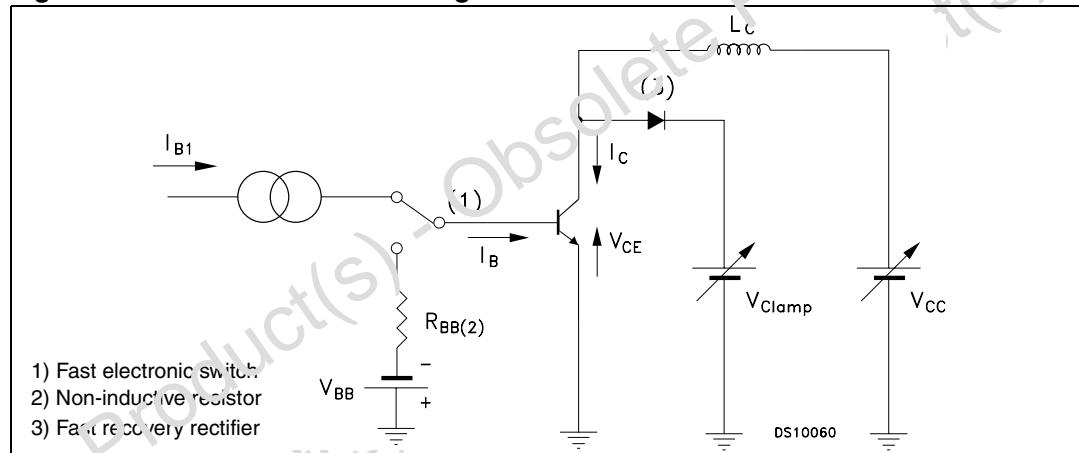


Figure 14. Inductive load switching test circuit

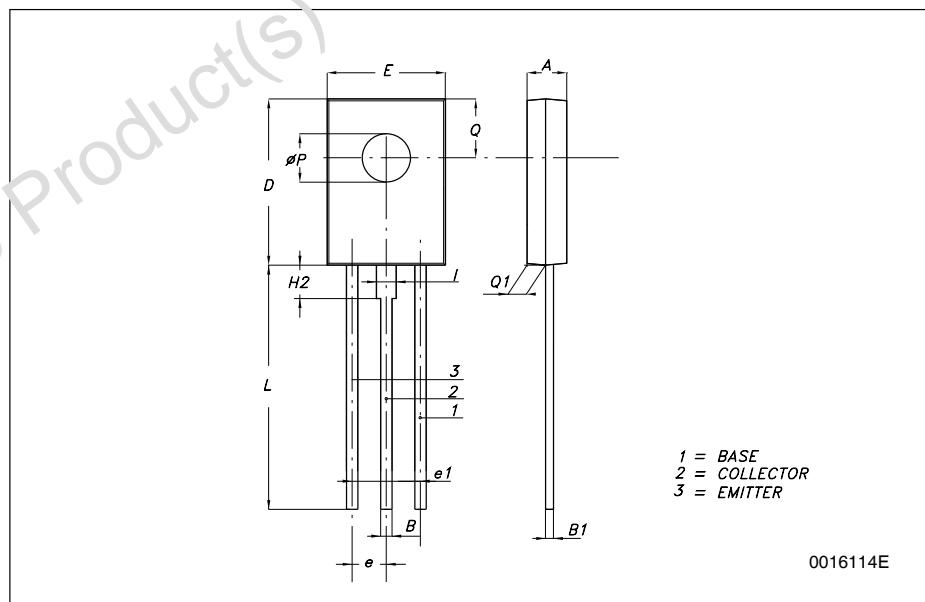


3 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

SOT-32 (TO-126) MECHANICAL DATA

| DIM. | mm. | | |
|------|------|------|-------|
| | MIN. | TYP | MAX. |
| A | 2.4 | | 2.9 |
| B | 0.64 | | 0.88 |
| B1 | 0.39 | | 0.63 |
| D | 10.5 | | 11.05 |
| E | 7.4 | | 7.8 |
| e | 2.04 | 2.29 | 2.4 |
| e1 | 4.07 | 4.58 | 5.08 |
| L | 15.3 | | 16 |
| P | 2.9 | | 3.2 |
| Q | | 3.8 | |
| Q1 | 1 | | 1.52 |
| H2 | | 2.15 | |
| I | | 1.27 | |



4 Revision history

Table 4. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 29-Sep-2003 | 1 | Initial release. |
| 10-Jul-2008 | 2 | Updated: $V_{CEO(sus)}$ condition in Table 3 on page 3 , SOT-32 mechanical data, cover page |

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