0.25 Ω Low-Voltage Dual SPDT Analog Switch

DESCRIPTION

The DG3535, DG3536 is a sub 1 Ω (0.25 Ω at 2.7 V) dual SPDT analog switches designed for low voltage applications.

The DG3535, DG3536 has on-resistance matching (less than 0.05 Ω at 2.7 V) and flatness (less than 0.2 Ω at 2.7 V) that are guaranteed over the entire voltage range. Additionally, low logic thresholds makes the DG3535, DG3536 an ideal interface to low voltage DSP control signals.

The DG3535, DG3536 has fast switching speed with break-before-make guaranteed. In the On condition, all switching elements conduct equally in both directions. Off-isolation and crosstalk is - 69 dB at 100 kHz.

The DG3535, DG3536 is built on Vishay Siliconix's high-density low voltage CMOS process. An eptiaxial layer is built in to prevent latchup. The DG3535, DG3536 contains the additional benefit of 2000 V ESD protection.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For MICRO FOOT analog switching products manufactured with tin/silver/copper (SnAgCu) device terminations, the lead (Pb)-free "-E1" suffix is being used as a designator.

FEATURES

- Low voltage operation
- Low on-resistance - R_{ON}: 0.25 Ω at 2.7 V
- - 69 dB OIRR at 2.7 V, 100 kHz
- MICRO FOOT® package
- ESD protection > 2000 V

Pb-free
RoHS
COMPLIANT

BENEFITS

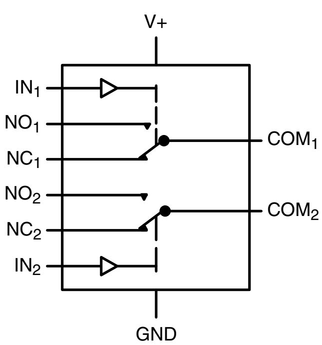
- Reduced power consumption
- High accuracy
- Reduce board space
- 1.6 V logic compatible
- High bandwidth

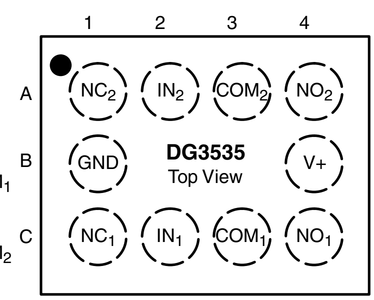
APPLICATIONS

- Cellular phones
- Speaker headset switching
- Audio and video signal routing
- PCMCIA cards
- Battery operated systems
- Relay replacement

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG3535, DG3536
MICRO FOOT 10-Bump

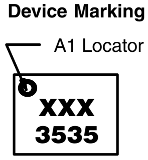




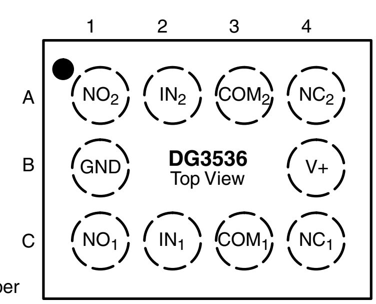
TRUTH TABLE

Logic	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON

Device Marking



3535 = Example Base Part Number
xxx = Data/Lot Traceability Code



ORDERING INFORMATION

Temp. Range	Package	Part Number
- 40 °C to 85 °C	MICRO FOOT: 10 Bump (4 x 3, 0.5 mm Pitch, 238 µm Bump Height)	DG3535DB-T5-E1 DG3535DB-T1-E1 DG3536DB-T5-E1

ABSOLUTE MAXIMUM RATINGS			
Parameter		**Limit**	**Unit**
Reference V+ to GND		- 0.3 to + 6	V
IN, COM, NC, NO[a]		- 0.3 to (V+ + 0.3 V)	
Continuous Current (NO, NC, COM)		± 300	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 500	
Storage Temperature	(D Suffix)	- 65 to 150	°C
Package Solder Reflow Conditions[b]	IR/Convection	250	
ESD per Method 3015.7		> 2	kV
Power Dissipation (Packages)[c]	MICRO FOOT: 10 Bump (4 x 3 mm)[d]	457	mW

Notes:
a Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b Refer to IPC/JEDEC (J-STD-020B)
c All bumps welded or soldered to PC board.
d Derate 5.7 mW/°C above 70 °C.

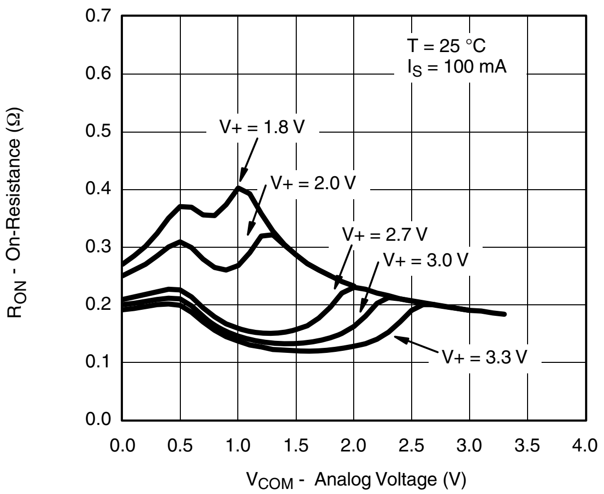
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 3.0 V)							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** $V+ = 3$ V, ± 10 %, $V_{IN} = 0.5$ V or 1.4 V[e]	**Temp.**[a]	**Limits - 40 to 85 °C Min.**[b]	**Typ.**[c]	**Max.**[b]	**Unit**
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance[d]	R_{ON}	$V+ = 2.7$ V, $V_{COM} = 0.6/1.5$ V, I_{NO}, $I_{NC} = 100$ mA	Room Full		0.25	0.4 0.5	Ω
R_{ON} Flatness[d]	R_{ON} Flatness		Room			0.15	
On-Resistance Match Between Channels[d]	$\Delta R_{DS(on)}$		Room			0.05	
Switch Off Leakage Current	$I_{NO(off)}$, $I_{NC(off)}$	$V+ = 3.3$ V, V_{NO}, $V_{NC} = 0.3$ V/3 V, $V_{COM} = 3$ V/0.3 V	Room Full	- 2 - 20		2 20	nA
	$I_{COM(off)}$		Room Full	- 2 - 20		2 20	
Channel-On Leakage Current	$I_{COM(on)}$	$V+ = 3.3$ V, V_{NO}, $V_{NC} = V_{COM} = 0.3$ V/3 V	Room Full	- 2 - 20		2 20	
Digital Control							
Input High Voltage[d]	V_{INH}		Full	1.4			V
Input Low Voltage	V_{INL}		Full			0.5	
Input Capacitance	C_{in}		Full		10		pF
Input Current	I_{INL} or I_{INH}	$V_{IN} = 0$ or V+	Full	1		1	µA

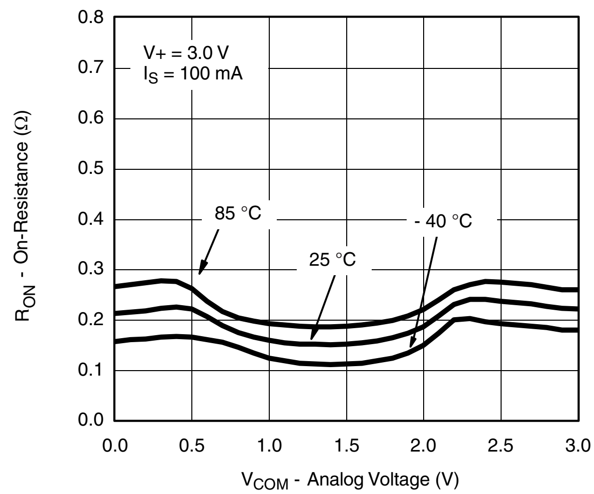
SPECIFICATIONS (V+ = 3.0 V)							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 3 V, ± 10 %, V_{IN} = 0.5 V or 1.4 V[e]	**Temp.**[a]	**Limits** - 40 °C to 85 °C **Min.**[b]	**Typ.**[c]	**Max.**[b]	**Unit**
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 2.0 V, R_L = 50 Ω, C_L = 35 pF	Room Full		52	82 90	ns
Turn-Off Time	t_{OFF}		Room Full		43	73 78	
Break-Before-Make Time	t_d		Room	1	6		
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 1.5 V, R_{GEN} = 0 Ω	Full		21		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz	Room		- 69		dB
Crosstalk[d]	X_{TALK}		Room		- 69		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		145		pF
	$C_{NC(off)}$		Room		145		
Channel-On Capacitance[d]	$C_{NO(on)}$		Room		406		
	$C_{NC(on)}$		Room		406		
Power Supply							
Power Supply Current	I+	V_{IN} = 0 or V+	Room Full		0.001	1.0 1.0	µA

Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.

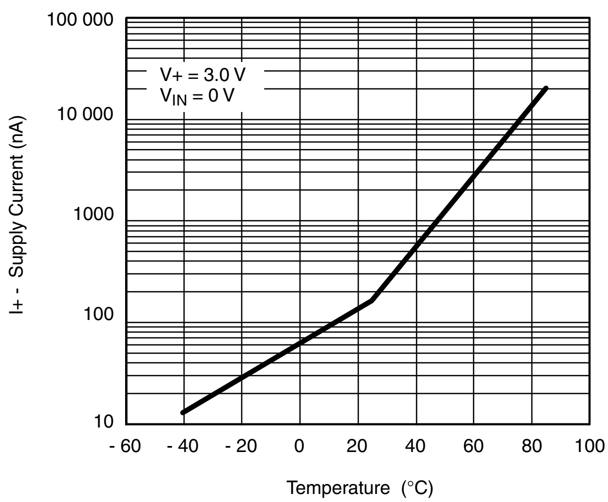
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



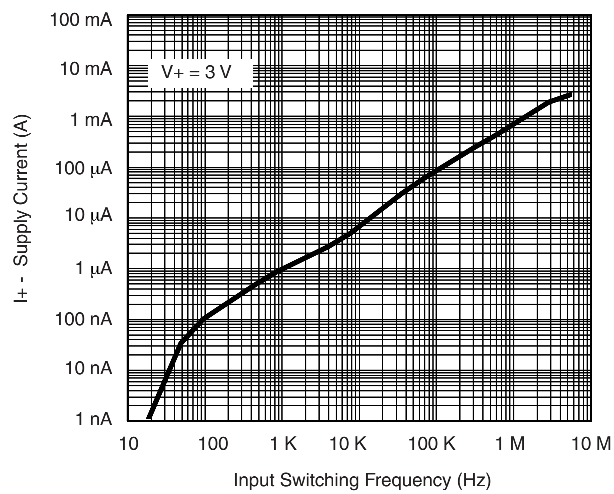
R_{ON} vs. V_{COM} and Supply Voltage



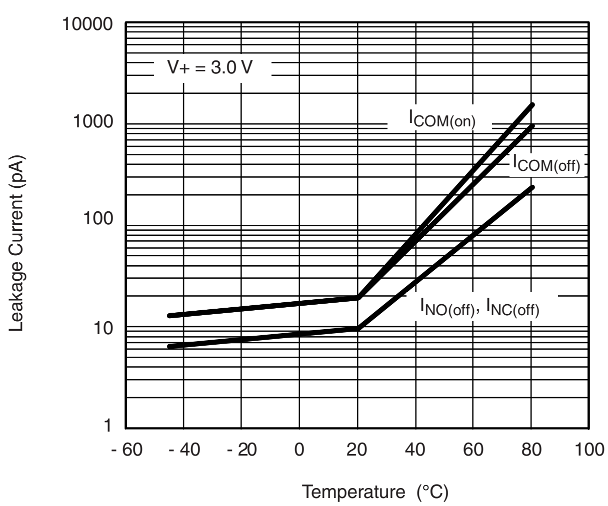
R_{ON} vs. Analog Voltage and Temperature (NC1)



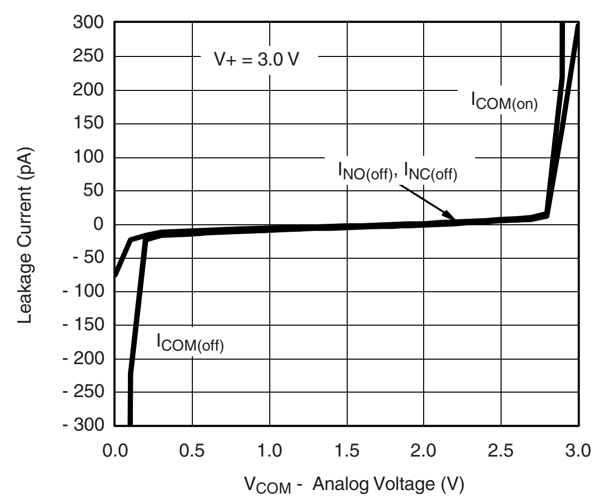
Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency

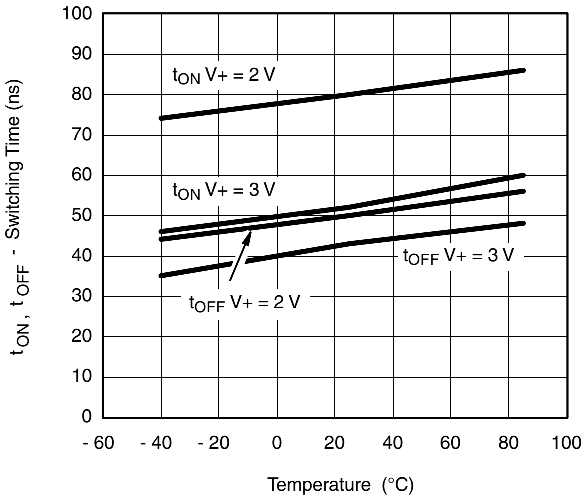


Leakage Current vs. Temperature

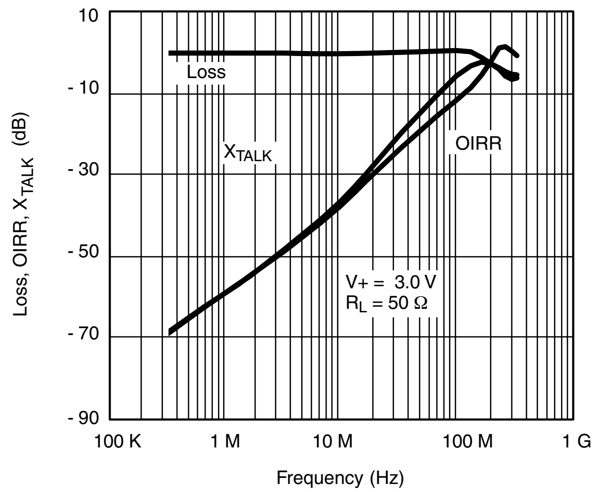


Leakage vs. Analog Voltage

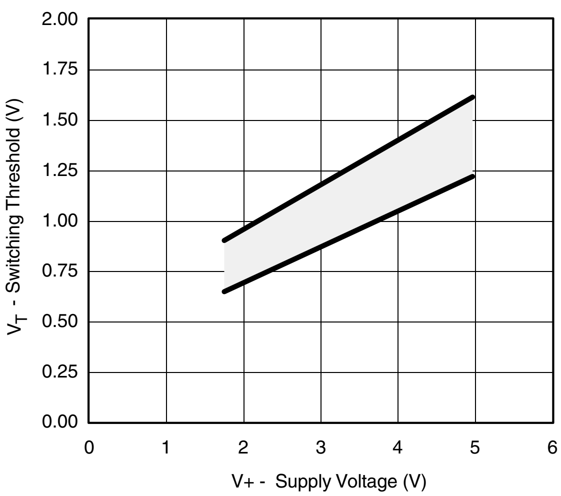
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



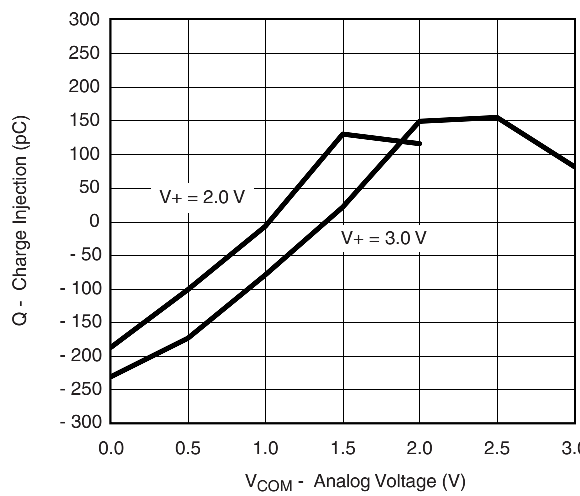
Switching Time vs. Temperature



Insertion Loss, Off-Isolation Crosstalk vs. Frequency

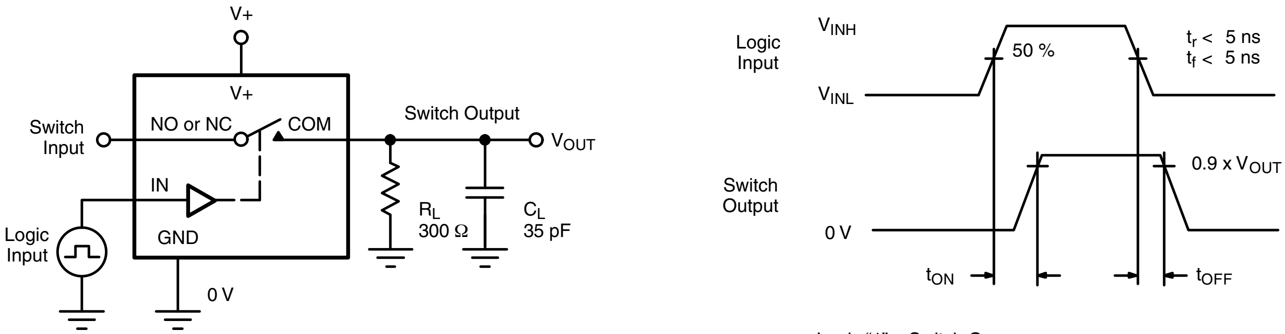


Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage

TEST CIRCUITS

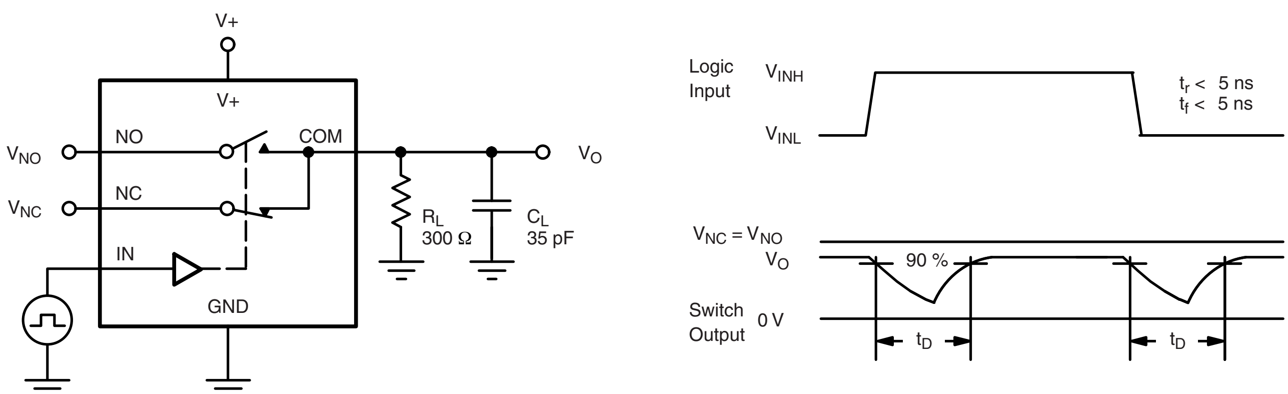


C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$

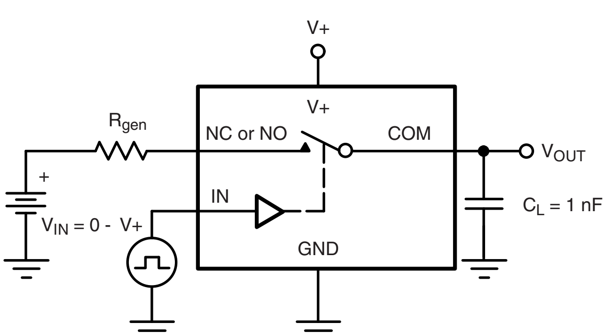
Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

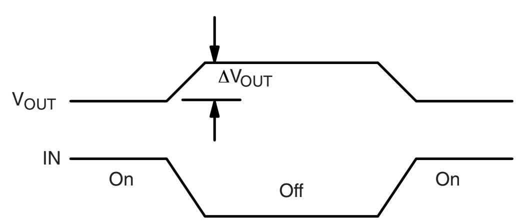
Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

Figure 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

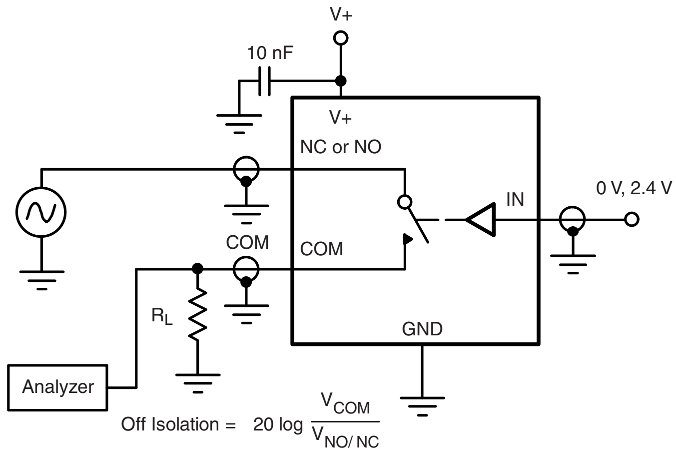


Figure 4. Off-Isolation

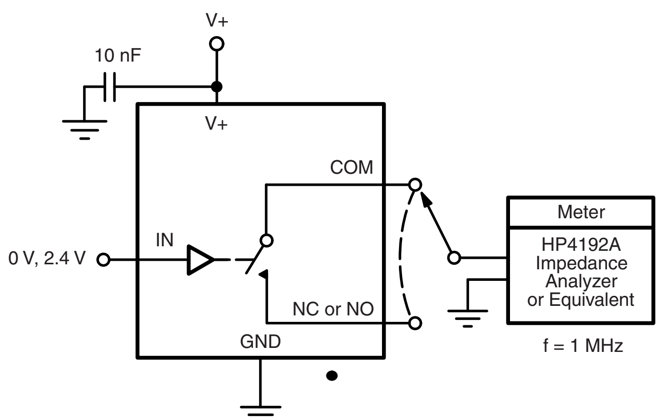
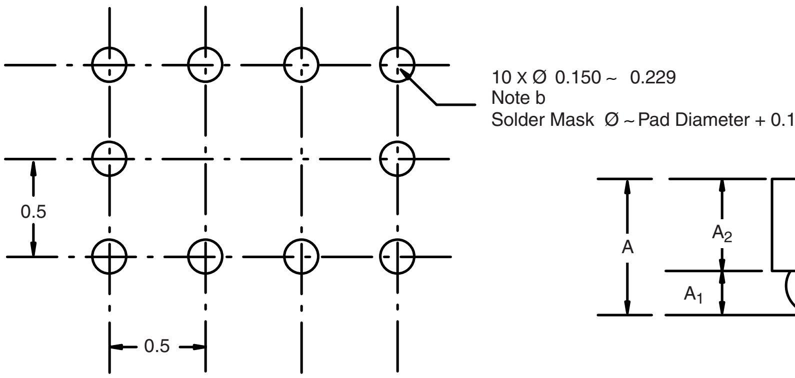


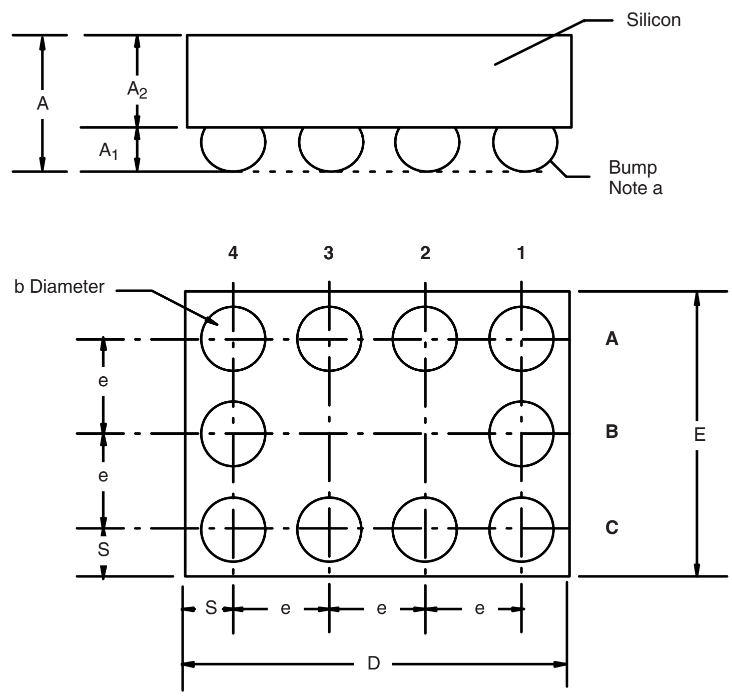
Figure 5. Channel Off/On Capacitance

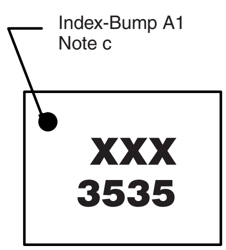
PACKAGE OUTLINE

MICRO FOOT: 10 BUMP (4 x 3, 0.5 mm PITCH, 0.238 mm BUMP HEIGHT)



Recommended Land Pattern





Top Side (Die Back)

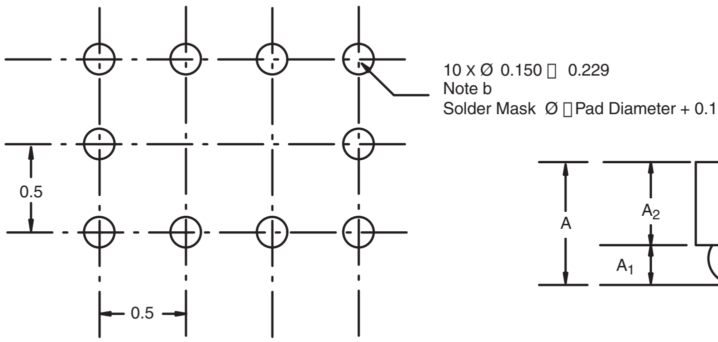
Notes (Unless Otherwise Specified):
a. Bump is Lead Free Sn/Ag/Cu.
b. Non-solder mask defined copper landing pad.
c. Laser Mark on silicon die back; back-lapped, no coating. Shown is not actual marking; sample only.

Dim.	Millimeters[a]		Inches	
	Min.	**Max.**	**Min.**	**Max.**
A	0.688	0.753	0.0271	0.0296
A_1	0.218	0.258	0.0086	0.0102
A_2	0.470	0.495	0.0185	0.0195
b	0.306	0.346	0.0120	0.0136
D	1.980	2.020	0.0780	0.0795
E	1.480	1.520	0.0583	0.0598
e	0.5 BASIC		0.0197 BASIC	
S	0.230	0.270	0.0091	0.0106

Notes:
a. Use millimeters as the primary measurement.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72961.

MICRO FOOT: 10-BUMP (4 mm x 3 mm, 0.5 mm PITCH, 0.238 mm BUMP HEIGHT)



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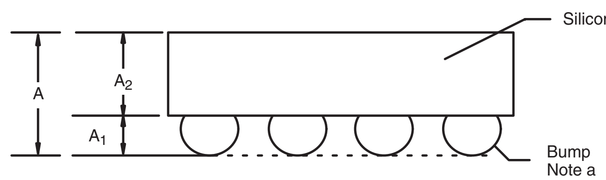
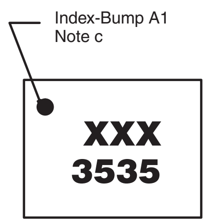
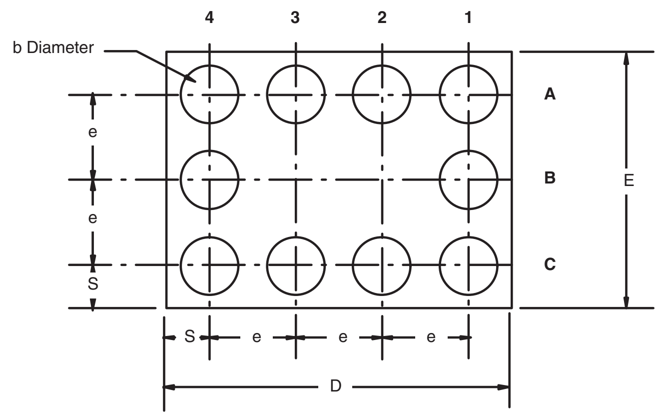




Top Side (Die Back)



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ECN: S11-1065-Rev. A, 13-Jun-11
DWG: 6001

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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

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