# IS42SM32160C
# IS42RM32160C

## 16Mx32
## 512Mb Mobile Synchronous DRAM

**NOVEMBER 2010**

### FEATURES:

- Fully synchronous; all signals referenced to a positive clock edge
- Internal bank for hiding row access and precharge
- Programmable CAS latency: 2, 3
- Programmable Burst Length: 1, 2, 4, 8, and Full Page
- Programmable Burst Sequence:
- Sequential and Interleave
- Auto Refresh (CBR)
- TCSR (Temperature Compensated Self Refresh)
- PASR (Partial Arrays Self Refresh): 1/16, 1/8, 1/4, 1/2, and Full
- Deep Power Down Mode (DPD)
- Driver Strength Control (DS): 1/4, 1/2, and Full

### OPTIONS:

- Configuration: 16Mx32
- Power Supply:
  IS42SMxxx - $V_{DD}/V_{DDQ}$ = 3.3V
  IS42RMxxx - $V_{DD}/V_{DDQ}$ = 2.5V
- Package: 90 Ball BGA (8x13mm)
- Temperature Range:
  Commercial (0°C to +70°C)
  Industrial (-40°C to +85°C)
- Die revision: C

### ADDRESS TABLE

| **Parameter** | **16Mx32** |
|---|---|
| Configuration | 4M x 32 x 4 banks |
| Bank Address Pins | BA0, BA1 |
| Autoprecharge Pins | A10/AP |
| Row Addresses | A0 – A12 |
| Column Addresses | A0 – A8 |
| Refresh Count | 8K / 64ms |

### DESCRIPTION:

ISSI's IS42SM/RM32160C is a 512Mb Mobile Synchronous DRAM configured as a quad 4M x32 DRAM. It achieves high-speed data transfer using a pipeline architecture with a synchronous interface. All inputs and outputs signals are registered on the rising edge of the clock input, CLK. The 512Mb SDRAM is internally configured by stacking two 256Mb, 16Mx16 devices. Each of the 4M x32 banks is organized as 8192 rows by 512 columns by 32 bits.

### KEY TIMING PARAMETERS

| Parameter | -7 | -75 | Unit |
|---|---|---|---|
| CLK Cycle Time | | | |
| $\overline{CAS}$ Latency = 3 | 7 | 7.5 | ns |
| $\overline{CAS}$ Latency = 2 | 9.6 | 9.6 | ns |
| CLK Frequency | | | |
| $\overline{CAS}$ Latency = 3 | 143 | 133 | Mhz |
| $\overline{CAS}$ Latency = 2 | 104 | 104 | Mhz |
| Access Time from CLK | | | |
| $\overline{CAS}$ Latency = 3 | 5.4 | 5.4 | ns |
| $\overline{CAS}$ Latency = 2 | 7 | 7 | ns |

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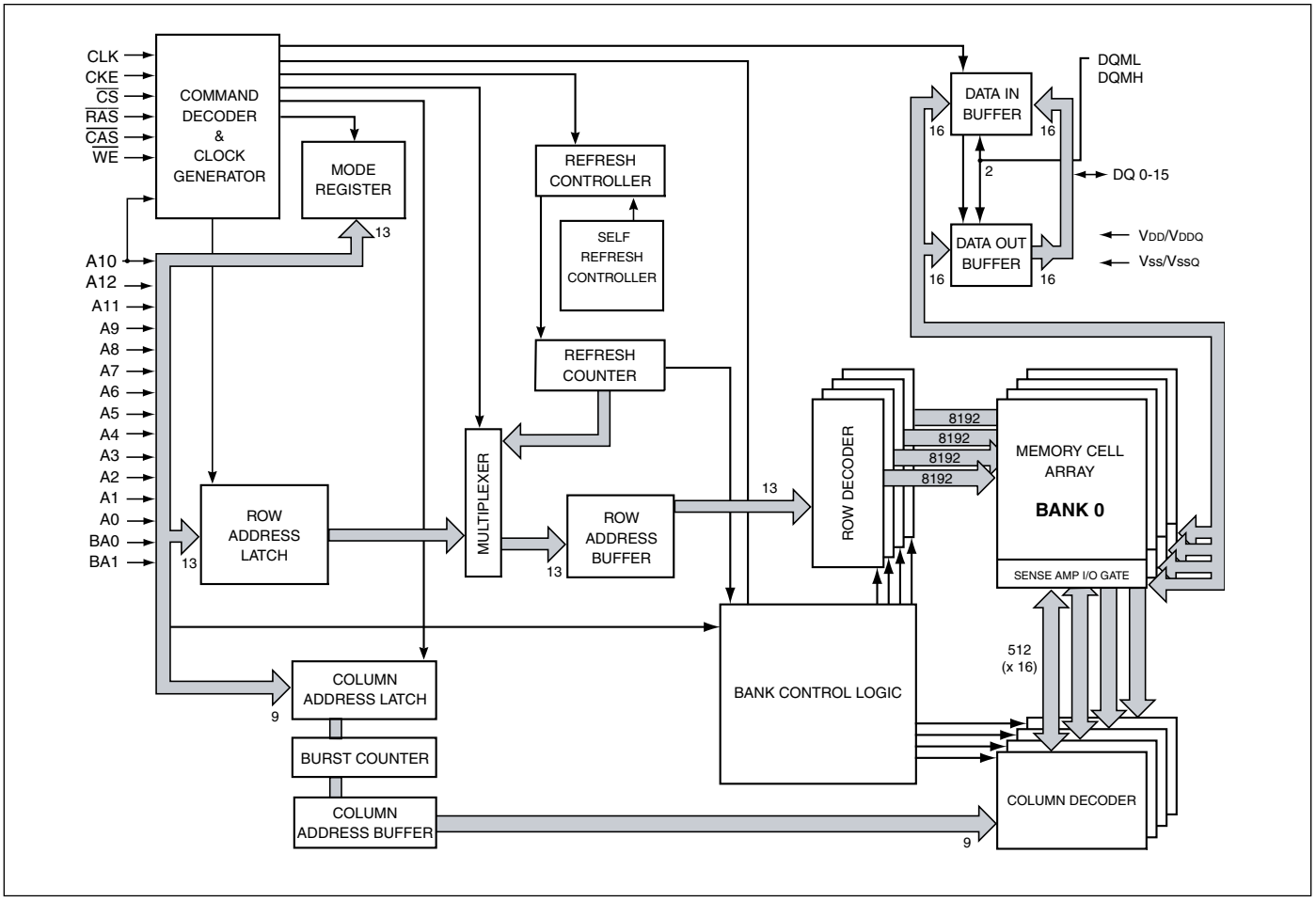
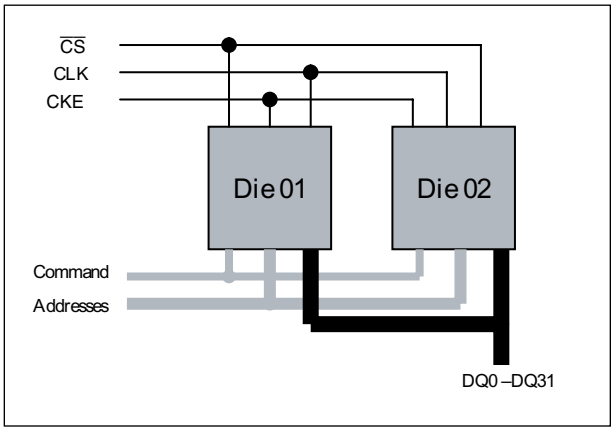
## FUNCTIONAL BLOCK DIAGRAM (16Mx16)




## FUNCTIONAL BLOCK DIAGRAM (16Mx32)

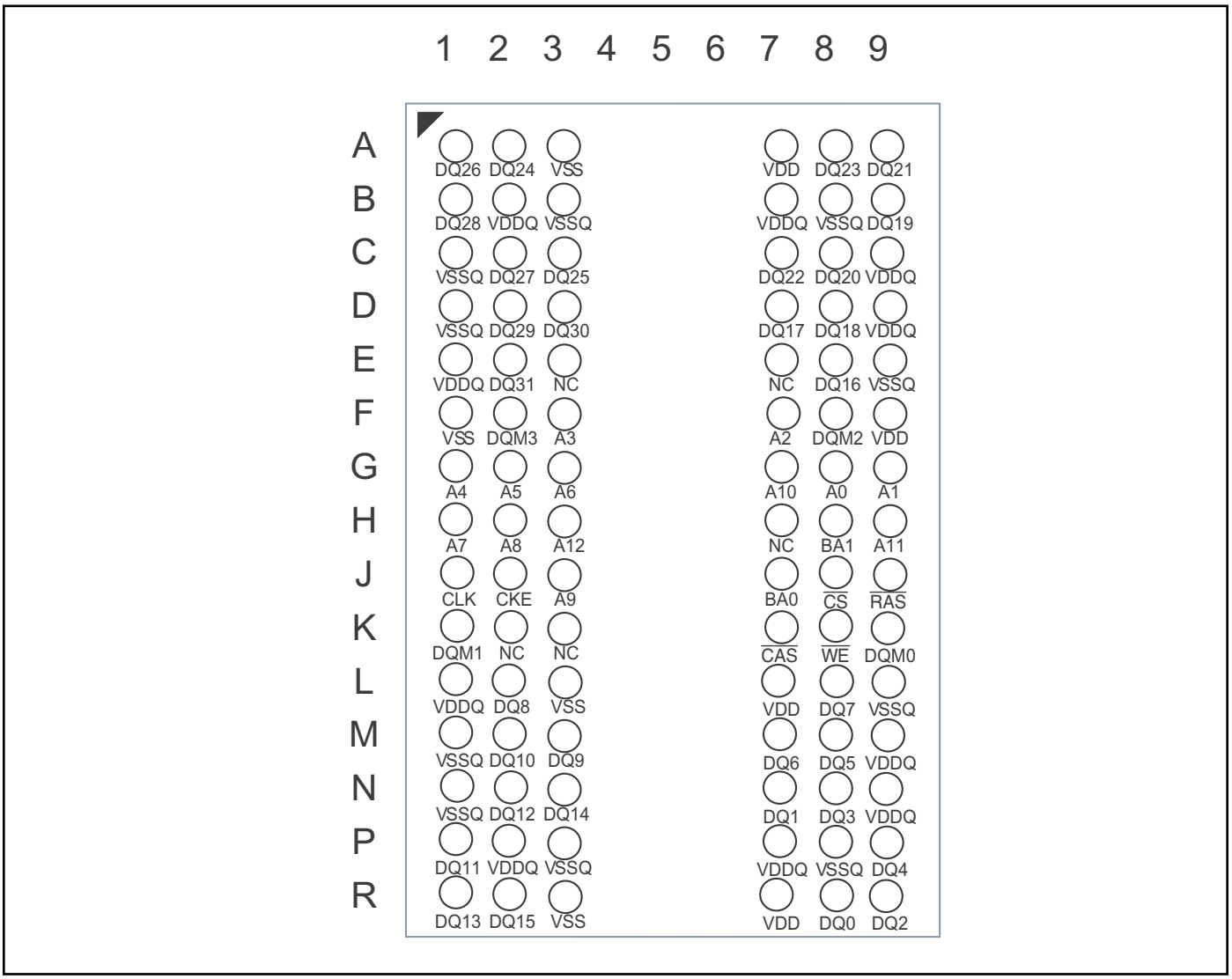


## PIN DESCRIPTIONS

| Symbol | Type | Description |
|---|---|---|
| **CLK** | **Input** | Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers. |
| **CKE** | **Input** | Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes. CKE is synchronous except after the device enters Power Down and Self Refresh modes, where CKE becomes asynchronous until exiting the same mode. The input buffers, including CLK, are disabled during Power Down and Self Refresh modes, providing low standby power. |
| **BA0, BA1** | **Input** | Bank Select: BA0 and BA1 defines to which bank the BankActivate, Read, Write, or BankPrecharge command is being applied. |
| **A0-A12** | **Input** | Address Inputs:A0-A12 are sampled during the BankActivate command (row address A0-A12) and Read/ Write command (column address A0-A8 with A10 defining Auto Precharge) to select one location in the respective bank. During a Precharge command,A10 is sampled to determine if all banks are to be precharged (A10 =HIGH).<br><br>The address inputs also provide the op-code during a Mode Register Set . |
| $\overline{CS}$ | **Input** | Chip Select: $\overline{CS}$ enables (sampled LOW) and disables (sampled HIGH) the command decoder.All commands are masked when $\overline{CS}$ is sampled HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. It is considered part of the command code. |
| $\overline{RAS}$ | **Input** | Row Address Strobe: The $\overline{RAS}$ signal defines the operation commands in conjunction with the $\overline{CAS}$ and $\overline{WE}$ signals and is latched at the positive edges of CLK. When $\overline{RAS}$ and $\overline{CS}$ are asserted "LOW" and $\overline{CAS}$ is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the $\overline{WE}$ signal. When the $\overline{WE}$ is asserted "HIGH," the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the $\overline{WE}$ is asserted "LOW," the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation. |
| $\overline{CAS}$ | **Input** | Column Address Strobe: The $\overline{CAS}$ signal defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{WE}$ signals and is latched at the positive edges of CLK. When $\overline{RAS}$ is held "HIGH" and $\overline{CS}$ is asserted "LOW," the column access is started by asserting $\overline{CAS}$ "LOW." Then, the Read or Write command is selected by asserting $\overline{WE}$ "LOW" or "HIGH." |
| $\overline{WE}$ | **Input** | Write Enable: The $\overline{WE}$ signal defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{CAS}$ signals and is latched at the positive edges of CLK. The $\overline{WE}$ input is used to select the BankActivate or Precharge command and Read or Write command. |
| **DQM0-3** | **Input** | Data Input/Output Mask: DQM0-DQM3 are byte specific, nonpersistent I/O buffer controls. The I/O buffers are placed in a high-z state when DQM is sampled HIGH. Input data is masked when DQM is sampled HIGH during a write cycle. Output data is masked (two-clock latency) when DQM is sampled HIGH during a read cycle. DQM3 masks DQ31-DQ24, DQM2 masks DQ23-DQ16, DQM1 masks DQ15-DQ8, and DQM0 masks DQ7-DQ0 |
| **DQ0-31** | **Input/ Output** | Data I/O: The DQ0-31 input and output data are synchronized with the positive edge of CLK. The I/Os are byte-maskable during Reads and Writes. |

## PIN CONFIGURATION

PACKAGE CODE: B 90 BALL FBGA (Top View) (8.00 mm x 13.00 mm Body, 0.8 m Ball Pitch)




## PIN DESCRIPTIONS

| | |
|---|---|
| A0-A12 | Row Address Input |
| A0-A8 | Column Address Input |
| BA0, BA1 | Bank Select Address |
| DQ0 to DQ31 | Data I/O |
| CLK | System Clock Input |
| CKE | Clock Enable |
| $\overline{CS}$ | Chip Select |
| $\overline{RAS}$ | Row Address Strobe Command |
| $\overline{CAS}$ | Column Address Strobe Command |

| | |
|---|---|
| $\overline{WE}$ | Write Enable |
| DQM0-DQM3 | x32 Input/Output Mask |
| $V_{DD}$ | Power |
| Vss | Ground |
| $V_{DDQ}$ | Power Supply for I/O Pin |
| $V_{SSQ}$ | Ground for I/O Pin |
| NC | No Connect |

## Mobile SDRAM Functionality

ISSI's 512Mb Mobile SDRAMs are pin compatible and have similar functionality with ISSI's standard SDRAMs, but offer lower operating voltages and power saving features. For detailed descriptions of pin functions, command truth tables, functional truth tables, device operation as well as timing diagrams please refer to ISSI document "Mobile Synchronous DRAM Device Operations & Timing Diagrams" listed at www.issi.com

# REGISTER DEFINITION

## Mode Register (MR) & Extended Mode Register (EMR)

There are two mode registers in the Mobile SDRAM; Mode Register (MR) and Extended Mode Register (EMR). The Mode Register is discussed below, followed by the Extended Mode Register. The Mode Register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of burst length, a burst type, CAS Latency, operating mode, and a write burst mode. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

The EMR controls the functions beyond those controlled by the MR. These additional functions are special features of the Mobile SDRAM. They include temperature-compensated self refresh (TCSR) control, partial-array self refresh (PASR), and output drive strength. The EMR is programmed via the MODE REGISTER SET command with BA1 = 1 and BA0 = 0 and retains the stored information until it is programmed again or the device loses power. Not programming the extended mode register upon initialization will result in default settings for the low-power features. The extended mode will default with the temperature sensor enabled, full drive strength, and full array (all 4 banks) refresh.

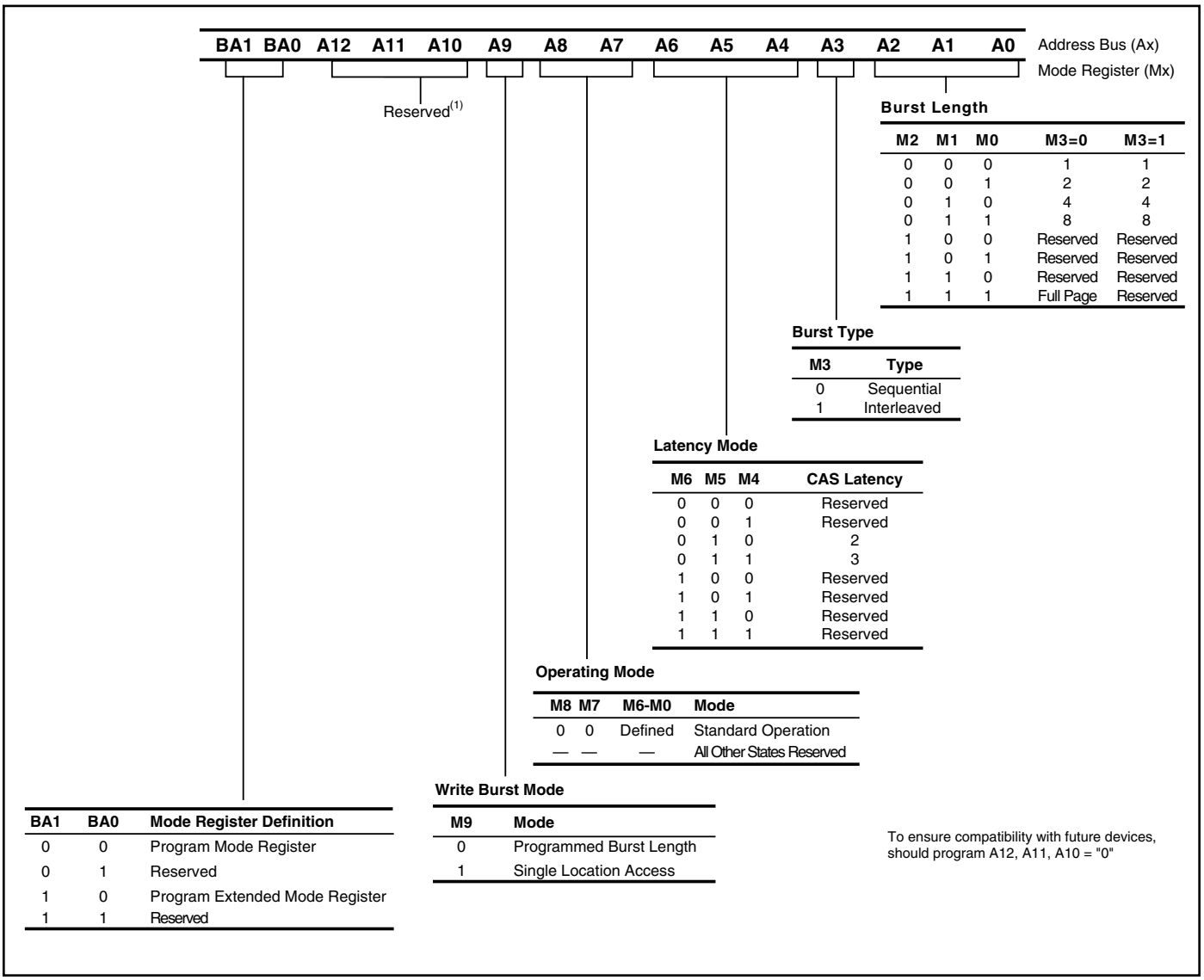
## Mode Register Definition

The MR is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in Figure MODE REGISTER DEFINITION. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0 - M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4 - M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the WRITE burst mode, and M10, M11, and M12 are reserved for future use.

The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

## MODE REGISTER DEFINITION




## Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in MODE REGISTER DEFINITION. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4 or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A8 (x32) when the burst length is set to two; by A2-A8 (x32) when the burst length is set to four; and by A3-A8 (x32) when the burst length is set to eight. The remaining (least significant) address bit(s) are used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

### Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in BURST DEFINITION table.

## BURST DEFINITION

| Burst Length | Starting Column Address | | | Order of Accesses Within a Burst | |
|---|---|---|---|---|---|
| | | | | Type = Sequential | Type = Interleaved |
| | | | A 0 | | |
| 2 | | | 0 | 0-1 | 0-1 |
| | | | 1 | 1-0 | 1-0 |
| | | A 1 | A 0 | | |
| | | 0 | 0 | 0-1-2-3 | 0-1-2-3 |
| 4 | | 0 | 1 | 1-2-3-0 | 1-0-3-2 |
| | | 1 | 0 | 2-3-0-1 | 2-3-0-1 |
| | | 1 | 1 | 3-0-1-2 | 3-2-1-0 |
| | A 2 | A 1 | A 0 | | |
| | 0 | 0 | 0 | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-5-6-7 |
| | 0 | 0 | 1 | 1-2-3-4-5-6-7-0 | 1-0-3-2-5-4-7-6 |
| | 0 | 1 | 0 | 2-3-4-5-6-7-0-1 | 2-3-0-1-6-7-4-5 |
| 8 | 0 | 1 | 1 | 3-4-5-6-7-0-1-2 | 3-2-1-0-7-6-5-4 |
| | 1 | 0 | 0 | 4-5-6-7-0-1-2-3 | 4-5-6-7-0-1-2-3 |
| | 1 | 0 | 1 | 5-6-7-0-1-2-3-4 | 5-4-7-6-1-0-3-2 |
| | 1 | 1 | 0 | 6-7-0-1-2-3-4-5 | 6-7-4-5-2-3-0-1 |
| | 1 | 1 | 1 | 7-0-1-2-3-4-5-6 | 7-6-5-4-3-2-1-0 |
| Full Page (y) | n = A0-A9 (x8) (location 0-y) | | | Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... …Cn - 1, Cn… | Not Supported |

### CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available by clock edge n + m. The DQs will start driving as a result of the clock edge one cycle earlier (n + m - 1), and provided that the relevant access times are met, the data will be valid by clock edge n + m. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in CAS Latency diagrams.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

### Operating Mode

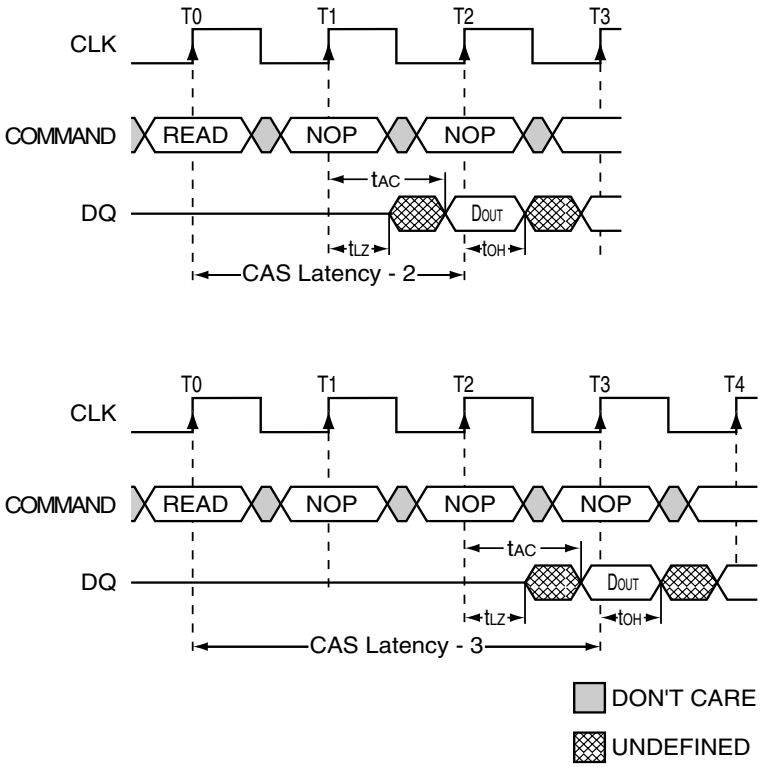
The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

### Write Burst Mode

When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

## CAS LATENCY



## EXTENDED MODE REGISTER DEFINITION

| BA1 | BA0 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | Address Bus (Ax) |
| | | | | | | | | | | | | | | | Ext. Mode Reg. (Ex) |

**PASR**

| E2 | E1 | E0 | Partial Array Self Refresh Coverage |
|---|---|---|---|
| 0 | 0 | 0 | Fully array (4 banks) - (Default) |
| 0 | 0 | 1 | Half array (banks 0, 1) |
| 0 | 1 | 0 | Quarter array (bank 0) |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | One-eighth array (1/2 bank 0) |
| 1 | 1 | 0 | One-sixteenth array (1/4 bank 0) |
| 1 | 1 | 1 | Reserved |

**TCSR**

| E4 | E3 | Max. Case Temp. |
|---|---|---|
| 0 | 0 | 70°C |
| 0 | 1 | 45°C |
| 1 | 0 | 15°C |
| 1 | 1 | 85°C (Default) |

**DS**

| E6 | E5 | Driver Strength |
|---|---|---|
| 0 | 0 | Full strength driver (Default) |
| 0 | 1 | Half strength driver |
| 1 | 0 | Quarter strength driver |
| 1 | 1 | Reserved |

**set to "0"**

| E12 | E11 | E10 | E9 | E8 | E7 | E6-E0 | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | Valid | Normal operation |
| – | – | – | – | – | – | – | All other states reserved |

| BA1 | BA0 | Mode Register Definition |
|---|---|---|
| 0 | 0 | Program Mode Register |
| 0 | 1 | Reserved |
| 1 | 0 | Program Extended mode Register |
| 1 | 1 | Reserved |

The extended mode register is programmed via the MODE REGISTER SET command (BA1 = 1, BA0 = 0) and retains the stored information until it is programmed again or the device loses power. The extended mode register must be programmed with E7 through E12 set to “0.” The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation. The extended mode register must be programmed to ensure proper operation.

### Temperature-Compensated Self Refresh (TCSR)

TCSR allows the controller to program the refresh interval during self refresh mode, according to the case temperature of the mobile device. This allows great power savings during self refresh during most operating temperature ranges. Only during extreme temperatures would the controller have to select a higher TCSR level that will guarantee data during self refresh.

Every cell in the DRAM requires refreshing due to the capacitor losing its charge over time. The refresh rate is dependent on temperature. At higher temperatures a capacitor loses charge quicker than at lower temperatures, requiring the cells to be refreshed more often. Historically, during self refresh, the refresh rate has been set to accommodate the worst case, or highest temperature range, expected. Thus, during ambient temperatures, the power consumed during refresh was unnecessarily high because the refresh rate was set to accommodate the higher temperatures. Setting E4 and E3 allows the DRAM to accommodate more specific temperature regions during self refresh. The default for ISSI 512Mb Mobile SDRAM is TCSR = 85°C to guarantee refresh operation. This mode of operation has a higher current consumption because the self refresh oscillator is set to refresh the SDRAM cells more often than needed. By using an external temperature sensor to determine the operating temperature the Mobile SDRAM can be programmed for lower temperature and refresh rates, effectively reducing current consumption by a significant amount. There are four temperature settings, which will vary the self refresh current according to the selected temperature. This selectable refresh rate will save power when the Mobile DRAM is operating at normal temperatures.

## Partial-Array Self Refresh (PASR)

For further power savings during self refresh, the PASR feature allows the controller to select the amount of memory that will be refreshed during self refresh. The refresh options are all banks (banks 0, 1, 2, and 3); two banks (banks 0 and 1); and one bank (bank 0). In addition partial amounts of bank 0 (half or quarter of the bank) may be selected. WRITE and READ commands occur to any bank selected during standard operation, but only the selected banks in PASR will be refreshed during self refresh. It's important to note that data in banks 2 and 3 will be lost when the two-bank option is used. Data will be lost in banks 1, 2, and 3 when the one-bank option is used.

## Driver Strength (DS)

Bits E5 and E6 of the EMR can be used to select the driver strength of the DQ outputs. This value should be set according to the application's requirements. The default is Full Driver Strength.

## Deep Power Down (DPD)

Deep power down mode is for maximum power savings and is achieved by shutting down power to the entire memory array of the mobile device. Data will be lost once deep power down mode is executed.

DPD mode is entered by having all banks idle, CS and WE held low, with RAS and CAS HIGH at the rising edge of the clock, while CKE is LOW. CKE must be held LOW during DPD mode. To exit DPD mode, CKE must be asserted HIGH. Upon exit from DPD mode, at least 200µs of valid clocks with either NOP or COMMAND INHIBIT commands are applied to the command bus, followed by a full Mobile SDRAM initialization sequence, is required.

# ELECTRICAL SPECIFICATIONS

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Parameters | | Rating | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage (with respect to Vss) | | -0.5 to +4.6 | V |
| $V_{DDQ}$ | Supply Voltage for Output (with respect to $V_{SSQ}$) | | -0.5 to +4.6 | V |
| $V_{IN}$ | Input Voltage (with respect to Vss) | | -0.5 to $V_{DD}$+0.5 | V |
| $V_{OUT}$ | Output Voltage (with respect to $V_{SSQ}$) | | -1.0 to $V_{DD}$+0.5 | V |
| $I_{CS}$ | Short circuit output current | | 50 | mA |
| $P_D$ | Power Dissipation ($T_A$ = 25°C) | | 1 | W |
| $T_{OPT}$ | Operating Temperature | Com. | 0 to +70 | °C |
| | | Ind. | -40 to +85 | °C |
| $T_{STG}$ | Storage Temperature | | –65 to +150 | °C |

**Note:**
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are reference to Vss.

## CAPACITANCE

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance, address and control pin | 5.0 | 7.0 | pF |
| $C_{CLK}$ | Input Capacitance, CLK pin | 5.0 | 7.6 | pF |
| $C_{IO}$ | Data Input/Output Capacitance | 4 | 6.5 | pF |

## DC RECOMMENDED OPERATING CONDITIONS

### IS42SMxxx - 3.3V Operation

| Symbol | Parameters | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| $V_{DDQ}$ | I/O Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| $V_{IH}$(1) | Input High Voltage | 2.0 | – | $V_{DDQ}$+0.3 | V |
| $V_{IL}$(2) | Input Low Voltage | -0.3 | – | 0.8 | V |
| $I_{IL}$ | Input Leakage Current (0V ≤ $V_{IN}$ ≤ $V_{DD}$) | -5 | – | +5 | µA |
| $I_{OL}$ | Output Leakage Current (Output disabled, 0V ≤ $V_{OUT}$ ≤ $V_{DD}$) | -5 | – | +5 | µA |
| $V_{OH}$ | Output High Voltage Current ($I_{OH}$ = -2mA) | 2.4 | – | – | V |
| $V_{OL}$ | Output Low Voltage Current ($I_{OL}$ = 2mA) | – | – | 0.4 | V |

### IS42RMxxx - 2.5V Operation

| Symbol | Parameters | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 2.3 | 2.5 | 2.7 | V |
| $V_{DDQ}$ | I/O Supply Voltage | 2.3 | 2.5 | 2.7 | V |
| $V_{IH}$(1) | Input High Voltage | 2.0 | - | $V_{DD}$+0.3 | V |
| $V_{IL}$(2) | Input Low Voltage | -0.3 | - | 0.55 | V |
| $I_{IL}$ | Input Leakage Current (0V ≤ $V_{IN}$ ≤ $V_{DD}$) | -5 | – | +5 | µA |
| $I_{OL}$ | Output Leakage Current (Output disabled, 0V ≤ $V_{OUT}$ ≤ $V_{DD}$) | -5 | – | +5 | µA |
| $V_{OH}$ | Output High Voltage Current ($I_{OH}$ = -2mA) | $V_{DD}$-0.2 | – | - | V |
| $V_{OL}$ | Output Low Voltage Current ($I_{OL}$ = 2mA) | - | – | 0.2 | V |

Notes:
1. $V_{IH}$ (overshoot): $V_{IH}$ (max) = $V_{DDQ}$ +1.2V (pulse width < 3ns).
2. $V_{IL}$ (undershoot): $V_{IH}$ (min) = -1.2V (pulse width < 3ns).
3. All voltages are referenced to Vss.

Contact Product Marketing for 3.0V ± 10% support.

## DC ELECTRICAL CHARACTERISTICS VDD = 3.3V / 2.5V x32

| Symbol | Parameter | Test Condition | -7 | –75 | Unit |
|---|---|---|---|---|---|
| $I_{DD}1$ (1) | Operating Current | One Bank Active, CL = 3, BL = 1, tCLK = tCLK(min), tRC = tRC(min) | 140 | 130 | mA |
| $I_{DD}2P$ (4) | Precharge Standby Current (In Power-Down Mode) | CKE ≤ $V_{IL}$ (max), tCK = 15ns $\overline{CS}$ ≥ $V_{DD}$ - 0.2V | 2 | 2 | mA |
| $I_{DD}2PS$ (4) | Precharge Standby Current With Clock Stop (In Power-Down Mode) | CKE ≤ $V_{IL}$ (max), CLK ≤ $V_{IL}$ (max) $\overline{CS}$ ≥ $V_{DD}$ - 0.2V | 2 | 2 | mA |
| $I_{DD}2N$(2) | Precharge Standby Current (In Non Power-Down Mode) | $\overline{CS}$ ≥ $V_{DD}$ - 0.2V, CKE ≥ $V_{IH}$ (min) tCK = 15 ns | 50 | 50 | mA |
| $I_{DD}2NS$ | Precharge Standby Current With Clock Stop (In Non-Power Down Mode) | $\overline{CS}$ ≥ $V_{DD}$ - 0.2V, CKE ≥ $V_{IH}$ (min) All Inputs Stable | 30 | 30 | mA |
| $I_{DD}3P$(2) | Active Standby Current (In Power-Down Mode) | CKE ≤ $V_{IL}$ (max), $\overline{CS}$ ≥ $V_{DD}$ - 0.2V tCK = 15 ns | 5 | 5 | mA |
| $I_{DD}3PS$ | Active Standby Current With Clock Stop (In Power-Down Mode) | CKE ≤ $V_{IL}$ (max), CLK ≤ $V_{IL}$ (max) $\overline{CS}$ ≥ $V_{DD}$ - 0.2V | 5 | 5 | mA |
| $I_{DD}3N$(2) | Active Standby Current (In Non Power-Down Mode) | $\overline{CS}$ ≥ $V_{DD}$ - 0.2V, CKE ≥ $V_{IH}$ (min) tCK = 15 ns | 65 | 65 | mA |
| $I_{DD}3NS$ | Active Standby Current With Clock Stop (In Non Power-Down Mode) | $\overline{CS}$ ≥ $V_{DD}$ - 0.2V, CKE ≥ $V_{IH}$ (min) All Inputs Stable | 35 | 35 | mA |
| $I_{DD}4$ | Operating Current | All Banks Active, BL =Full, CL = 3 tCK = tCK(min) | 180 | 170 | mA |
| $I_{DD}5$ | Auto-Refresh Current | tRC = tRC(min), tCLK = tCLK(min) | 260 | 250 | mA |
| $I_{DD}6$ | Self-Refresh Current | CKE ≤ 0.2V | 2.4 | 2.4 | mA |
| $I_{DD}7$ | Self-Refresh: CKE = LOW; $t_{CK}$ = $t_{CK}$ (MIN); Address, Control, and Data bus inputs are stable | Full Array, 85°C<br>Full Array, 45°C<br>Half Array, 85°C<br>Half Array, 45°C<br>1/4th Array, 85°C<br>1/4th Array, 45°C<br>1/8th Array, 85°C<br>1/8th Array, 45°C<br>1/16th Array, 85°C<br>1/16th Array, 45°C | 2.4<br>1.6<br>2.0<br>1.3<br>1.6<br>1.1<br>1.4<br>0.9<br>1.2<br>0.8 | | mA |
| $I_{ZZ}$(3,4) | Deep Power Down Current | CKE ≤ 0.2V | 40 | 40 | µA |

Notes:
1. $I_{DD}$ (max) is specified at the output open condition.
2. Input signals are changed one time during 30ns.
3. Izz values shown are nominal at 25°C. Izz is not testsed.
4. Tested after 500ms delay.

## AC ELECTRICAL CHARACTERISTICS (1, 2, 3)

| | | | -7 | | -75 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | | **Min.** | **Max.** | **Min.** | **Max.** | **Unit** |
| tCK3 | Clock Cycle Time | CAS Latency = 3 | 7 | – | 7.5 | – | ns |
| tCK2 | | CAS Latency = 2 | 9.6 | – | 9.6 | – | ns |
| tAC3 | Access Time From CLK | CAS Latency = 3 | – | 5.4 | – | 5.4 | ns |
| tAC2 | | CAS Latency = 2 | – | 7.0 | – | 7.0 | ns |
| tCHI | CLK HIGH Level Width | | 2.5 | – | 2.5 | – | ns |
| tCL | CLK LOW Level Width | | 2.5 | – | 2.5 | – | ns |
| tOH3 | Output Data Hold Time | CAS Latency = 3 | 2.7 | – | 2.7 | – | ns |
| tOH2 | | CAS Latency = 2 | 2.7 | – | 2.7 | – | ns |
| tLZ | Output LOW Impedance Time | | 0 | – | 0 | – | ns |
| tHZ | Output HIGH Impedance Time | CAS Latency = 3 | 2.7 | 5.4 | 2.7 | 5.4 | ns |
| | | CAS Latency = 2 | 2.7 | 7.0 | 2.7 | 7.0 | |
| tDS | Input Data Setup Time (2) | | 1.5 | – | 1.5 | – | ns |
| tDH | Input Data Hold Time (2) | | 1.0 | – | 1.0 | – | ns |
| tAS | Address Setup Time (2) | | 1.5 | – | 1.5 | – | ns |
| tAH | Address Hold Time (2) | | 1.0 | – | 1.0 | – | ns |
| tCKS | CKE Setup Time (2) | | 1.5 | – | 1.5 | – | ns |
| tCKH | CKE Hold Time (2) | | 1.0 | – | 1.0 | – | ns |
| tCS | Command Setup Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)(2) | | 1.5 | – | 1.5 | – | ns |
| tCH | Command Hold Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)(2) | | 1.0 | – | 1.0 | – | ns |
| tRC | Command Period (REF to REF / ACT to ACT) | | 67.5 | – | 67.5 | – | ns |
| tRAS | Command Period (ACT to PRE) | | 45 | 100K | 45 | 100K | ns |
| tRP | Command Period (PRE to ACT) | | 19 | – | 19 | – | ns |
| tRCD | Active Command to Read/Write Command Delay Time | | 19 | – | 19 | – | ns |
| tRRD | Command Period (ACT [0] to ACT [1]) | | 14 | – | 15 | – | ns |
| tDPL | Input Data to Precharge Command Delay Time | | 14 | – | 15 | – | ns |
| tDAL | Input Data to Active/Refresh Command Delay Time (During Auto-Precharge) | | 35 | – | 37.5 | – | ns |
| tMRD | Mode Register Program Time | | 14 | – | 15 | – | ns |
| tDDE | Power Down Exit Setup Time | | 7 | – | 7.5 | – | ns |
| tSRX | Exit Self-Refresh to Active Time | | 80 | – | 80 | – | ns |
| tT | Transition Time | | 0.3 | 1.2 | 0.3 | 1.2 | ns |
| tREF | Refresh Cycle Time | 8K times | – | 64 | – | 64 | ms |

Notes:
1. The power-on sequence must be executed before starting memory operation.
2. Measured with tT = 1 ns. If clock rising time is longer than 1ns, (tR /2 - 0.5) ns should be added to the parameter.
3. The reference level is 1.4V when measuring input signal timing. Rise and fall times are measured between $V_{IH}$(min.) and $V_{IL}$ (max).

## OPERATING FREQUENCY / LATENCY RELATIONSHIPS

| SYMBOL | PARAMETER | -7 | -75 | UNITS |
|---|---|---|---|---|
| — | Clock Cycle Time | 7 | 7.5 | ns |
| — | Operating Frequency | 143 | 133 | MHz |
| $t_{CAC}$ | $\overline{CAS}$ Latency | 3 | 3 | cycle |
| $t_{RCD}$ | Active Command To Read/Write Command Delay Time | 3 | 3 | cycle |
| $t_{RAC}$ | $\overline{RAS}$ Latency ($t_{RCD}$ + $t_{CAC}$) $\overline{CAS}$ Latency = 3 | 6 | 6 | cycle |
| $t_{RC}$ | Command Period (REF to REF / ACT to ACT) | 10 | 9 | cycle |
| $t_{RAS}$ | Command Period (ACT to PRE) | 7 | 6 | cycle |
| $t_{RP}$ | Command Period (PRE to ACT) | 3 | 3 | cycle |
| $t_{RRD}$ | Command Period (ACT[0] to ACT [1]) | 2 | 2 | cycle |
| $t_{CCD}$ | Column Command Delay Time (READ, READA, WRIT, WRITA) | 1 | 1 | cycle |
| $t_{DPL}$ | Input Data To Precharge Command Delay Time | 2 | 2 | cycle |
| $t_{DAL}$ | Input Data To Active/Refresh Command Delay Time (During Auto-Precharge) | 5 | 5 | cycle |
| $t_{RBD}$ | Burst Stop Command To Output in HIGH-Z Delay Time (Write) $\overline{CAS}$ Latency = 3 | 3 | 3 | cycle |
| $t_{WBD}$ | Burst Stop Command To Input in Invalid Delay Time (Write) | 0 | 0 | cycle |
| $t_{RQL}$ | Precharge Command To Output in HIGH-Z Delay Time (Read) $\overline{CAS}$ Latency = 3 | 3 | 3 | cycle |
| $t_{WDL}$ | Precharge Command To Input in Invalid Delay Time (Write) | 0 | 0 | cycle |
| $t_{PQL}$ | Last Output To Auto-Precharge Start Time (Read) $\overline{CAS}$ Latency = 3 | -2 | -2 | cycle |
| $t_{QMD}$ | DQM To Output Delay Time (Read) | 2 | 2 | cycle |
| $t_{DMD}$ | DQM To Input Delay Time (Write) | 0 | 0 | cycle |
| $t_{MRD}$ | Mode Register Set To Command Delay Time | 2 | 2 | cycle |

## Ordering Information – $V_{DD}$ = 3.3V

### Commercial Range: (0°C to +70°C)

| Frequency | Speed (ns) | Order Part No. | Package |
|---|---|---|---|
| 143 MHz | 7.0 | IS42SM32160C-7BL | 8x13mm BGA, Lead-free |
| 133 MHz | 7.5 | IS42SM32160C-75BL | 8x13mm BGA, Lead-free |

### Industrial Range: (-40°C to +85°C)

| Frequency | Speed (ns) | Order Part No. | Package |
|---|---|---|---|
| 143 MHz | 7.0 | IS42SM32160C-7BLI | 8x13mm BGA, Lead-free |
| 133 MHz | 7.5 | IS42SM32160C-75BLI | 8x13mm BGA, Lead-free |

## Ordering Information – $V_{DD}$ = 2.5V

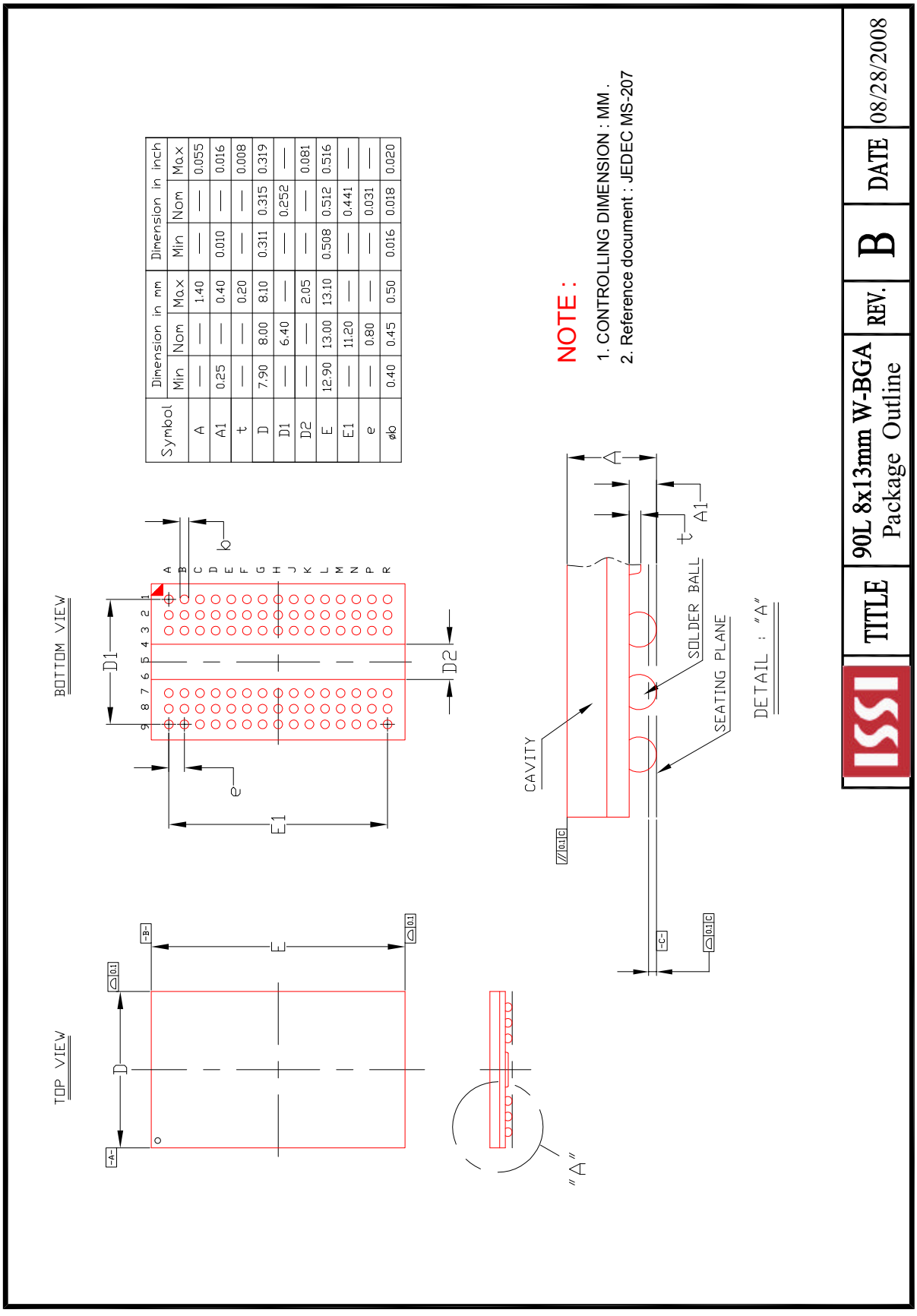
### Commercial Range: (0°C to +70°C)

| Frequency | Speed (ns) | Order Part No. | Package |
|---|---|---|---|
| 133 MHz | 7.5 | IS42RM32160C-75BL | 8x13mm BGA, Lead-free |

### Industrial Range: (-40°C to +85°C)

| Frequency | Speed (ns) | Order Part No. | Package |
|---|---|---|---|
| 133 MHz | 7.5 | IS42RM32160C-75BLI | 8x13mm BGA, Lead-free |

*Contact ISSI for leaded parts support.




| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | — | — | 1.40 | — | — | 0.055 |
| A1 | 0.25 | — | 0.40 | 0.010 | — | 0.016 |
| t | — | — | 0.20 | — | — | 0.008 |
| D | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| D1 | — | 6.40 | — | — | 0.252 | — |
| D2 | — | — | 2.05 | — | — | 0.081 |
| E | 12.90 | 13.00 | 13.10 | 0.508 | 0.512 | 0.516 |
| E1 | — | 11.20 | — | — | 0.441 | — |
| e | — | 0.80 | — | — | 0.031 | — |
| øb | 0.40 | 0.45 | 0.50 | 0.016 | 0.018 | 0.020 |