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NTE861
Integrated Circuit
Quad, Normally Open, SPST JFET
Analog Switch w/Disable

Description:

The NTE861 is a monolithic combination of bipolar and JFET technology producing a one chip quad JFET switch. A unique circuit technique is employed to maintain a constant resistance over the analog voltage range of ±10V. The input is designed to operate from minimum TTL levels, and switch operation also ensures a break–before–make action.

Features:

- Analog signals are not loaded
- Constant “ON” resistance for signals up to ±10V and 100kHz
- Pin compatible with CMOS switches with the advantage of blow out free handling
- Small signal analog signals to 50MHz
- Break–before–make action
- High open switch isolation at 1.0MHz
- Low leakage in “OFF” state
- TTL, DTL, RTL compatibility
- Single disable pin opens all switches in package

This device operates from a ±15V supply and swings a ±10V analog signal. The JFET switches are designed for applications where a dc to medium frequency analog signal needs to be controlled.

Absolute Maximum Ratings:

Positive Supply–Negative Supply ($V_{CC} - V_{EE}$) 36V
Reference Voltage . . . . . $V_{EE} \le V_R \le V_{CC}$
Logic Input Voltage . . . . . $V_R - 4.0V \le V_{IN} \le V_R + 6.0V$
Analog Voltage . . . . . $V_{EE} \le V_A \le V_{CC} + 6V$; $V_A \le V_{EE} + 36V$
Analog Current . . . . . $I_A < 20mA$
Power Dissipation (Note 1) 500mW
Operating Temperature Range . . . . . 0° to 70°C
Storage Temperature . . . . . –65° to 150°C
Typical Thermal Resistance, Junction–to–Ambient, R_{thJA} . . . . . 85°C/W
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C

Note 1 For operating at high temperature this device must be derated based on a +100°C maximum junction temperature and a thermal resistance of +150°C/W.

Electrical Characteristics: (Note 2)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
"ON" Resistance	R_{ON}	V_A = 0, I_D = 1mA	T_A = +25°C	–	150	250	Ω
				–	200	350	Ω
"ON" Resistance Matching	R_{ON} Match	T_A = +25°C		–	10	50	Ω
Analog Range	V_A			±10	±11	–	V
Leakage Current in "ON" Condition	$I_{S(ON)}$ + $I_{D(ON)}$	Switch "ON", V_S = V_D = ±10V	T_A = +25°C	–	0.3	10	nA
				–	3	30	nA
Source Current in "OFF" Condition	$I_{S(OFF)}$	Switch "OFF", V_S = +10V, V_D = –10V	T_A = +25°C	–	0.4	10	nA
				–	3	30	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$		T_A = +25°C	–	0.1	10	nA
				–	3	30	nA
Logical "1" Input Voltage	V_{INH}			2.0	–	–	V
Logical "0" Input Voltage	V_{INL}			–	–	0.8	V
Logical "1" Input Current	I_{INH}	V_{IN} = 5V	T_A = +25°C	–	3.6	40	µA
				–	–	100	µA
Logical "0" Input Current	I_{INL}	V_{IN} = 0.8V	T_A = +25°C	–	–	0.1	µA
				–	–	1.0	µA
Delay Time "ON"	t_{ON}	V_S = ±10V, T_A = +25°C		–	500	–	ns
Delay Time "OFF"	t_{OFF}	V_S = ±10V, T_A = +25°C		–	90	–	ns
Break–Before–Make	$t_{ON} - t_{OFF}$	V_S = ±10V, T_A = +25°C		–	80	–	ns
Source Capacitance	$C_{S(OFF)}$	Switch "OFF", V_S = ±10V, T_A = +25°C		–	4.0	–	pF
Drain Capacitance	$C_{D(OFF)}$	Switch "OFF", V_D = ±10V, T_A = +25°C		–	3.0	–	pF
Active Source and Drain Capacitance	$C_{S(ON)}$ + $C_{D(ON)}$	Switch "ON", V_S = V_D = ±10V, T_A = +25°C		–	5.0	–	pF
"OFF" Isolation	$I_{SO(OFF)}$	T_A = +25°C, Note 3		–	–50	–	dB
Crosstalk	CT	T_A = +25°C, Note 3		–	–65	–	dB
Analog Slew Rate	SR	T_A = +25°C, Note 4		–	50	–	V/µs
Disable Current	I_{DIS}	Note 5	T_A = +25°C	–	0.6	1.5	mA
				–	0.9	2.3	mA
Negative Supply Current	I_{EE}	All Switches "OFF", V_S = ±10V	T_A = +25°C	–	4.3	7.0	mA
				–	6.0	10.5	mA
Reference Supply Current	I_R		T_A = +25°C	–	2.7	5.0	mA
				–	3.8	7.5	mA
Positive Supply Current	I_{CC}		T_A = +25°C	–	7.0	9.0	mA
				–	9.8	13.5	mA

Note 2. V_{CC} = +15V, V_{EE} = –15V, V_R = 0V, and limits apply for –25°C ≤ T_A ≤ +85°C unless otherwise specified.

Note 3. These parameters are limited by the pin to pin capacitance of the package.

Note 4. This is the analog signal slew rate above which the signal is distorted as a result of finite internal slew rates.

Note 5. All switches in the device are turned "OFF" by saturating a transistor at the disable node. The delay times will be approximately equal to the t_{ON} or t_{OFF} plus the delay introduced by the external transistor.

Pin Connection Diagram