



TPS795 Ultralow-Noise, High-PSRR, Fast, RF, 500-mA Low-Dropout Linear Regulators

1 Features

- 500-mA Low-Dropout Regulator With Enable
- Available in Fixed and Adjustable (1.2-V to 5.5-V) Versions
- High PSRR (50 dB at 10 kHz)
- Ultralow Noise (33 μV_{RMS} , TPS79530)
- Fast Start-Up Time (50 μs)
- Stable With a 1- μF Ceramic Capacitor
- Excellent Load and Line Transient Response
- Low Dropout Voltage (110 mV at Full Load, TPS79530)
- 6-Pin SOT-223 and 3-mm \times 3-mm WSON Packages

2 Applications

- RF: VCOs, Receivers, ADCs
- Audio
- *Bluetooth*[®], Wireless LAN
- Cellular and Cordless Telephones
- Handheld Organizers, PDAs

3 Description

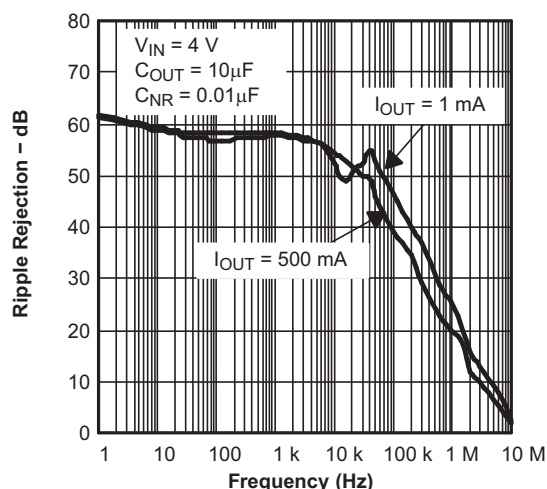
The TPS795 family of low-dropout (LDO), low-power linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in small outline, 6-pin SOT-223 and 3-mm \times 3-mm WSON packages. Each device in the family is stable with a small 1- μF ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (for example, 110 mV at 500 mA). Each device achieves fast start-up times (approximately 50 μs with a 0.001- μF bypass capacitor) while consuming very low quiescent current (265 μA , typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 μA . The TPS79530 device exhibits approximately 33 μV_{RMS} of output voltage noise at 3-V output with a 0.1- μF bypass capacitor. Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from the high-PSRR and low-noise features, as well as from the fast response time.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS795	SOT-223 (6)	6.50 mm \times 3.50 mm
	WSON (8)	3.00 mm \times 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

TPS79530 Ripple Rejection vs Frequency



TPS79530 vs Frequency

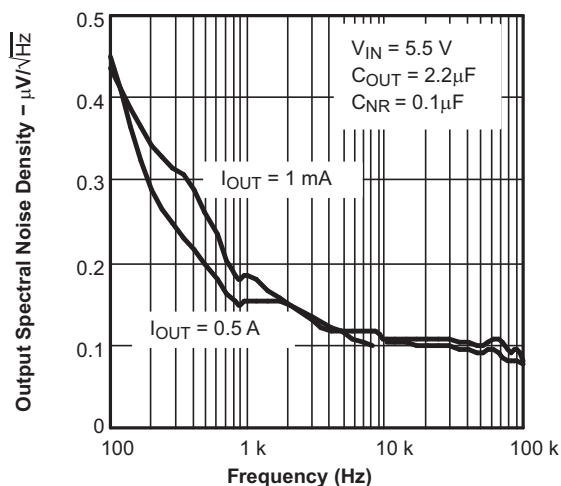


Table of Contents

1 Features	1	8.1 Application Information.....	13
2 Applications	1	8.2 Typical Application	13
3 Description	1	8.3 Do's and Don'ts	15
4 Revision History	2	9 Power Supply Recommendations	16
5 Pin Configuration and Functions	3	10 Layout	16
6 Specifications	4	10.1 Layout Guidelines	16
6.1 Absolute Maximum Ratings	4	10.2 Layout Examples	17
6.2 ESD Ratings	4	10.3 Thermal Considerations	18
6.3 Recommended Operating Conditions	4	10.4 Estimating Junction Temperature	19
6.4 Thermal Information	4	11 Device and Documentation Support	21
6.5 Electrical Characteristics	5	11.1 Device Support	21
6.6 Typical Characteristics	6	11.2 Documentation Support	21
7 Detailed Description	10	11.3 Community Resources	21
7.1 Overview	10	11.4 Trademarks	21
7.2 Functional Block Diagrams	10	11.5 Electrostatic Discharge Caution	21
7.3 Feature Description	11	11.6 Glossary	22
7.4 Device Functional Modes	12	12 Mechanical, Packaging, and Orderable Information	22
8 Application and Implementation	13		

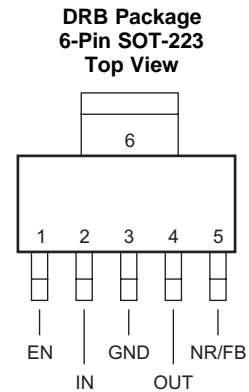
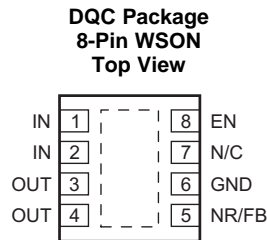
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (August 2010) to Revision I	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Changed front-page graphic	1
• Changed <i>Pin Configuration and Functions</i> section; updated table format and added pinout drawings	3
• Changed "free-air" to "junction" temperature in condition statement for <i>Absolute Maximum Ratings</i>	4
• Deleted Start-up time symbol	5
• Corrected min value for $I_{EN(HI)}$ parameter	5
• Added <i>Thermal shutdown temperature</i> specification to <i>Electrical Characteristics</i>	5
• Added <i>Operating junction temperature</i> specification to <i>Electrical Characteristics</i>	5
• Added condition statement to <i>Typical Characteristics</i> section	6
• Changed title for <i>Thermal Protection</i> section	18

Changes from Revision G (July, 2006) to Revision H	Page
• Replaced the <i>Dissipation Ratings</i> table with the <i>Thermal Information</i> table	4
• Updated the <i>Thermal Protection</i> section	18

5 Pin Configuration and Functions



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	SOT-223	WSON		
IN	2	1, 2	I	Unregulated input to the device
GND	3, 6	6	—	Regulator ground
EN	1	8	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
NR	5	5	—	Noise-reduction pin for fixed versions only. Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, which improves power-supply rejection and reduces output noise. (Not available on adjustable versions.)
FB	5	5	I	Feedback input voltage for the adjustable device. (Not available on fixed voltage versions.)
OUT	4	3, 4	O	Regulator output
N/C	—	7	—	No internal connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Voltage	IN	−0.3	6	V
	EN	−0.3	$V_{IN} + 0.3$	
	OUT		6	
Current	Peak output	Internally limited		
Power dissipation	Continuous total	See Thermal Information		
Temperature	Junction, T_J	−40	150	°C
	Storage, T_{stg}	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		5.5	V
I_{OUT}	Output current	0		0.5	A
T_J	Operating junction temperature	−40		125	°C

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC ⁽¹⁾⁽²⁾		TPS795 ⁽³⁾		UNIT
		DRB (SOT-223)	DCQ (WSON)	
		6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.8	70.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	83	70	
Ψ_{JT}	Junction-to-top characterization parameter	2.1	6.8	
Ψ_{JB}	Junction-to-board characterization parameter	17.8	30.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.1	6.3	

- (1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics application report, SPRA953](#).

- (2) For thermal estimates of this device based on PCB copper area, see the [TI PCB Thermal Calculator](#).

- (3) Thermal data for the DRB and DCQ packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:

- (a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2-mm x 2-mm thermal via array.

- ii. DCQ: The exposed pad is connected to the PCB ground layer through a 3-mm x 2-mm thermal via array.

- (b) i. DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.

- ii. DCQ: Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.

- (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in x 3in copper area. To understand the effects of the copper area on thermal performance, see [Thermal Considerations](#) and [Estimating Junction Temperature](#) of this data sheet.

6.5 Electrical Characteristics

Over recommended operating temperature range ($T_J = -40^{\circ}\text{C}$ to 125°C), $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}^{(1)}$, $I_{OUT} = 1\text{ mA}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, unless otherwise noted. Typical values are at 25°C .

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage ⁽¹⁾			2.7		5.5	V
V_{FB}	Internal reference (TPS79501)			1.200	1.225	1.25	V
I_{OUT}	Continuous output current			0		500	mA
V_{OUT}	Output voltage range	TPS79501		1.225		$5.5 - V_{DO}$	V
	Accuracy	TPS79501 ⁽²⁾	$0\text{ }\mu\text{A} \leq I_{OUT} \leq 500\text{ mA}$, $V_{OUT(nom)} + 1\text{ V} \leq V_{IN} \leq 5.5\text{ V}^{(1)}$	$0.98V_{OUT(nom)}$	$V_{OUT(nom)}$	$1.02V_{OUT(nom)}$	V
		Fixed $V_{OUT} < 5\text{ V}$	$0\text{ }\mu\text{A} \leq I_{OUT} \leq 500\text{ mA}$, $V_{OUT(nom)} + 1\text{ V} \leq V_{IN} \leq 5.5\text{ V}^{(1)}$	-2%		2%	
$\Delta V_{O(\Delta VI)}$	Line regulation ⁽¹⁾		$V_{OUT} + 1\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		0.05	0.12	%/V
$\Delta V_{O(\Delta IO)}$	Load regulation		$0\text{ }\mu\text{A} \leq I_{OUT} \leq 500\text{ mA}$		3		mV
V_{DO}	Dropout voltage ⁽³⁾ ($V_{IN} = V_{OUT(nom)} - 0.1\text{ V}$)	TPS79530	$I_{OUT} = 500\text{ mA}$		110	170	mV
		TPS79533	$I_{OUT} = 500\text{ mA}$		105	160	
I_{CL}	Output current limit		$V_{OUT} = 0\text{ V}$	2.4	2.8	4.2	A
I_{GND}	Ground pin current		$0\text{ }\mu\text{A} \leq I_{OUT} \leq 500\text{ mA}$		265	385	μA
I_{SHDN}	Shutdown current ⁽⁴⁾		$V_{EN} = 0\text{ V}$, $2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		0.07	1	μA
I_{FB}	Feedback pin current		$V_{FB} = 1.225\text{ V}$			1	μA
PSRR	Power-supply rejection ratio (TPS79530)		$f = 100\text{ Hz}$, $I_{OUT} = 10\text{ mA}$		59		dB
			$f = 100\text{ Hz}$, $I_{OUT} = 500\text{ mA}$		58		
			$f = 10\text{ kHz}$, $I_{OUT} = 500\text{ mA}$		50		
			$f = 100\text{ kHz}$, $I_{OUT} = 500\text{ mA}$		39		
V_n	Output noise voltage (TPS79530)		BW = 100 Hz to 100 kHz, $I_{OUT} = 500\text{ mA}$	$C_{NR} = 0.001\text{ }\mu\text{F}$	46		μV_{RMS}
				$C_{NR} = 0.0047\text{ }\mu\text{F}$	41		
				$C_{NR} = 0.01\text{ }\mu\text{F}$	35		
				$C_{NR} = 0.1\text{ }\mu\text{F}$	33		
	Start-up time (TPS79530)		$R_L = 6\text{ }\Omega$, $C_{OUT} = 1\text{ }\mu\text{F}$	$C_{NR} = 0.001\text{ }\mu\text{F}$	50		μs
				$C_{NR} = 0.0047\text{ }\mu\text{F}$	75		
				$C_{NR} = 0.01\text{ }\mu\text{F}$	110		
$V_{EN(HI)}$	Enable high (enabled)		$2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	1.7		V_{IN}	V
$V_{EN(LO)}$	Enable low (shutdown)		$2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$			0.7	V
$I_{EN(HI)}$	Enable pin current, enabled		$V_{EN} = 0\text{ V}$	-1		1	μA
UVLO	Undervoltage lockout		V_{CC} rising	2.25		2.65	V
	Hysteresis				100		mV
T_{sd}	Thermal shutdown temperature		Shutdown, temperature increasing		165		$^{\circ}\text{C}$
			Reset, temperature decreasing		140		
T_J	Operating junction temperature			-40		125	$^{\circ}\text{C}$

(1) Minimum V_{IN} is 2.7 V or $V_{OUT} + V_{DO}$, whichever is greater.

(2) Tolerance of external resistors not included in this specification.

(3) Dropout is not measured for the TPS79501 and TPS79525 because minimum $V_{IN} = 2.7\text{ V}$.

(4) For adjustable version, this applies only after V_{IN} is applied; then V_{EN} transitions high to low.

6.6 Typical Characteristics

At $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, $C_{IN} = 2.2\text{ }\mu\text{F}$, and $T_J = 25^\circ\text{C}$, unless otherwise noted.

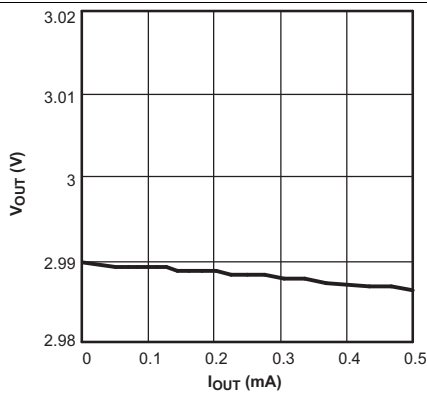


Figure 1. TPS79530 Output Voltage vs Output Current

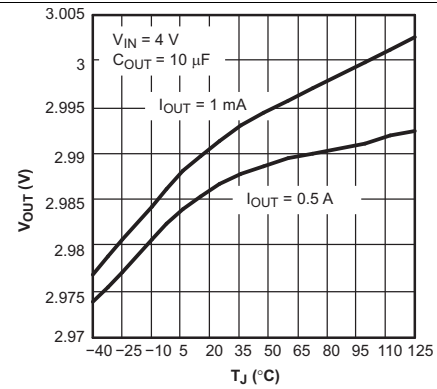


Figure 2. TPS79530 Output Voltage vs Junction Temperature

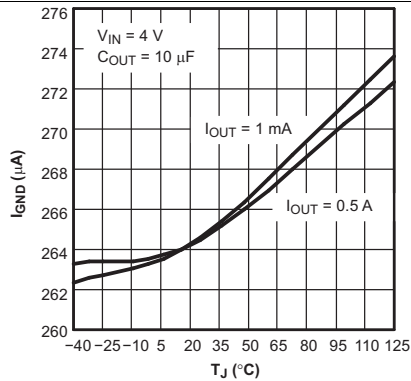


Figure 3. TPS79530 Ground Current vs Junction Temperature

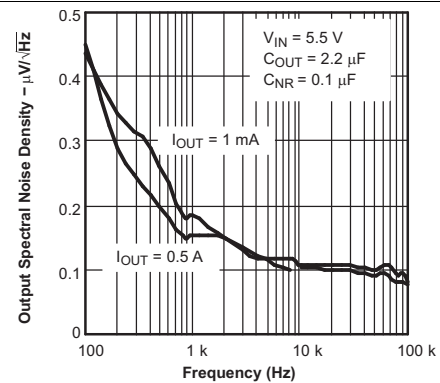


Figure 4. TPS79530 Output Spectral Noise Density vs Frequency

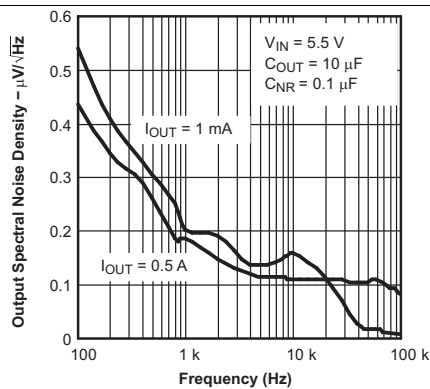


Figure 5. TPS79530 Output Spectral Noise Density vs Frequency

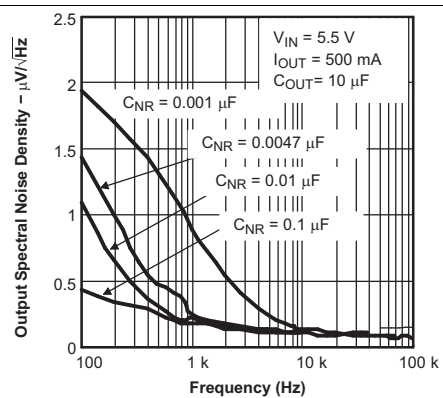


Figure 6. TPS79530 Output Spectral Noise Density vs Frequency

Typical Characteristics (continued)

At $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, $C_{IN} = 2.2\text{ }\mu\text{F}$, and $T_J = 25^\circ\text{C}$, unless otherwise noted.

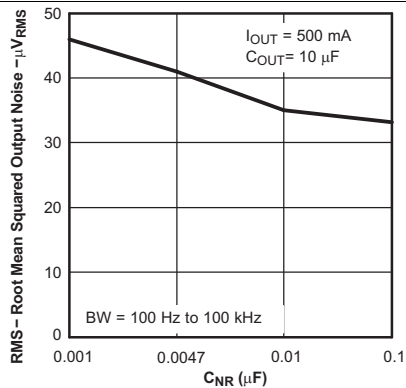


Figure 7. TPS79530 Root Mean Squared Output Noise vs C_{NR}

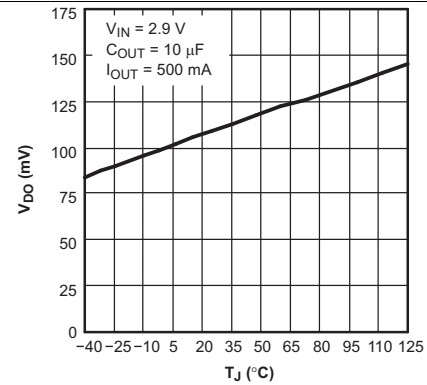


Figure 8. TPS79530 Dropout Voltage vs Junction Temperature

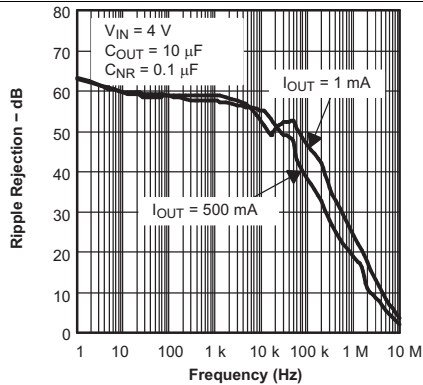


Figure 9. TPS79530 Ripple Rejection vs Frequency

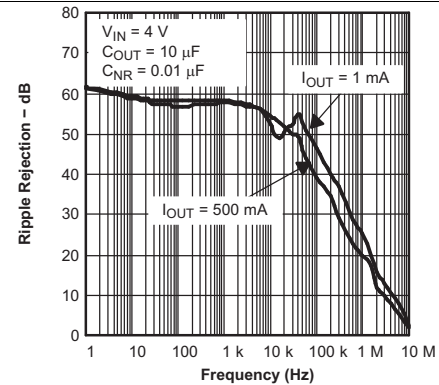


Figure 10. TPS79530 Ripple Rejection vs Frequency

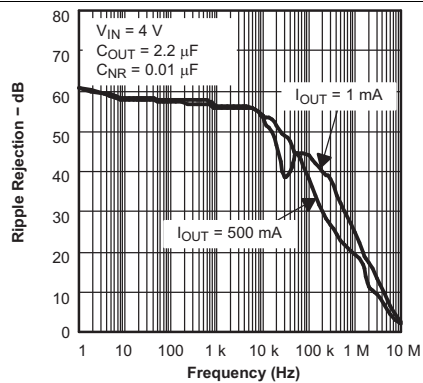


Figure 11. TPS79530 Ripple Rejection vs Frequency

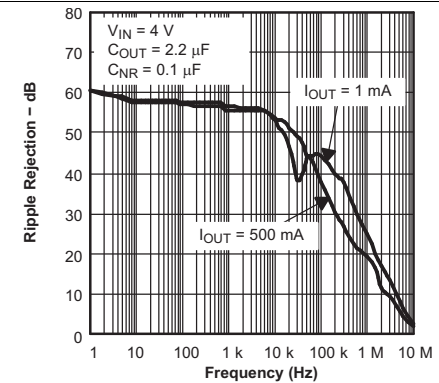


Figure 12. TPS79530 Ripple Rejection vs Frequency

Typical Characteristics (continued)

At $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, $C_{IN} = 2.2\text{ }\mu\text{F}$, and $T_J = 25^\circ\text{C}$, unless otherwise noted.

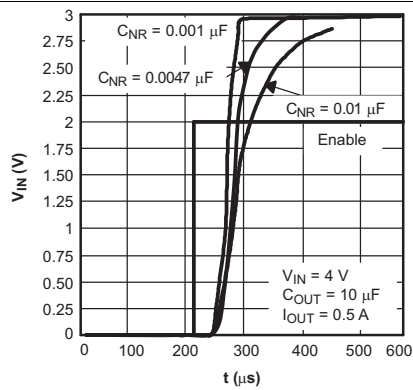


Figure 13. TPS79530 Start-Up Time

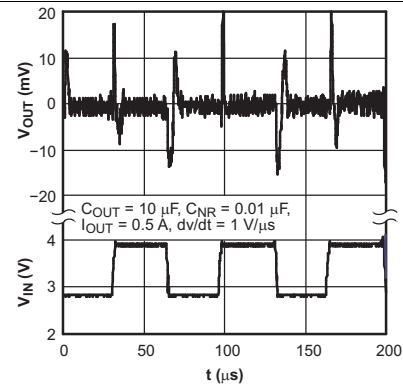


Figure 14. TPS79518 Line Transient Response

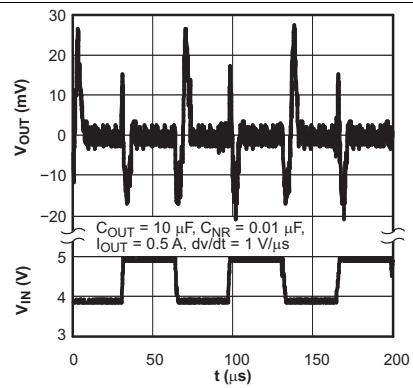


Figure 15. TPS79530 Line Transient Response

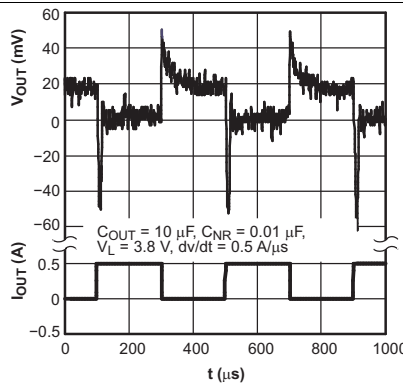


Figure 16. TPS79530 Load Transient Response

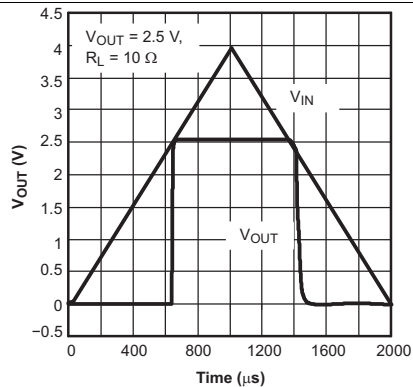


Figure 17. TPS79525 Power Up and Power Down

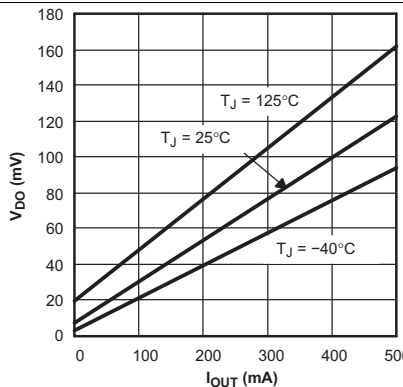


Figure 18. TPS79530 Dropout Voltage vs Output Current

Typical Characteristics (continued)

At $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, $C_{IN} = 2.2\text{ }\mu\text{F}$, and $T_J = 25^\circ\text{C}$, unless otherwise noted.

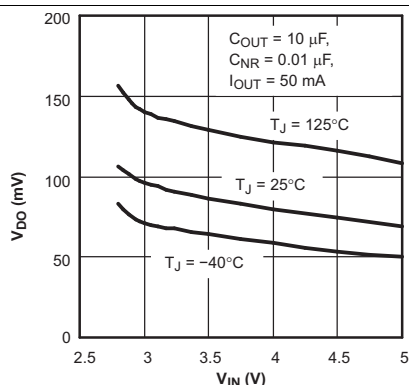


Figure 19. TPS79501 Dropout Voltage vs Input Voltage

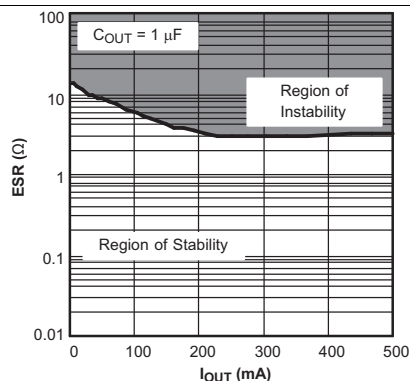


Figure 20. TPS79530 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

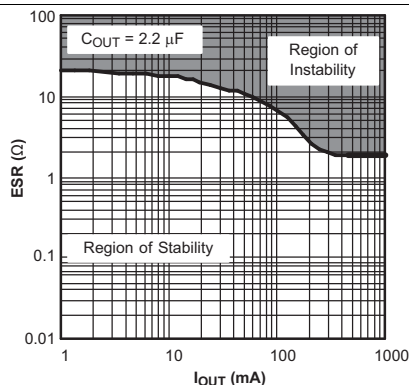


Figure 21. TPS79530 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

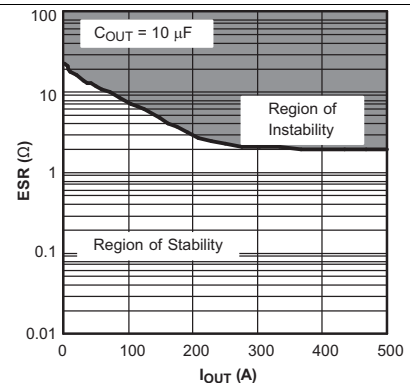


Figure 22. TPS79530 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

7 Detailed Description

7.1 Overview

The TPS795 family of LDO regulators combines the high performance required of many RF and precision analog applications with low current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection at very low headroom ($V_{IN} - V_{OUT}$). A noise-reduction pin is provided to bypass noise generated by the band-gap reference and to improve PSRR, while a quick-start circuit quickly charges this capacitor at start-up. All versions have thermal and overcurrent protection, and are fully specified from -40°C to 125°C .

7.2 Functional Block Diagrams

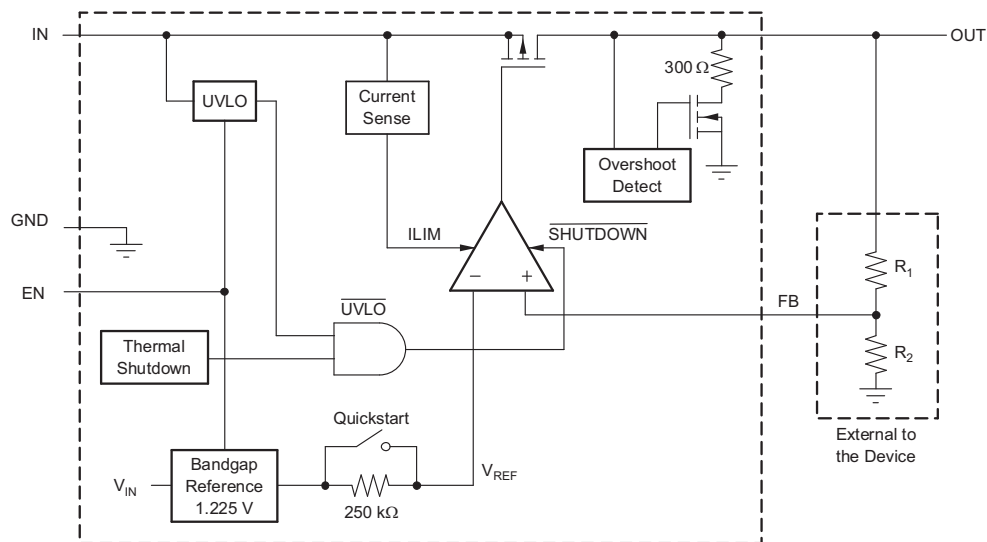


Figure 23. Functional Block Diagram—Adjustable Version

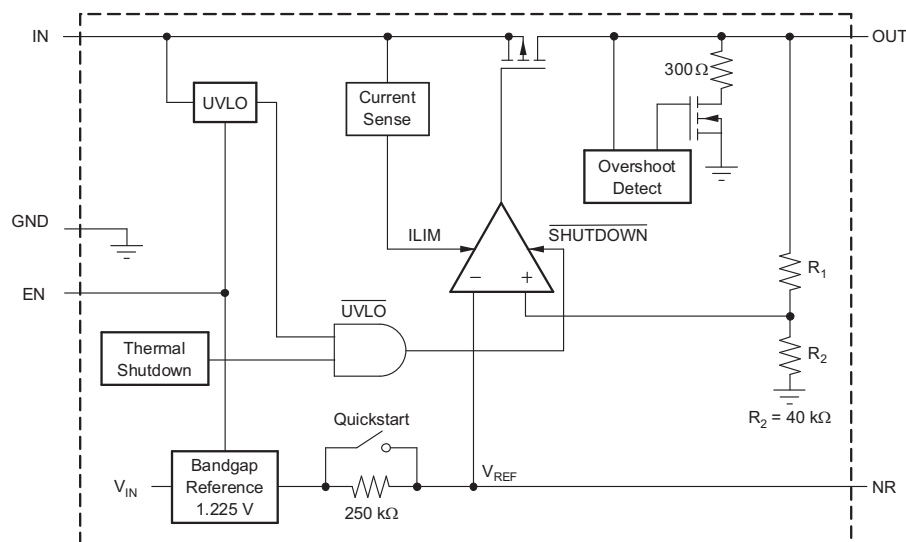


Figure 24. Functional Block Diagram—Fixed Versions

7.3 Feature Description

7.3.1 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

7.3.2 Start-Up

The TPS795 uses a start-up circuit to quickly charge the noise reduction capacitor, C_{NR} , if present (see [Functional Block Diagrams](#)). This circuit allows for the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate for this configuration.

For the fastest start-up, apply V_{IN} first, and then drive the enable pin (EN) high. If EN is tied to IN, start-up is somewhat slower. To ensure that C_{NR} is fully charged during start-up, use a 0.1- μ F or smaller capacitor.

7.3.3 Undervoltage Lockout (UVLO)

The TPS795 uses an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has approximately 100 mV of hysteresis to help reject input voltage drops when the regulator first turns on.

7.3.4 Regulator Protection

The TPS795 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS795 features internal current limiting and thermal protection. During normal operation, the TPS795 limits output current to approximately 2.8 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C (T_{sd}), thermal-protection circuitry shuts it down. Once the device has cooled down to less than approximately 140°C, regulator operation resumes.

7.4 Device Functional Modes

Table 1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Disabled	—	$V_{EN} < V_{EN(LO)}$	—	$T_J > T_{sd}$

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$).
- The enable voltage has previously exceeded the enable rising threshold voltage and not yet decreased below the enable falling threshold.
- The output current is less than the current limit ($I_{OUT} < I_{CL}$).
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{sd}$).

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature ($T_J > T_{sd}$).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS795 family of LDO regulators has been optimized for use in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (265 μ A, typically), and an enable input to reduce supply currents to less than 1 μ A when the regulator is turned off.

8.2 Typical Application

A typical application circuit is shown in [Figure 25](#).

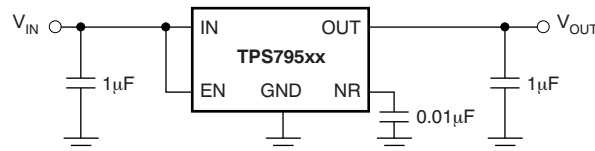


Figure 25. Typical Application Circuit

8.2.1 Design Requirements

[Table 2](#) lists the design requirements.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.3 V
Output voltage	2.5 V
Maximum output current	500 mA

8.2.2 Detailed Design Procedure

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND terminal current, and power the load.

8.2.2.1 Input and Output Capacitor Requirements

Although not required, it is good analog design practice to place a 0.1- μ F to 2.2- μ F capacitor near the input of the regulator to counteract reactive input sources. A higher-value input capacitor may be necessary if large, fast-rise time load transients are anticipated and the device is located several inches from the power source.

Like most low dropout regulators, the TPS795 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitor is 1 μ F. Any 1- μ F or larger ceramic capacitor is suitable.

8.2.2.2 Output Noise

The internal voltage reference is a key source of noise in an LDO regulator. The TPS795 has an NR pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. For the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1 μF to ensure that it is fully charged during the quickstart time provided by the internal switch shown in [Functional Block Diagrams](#).

For example, the TPS79530 exhibits 40 μV_{RMS} of output voltage noise using a 0.1-μF ceramic bypass capacitor and a 10-μF ceramic output capacitor. The output starts up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 250-kΩ resistor and external capacitor.

8.2.2.3 Dropout Voltage

The TPS795 uses a PMOS pass transistor to achieve a low dropout voltage. When $(V_{IN} - V_{OUT})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and $r_{DS(on)}$ of the PMOS pass element is the input-to-output resistance. Because the PMOS device behaves like a resistor in dropout, V_{DO} approximately scales with the output current.

As with any linear regulator, PSRR degrades as $(V_{IN} - V_{OUT})$ approaches dropout. This effect is illustrated in [Figure 9](#) through [Figure 12](#).

8.2.2.4 Programming the TPS79501 Adjustable LDO Regulator

The output voltage of the TPS79501 adjustable regulator is programmed using an external resistor divider as shown in [Figure 26](#).

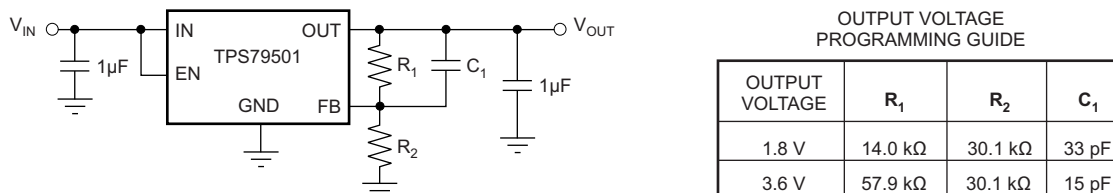


Figure 26. Typical Application, Adjustable Output

The output voltage is calculated using [Equation 1](#).

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2} \right)$$

where

- $V_{REF} = 1.2246$ V typical (the internal reference voltage) (1)

Resistors R_1 and R_2 should be chosen for approximately 40-μA divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values should be avoided, as leakage current at FB increases the output voltage error.

The recommended design procedure is to choose $R_2 = 30.1$ kΩ to set the divider current at 40 μA, $C_1 = 15$ pF for stability, and then calculate R_1 using [Equation 2](#).

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R_2 \quad (2)$$

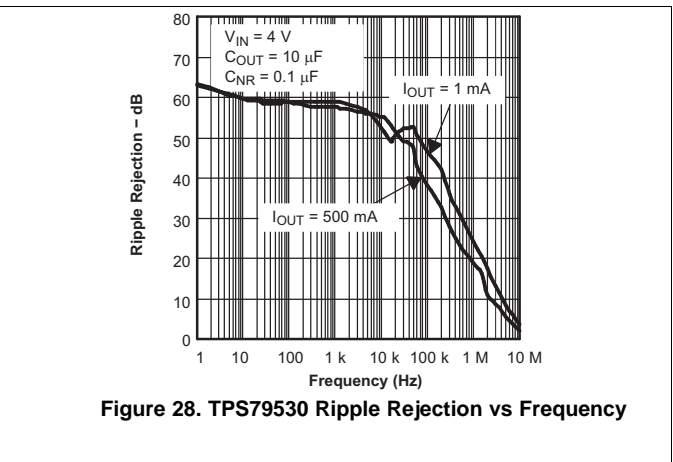
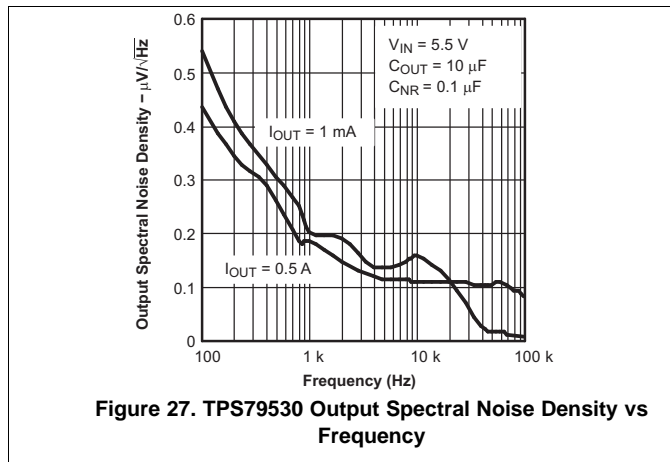
To improve the stability of the adjustable version, TI suggests placing a small compensation capacitor between OUT and FB.

The approximate value of this capacitor can be calculated using [Equation 3](#).

$$C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)} \quad (3)$$

The suggested value of this capacitor for several resistor ratios is shown in the table within [Figure 26](#). If this capacitor is not used (such as in a unity-gain configuration), then the minimum recommended output capacitor is 2.2 μF instead of 1 μF .

8.2.3 Application Curves



8.3 Do's and Don'ts

Place at least one 1- μF ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Connect a 0.1- μF or larger, low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator.

Do not exceed the absolute maximum ratings.

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range from 2.7 V to 5.5 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply is well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendation to Improve PSRR and Noise Performance

To improve AC measurements like PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

10.1.2 Regulator Mounting

The tab of the 6-pin SOT-223 package is electrically connected to ground. For best thermal performance, solder the tab of the surface-mount version directly to a circuit-board copper area. Increasing the copper area improves heat dissipation.

Solder pad footprint recommendations for the devices are presented in application report [SBFA015](#), *Solder Pad Recommendations for Surface-Mount Devices*, available from the TI website (www.ti.com).

10.2 Layout Examples

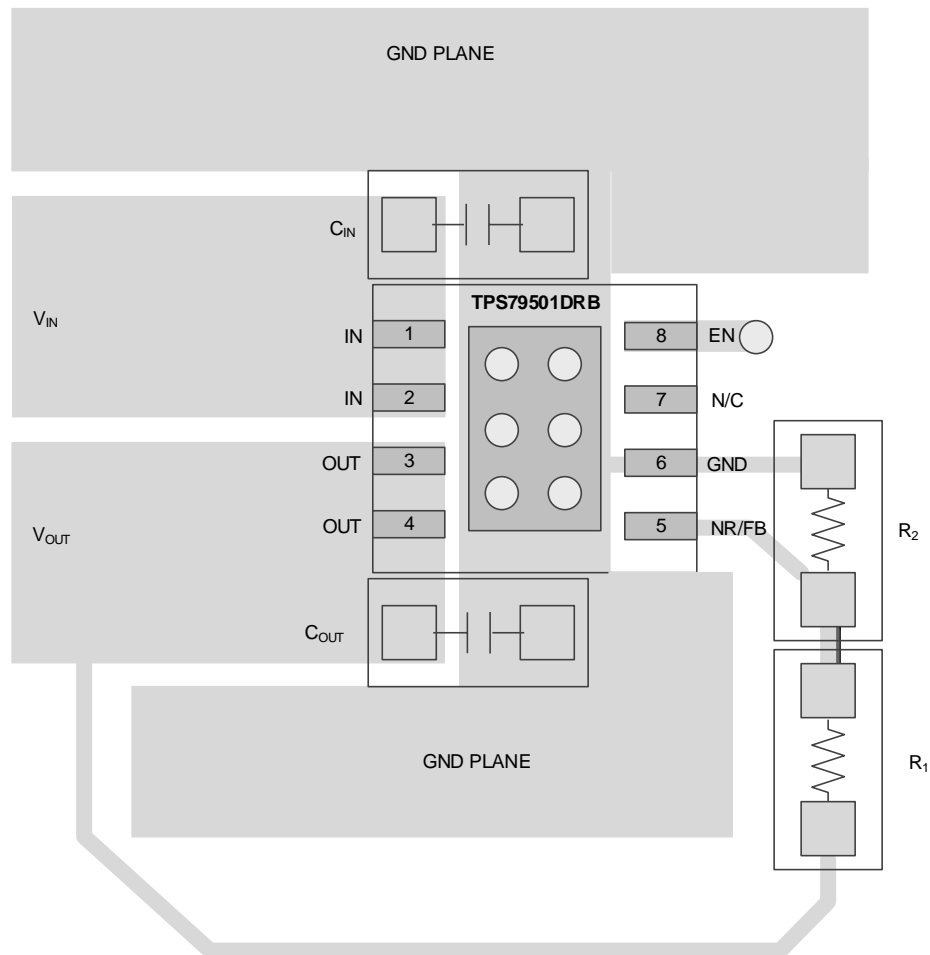


Figure 29. TPS79501 (Adjustable Voltage Version)—Layout Example

Layout Examples (continued)

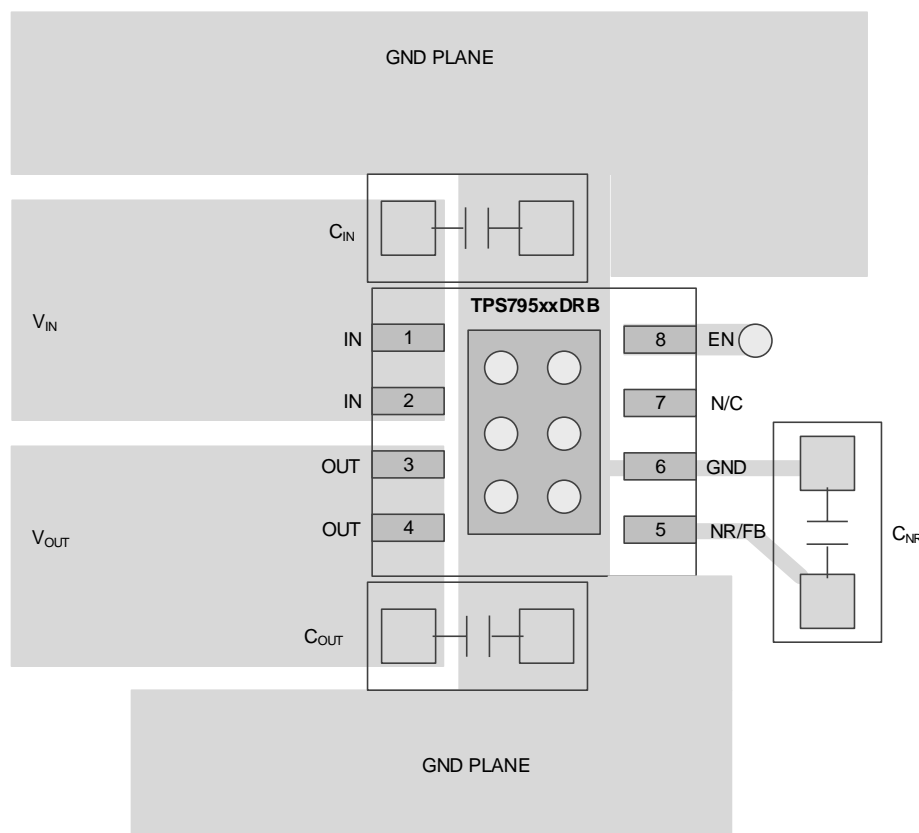


Figure 30. TPS795 (Fixed Voltage Versions)—Layout Example

10.3 Thermal Considerations

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using [Equation 4](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

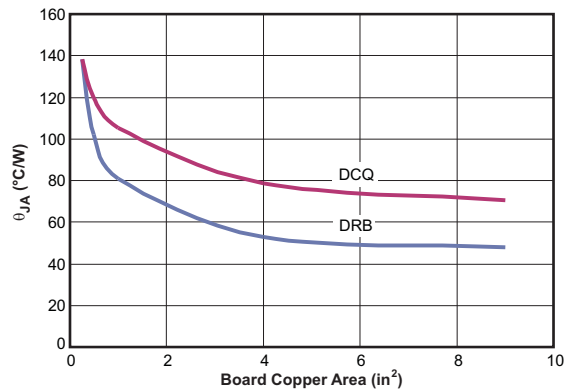
Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the WSON (DRB) package, the primary conduction path for heat is through the exposed pad to the printed-circuit-board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. On the SOT-223 (DCQ) package, the primary conduction path for heat is through the tab to the PCB. The tab should be connected to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using [Equation 5](#):

$$R_{\theta JA} = \frac{(+125^{\circ}\text{C} - T_A)}{P_D} \quad (5)$$

Thermal Considerations (continued)

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using [Figure 31](#).



Note: θ_{JA} value at board size of 9 in.² (that is, 3 in. × 3 in.) is a JEDEC standard.

Figure 31. θ_{JA} vs Board Size

[Figure 31](#) shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effect of heat spreading in the ground plane and should not be used to estimate the thermal performance in real application environments.

NOTE

When the device is mounted on an application PCB, it is strongly recommended to use Ψ_{JT} and Ψ_{JB} , as explained in [Estimating Junction Temperature](#).

10.4 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB} , as shown in [Thermal Information](#), the junction temperature can be estimated with corresponding formulas (given in [Equation 6](#)). For backwards compatibility, an older $\theta_{JC, Top}$ parameter is also listed.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \cdot P_D$$

$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \cdot P_D$$

where

- P_D is the power dissipation shown by [Equation 5](#)
- T_T is the temperature at the center-top of the IC package
- T_B is the PCB temperature measured 1 mm away from the IC package on the PCB surface (see [Figure 33](#)) (6)

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B , see the application note [SBVA025, Using New Thermal Metrics](#), available for download at www.ti.com.

Estimating Junction Temperature (continued)

As shown in Figure 32, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with Equation 6 is a good way to estimate T_J by simply measuring T_T or T_B , regardless of the application board size.

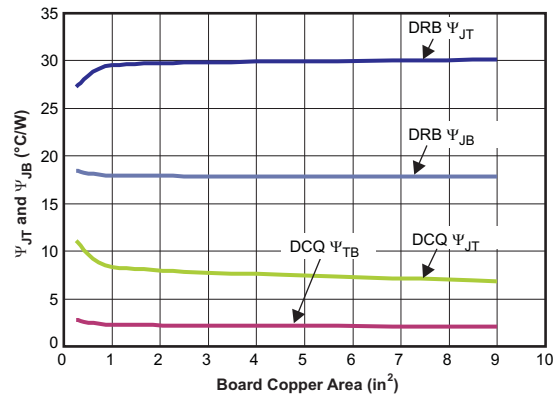


Figure 32. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the application report [SBVA025](#), *Using New Thermal Metrics*, available at [www.ti.com](#).

For further information, see the application report [SPRA953](#), *IC Package Thermal Metrics*, also available on the TI website.

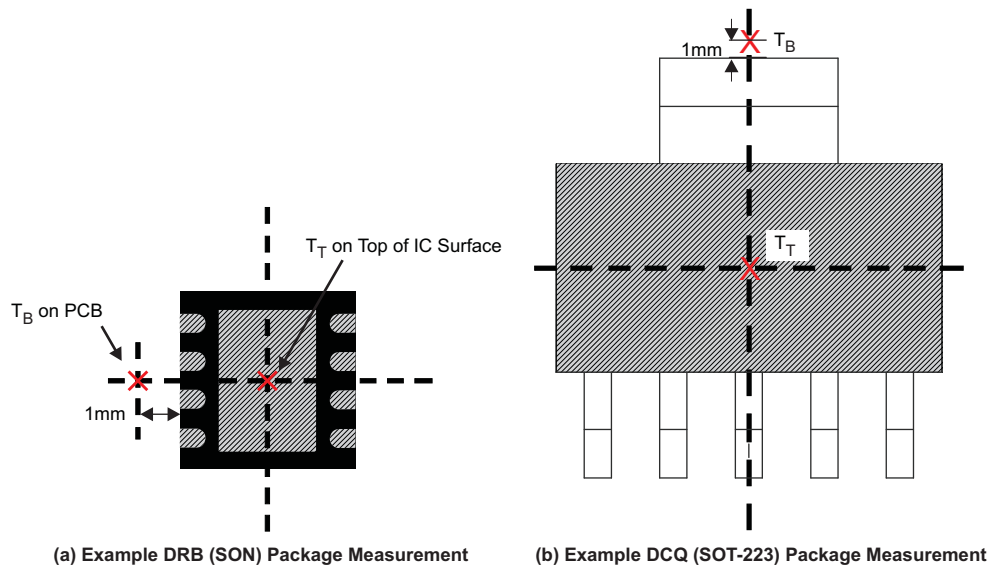


Figure 33. Measuring Point for T_T and T_B

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS795. The [TPS79501DRBEVM evaluation module](#) related (and [user's guide](#)) can be requested at the TI website through the product folders or purchased [directly from the TI eStore](#).

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS795 is available through the product folders under *Tools & Software*.

11.1.2 Device Nomenclature

Table 3. Device Nomenclature⁽¹⁾

PRODUCT	V _{OUT}
TPS795xx(x) yyy z	xx(x) is nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). yyy is package designator. z is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

- *Using New Thermal Metrics*, [SBVA025](#)
- *IC Package Thermal Metrics*, [SPRA953](#)
- *TPS79501DRBEVM User's Guide*, [SBVU016](#)
- *Using New Thermal Metrics*, [SBVA025](#)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

Bluetooth is a registered trademark of Bluetooth SIG, Inc.

All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79501DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	PS79501	Samples
TPS79501DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79501	Samples
TPS79501DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	PS79501	Samples
TPS79501DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUH	Samples
TPS79501DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUH	Samples
TPS79501DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUH	Samples
TPS79501DRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUH	Samples
TPS79516DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79516	Samples
TPS79516DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79516	Samples
TPS79516DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79516	Samples
TPS79516DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79516	Samples
TPS79518DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79518	Samples
TPS79518DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79518	Samples
TPS79518DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79518	Samples
TPS79518DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79518	Samples
TPS79525DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79525	Samples
TPS79525DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79525	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79525DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79525	Samples
TPS79525DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79525	Samples
TPS79530DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79530	Samples
TPS79530DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79530	Samples
TPS79530DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79530	Samples
TPS79533DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	PS79533	Samples
TPS79533DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79533	Samples
TPS79533DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	PS79533	Samples
TPS79533DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79533	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

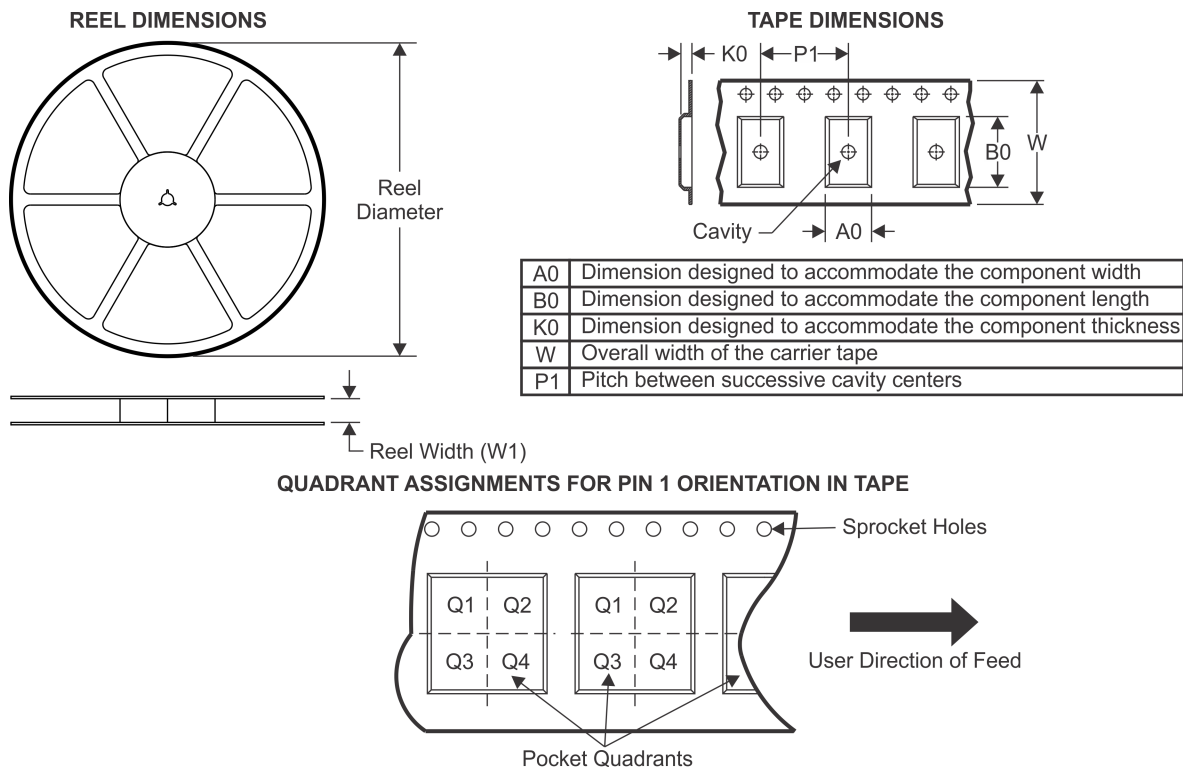
⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79501DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79501DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79501DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79516DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79518DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79525DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79530DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79533DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79533DCQRG4	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS

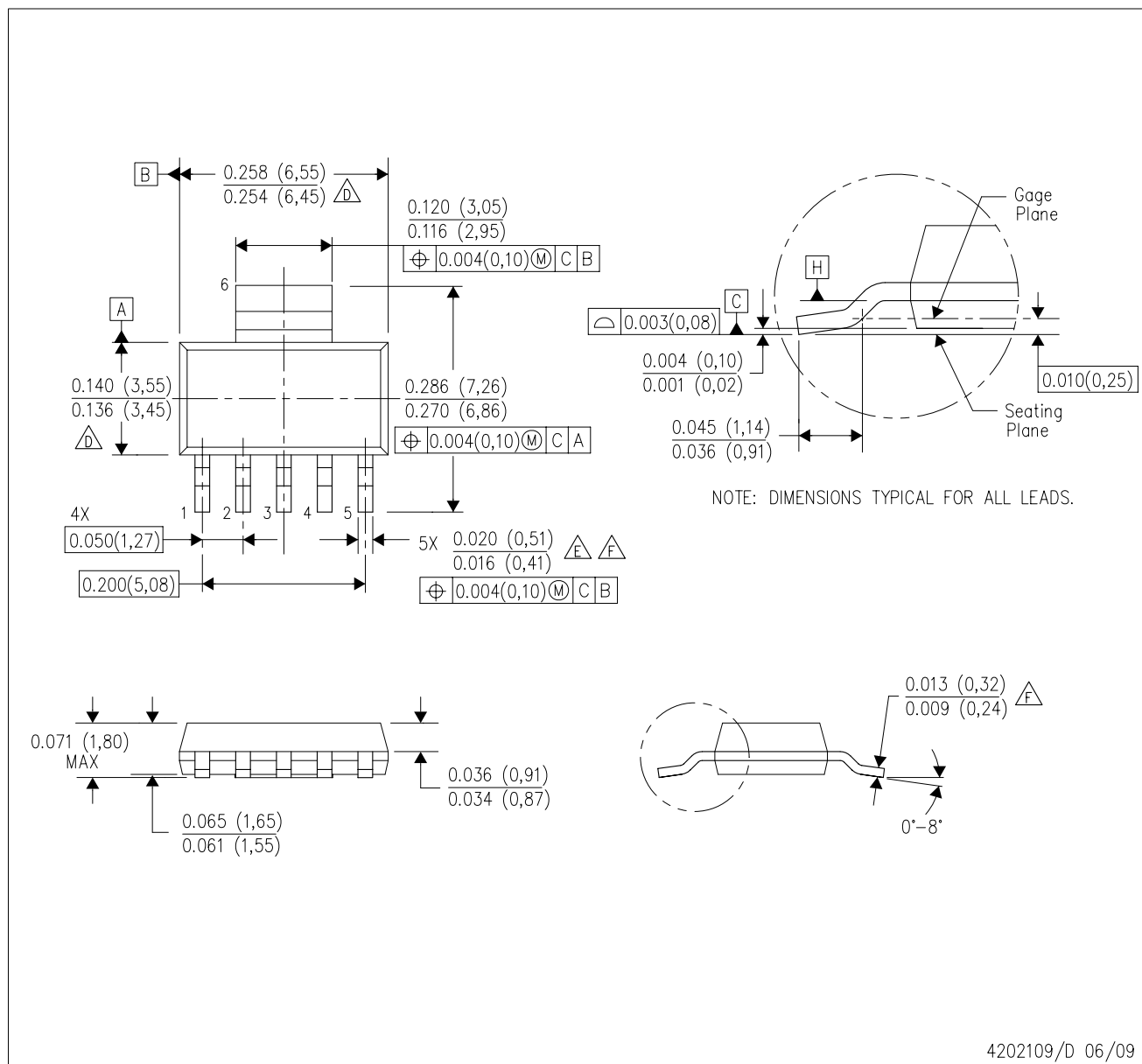


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79501DCQR	SOT-223	DCQ	6	2500	367.0	367.0	35.0
TPS79501DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS79501DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS79516DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS79518DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS79525DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS79530DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS79533DCQR	SOT-223	DCQ	6	2500	367.0	367.0	35.0
TPS79533DCQRG4	SOT-223	DCQ	6	2500	346.0	346.0	29.0

DCQ (R-PDSO-G6)

PLASTIC SMALL-OUTLINE

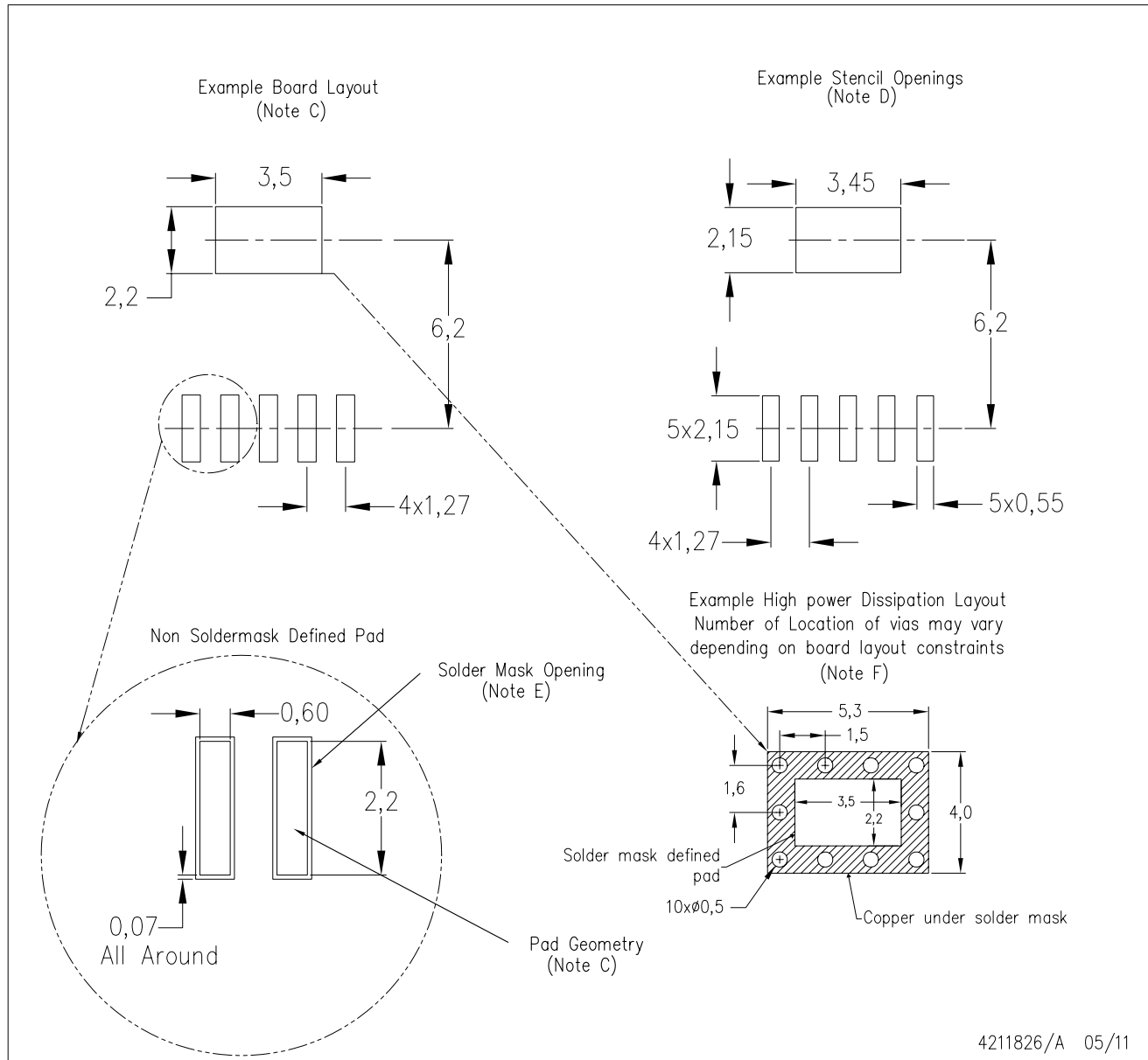


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Controlling dimension in inches.
- Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
- Lead width dimension does not include dambar protrusion.
- Lead width and thickness dimensions apply to solder plated leads.
- G. Interlead flash allow 0.008 inch max.
- H. Gate burr/protrusion max. 0.006 inch.
- I. Datums A and B are to be determined at Datum H.

DCQ (R-PDSO-G6)

PLASTIC SMALL OUTLINE



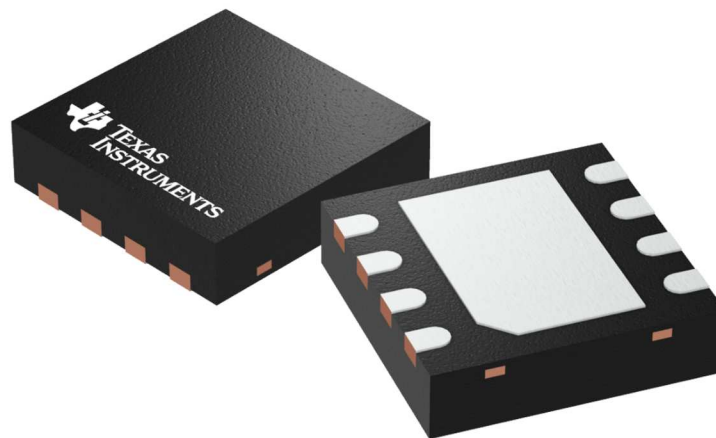
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-SM-782 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
 - Please refer to the product data sheet for specific via and thermal dissipation requirements.

DRB 8

GENERIC PACKAGE VIEW

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



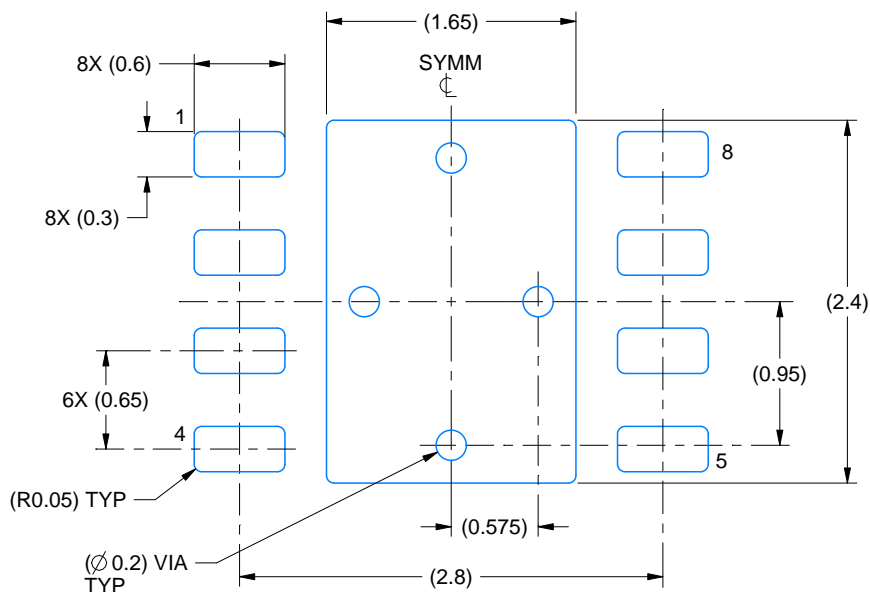
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

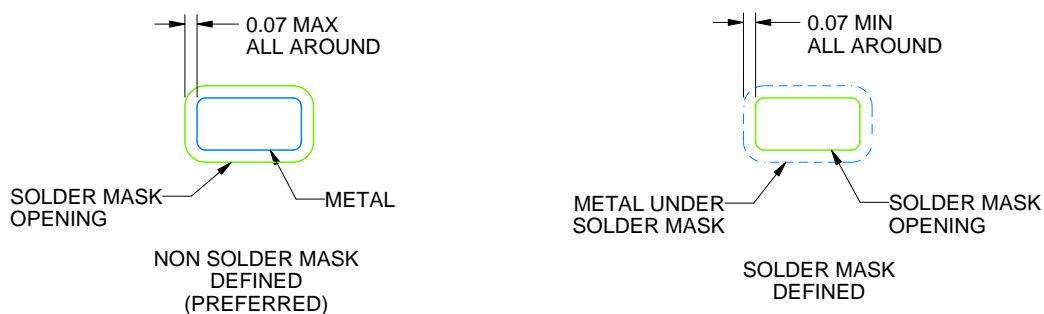
DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

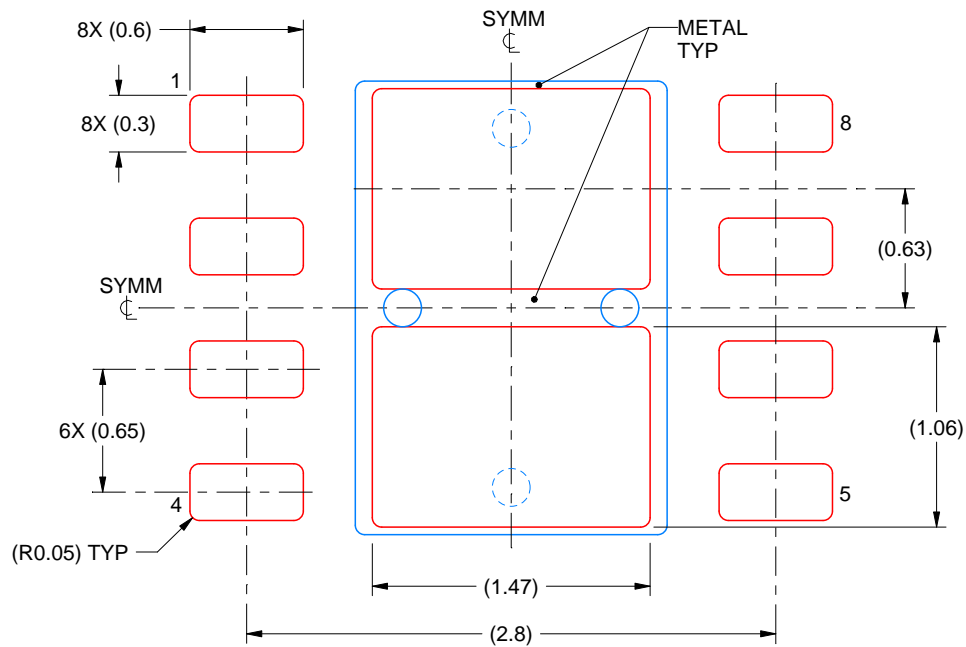
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.