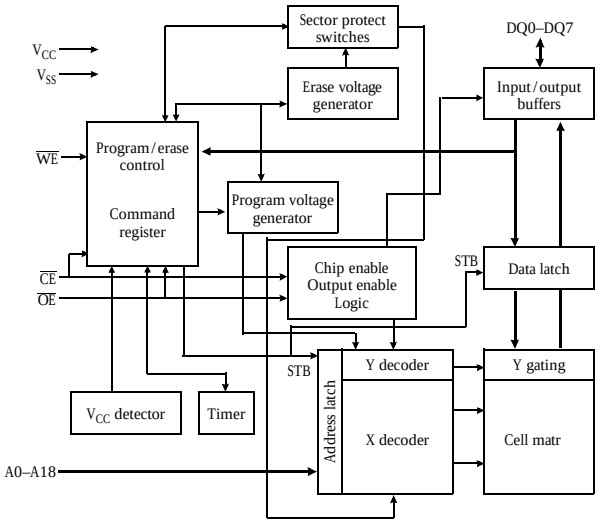
5V 512K×8 CMOS Flash EEPROM

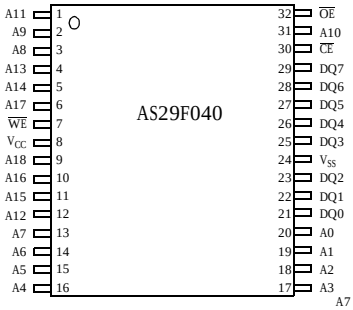
Features

- Organization:512K words × 8 bits
- Industrial and commercial temperature
- Sector architecture
  - Eight 64K byte sectors
  - Erase any combination of sectors or full chip
- Single 5.0±0.5V power supply for read/write operations
- Sector protection
- High speed 55/70/90/120/150 ns address access time
- Automated on-chip programming algorithm
  - Automatically programs/verifies data at specified address
- Automated on-chip erase algorithm
  - Automatically preprograms/erases chip or specified sectors
- 10,000 write/erase cycle endurance
- Low power consumption
  - 30 mA maximum read current
  - 60 mA maximum program current
  - 400 µA typical standby current
- JEDEC standard software, packages and pinouts
  - 32-pin TSOP
  - 32-pin PLCC
- Detection of program/erase cycle completion
  - DQ7 $\overline{\text{DATA}}$ polling
  - DQ6 toggle bit
- Erase suspend/resume
  - Supports reading data from or programming data to a sector not being erased
- Low V_{CC} write lock-out below 2.8V

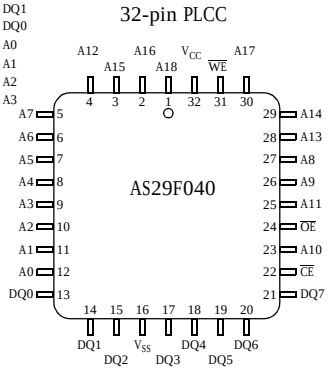
Logic block diagram



Pin arrangement



32-pin TSOP



Selection guide

		AS29F040-55	AS29F040-70	AS29F040-90	AS29F040-120	AS29F040-150	Unit
Maximum access time	t_{AA}	55	70	90	120	150	ns
Maximum chip enable access time	t_{CE}	55	70	90	120	150	ns
Maximum output enable access time	t_{OE}	25	30	35	50	55	ns

Functional description

The AS29F040 is a 4-megabit, 5-volt-only Flash memory device organized as 512K bytes of 8 bits each. For flexible erase an program capability, the 4 megabits of data is divided into eight 64K-byte sectors. The ×8 data appears on DQ0–DQ7. The AS29F040 is offered in JEDEC standard 32-pin TSOP and 32-pin PLCC packages. This device is designed to be programmed an erased in-system with a single 5.0V V_{CC} supply. The device can also be reprogrammed in standard EPROM programmers.

The AS29F040 offers access times of 55/70/90/120/150 ns, allowing 0-wait state operation of high-speed microprocessors. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls

The AS29F040 is fully compatible with the JEDEC single power supply Flash standard. Write commands to the command register use standard microprocessor write timings. An internal state machine uses register contents to control the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Read data operates from the device in the same manner as other Flash or EPROM devices. The program command sequence is used to invoke the automated on-chip programming algorithm that automatically times the program pulse widths and verifies proper cell margin. The erase command sequence is used to invoke the automated on-chip erase algorithm that preprograms the sector if it is not already programmed before executing the erase operation, times the erase pulse widths, and verifies proper cell margin.

Sector erase architecture allows specified sectors of memory to be erased and reprogrammed without altering data in other sectors. A sector typically erases and verifies within 1.0 seconds. Hardware sector protection disables both program and erase operations in any or all combinations of the eight sectors. The device provides true background erase with Erase Suspend, which puts erase operations on hold to either read data from or program data to a sector that is not being erased. The chip erase command will automatically erase all unprotected sectors.

A factory shipped AS29F040 is fully erased (all bits = 1). The programming operation sets bits to 0. Data is programmed into the array one byte at a time in any sequence and across sector boundaries. A sector must be erased to change bits from 0 to 1. Erase returns all bytes in a sector to the erased state (all bits = 1). Each sector is erased individually with no effect on other sectors.

The device features single 5.0V power supply operation for read, write, and erase functions. Internally generated and regulate voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations during power transtitions. $\overline{DATA}$ polling of DQ7 or toggle bit (DQ6) may be used to detect end-of-program or erase operations. The device automatically resets to read mode after program and/or erase operations are completed.

The AS29F040 resists accidental erasure or spurious programming signals resulting from power transitions. Control register architecture permits the alteration of memory contents only after successful completion of specific command sequences. During power up, the device is set to read mode with all program and/or erase commands disabled when V_{CC} is less than V_{LKO} (lockout voltage). The command registers are not affected by noise pulses of less than 5 ns on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$. $\overline{CE}$ and $\overline{WE}$ must be logical zero and $\overline{OE}$ a logical one to initiate write commands.

The AS29F040 uses Fowler-Nordheim tunnelling to electrically erase all bits within a sector simultaneously. Bytes are programme one at a time using the EPROM programming mechanism of hot electron injection.

Operating modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	DQ0-DQ7
ID read MFR code	L	L	H	L	L	L	V_{ID}	Code
ID read device code	L	L	H	H	L	L	V_{ID}	Code
Read	L	L	H	A0	A1	A6	A9	D_{OUT}
Standby	H	X	X	X	X	X	X	High Z
Output disable	L	H	H	X	X	X	X	High Z
Write	L	H	L	A0	A1	A6	A9	D_{IN}
Enable sector protect	L	V_{ID}	Pulse/L	L	H	L	V_{ID}	X
Sector unprotect	L	V_{ID}	Pulse/L	L	H	H	V_{ID}	X
Verify sector protect	L	L	H	L	H	L	V_{ID}	Code

L = Low ($<V_{IL}$); H = High ($>V_{IH}$); V_{ID} = 12.0 ± 0.5V; X = don't car .

Mode definitions

Item	Description
ID MFR code, device code	Selected by A9 = V_{ID}(11.5–12.5V), $\overline{CE}$ = $\overline{OE}$ = A1 = A6 = L, enabling outputs. When A0 is low (V_{IL}) the output data = 52h, a unique Mfr. code for Alliance Semiconductor Flash products. When A0 is high (V_{IH}), D_{OUT} represents the device code for the AS29F040.
Read mode	Selected with $\overline{CE}$ = $\overline{OE}$ = L, $\overline{WE}$ = H. Data is valid in t_{ACC} time after addresses are stable, t_{CE} after $\overline{CE}$ is low and t_{OE} after $\overline{OE}$ is low.
Standby	Selected with $\overline{CE}$ = H. Part is powered down, and I_{CC} reduced to <1.0 mA for TTL input levels and <100 µA for CMOS levels. If activated during an automated on-chip algorithm, the device completes the operation before entering standby.
Output disable	Part remains powered up; but outputs disabled with $\overline{OE}$ pulled high.
Write	Selected with $\overline{CE}$ = $\overline{WE}$ = L, $\overline{OE}$ = H. Accomplish all Flash erasure and programming through the command register. Contents of command register serve as inputs to the internal state machine. Address latching occurs on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs late . Data latching occurs on the rising edge $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Filters on $\overline{WE}$ prevent spurious noise events from appearing as write commands.
Enable sector protect	Hardware protection circuitry implemented with external programming equipment causes the device to disable program and erase operations for specified sectors.
Sector unprotect	Disables sector protection for all sectors using external programming equipment. All sectors must be protected prior to sector unprotection.
Verify sector protect	Verifies write protection for sector. Sectors are protected from program/erase operations on commercial programming equipment. Determine if sector protection exists in a system by writing the ID read command sequence and reading location XXX02h, where address bits A16–18 select the defined sector addresses. A logical 1 on DQ0 indicates a protected sector; a logical 0 indicates an unprotected sector.

Sector architecture and address table

Sector		Equal sector architecture			ID sector address		
		Addresses	Size (Kbytes)		A18	A17	A16
0		00000h–0FFFFh	64		0	0	0
1		10000h–1FFFFh	64		0	0	1
2		20000h–2FFFFh	64		0	1	0
3		30000h–3FFFFh	64		0	1	1
4		40000h–4FFFFh	64		1	0	0
5		50000h–5FFFFh	64		1	0	1
6		60000h–6FFFFh	64		1	1	0
7		70000h–7FFFFh	64		1	1	1

READ codes

Mode	A18–A16	A9	A8–A7	A6	A5–A2	A1	A0	Code on DQ0–DQ7
MFG code (Alliance Semiconductor)	X	V_{ID}	X	L	X	L	L	52h
Device code	X	V_{ID}	X	L	X	L	H	A4h
Sector protection	Sector address	V_{ID}	Sector address	L	Sector address	H	L	01h protected 00h unprotected

L = Low ($<V_{IL}$); H = High ($>V_{IH}$); X = Don't care.

Command format

Command sequence	Required bus cycles	1st bus write cycle		2nd bus write cycle		3rd bus write cycle		4th bus read/write cycle		5th bus write cycle		6th bus write cycle	
		Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Reset/read	1	XXXXh	F0h	Read Address	Read Data								
Reset/read	4	5555h	AAh	2AAAh	55h	5555h	F0h	Read Address	Read Data				
Autoselect ID read	4	5555h	AAh	2AAAh	55h	5555h	90h	00h MFR code	52h				
								01h Device code	A4h				
								XXX02h Sector protection	01 = protected 00 = unprotected				
Program	4	5555h	AAh	2AAAh	55h	5555h	A0h	Program Address	Program Data				
Chip erase	6	5555h	AAh	2AAAh	55h	5555h	80h	5555h	AAh	2AAAh	55h	5555h	10h
Sector erase	6	5555h	AAh	2AAAh	55h	5555h	80h	5555h	AAh	2AAAh	55h	Sector Address	30h
Sector erase suspend	1	XXXXh	B0h										
Sector erase resume	1	XXXXh	30h										

1 Bus operations defined in "Mode definitions," on page 3.
2 Reading from or programming to non-erasing sectors allowed in Erase Suspend mode.
3 Address bit A15 = X = Don't care for all address commands except Program Address.
4 Address bit A16 = X = Don't care for all address commands except Program Address and Sector Address.
5 Address bit A17 = X = Don't care for all address commands except Program Address and Sector Address.
6 Address bit A18 = X = Don't care for all address commands except Program Address and Sector Address.

Command definitions

Item	Description
Reset/read	Initiate read or reset operations by writing the read/reset command sequence into the command register. This allows the microprocessor to retrieve data from the memory. Device remains in read mode until command register contents are altered. Device automatically powers up in read/reset state. This feature allows only reads, therefore ensuring no spurious memory content alterations during power up.
ID read	AS29F040 provides manufacturer and device codes in two ways. External PROM programmers typically access the device codes by driving +12V on A9. AS29F040 also contains an ID read command to read the device code with only +5V, since multiplexing +12V on address lines is generally undesirable. Initiate device ID read by writing the ID read command sequence into the command register. Follow with a read sequence from address XXX00h to return MFG code. Follow ID read command sequence with a read sequence from address XXX01h to return device code. To verify write protect status on sectors, read address XXX02h. Sector addresses A18–A16 produce a1 on DQ0 for protected sector and a 0 for unprotected sector. Exit from ID read mode with Read/Reset command sequence.
Byte/word programming	Programming the AS29F040 is a four bus cycle operation performed on a byte-by-byte basis. Two unlock write cycles precede the program setup command and program data write cycle. Upon execution of the program command, no additional CPU controls or timings are necessary. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever is last; data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever is first. The AS29F040's automated on-chip program algorithm provides adequate internally-generated programming pulses and verifies the programmed cell margin. Check programming status by sampling data on the $\overline{DATA}$ polling (DQ7), or toggle bit (DQ6). The AS29F040 returns the equivalent data that was written to it (as opposed to complemented data), to complete the programming operation. The AS29F040 ignores commands written during the programming operation. AS29F040 allows programming in any sequence, across any sector boundary. Changing data from 0 to 1 requires an erase operation. Attempting to program data 0 to 1 results in DQ5 = 1 (exceeded programming time limits); reading this data after a read/reset operation returns a 0. When programming time limit is exceeded, DQ5 reads high, and DQ6 continues to toggle. In this state , areset command returns the device to read mode.
Chip erase	Chip erase requires six bus cycles: two unlock write cycles; a setup command, two additional unlock write cycles; and finally the Chip erase command. Chip erase does not require logical 0s to be written prior to erasure. When the automated on-chip erase algorithm is invoked with the Chip erase command sequence, AS29F040 automatically programs and verifies the entire memory array for an all-zero pattern prior to erase. The AS29F040 returns to read mode upon completion of chip erase unless DQ5 is set high as a result of exceeding time limit.

Item	Description
Sector erase	Sector erase requires six bus cycles: two unlock write cycles, a setup command, two additional unlock write cycles, and finally the sector erase command. Identify the sector to be erased by addressing any location in the sector. The address is latched on the falling edge of $\overline{WE}$; the command, 30h, is latched on the rising edge of $\overline{WE}$. The sector erase operation begins after a 80 µs time-out. To erase multiple sectors, write the sector erase command to each of the addresses of sectors to erase after following the six bus cycle operation above. Timing between writes of additional sectors must be <80 µs, or the AS29F040 ignores the command and erasure begins. During the erase time-out period any falling edge of $\overline{WE}$ resets the time-out. Any command (other than sector erase or erase suspend) during the time-out period resets the AS29F040 to read mode, and the device ignores the sector erase command string. Erase such ignored sectors by restarting the sector erase command on the ignored sectors. The entire array need not be written with 0s prior to erasure. AS29F040 writes 0s to the entire sector prior to electrical erase; writing of 0s affects only selected sectors, leaving non-selected sectors unaffected. AS29F040 requires no CPU control or timing signals during sector erase operations. Automatic sector erase begins after erase time-out from the last rising edge of $\overline{WE}$ from the sector erase command stream and ends when the $\overline{DATA}$ polling (DQ7) is logical 1. $\overline{DATA}$ polling must be performed on addresses that fall within the sectors being erased. AS29F040 returns to read mode after sector erase unless DQ5 is set high by exceeding the time limit.
Erase suspend	Erase suspend allows interruption of sector erase operations to perform data reads from or writes to a sector not being erased. Erase suspend applies only during sector erase operations, including the time-out period. Writing an erase suspend command during sector erase time-out results in immediate termination of the time-out period and suspension of erase operation. AS29F040 ignores any commands during erase suspend other than read/reset, program, or erase resume commands. Writing the Erase Resume command continues erase operations. Addresses are DON'T CARE when writing Erase suspend or Erase resume commands. AS29F040 takes 0.2–15 µs to suspend erase operations after receiving erase suspend command. To determine completion of erase suspend, check DQ6 after selecting an address of a sector not being erased. Check DQ2 in conjunction with DQ6 to determine if a sector is being erased. AS29F040 ignores redundant writes of erase suspend. While in erase-suspend mode AS29F040 allows reading data (erase-suspend-read mode) from or programming data (erase-suspend-program mode) to any sector not undergoing sector erase, treated as standard read or standard programming mode. AS29F040 defaults to erase-suspend-read mode while an erase operation has been suspended. Write the resume command 30h to continue operation of sector erase. AS29F040 ignores redundant writes of the resume command. AS29F040 permits multiple suspend/resume operations during sector erase.
Sector protect	When attempting to write to a protected sector, $\overline{DATA}$ polling andToggle Bit 1 (DQ6) are activated for about <1 µs. When attempting to erase a protected sector, $\overline{DATA}$ polling andToggle Bit 1 (DQ6) are activated for about <5 µs. In both cases, the device returns to read mode without altering the specified sectors.

Status operations

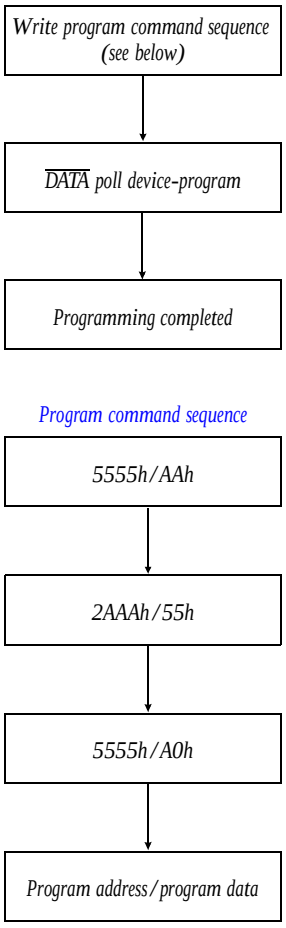
$\overline{\text{DATA}}$ polling (DQ7)	Only active during automated on-chip algorithms or sector erase time outs. DQ7 reflects complement of data last written when read during the automated on-chip algorithm (0 during erase algorithm); reflects true data when read after completion of an automated on-chip algorithm (1 after completion of erase agorithm).
Toggle bit 1 (DQ6)	Active during automated on-chip algorithms or sector time outs. DQ6 toggles when $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggles, or an Erase Resume command is invoked. When the automated on-chip algorithm is complete, DQ6 stops toggling and valid data can be read. DQ6 is valid after the rising edge of the fourth pulse of $\overline{\text{WE}}$ during programming; after the rising edge of the sixth $\overline{\text{WE}}$ pulse during chip erase; after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse for sector erase. For protected sectors, DQ6 toggles for <1 µs during writes, and <5 µs during erase (if all selected sectors are protected).
Exceeding time limit (DQ5)	Indicates unsuccessful completion of program/erase operation (DQ5 = 1). $\overline{\text{DATA}}$ polling remains active; $\overline{\text{CE}}$ powers the device down to 2 mA. If DQ5 = 1 during chip erase, all or some sectors are defective; during sector erase, the sector is defective (in this case, reset the device and execute a program or erase command sequence to continue working with functional sectors); during byte programming, that particular byte is defective. Attempting to program 0 to 1 will set DQ5 = 1.
Sector erase timer (DQ3)	Checks whether sector erase timer window is open. If DQ3 = 1, erase is in progress; no commands will be accepted. If DQ3 = 0, the device will accept additional sector erase commands. Check DQ3 before and after each Sector Erase command to verify that the command was accepted.
Toggle bit 2 (DQ2)	During sector erase, DQ2 toggles with $\overline{\text{OE}}$ or $\overline{\text{CE}}$ only during an attempt to read a sector being erased. During chip erase, DQ2 toggles with $\overline{\text{OE}}$ or $\overline{\text{CE}}$ for all addresses. If DQ5 = 1, DQ2 toggles only at sector addresses where failure occurred, and will not toggle at other sector addresses. Use DQ2 in conjunction with DQ6 to determine whether device is in auto erase or erase suspend mode.

Write operation status

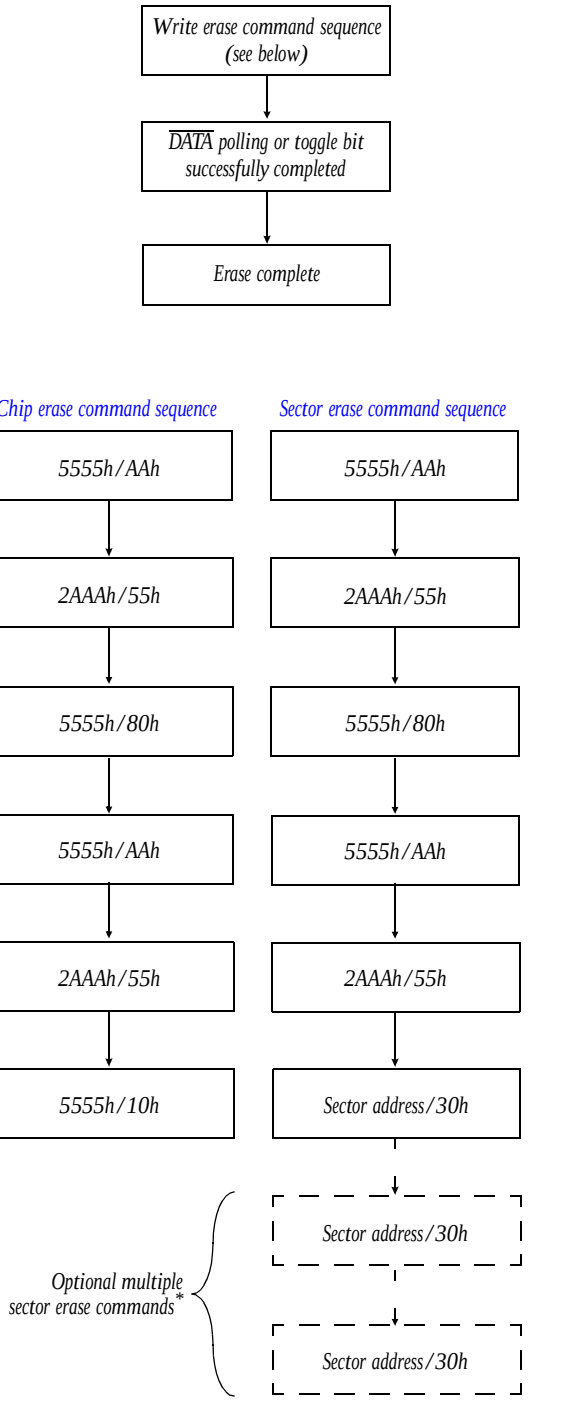
	Status		DQ7	DQ6	DQ5	DQ3	DQ2
In progress	Auto programming (byte)		$\overline{\text{DQ}}$7	Toggle	0	0	No toggle
	Program/erase in auto erase		0	Toggle	0	1	Toggle*
	Erase suspend mode	Read erasing sector	1	No toggle	0	0	Toggle
		Read non-erasing sector	Data	Data	Data	Data	Data
		Program in erase suspend	$\overline{\text{DQ}}$7	Toggle	0	0	Toggle*
Exceeded time limits	Auto programming (byte)		$\overline{\text{DQ}}$7	Toggle	1	0	No toggle
	Program/erase in auto erase		0	Toggle	1	1	Toggle†
	Program in erase suspend		$\overline{\text{DQ}}$7	Toggle	1	0	No toggle†

* Toggles with $\overline{\text{OE}}$ or $\overline{\text{CE}}$ only for erasing or erase suspended sector addresses.
† Toggles with $\overline{\text{OE}}$ or $\overline{\text{CE}}$ only for erasing or erase suspended sector addresses.

Automated on-chip programming algorithm for each byte

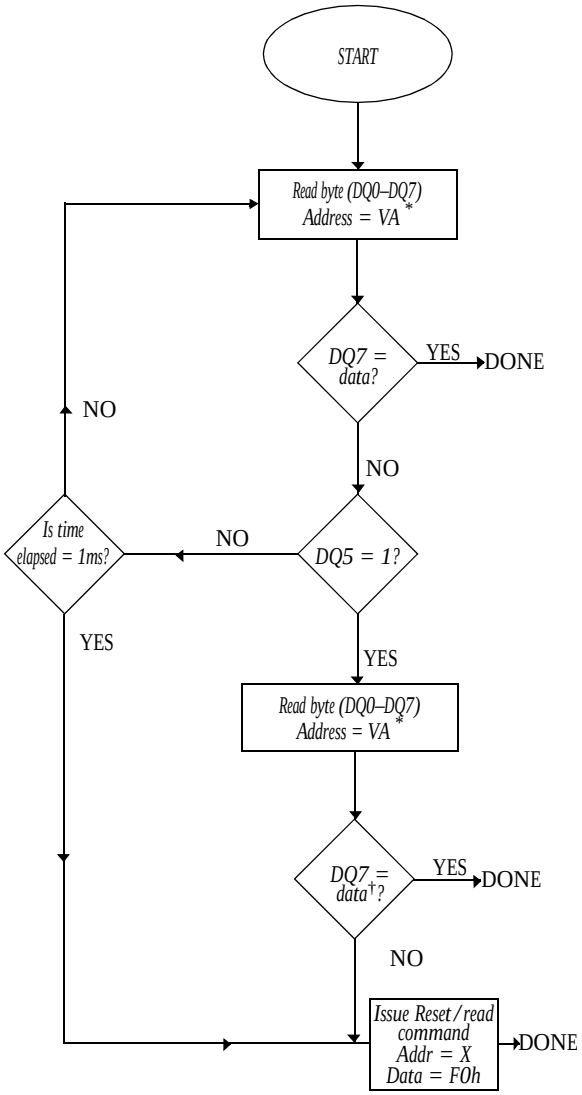


Automated on-chip erase algorithm



* The system software should check the status of DQ3 prior to and following each subsequent sector erase command to ensure command completion. The device may not have accepted the command if DQ3 is high on second status check.

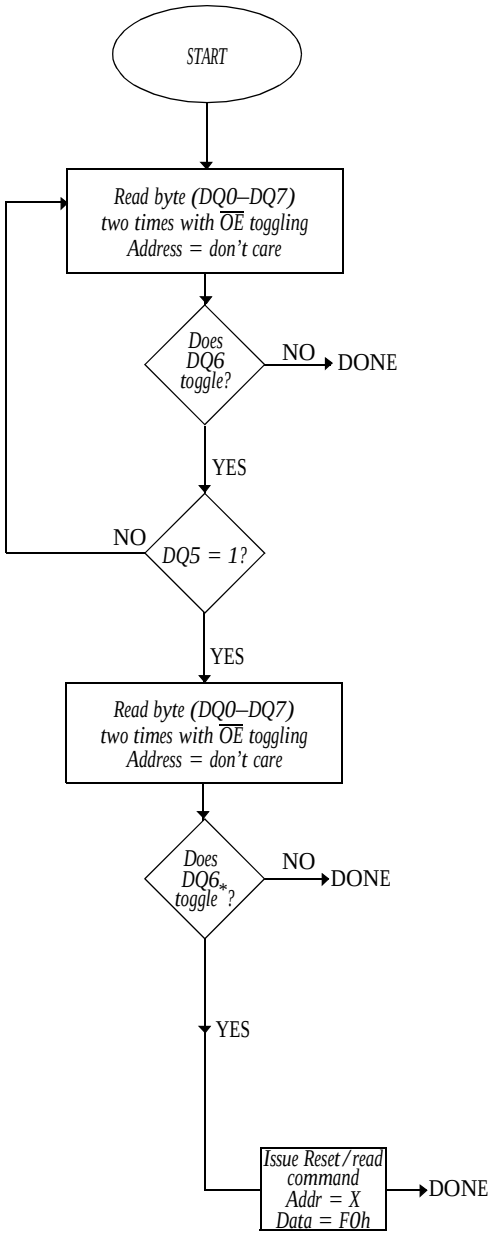
DATA polling algorithm



* VA = Byte address for programming. VA = any of the sector addresses within the sector being erased during sector erase. VA = valid address equals any non-protected sector group address during chip erase.

† DQ7 rechecked even if DQ5 = 1 because DQ5 and DQ7 may not change simultaneously.

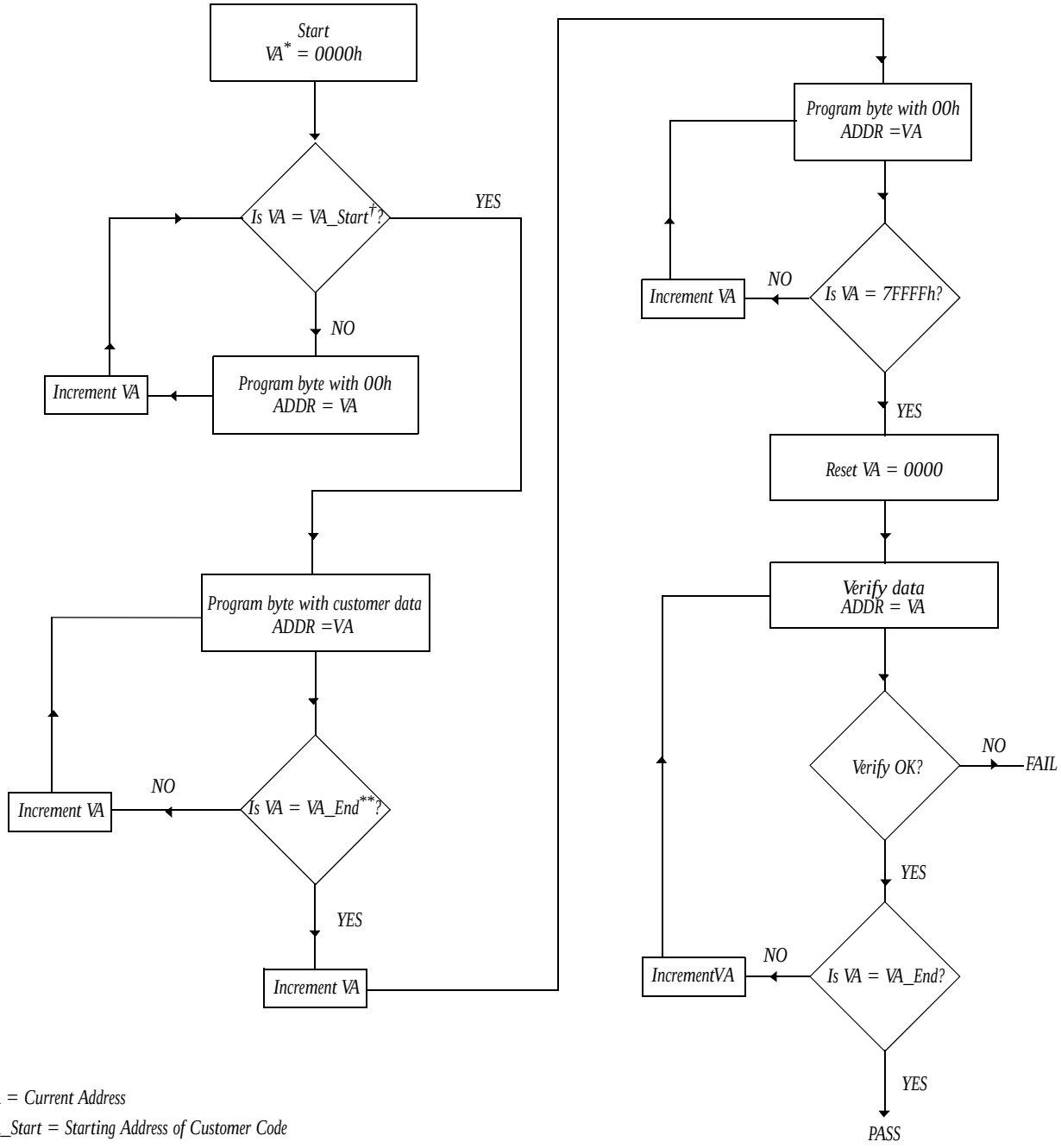
Toggle bit algorithm



* DQ6 rechecked even if DQ5 = 1 because DQ6 may stop toggling when DQ5 changes to 1.

FLASH

Programming algorithm for chip



* VA = Current Address

† VA_Start = Starting Address of Customer Code

** VA_End = Ending Address of Customer Code

DC electrical characteristics

V_{CC} = 5.0±0.5V

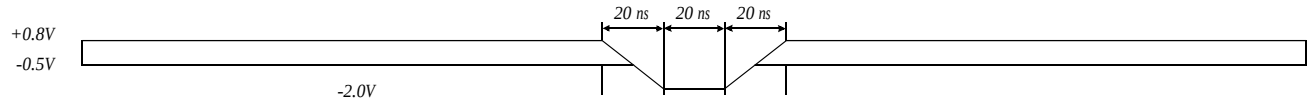
Parameter	Symbol	Test conditions	Min	Max	Unit
Input load current	I_{LI}	V_{IN} = V_{SS} to V_{CC}, V_{CC} = $V_{CC\ MAX}$	-	±1	µA
A9 Input load current	I_{LIT}	V_{CC} = $V_{CC\ MAX}$, A9 = 12.5V		90	µA
Output leakage current	I_{LO}	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = $V_{CC\ MAX}$	-	±1	µA
Output short circuit current*	I_{OS}	V_{OUT} = 0.5V	-	200	mA
Active current, read @ 6MHz†	I_{CC}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	-	30	mA
Active current, program/erase**	I_{CC2}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	-	60	mA
Standby current (TTL)	I_{SB1}	$\overline{CE}$ = $\overline{OE}$ = V_{IH}, V_{CC} = $V_{CC\ MAX}$	-	1.0	mA
Standby current (CMOS)	I_{SB2}	$\overline{CE}$ = V_{CC} + 0.5V, $\overline{OE}$ = V_{IH}, V_{CC} = $V_{CC\ MAX}$	-	400	µA
Input low voltage	V_{IL}		-0.5	0.8	V
Input high voltage	V_{IH}		2.0	V_{CC} + 0.5	V
Output low voltage	V_{OL}	I_{OL} = 12mA, V_{CC} = $V_{CC\ MIN}$	-	0.45	V
Output high voltage	V_{OH1}	I_{OH} = -2.5 mA, V_{CC} = $V_{CC\ MIN}$	2.4	-	V
	V_{OH2}	I_{OH} = -100 µA, V_{CC} = $V_{CC\ MIN}$	V_{CC} - 0.4	-	V
Low V_{CC} lock out voltage	V_{LKO}		2.8	4.2	V
Input HV select voltage	V_{ID}		11.5	12.5	V

* Not more than one output tested simultaneously. Duration of the short circuit must not be >1 second. $_{OUT}$ = 0.5V was selected to avoid test problems caused by tester ground degradation. (This parameter is sampled and not 100% tested, but guaranteed by characterization.)

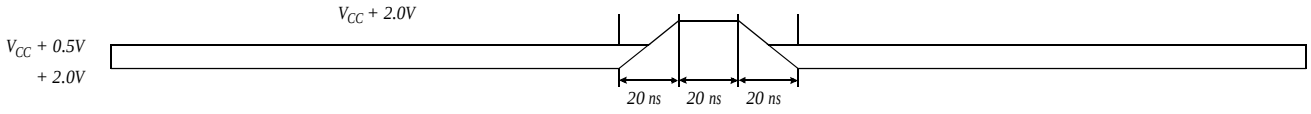
† The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 6 MHz). The frequency component typically is less than 2 mA/MHz with $\overline{OE}$ at V_{IH}.

** I_{CC} active while program or erase operations are in progress.

Maximum negative overshoot waveform



Maximum positive overshoot waveform



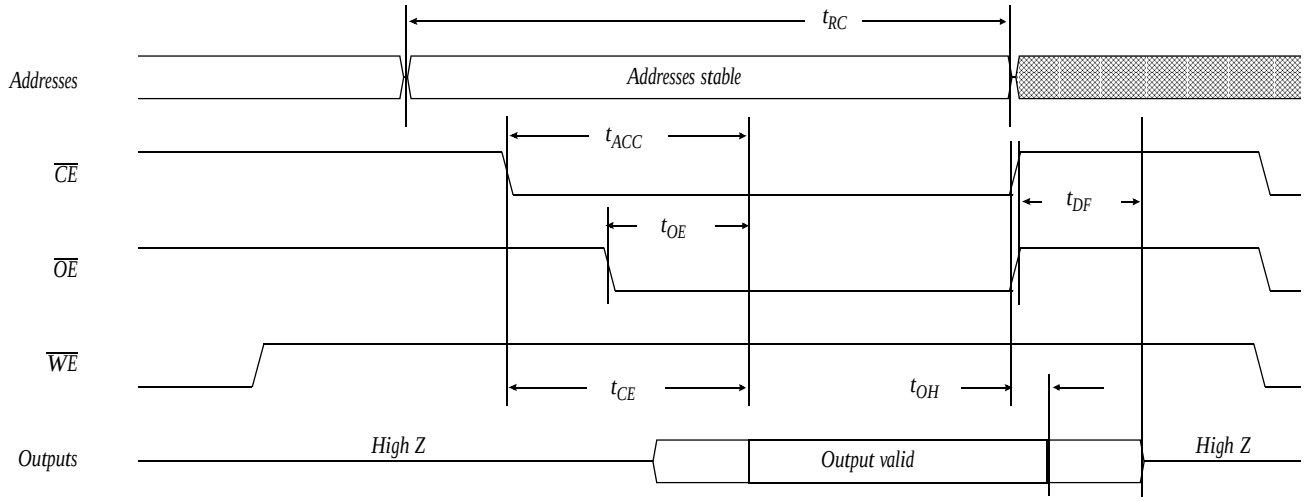
AC parameters: read cycle

JEDEC Symbol	Std Symbol	Parameter	-55		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read cycle time	55	-	70	-	90	-	120	-	150	-	ns
t_{AVQV}	t_{ACC}	Address to output delay	-	55	-	70	-	90	-	120	-	150	ns
t_{ELQV}	t_{CE}	Chip enable to output	-	55	-	70	-	90	-	120	-	150	ns
t_{GLQV}	t_{OE}	Output enable to output	-	25	-	30	-	35	-	50	-	55	ns
t_{EHQZ}	t_{DF}	Chip enable to output High Z	-	15	-	20	-	20	-	30	-	35	ns
t_{GHQZ}	t_{DF}	Output enable to output High Z	-	15	-	20	-	20	-	30	-	35	ns
t_{AXQX}	t_{OH}	Output hold time from addresses, $\overline{CE}$ or $\overline{OE}$, whichever occurs first	0	-	0	-	0	-	0	-	0	-	ns

Key to switching waveforms

Rising input Falling input Undefined / don't care

Read waveform



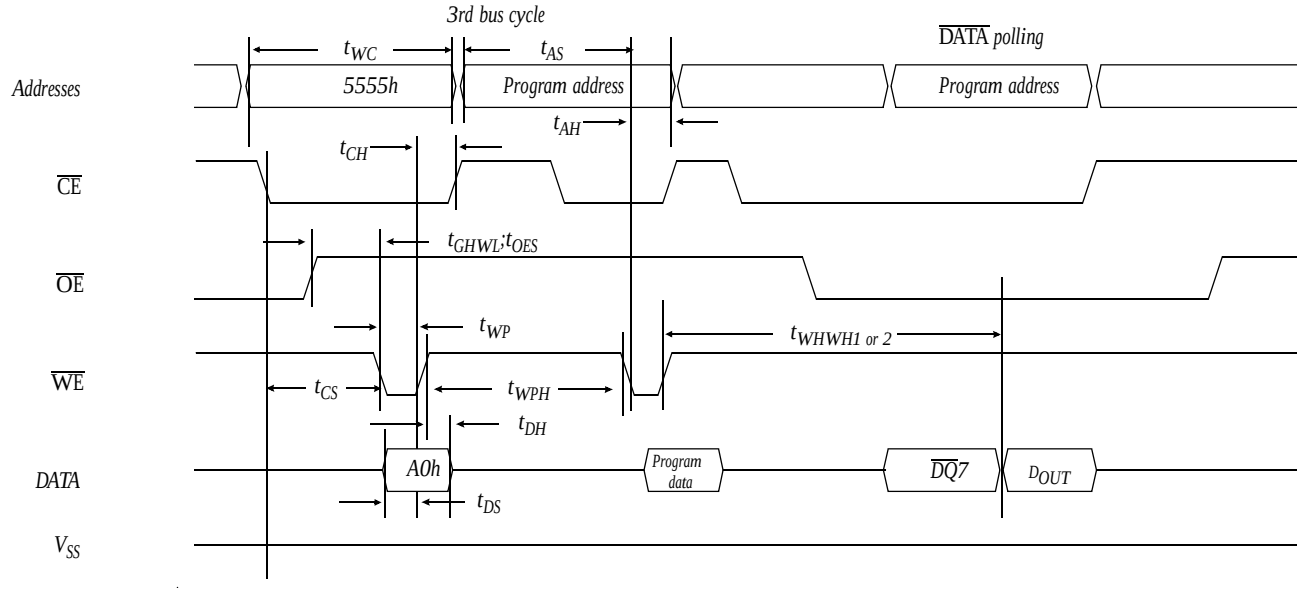
AC parameters — write cycle

$\overline{WE}$ controlled

JEDEC Symbol	Std Symbol	Parameter	-55		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write cycle time	55	-	70	-	90	-	120	-	150	-	ns
t_{AVWL}	t_{AS}	Address setup time	0	-	0	-	0	-	0	-	0	-	ns
t_{WLAX}	t_{AH}	Address hold time	40	-	45	-	45	-	50	-	50	-	ns
t_{DVWH}	t_{DS}	Data setup time	25	-	30	-	45	-	50	-	50	-	ns
t_{WHDX}	t_{DH}	Data hold time	0	-	0	-	0	-	0	-	0	-	ns
	t_{OES}	Output enable setup time	0	-	0	-	0	-	0	-	0	-	ns
	t_{OEH}	Output enable hold time: Toggle and $\overline{DATA}$ polling	10	-	10	-	10	-	10	-	10	-	ns
t_{GHWL}	t_{GHWL}	Read recover time before write	0	-	0	-	0	-	0	-	0	-	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ setup time	0	-	0	-	0	-	0	-	0	-	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ hold time	0	-	0	-	0	-	0	-	0	-	ns
t_{WLWH}	t_{WP}	Write pulse width	35	-	35	-	45	-	50	-	50	-	ns
t_{WHWL}	t_{WPH}	Write pulse width high	20	-	20	-	20	-	20	-	20	-	ns
t_{WHWH1}	t_{WHWH1}	Programming pulse time	15	-	15	-	15	-	15	-	15	-	µs
t_{WHWH2}	t_{WHWH2}	Erase operation	0.3	-	0.3	-	0.3	-	0.3	-	0.3	-	sec

Write waveform

$\overline{WE}$ controlled



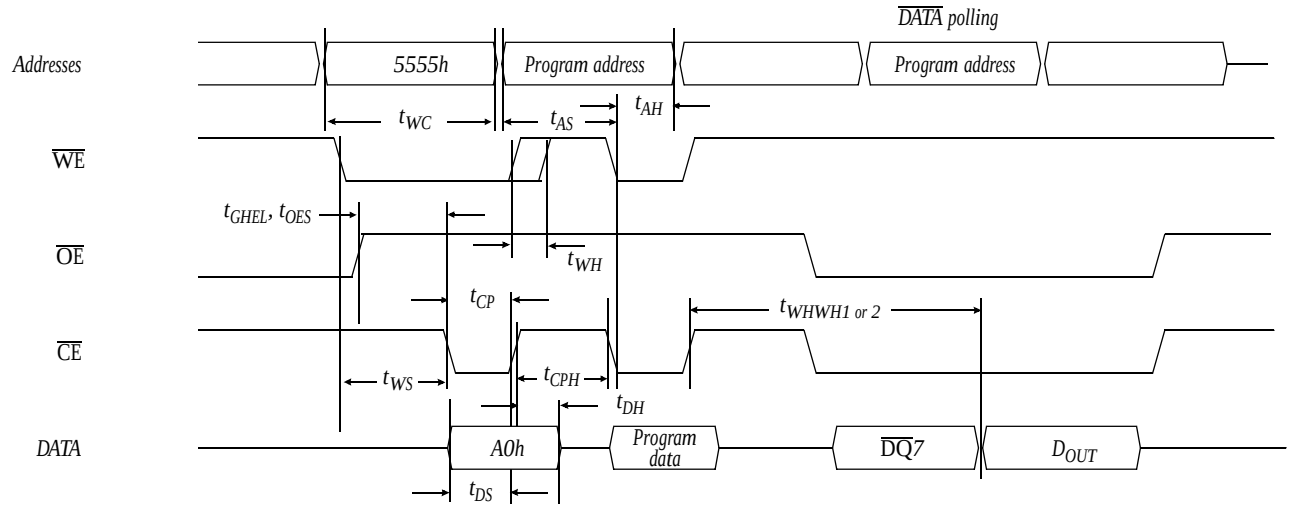
AC parameters—write cycle 2

$\overline{CE}$ controlled

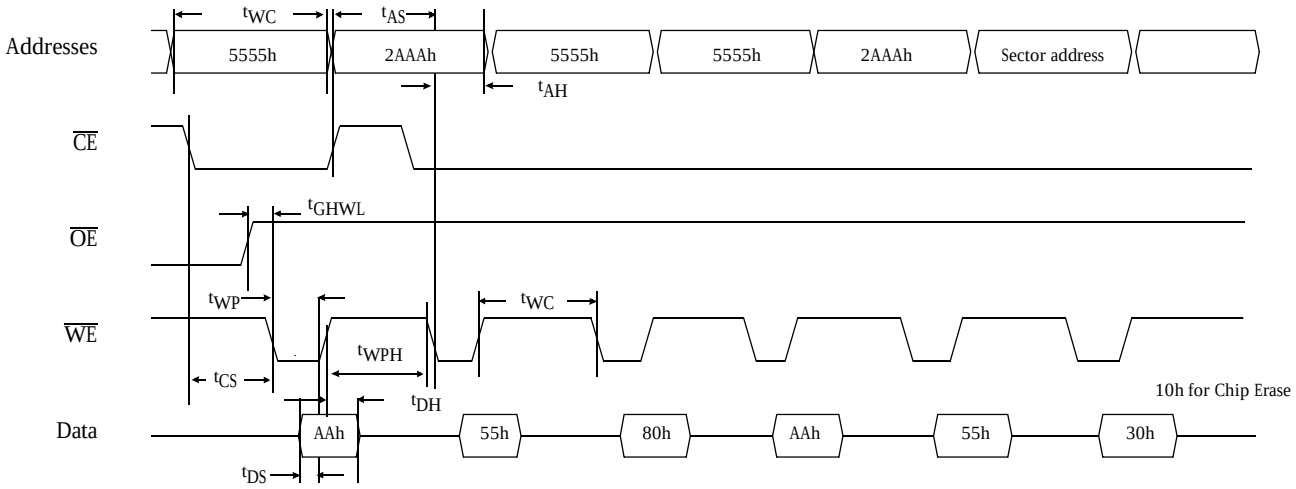
JEDEC Symbol	Std Symbol	Parameter	-55		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write cycle time	55	-	70	-	90	-	120	-	150	-	ns
t_{AVEL}	t_{AS}	Address setup time	0	-	0	-	0	-	0	-	0	-	ns
t_{ELAX}	t_{AH}	Address hold time	40	-	45	-	45	-	50	-	50	-	ns
t_{DVEH}	t_{DS}	Data setup time	25	-	30	-	45	-	50	-	50	-	ns
t_{EHDX}	t_{DH}	Data hold time	0	-	0	-	0	-	0	-	0	-	ns
	t_{OES}	Output enable setup time	0	-	0	-	0	-	0	-	0	-	ns
	t_{OEH}	Output enable hold time: Toggle and DATA polling	10	-	10	-	10	-	10	-	10	-	ns
t_{GHEL}	t_{GHEL}	Read recover time before write	0	-	0	-	0	-	0	-	0	-	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ setup time	0	-	0	-	0	-	0	-	0	-	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ hold time	0	-	0	-	0	-	0	-	0	-	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ pulse width	35	-	35	-	45	-	50	-	50	-	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ pulse width high	20	-	20	-	20	-	20	-	20	-	ns
t_{WHWH1}	t_{WHWH1}	Programming pulse time	15	-	15	-	15	-	15	-	15	-	µs
t_{WHWH2}	t_{WHWH2}	Erase operation	0.3	-	0.3	-	0.3	-	0.3	-	0.3	-	sec

Write waveform 2

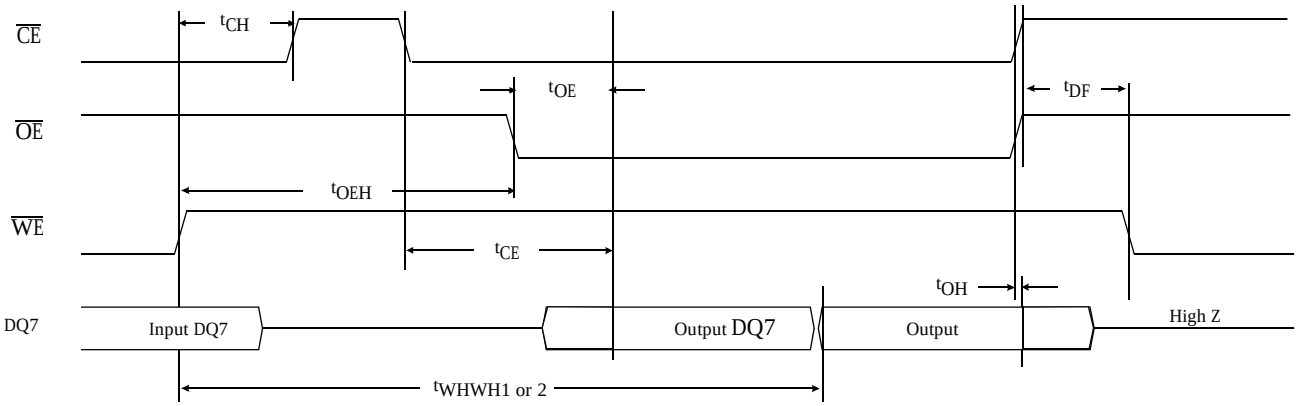
$\overline{CE}$ controlled



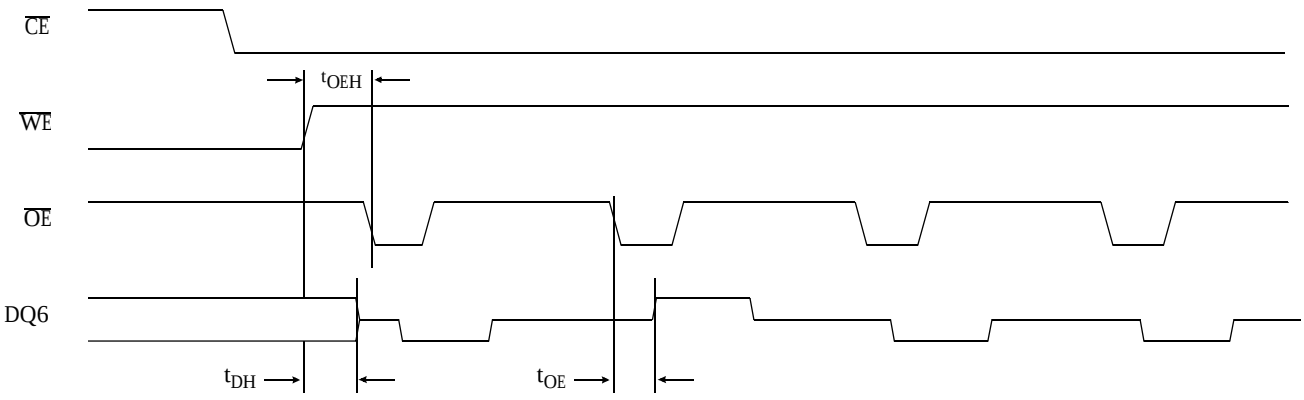
Erase waveform



DATA polling waveform



Toggle bit waveform



Erase and programming performance

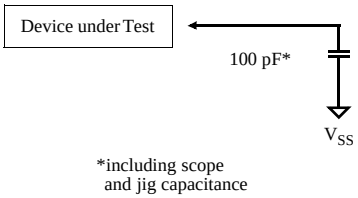
Parameter	Limits			Unit
	Min	Typical	Max	
Sector erase and verify-1 time (excludes 00h programming prior to erase)	-	1.0	-	sec
Byte program time	-	45	-	µs
Chip programming time	-	23	-	sec
Erase/program cycles	-	-	10,000	cycles

Latchup tolerance

Parameter	Min	Max	Unit
Input voltage with respect to V_{SS} on A9 and $\overline{OE}$	-1.0	+13.0	V
Input voltage with respect to V_{SS} on all DQ, address and control pins	-1.0	V_{CC}+1.0	V
Current	-100	+100	mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0V, one pin at a time.

AC test conditions



Test condition			Unit
Output load	1 TTL gate		
Input rise and fall times	5		ns
Input pulse levels	0.0-3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Input voltage (Input or DQ pin)	V_{IN}	–2.0	+7.0	V
Input voltage (A9 pin, $\overline{OE}$)	V_{IN}	–2.0	+13.0	V
Power supply voltage	V_{CC}	-0.5	+5.5	V
Operating temperature	T_{OPR}	–55	+125	°C
Storage temperature (plastic)	T_{STG}	–65	+125	°C
Short circuit output current	I_{OUT}	-	200	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0V, one pin at a time.

Recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	+4.5	5.0	+5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.0	-	V_{CC} + 0.5	V
	V_{IL}	–0.5	-	0.8	V

TSOP pin capacitance

Symbol	Parameter	Test setup	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control pin capacitance	V_{IN} = 0	7.5	9	pF

PLCC pin capacitance

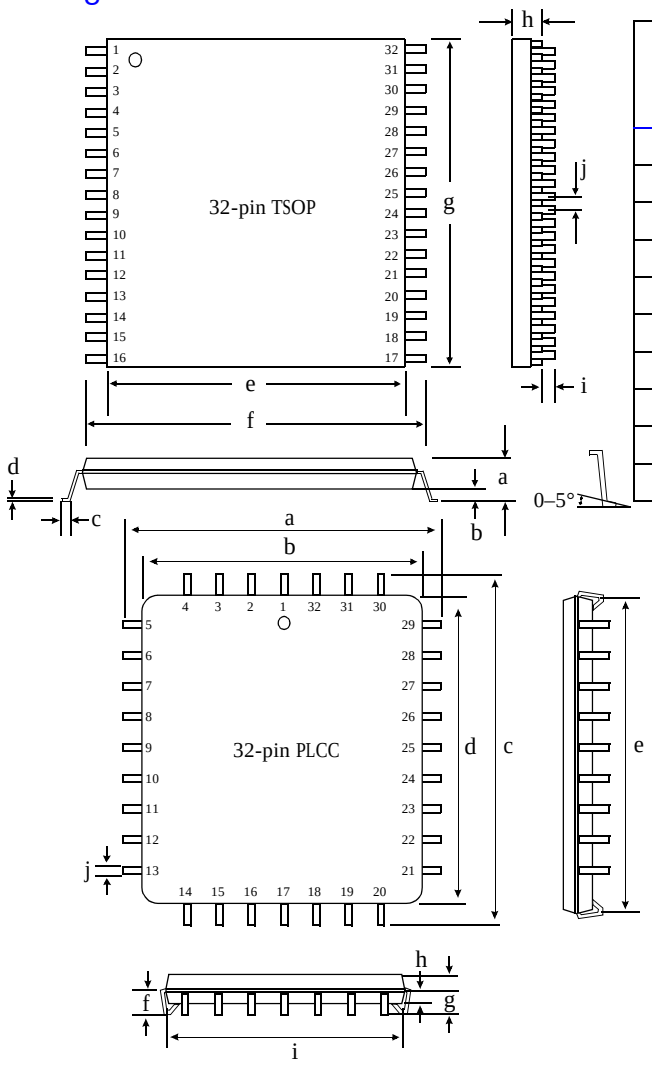
Symbol	Parameter	Test setup	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control pin capacitance	V_{IN} = 0	7.5	9	pF

Data retention

Parameter	Temp. (°C)	Min	Unit
Minimum pattern data retention time	150°	10	years
	125°	20	years

FLASH

Package dimensions



	32-pin TSOP	
	min (mm)	max (mm)
a		1.20
b		0.25
c	0.5	0.7
d	0.1	0.21
e	18.30	18.50
f	19.80	20.20
g	7.90	8.10
h	0.95	1.05
i	0.05	0.15
j		0.50

	32-pin PLCC
	typical (inch)
a	0.49
b	0.45
c	0.59
d	0.55
e	0.52
f	0.09
g	0.136
h	0.075
i	0.52
j	0.028

JEDEC outline	MS-016 AE
Body size	0.450 in. × 0.550 in.
Package thickness	0.110 in.
Board standoff	0.020 in. (min)
Lead pitch	0.050 in.
Coplanarity	0.004 in. (max)

AS29F040 ordering codes*

Package \ Access time	55ns (commercial/industrial)	70 ns (commercial/industrial)	90 ns (commercial/industrial)	120 ns (commercial/industrial)	150 ns (commercial/industrial)
TSOP, 8×20 mm, 32-pin	AS29F040-55TC AS29F040-55TI	AS29F040-70TC AS29F040-70TI	AS29F040-90TC AS29F040-90TI	AS29F040-120TC AS29F040-120TI	AS29F040-150TC AS29F040-150T
PLCC, 0.55×0.45”, 32-pin	AS29F040-55LC AS29F040-55LI	AS29F040-70LC AS29F040-70LI	AS29F040-90LC AS29F040-90LI	AS29F040-120LC AS29F040-120LI	AS29F040-150LC AS29F040-150LI

AS29F040 part numbering system

AS29F	040	–XXX	X	X
Flash EEPROM prefix	Device number	Address access time	Package: L= PLCC T= TSOP	Temperature range: C = Commercial: 0°C to 70°C I = Industrial: -40°C to 85°C

* Industrial and Commercial temperature range available