19-0125; Rev. 1; 8/93

MAXIM

Dual-Slot PCMCIA Analog Power Controller

General Description

The MAX780A provides the power switching and status signals necessary to control two Personal Computer Memory Card International Association (PCMCIA) Release 2.0 card slots. The MAX780A, used in conjunction with a PC Card Interface Digital Controller, forms a complete, minimum component count PCMCIA interface for palmtop and notebook computers.

The MAX780A incorporates two 0V/+5V/+12V/high-impedance power outputs for flash V_{PP} programming, level shifters for power MOSFET control of two separate +3.3V/+5V supplies, and two V_{PP} power-ready status signals. The MAX780A may be directly connected to the control outputs from a PCMCIA digital controller, or may be configured to use internal edge-triggered registers for connection to the CPU data bus.

The MAX780B has all the features of the MAX780A but omits the reference and V_{PP} valid indicators. The MAX780C has all the features of the MAX780A but omits the registers for the digital inputs. The MAX780D omits the reference, the V_{PP} valid indicators, and the digital input registers.

Part Number	Reference & V_{PP} Status Indicators	Registers for Direct Connection to CPU Data Bus	Dual V_{PP} Switches & Level Shifters for V_{CC} Switching
MAX780A	✔	✔	✔
MAX780B		✔	✔
MAX780C	✔		✔
MAX780D			✔

Applications

Notebook and Palmtop Computers

Personal Organizers

Digital Cameras

Handiterminals

Bar-Code Readers

Features

- **SSOP Circuit Fits in 0.09in^2**
- **Smallest Complete Analog Controller for Two PCMCIA (Release 2.0/JEIDA 4.1) PC Card Sockets**
- **Dual V_{CC} Contols and V_{PP} Outputs**
- **Logic-Compatible with Industry-Standard PCMCIA Digital Controllers:**
  - **Intel 82365SL_DF**
  - **Fujitsu MB86301**
  - **Chips and Technology F8680**
  - **Cirrus Logic CL-PD6720**
- **0V/+5V/+12V/High-Impedance V_{PP} Outputs**
- **Internal 1.6Ω V_{PP} Power Switches**
- **Dual Voltage 3.3V/5V V_{CC} Operation**
- **V_{PP} Power-Ready Status Signals**
- **130µA Quiescent Supply Current (3.5µA in Shutdown)**
- **Break-Before-Make Switching**

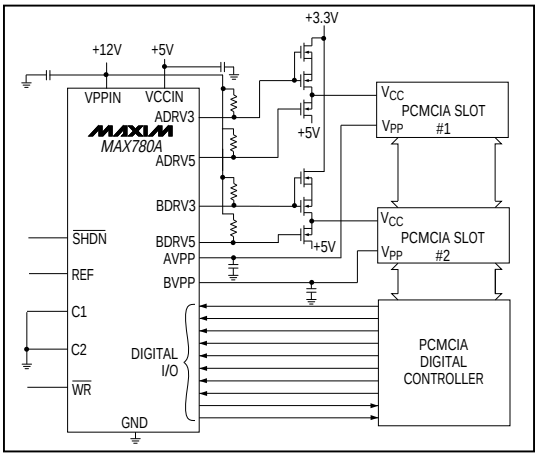
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX780ACNG	0°C to +70°C	24 Narrow Plastic DIP
MAX780ACAG	0°C to +70°C	24 SSOP
MAX780AC/D	0°C to +70°C	Dice*
MAX780AENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX780AEAG	-40°C to +85°C	24 SSOP

Ordering Information continued on last page.

** Contact factory for dice specifications.*

Typical Operating Circuit



Call toll free 1-800-998-8800 for free samples or literature.

ABSOLUTE MAXIMUM RATINGS

VCCIN to GND ..... +7V, -0.3V
VPPIN to GND ..... +13.2V, -0.3V
ADRV5, ADRV3, BDRV5, BDRV3 to GND ... (VPPIN + 0.3V), -0.3V
AVPP, BVPP to GND ..... (VPPIN + 0.3V), -0.3V
All Other Pins to GND ..... (VCCIN + 0.3V), -0.3V
Continuous Power Dissipation (T_A = +70°C)
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
24-Pin Narrow Plastic DIP (derate 13.33 mW/°C above +70°C) . 1067mW
24-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX780_C__ ..... 0°C to +70°C
MAX780_E__ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCCIN = +5V, VPPIN = +12V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
VCCIN Input Voltage Range			2.85		5.5	V
VPPIN Input Voltage Range			0		12.6	V
VCCIN Supply Current	5V mode			130	300	µA
	12V or 0V mode			60		
VPPIN Supply Current	VPPIN = 12.6V	12V mode		185	450	µA
		5V mode		10		
VCCIN Standby Current	$\overline{SHDN}$ = 0V, all logic inputs at GND or VCCIN			3.5	10	µA
VPPIN Standby Current	$\overline{SHDN}$ = 0V, VPPIN = 4.75V			0.1	1	µA
DC CHARACTERISTICS						
AVPP, BVPP Switch Resistance	VPPIN = 11.4V, 0mA < I_{LOAD} < 60mA, 12V mode			1.6	2.45	Ω
	VCCIN = 4.5V, 0mA < I_{LOAD} < 1mA, 5V mode			30	50	
	VPPIN = 11.4V, 0mA < I_{LOAD} < 1mA, 0V mode			140	300	
ADRV3, ADRV5, BDRV3, BDRV5 Leakage Current	High-impedance mode			1	50	nA
ADRV3, ADRV5, BDRV3, BDRV5 Output Voltage Low	I_{LOAD} = 1mA			0.1	0.4	V
VOLTAGE REFERENCE (MAX780A and MAX780C only)						
REF Voltage	I_{LOAD} = 0µA	MAX780_C	1.22	1.25	1.28	V
		MAX780_E	1.21	1.25	1.29	
REF Temperature Coefficient				20		ppm/°C
REF Line Regulation	VCCIN = 2.85V to 5.5V			0.5		mV/V
REF Load Regulation	I_{LOAD} = 0µA to 100µA			2		µV/µA
$\overline{AGPI}$, $\overline{BGPI}$ Power-Ready Threshold	MAX780_C		10.72	11.05	11.40	V
	MAX780_E		10.68	11.05	11.40	
$\overline{AGPI}$, $\overline{BGPI}$ Power-Ready Hysteresis	12V mode	VPPIN ↓		130		mV
		VPPIN ↑		0		

ELECTRICAL CHARACTERISTICS (continued)

(VCCIN = +5V, VPPIN = +12V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC SECTION					
Logic Input Leakage Current				1	µA
Logic Input High		2.4			V
Logic Input Low				0.8	V
$\overline{AGPI}$, $\overline{BGPI}$ Logic Output High	I_{LOAD} = 1mA	VCCIN -0.4	VCCIN -0.2		V
$\overline{AGPI}$, $\overline{BGPI}$ Logic Output Low	I_{LOAD} = 1mA		0.06	0.4	V

TIMING CHARACTERISTICS - MAX780A and MAX780B only

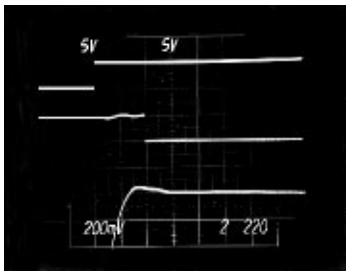
(VCCIN = +3.3V or +5.0V, VPPIN = +12.0V, see Figure 4, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{WR}$ Pulse Width	t_{LA}		125			ns
VPP, _VCC_ Setup Time	t_{AS}		100			ns
VPP, _VCC_ Hold Time	t_{AH}	(Note 1)	0			ns
VCC to _DRV_ Propagation Delay				50		ns

Note 1: Guaranteed by design, not production tested.

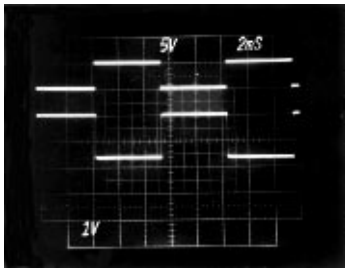
Typical Operating Characteristics

AVPP SWITCHING



5µs/div
C1 = C2 = 0V, AVPP0 = +5V, CIN = 10µF, C_A = 0.1µF

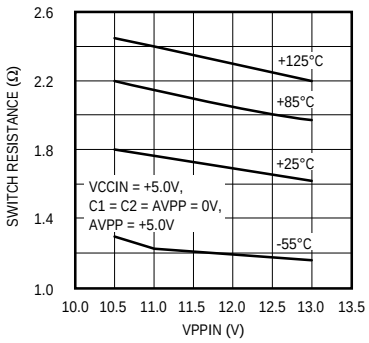
AVCC SWITCHING



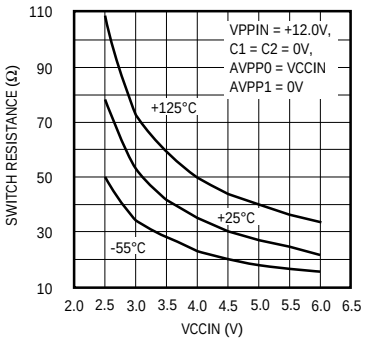
2ms/div
C1 = +5V, C2 = 0V, AVCC0 = +5V, M1 = M2 = 3055EL,
R_{LOAD} = 130Ω, C_C = 1µF

Typical Operating Characteristics (continued)

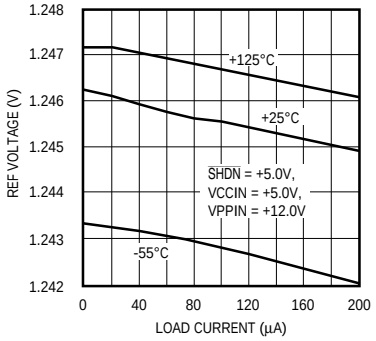
AVPP SWITCH RESISTANCE (12V MODE)



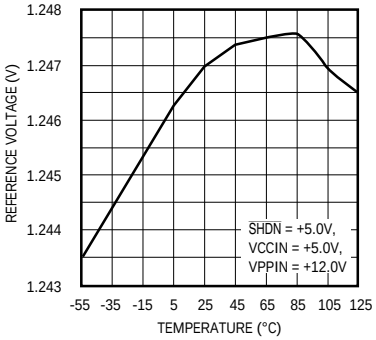
AVPP SWITCH RESISTANCE (5V MODE)



REFERENCE LOAD REGULATION



REFERENCE VOLTAGE vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
MAX780A/B/C	MAX780D		
1		C2	Pin-strap input that selects edge-triggered register or direct digital inputs. Tying C2 to VCCIN makes the logic inputs edge triggered; inputs to pins 4-11 are clocked in on the rising edge of $\overline{WR}$. Tying C2 to GND allows control signals to be directly applied to the logic inputs on pins 4-11. Connect to GND for MAX780C.
2	1	C1	Pin-strap input that selects one of two logic decode modes for the digital inputs. See Tables 1-3.
3		$\overline{WR}$	Write pulse input. When C2 is tied to VCCIN, a rising edge on $\overline{WR}$ clocks in the V_{CC} and V_{PP} enables. When C2 is tied to GND, inputs to $\overline{WR}$ have no effect. Connect to GND for MAX780C.
4, 5	2, 3	AVPP1, AVPP0	Logic inputs that control the voltage on AVPP.
6, 7	4, 5	BVPP1, BVPP0	Logic inputs that control the voltage on BVPP.
8, 9	6, 7	AVCC1, AVCC0	Logic inputs that control the state of the MOSFET gate drivers ADRV3 and ADRV5.
10, 11	8, 9	BVCC1, BVCC0	Logic inputs that control the state of the MOSFET gate drivers BDRV3 and BDRV5.
12, 13	10, 11	BDRV5, BDRV3	Open-drain gate driver outputs that control the MOSFETs that switch the V_{CC} pin of slot B to 0V, 3.0V/3.3V, or 5V.
14, 15	12, 13	ADRV5, ADRV3	Open-drain gate driver outputs that control the MOSFETs that switch the V_{CC} pin of slot A to 0V, 3.0V/3.3V, or 5V.
16		$\overline{BGPI}$	Logic-level power-ready output that stays low as long as BVPP is greater than 11.05V (MAX780A and MAX780C only). Make no connection to this pin for MAX780B.
17		$\overline{AGPI}$	Logic-level power-ready output that stays low as long as AVPP is greater than 11.05V (MAX780A and MAX780C only). Make no connection to this pin for MAX780B.
18	14	$\overline{SHDN}$	Logic input that shuts the MAX780 down to a low supply-current state when brought low. Asserting $\overline{SHDN}$ forces ADRV3, BDRV3, ADRV5, BDRV5, REF, $\overline{AGPI}$, and $\overline{BGPI}$ low. All V_{PP} inputs and outputs are functional for either state of $\overline{SHDN}$. Program AVPP and BVPP to 0V for lowest power consumption.
	15	N.C.	No connect. Not internally connected.
19		REF	1.25V reference voltage output (MAX780A and MAX780C only). Make no connection to this pin for MAX780B.)
20	16	BVPP	Switched output that provides 0V, 5V, or 12V to the V_{PP} pins of slot B.
21	17	AVPP	Switched output that provides 0V, 5V, or 12V to the V_{PP} pins of slot A.
22	18	VCCIN	+5V power input
23	19	VPPIN	+12V power input. VPPIN can have 0V or 5V applied as long as VCCIN = 5V.
24	20	GND	Ground

Table 1. AVPP Control Logic

C1	AVPP1	AVPP0	AVPP
0	0	0	0V
0	0	1	VCCIN
0	1	0	VPPIN
0	1	1	High-Z
1	0	0	0V
1	0	1	0V
1	1	0	VCCIN
1	1	1	VPPIN

Table 2. BVPP Control Logic

C1	BVPP1	BVPP0	BVPP
0	0	0	0V
0	0	1	VCCIN
0	1	0	VPPIN
0	1	1	High-Z
1	0	0	0V
1	0	1	0V
1	1	0	VCCIN
1	1	1	VPPIN

Table 3. ADRV3 and ADRV5 Control Logic

C1	AVCC1	AVCC0	ADRV3	ADRV5
0	0	0	0V	0V
0	0	1	Hi-Z	0V
0	1	0	0V	Hi-Z
0	1	1	0V	0V
1	0	0	0V	0V
1	0	1	0V	0V
1	1	0	0V	Hi-Z
1	1	1	Hi-Z	0V

Table 4. BDRV3 and BDRV5 Control Logic

C1	BVCC1	BVCC0	BDRV3	BDRV5
0	0	0	0V	0V
0	0	1	Hi-Z	0V
0	1	0	0V	Hi-Z
0	1	1	0V	0V
1	0	0	0V	0V
1	0	1	0V	0V
1	1	0	0V	Hi-Z
1	1	1	Hi-Z	0V

Detailed Description

V_{PP} Switching

All four versions (A, B, C, and D) of the MAX780 allow simple switching of PCMCIA card V_{PP} to 0V, 5V, and 12V. On-chip power MOSFETs connect AVPP and BVPP to either GND, VCCIN, or VPPIN. The AVPP0 and AVPP1 control logic inputs determine the state of AVPP. Likewise, BVPP0 and BVPP1 control BVPP.

To prevent V_{PP} overshoot due to parasitic inductance in the +12V supply, the VPPIN bypass capacitor (C_{IN}) should be 10 times greater than the capacitance from AVPP (C_A) or BVPP (C_B) to GND. Hence, when C_A and C_B are 0.1µF, C_{IN} should be 1.0µF.

The $\overline{AGPI}$ and $\overline{BGPI}$ status outputs signal when the V_{PP} lines are valid. $\overline{AGPI}$ goes low when AVPP exceeds 11.05V; $\overline{BGPI}$ goes low when BVPP exceeds 11.05V. The status outputs and the reference are only active when $\overline{SHDN}$ is high.

Pulling $\overline{SHDN}$ low puts the MAX780 into a low supply-current mode and disables the reference and the $\overline{AGPI}$ and $\overline{BGPI}$ status outputs. The V_{CC} level shifters ADRV5, ADRV3, BDRV5, BDRV3 are all forced low when $\overline{SHDN}$ is low. V_{PP} switching is not affected by the state of $\overline{SHDN}$. Program AVPP and BVPP to 0V for lowest power consumption when $\overline{SHDN}$ is low. Wait at least 200µs after bringing the MAX780 out of shutdown before checking $\overline{AGPI}$ or $\overline{BGPI}$ since the reference needs time to stabilize.

V_{CC} Switching

The MAX780 contains level shifters that simplify driving external power MOSFETs to switch PCMCIA card V_{CC} to 3.3V and 5V. While a PCMCIA card is being inserted into the socket, the V_{CC} pins on the card edge connector should be powered down to 0V so that "hot insertion" does not damage the PCMCIA card. The simplest way to accomplish this is to pull out a mechanical switch before the PCMCIA card is inserted. The mechanical switch can be pushed in only when the card has been fitted snugly into its socket. The MAX780 *Detailed Operating Circuit* shows this method.

In the *Detailed Operating Circuit,* (with the mechanical interlock switch closed) the PCMCIA card V_{CC} cannot be pulled more than a diode drop below 3.3V. The N-channel power MOSFET that connects V_{CC} to 3.3V has its drain tied to V_{CC} and its source tied to 3.3V, so that its body diode prevents the card's V_{CC} from falling to 0V. If it were rotated so that the source connected to V_{CC}, then applying 5V to V_{CC} would short the 5V supply to the 3.3V supply via the MOSFET's body diode.

If a mechanical interlock switch cannot be used, an extra MOSFET must be added, as shown in Figure 1. Placing two N-channel MOSFETs in series with their body diodes facing in opposite directions allows V_{CC} to be shut down to 0V without using a mechanical switch.

Switching Speed

The drive to the external MOSFETs ensures that the 3.3V supply is never connected to the 5V supply. This is done by turning these transistors off quickly (using active pull-down circuitry), and on more slowly (using external pull-up resistors). The turn-on delay depends on the value of the pull-up resistors, and on the gate capacitance of the switching transistors. To save power, use high-value resistors of up to 10MΩ. However, note that high-value resistors will increase the time it takes to turn on the switched supplies

Applications Information

The MAX780 can be used with PCMCIA controllers other than the Intel 82365SL DF. Figure 2 shows the logic connections to the Cirrus Logic CL-PD6720 PCMCIA Host Adapter.

The MAX780 does not need a PCMCIA controller to function. Tie C2 to VCCIN to allow direct V_{CC} and V_{PP} control from the system bus. Figure 3 shows the connection to the system bus. Figure 4 shows the timing requirements.

Reading from a PCMCIA Port without Using the V_{PP} Supply

In the *Typical Operating Circuit,* V_{CC} is switched to the PCMCIA ports using the 12V V_{PP} supply, which provides the gate drive needed to turn on the external N-channel MOSFETs. In some cases, the high-power V_{PP} supply is only available when information has to be written to the PCMCIA port, not when data is being read. The V_{PP} supply may have a quiescent current of several milliamps, so it consumes more power than is necessary simply to provide gate drive for some FETs.

In these circumstances, a separate gate-drive supply is needed to turn on the external FETs. Ideally it should have a low quiescent current and be capable of being turned off when read access to the PCMCIA port is not required. Doubling or tripling charge pumps can easily be built using a convenient clock signal from elsewhere in the system. Buffering the clock signal with a suitable gate provides on/off control, as shown in Figure 5.

When driven at 100kHz or more by a CMOS gate powered from 5V, the doubler circuit outputs 8.6V when loaded with 25kΩ (equivalent to four 100kΩ pull-up resistors). Under similar conditions, but when running from 3.3V, the tripler circuit produces 7.9V.

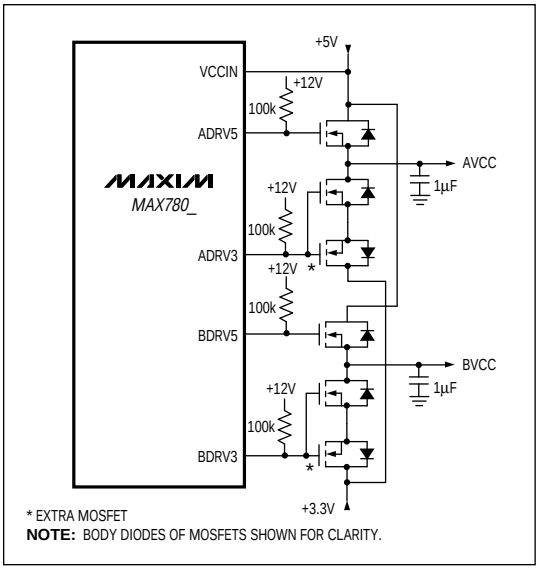


Figure 1. Using an Extra MOSFET to Replace the Mechanical Interlock

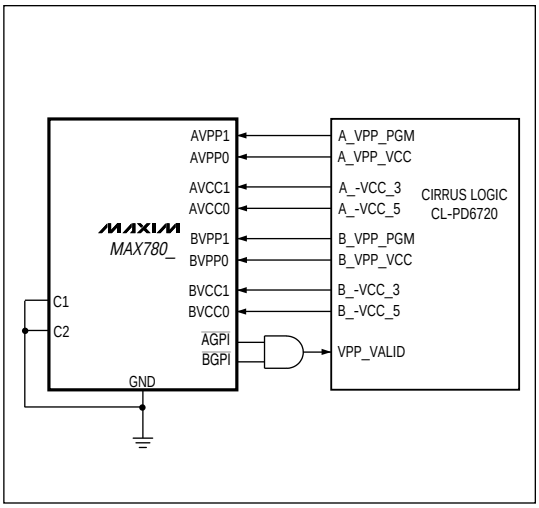


Figure 2. Logic Connections to CL-PD6720

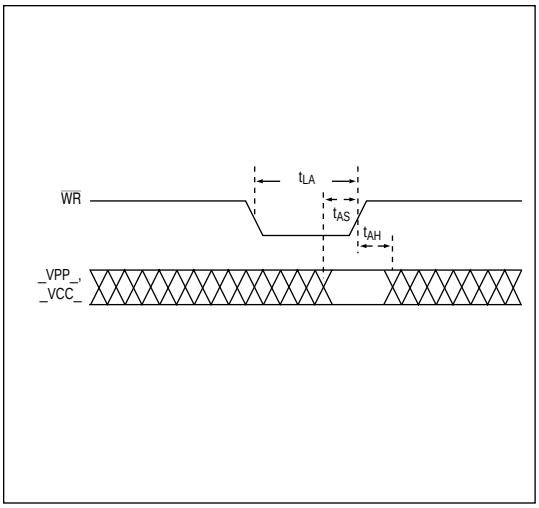


Figure 4. C2 = VCCIN Mode Timing

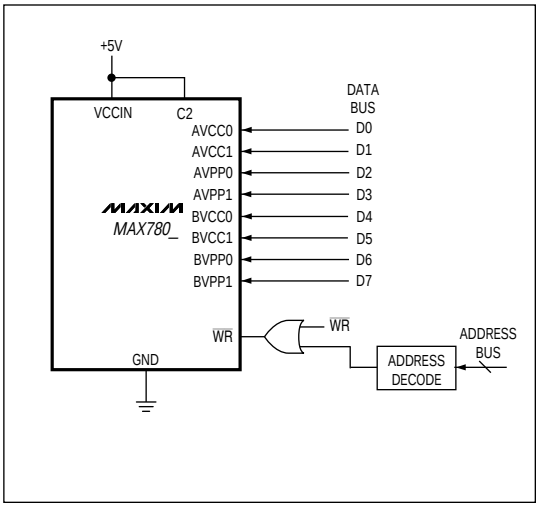


Figure 3. Direct Connection to System Bus

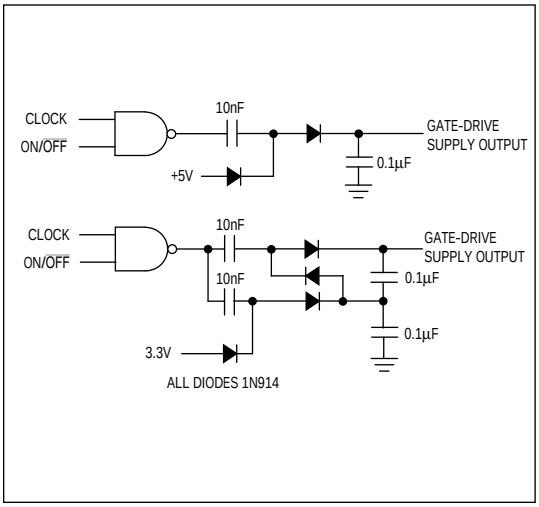
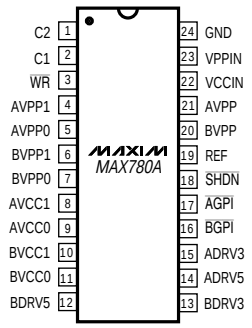


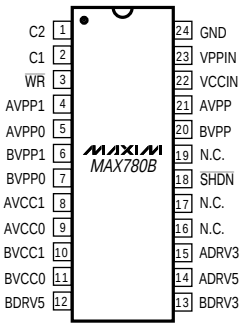
Figure 5. Alternative Gate-Drive Charge-Pump Supplies

Pin Configurations (continued)

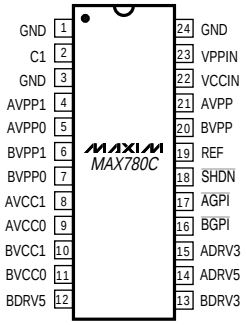
TOP VIEW



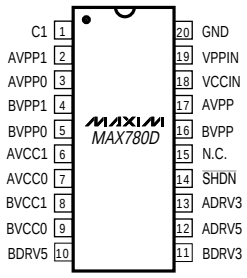
DIP/SSOP



DIP/SSOP



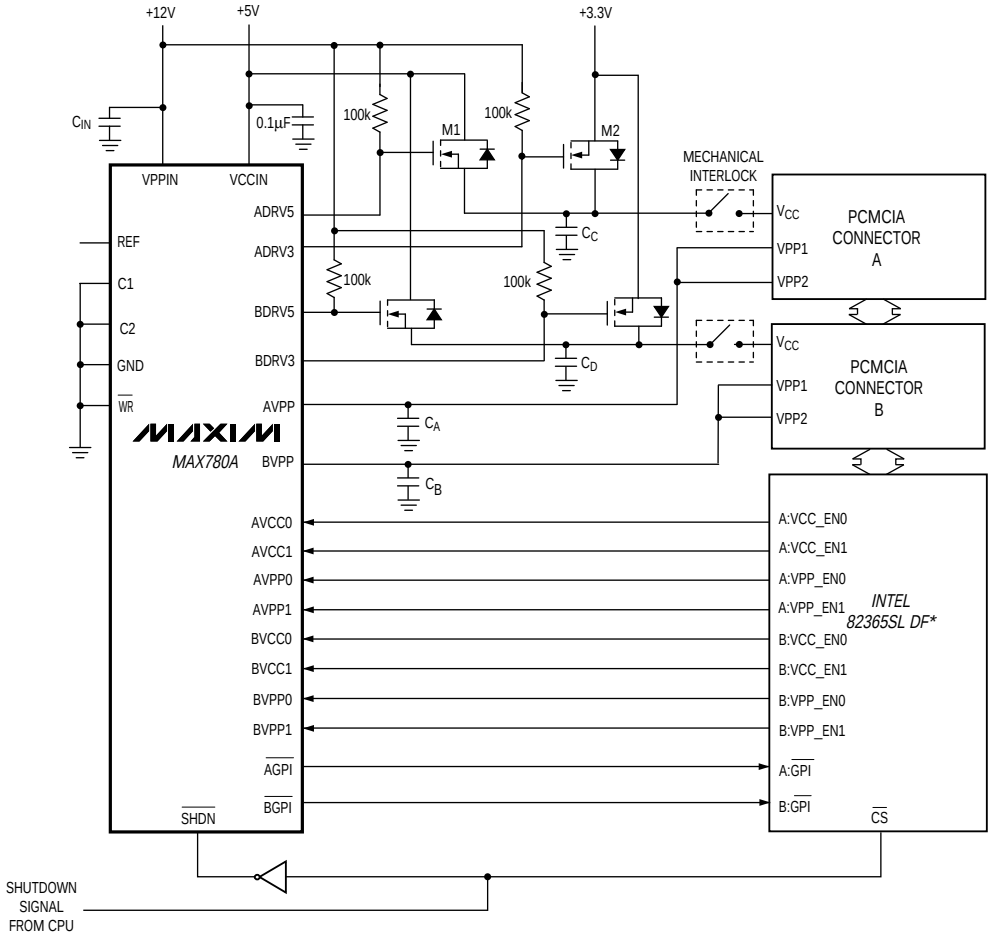
DIP/SSOP



DIP/SSOP

Dual-Slot PCMCIA Analog Power Controller

Detailed Operating Circuit



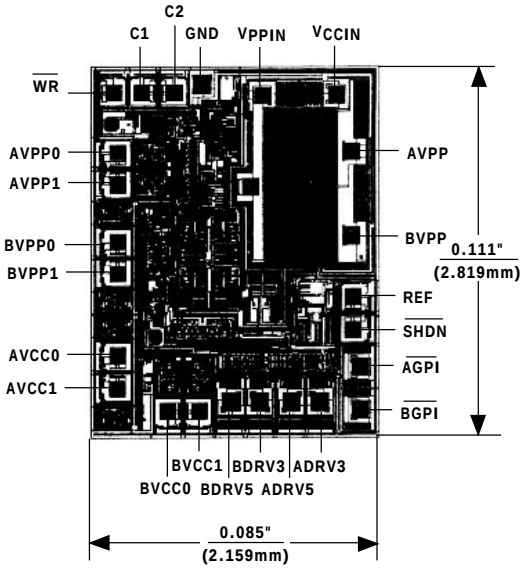
Dual-Slot PCMCIA Analog Power Controller

Ordering Information (continued)

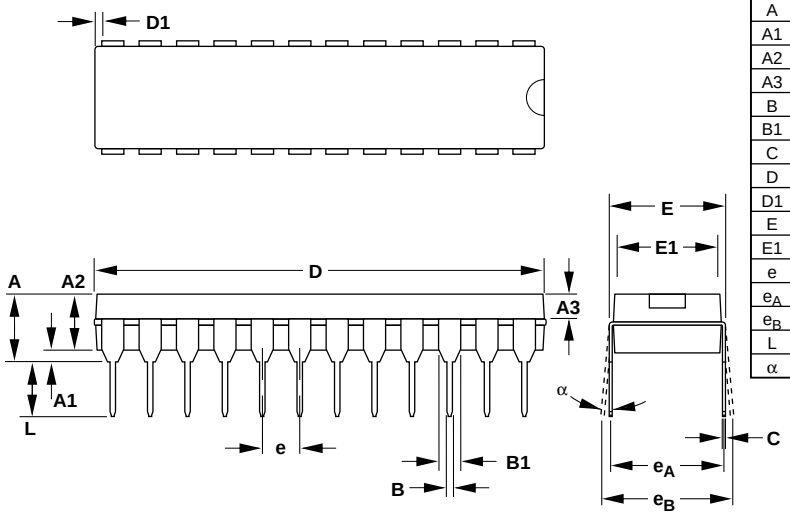
PART	TEMP. RANGE	PIN-PACKAGE
MAX780BCNG	0°C to +70°C	24 Narrow Plastic DIP
MAX780BCAG	0°C to +70°C	24 SSOP
MAX780BC/D	0°C to +70°C	Dice*
MAX780BENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX780BEAG	-40°C to +85°C	24 SSOP
MAX780CCNG	0°C to +70°C	24 Narrow Plastic DIP
MAX780CCAG	0°C to +70°C	24 SSOP
MAX780CC/D	0°C to +70°C	Dice*
MAX780CENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX780CEAG	-40°C to +85°C	24 SSOP
MAX780DCPP	0°C to +70°C	20 Plastic DIP
MAX780DCAP	0°C to +70°C	20 SSOP
MAX780DC/D	0°C to +70°C	Dice*
MAX780DEPP	-40°C to +85°C	20 Plastic DIP
MAX780DEAP	-40°C to +85°C	20 SSOP

** Contact factory for dice specifications.*

Chip Topography



Package Information

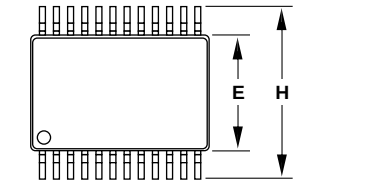


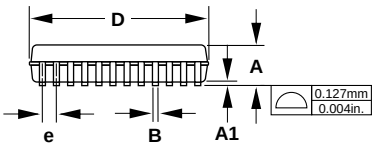
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	1.235	1.265	31.37	32.13
D1	0.050	0.080	1.27	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

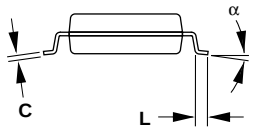
21-337A

24-PIN PLASTIC DUAL-IN-LINE (NARROW) PACKAGE

Package Information (continued)



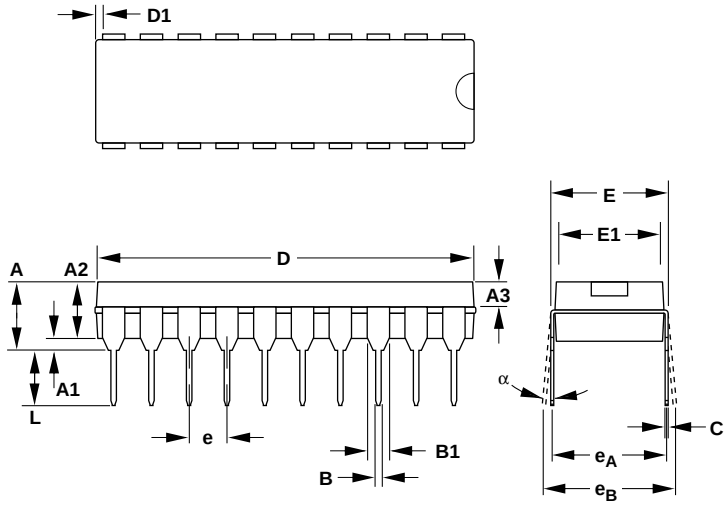




DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.005	0.009	0.13	0.22
D	0.278	0.328	7.07	8.33
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.022	0.037	0.55	0.95
α	0°	8°	0°	8°

21-0002A

24-PIN PLASTIC SHRINK SMALL-OUTLINE PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	1.015	1.045	25.78	26.54
D1	0.040	0.070	1.02	1.78
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

21-333A

20-PIN PLASTIC DUAL-IN-LINE PACKAGE

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