

OLED DISPLAY MODULE

Product Specification

CUSTOMER	Standard	
PRODUCT NUMBER	DD-12864YO-7A	
CUSTOMER APPROVAL		Date

INTERNAL APPROVALS		
Product Mgr	Doc. Control	Electr. Eng
Elijah Ebo	Anthony Perkins	Bazile Peter
Date: 13 Nov 07	Date: 13 Nov 07	Date: 13 Nov 07

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REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	13 Nov 07			First Issue	
B	18 April 08	10	3.3	Changed pin out information for BS1, BS2	

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1 MAIN FEATURES

ITEM	CONTENTS
Display Format	128 x 64 Dots
Overall Dimensions	73.00 x 41.86 x 2.00 mm
Colour	Monochrome Yellow
Active Area	61.41 x 30.69 mm
Viewing Area	63.41 x 32.69mm
Display Mode	Passive Matrix (2.70")
Driving Method	1/64 duty
Driver IC	SSD1325
Operating temperature	-30 ~ +70
Storage temperature	-40 ~ +80

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2 MECHANICAL SPECIFICATION

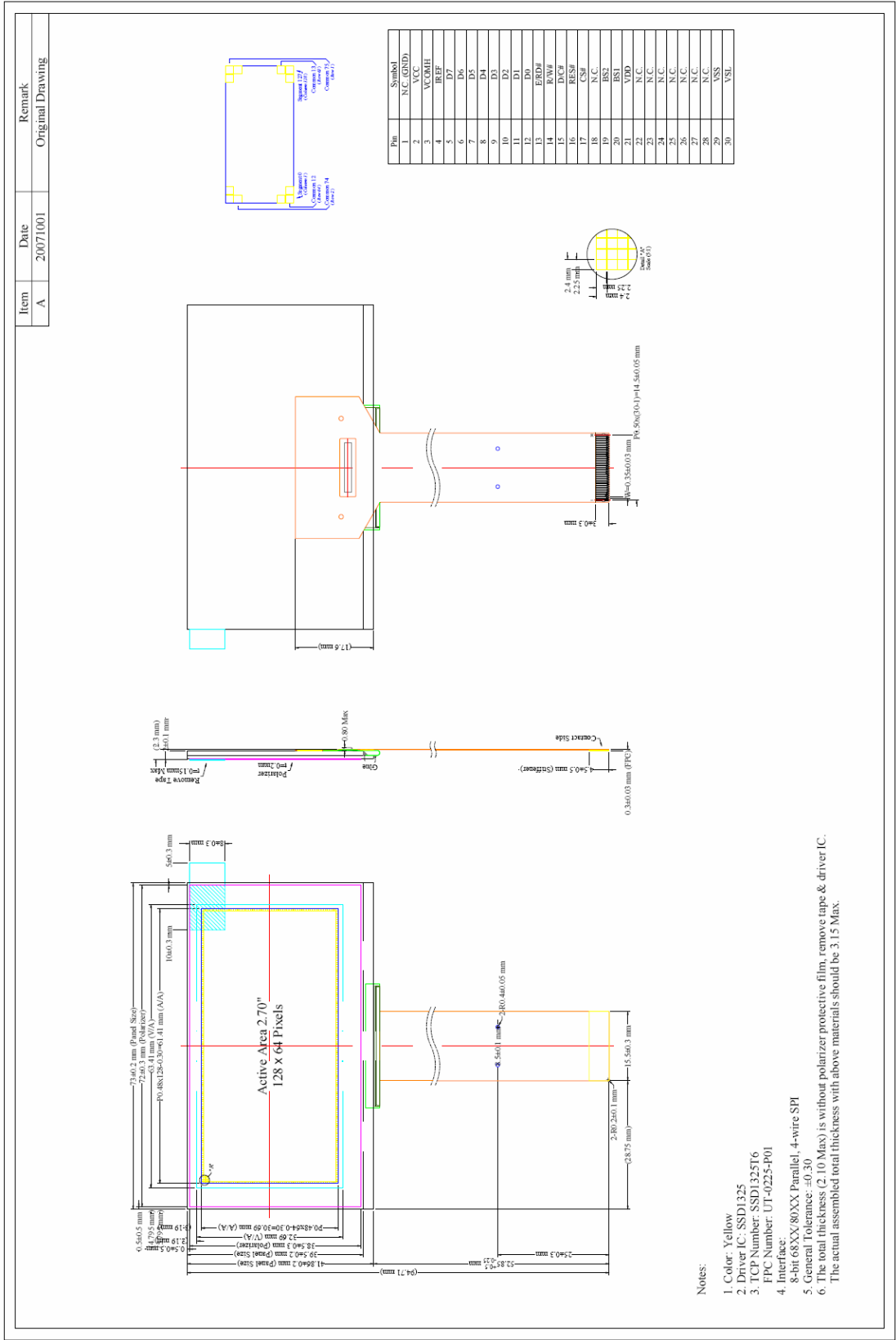
2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Display Format	128 x 64 Dots	Dots
Overall Dimensions	73.00 x 41.86 x 2.00	mm
Viewing Area	63.41 x 32.69	mm
Active Area	61.41 x 30.69	mm
Dot Size	0.45 x 0.45	mm
Dot Pitch	0.48 x 0.48	mm
Weight	21	g
IC Controller/Driver	SSD1325	

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2.2 MECHANICAL DRAWING



3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

VSS = 0 V, Ta = 25 °C

Item	Symbol	Min	Max	Unit	Note
Supply Voltage for logic	V _{DD}	-0.3	4.0	V	Note 1, 2
Supply voltage for Display	V _{CC}	0	16	V	
Operating Temperature	Top	-30	70	°C	
Storage Temperature	Tst	-40	80	°C	
Static Electricity	Be sure that you are grounded when handling displays.				

Note 1: All the above voltages are on the basis of “GND=0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent damage to the module may occur. Also for normal operations it's desirable to use this module under the conditions according to Section 3.2 “Electrical Characteristics”. If this module is used beyond these conditions the module may malfunction and the reliability could deteriorate.

3.2 ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.4	2.8	3.5	V
Supply Voltage for Display	V_{CC}	Note 3	14.25	15	15.75	V
High Level Input	V_{IH}	$I_{OUT}=0.1mA,$ 3.3MHz	$0.8 \times V_{DD}$	-	V_{DD}	V
Low Level Input	V_{IL}		0	-	$0.2 \times V_{DD}$	V
High Level Output	V_{OH}		$0.9 \times V_{DD}$	-	V_{DD}	V
Low Level Output	V_{OL}		0	-	$0.1 \times V_{DD}$	V
Operating current for V_{DD}	I_{DD}	Note 4	-	250	400	μA
		Note 5	-	250	400	
Operating current for V_{CC}	I_{CC}	Note 4	-	31	39	mA
		Note 5	-	53	66	
Sleep mode current for V_{DD}	$I_{DD\ SLEEP}$		-	1	2	μA
Sleep mode current for V_{CC}	$I_{CC\ SLEEP}$		-	1	2	μA

Note 3 Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customers request

Note 4 $V_{DD} = 2.8V$, $V_{CC} = 15V$, 50% display area turned on.

Note 5 $V_{DD} = 2.8V$, $V_{CC} = 15V$, 100% display area turned on.

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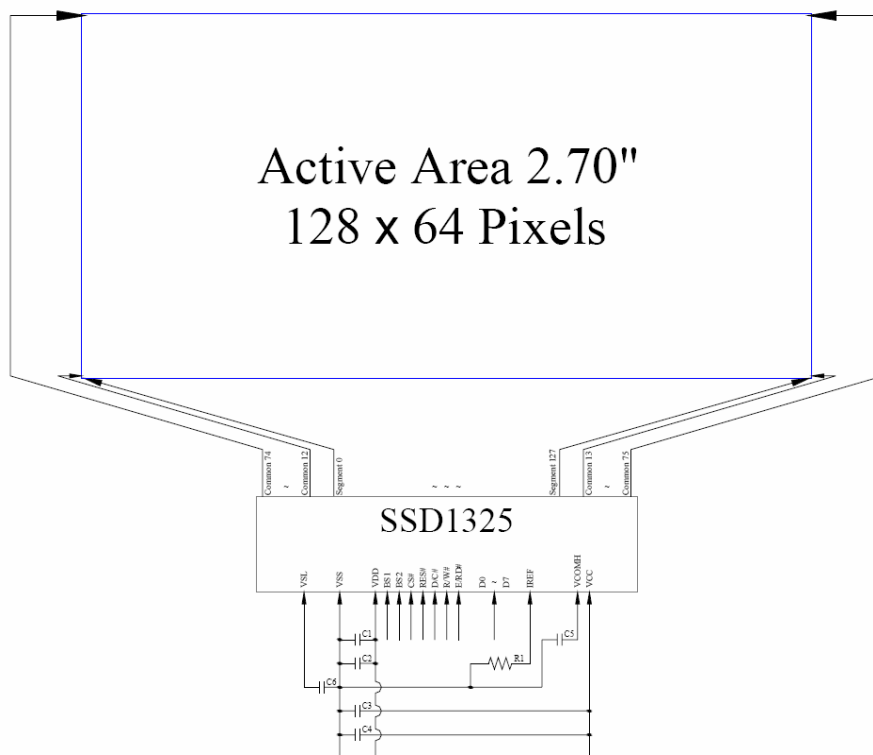
3.3 INTERFACE PIN ASSIGNMENT

No.	Symbol	Function
1	N.C.(GND)	Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.
2	VCC	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. It can be supplied externally or generated internally by using internal DC/DC voltage converter.
3	VCOMH	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. It can be supplied externally or internally. When VCOMH is generated internally, a capacitor should be connected between this pin and VSS.
4	IREF	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10μA.
5~12	D7~D0	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.
13	E/RD#	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when the pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
14	R/W#	Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
15	D/C#	Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams. When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register.
16	RES#	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed.
17	CS#	Chip Select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.
18	N.C.	No Connection

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19	BS2	Communicating Protocol Select These pins are MCU interface selection input. See the following table:			
20	BS1		68XX-parallel	80XX-parallel	Serial
		BS1	0	1	0
		BS2	1	1	0
21	VDD	Power Supply for Logic Circuit This is a voltage supply pin. It must be connected to external source.			
22~28	N.C.	Reserved Pin The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.			
29	VSS	Ground of OEL System This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.			
30	VSL	Voltage Output Low Level for SEG Signal This pin is the output for the voltage output low level for SEG signals. A capacitor should be connected between this pin and VSS.			

BLOCK DIAGRAM



MCU Interface Selection: BS1 and BS2

Pins connected to MCU interface: D7~D0, E/RD#, R/W#, D/C#, RES# and CS#.

C1, C3: 0.1µF

C2, C6: 4.7µF

C4: 10µF

C5: 4.7µF/25V Tantalum Capacitor

R1: 820 kΩ, $R1 = (\text{Voltage at IREF} - \text{BGGND}) / \text{IREF}$

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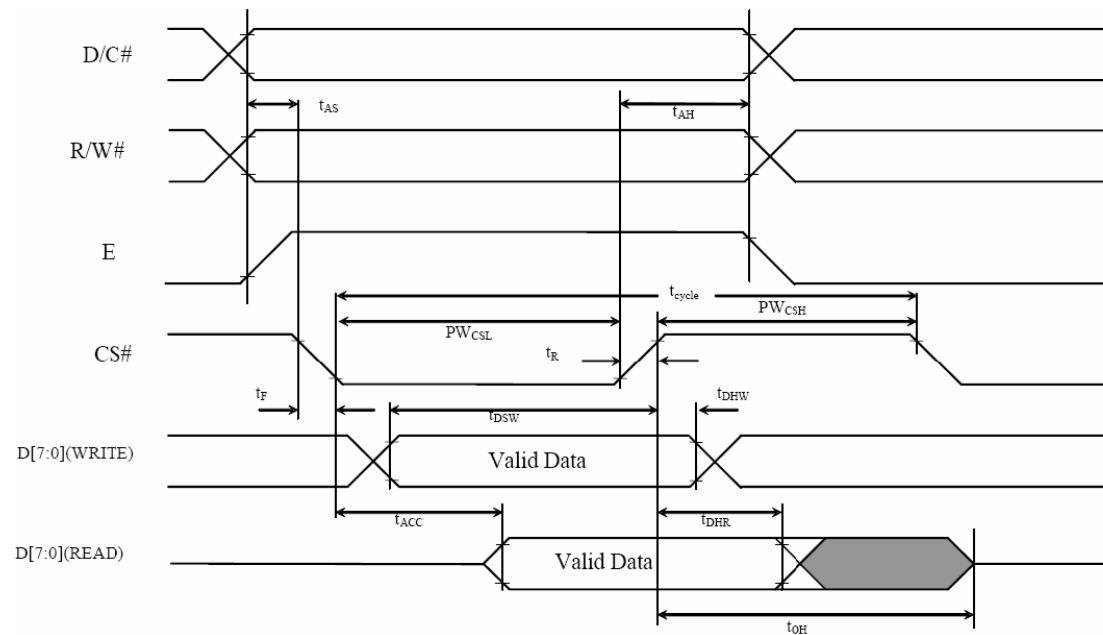
3.4 TIMING CHARACTERISTICS

3.4.1 AC CHARACTERISTICS

3.4.1.1 68XX-Series MPU Parallel Interface Timing Characteristics

VDD = 2.8V, Ta = 25°C

Symbol	Description	Min	Max	Unit
t _{cycle}	System Cycle Time	300	-	ns
t _{AS}	Address Setup Time	0	-	ns
t _{AH}	Address Hold Time	0	-	ns
t _{DSW}	Write Data Setup Time	40	-	ns
t _{DHW}	Write Data Hold Time	15	-	ns
t _{DHR}	Read Data Hold Time	20	-	ns
t _{OH}	Output Disable Time	-	70	ns
t _{ACC}	Access Time	-	140	ns
PWCSL	Chip Select Low Pulse Width (Read) Chip Select	120	-	ns
	Low Pulse width (Write)	60		
PWCSH	Chip Select High Pulse Width (Read) Chip Select	60	-	ns
	High Pulse Width (Write)	60		
t _R	Rise Time	-	15	ns
t _F	Fall Time	-	15	ns

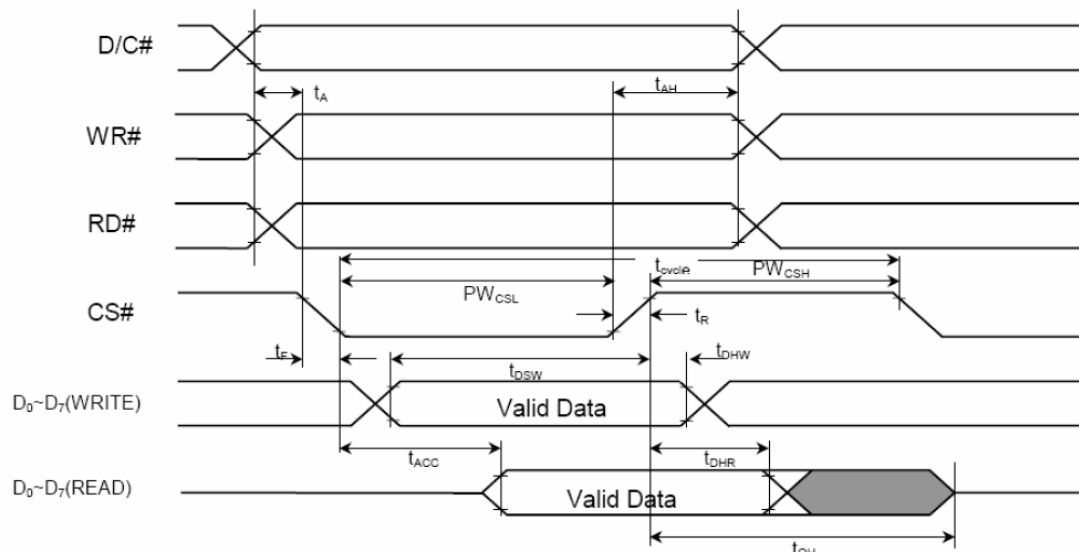


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3.4.1.2 80XX-Series MPU Parallel Interface Timing Characteristics

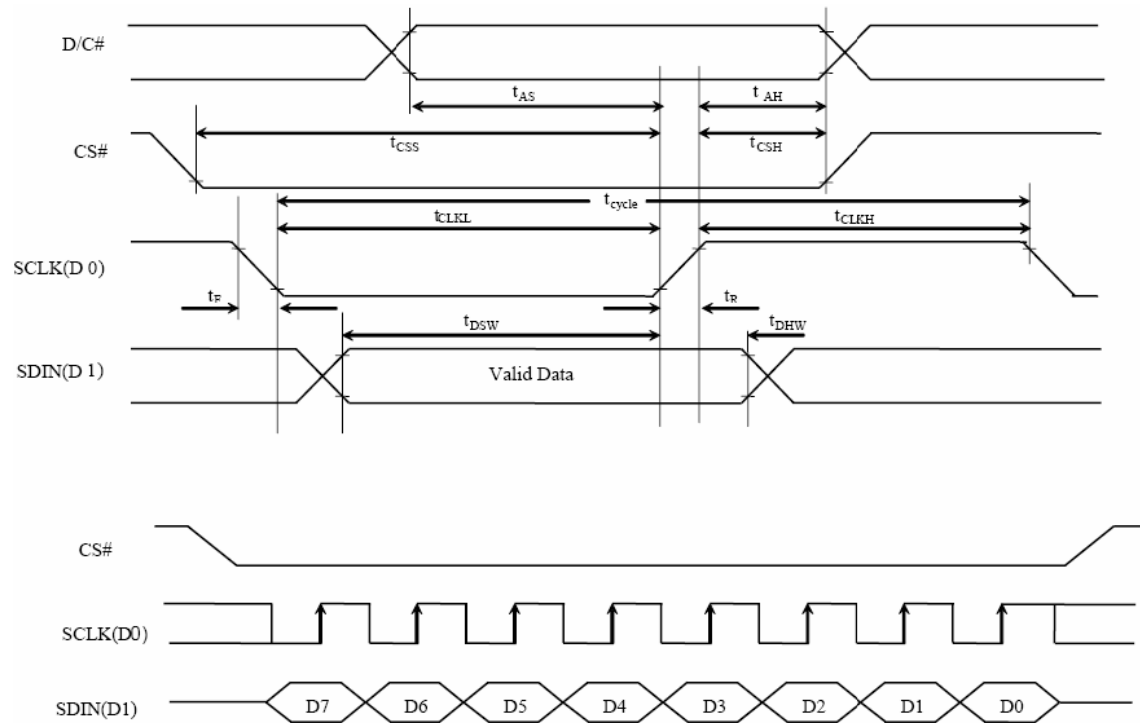
Symbol	Description	Min	Max	Unit
t _{cycle}	Clock Cycle Time	300	-	ns
t _{AS}	Address Setup Time	0	-	ns
t _{AH}	Address Hold Time	0	-	ns
t _{DSW}	Write Data Setup Time	40	-	ns
t _{DHW}	Write Data Hold Time	15	-	ns
t _{DHR}	Read Data Hold Time	20	-	ns
t _{OH}	Output Disable Time	-	70	ns
t _{ACC}	Access Time	-	140	ns
PW _{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse Width (Write)	60	-	ns
PW _{CSH}	Chip Select Setup High Pulse Width (Read)	60	-	ns
	Chip Select Setup High Pulse Width (Write)	60	-	ns
t _R	Rise Time	-	15	ns
t _F	Fall Time	-	15	ns



3.4.1.3 Serial Interface Timing Characteristics

VDD = 2.8V , Ta = 25°C

Symbol	Description	Min	Max	Unit
t _{cycle}	Clock Cycle Time	250	-	ns
t _{AS}	Address Setup Time	150	-	ns
t _{AH}	Address Hold Time	150	-	ns
t _{CSS}	Chip Select Setup Time	120	-	ns
t _{CSH}	Chip Select Hold Time	60	-	ns
t _{DSW}	Write Data Setup Time	100	-	ns
t _{DHW}	Write Data Hold Time	100	-	ns
t _{CLKL}	Serial Clock Low Time	100	-	ns
t _{CLKH}	Serial Clock High Time	100	-	ns
t _R	Rise Time	-	15	ns
t _F	Fall Time	-	15	ns



4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Brightness(White)	L _{br}	With Polarizer (Note 3)	70	100	-	cd/m ²
C.I.E.(White)	(X)	Without Polarizer	0.44	0.48	0.52	-
	(Y)		0.47	0.51	0.55	
Dark Room Contrast	CR		-	>1000:1	-	-
Viewing Angle			>160	-	-	degree

Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 15V.
 Software configuration follows Section 4.4 Initialization

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5 FUNCTIONAL SPECIFICATION

5.1 COMMANDS

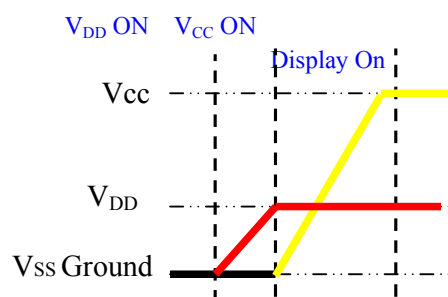
Please refer to the Technical Manual for the SSD1325

5.2 POWER UP/DOWN SEQUENCE

To protect panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the panel enough time to complete the action of charge and discharge before/after the operation.

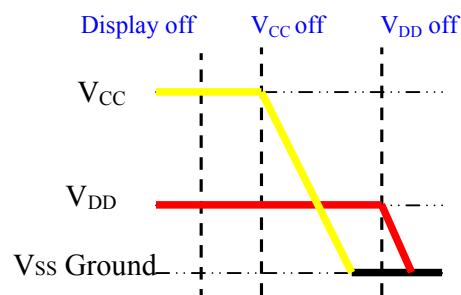
5.2.1 POWER UP SEQUENCE

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
(when V_{DD} is stable)
7. Send Display on command



5.2.2 POWER DOWN SEQUENCE

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
(When V_{PP} reach 0 and panel is completely discharges)
4. Power down V_{DD}



5.3 RESET CIRCUIT

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128x80 Display mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00H and COM0 mapped to row address 00H)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 80H
9. Normal display mode (Equivalent to A4h command)

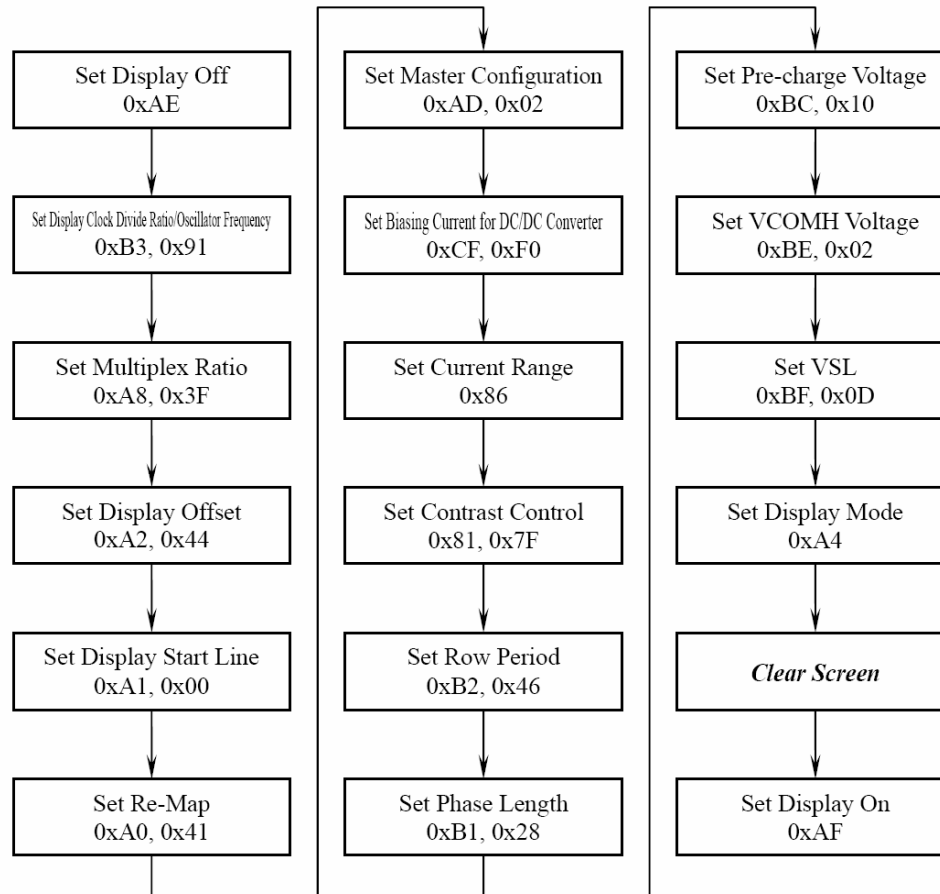
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5.4 ACTUAL APPLICATION EXAMPLE

Command usage and explanation of an actual example

<Initialisation Setting>

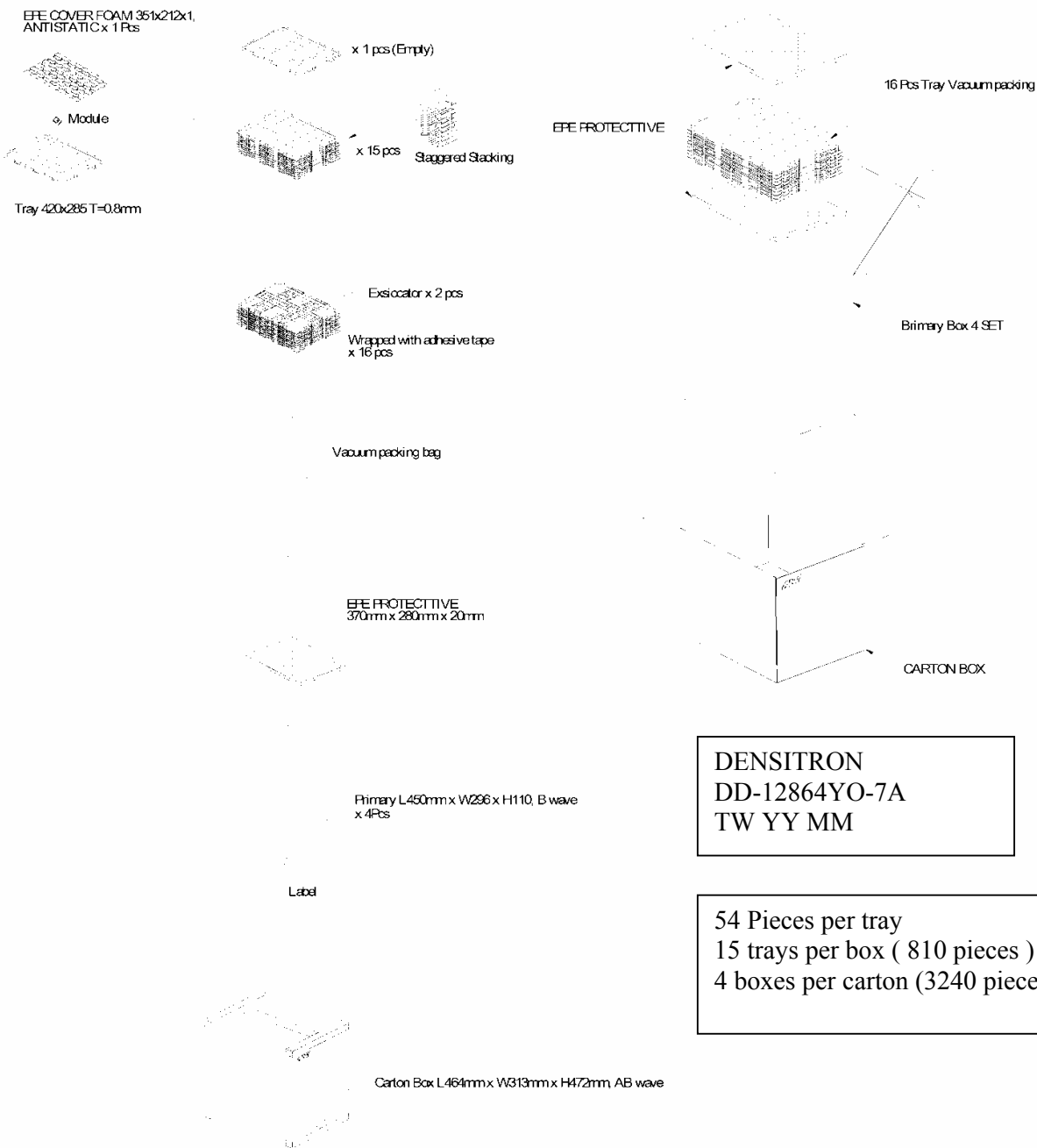


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

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6 PACKAGING AND LABELLING SPECIFICATION



DENSITRON
DD-12864YO-7A
TW YY MM

54 Pieces per tray
15 trays per box (810 pieces)
4 boxes per carton (3240 pieces)

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7 QUALITY ASSURANCE SPECIFICATION

7.1 CONFORMITY

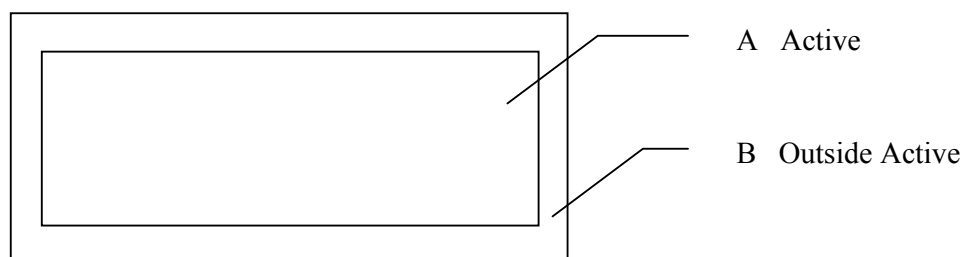
The performance, function and reliability of the shipped products conform to the Product Specification.

7.2 DELIVERY ASSURANCE

7.2.1 DELIVERY INSPECTION STANDARDS

IPC-AA610, class 2 electronic assemblies standard

7.2.2 Zone definition



7.2.3 Visual inspection

Test and measurement to be conducted under following conditions□

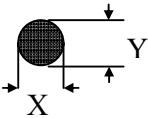
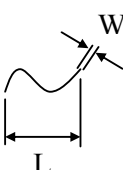
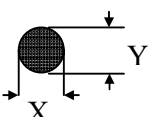
Temperature:	23±5°C
Humidity:	55±15%RH
Fluorescent lamp:	30 W
Distance between the Panel & Eyes of the Inspector:	≥30cm
Distance between the Panel & the lamp:	≥50cm

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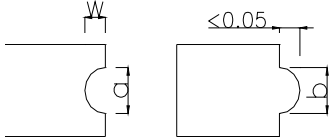
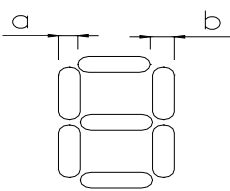
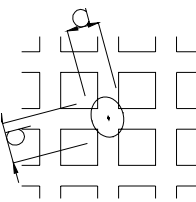
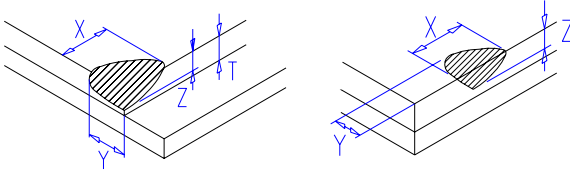
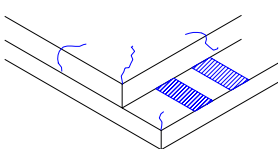
7.2.4 Standard of appearance inspection

Units: mm

Class	Item	Criteria																																			
Minor	Packing & Label	Outside & inside package	Presence of product no., lot no., quantity																																		
Critical		Product must not be mixed with others and quantity must not be different from that indicated on the label																																			
Major	Dimension	Product dimensions must be according to specification and drawing																																			
Major	Electrical	Product electrical characteristics must be according to specification																																			
Critical	OLED Display	Missing lines, short circuits or wrong patterns on OLED display are not allowed																																			
Minor	Black spot, white spot, dust	Round type: as per following drawing $\varnothing = (X+Y)/2$  <table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>$\varnothing < 0.1$</td><td>Any number</td><td rowspan="4">Any number</td></tr><tr><td>$0.1 < \varnothing < 0.2$</td><td>3</td></tr><tr><td>$0.2 < \varnothing < 0.25$</td><td>1</td></tr><tr><td>$0.25 < \varnothing$</td><td>0</td></tr></table> Line type: as per following drawing  <table><tr><th colspan="4">Acceptable quantity</th></tr><tr><th>Length</th><th>Width</th><th>Zone A</th><th>Zone B</th></tr><tr><td>--</td><td>$W \leq 0.05$</td><td>Any number</td><td rowspan="3">Any number</td></tr><tr><td>$L \leq 2.0$</td><td>$W \leq 0.1$</td><td>3</td></tr><tr><td>$L > 2.0$</td><td></td><td>0</td></tr></table> Total acceptable quantity: 3			Acceptable quantity			Size	Zone A	Zone B	$\varnothing < 0.1$	Any number	Any number	$0.1 < \varnothing < 0.2$	3	$0.2 < \varnothing < 0.25$	1	$0.25 < \varnothing$	0	Acceptable quantity				Length	Width	Zone A	Zone B	--	$W \leq 0.05$	Any number	Any number	$L \leq 2.0$	$W \leq 0.1$	3	$L > 2.0$		0
Acceptable quantity																																					
Size	Zone A	Zone B																																			
$\varnothing < 0.1$	Any number	Any number																																			
$0.1 < \varnothing < 0.2$	3																																				
$0.2 < \varnothing < 0.25$	1																																				
$0.25 < \varnothing$	0																																				
Acceptable quantity																																					
Length	Width	Zone A	Zone B																																		
--	$W \leq 0.05$	Any number	Any number																																		
$L \leq 2.0$	$W \leq 0.1$	3																																			
$L > 2.0$		0																																			
Minor	Polariser scratch	Scratch on protective film is permitted Scratch on polariser: same as No. 1																																			
Minor	Polariser bubble	$\varnothing = (X+Y)/2$  <table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>$\varnothing < 0.5$</td><td>Any number</td><td rowspan="2">Any number</td></tr><tr><td>$\varnothing > 0.5$</td><td>0</td></tr></table>			Acceptable quantity			Size	Zone A	Zone B	$\varnothing < 0.5$	Any number	Any number	$\varnothing > 0.5$	0																						
Acceptable quantity																																					
Size	Zone A	Zone B																																			
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$\varnothing > 0.5$	0																																				

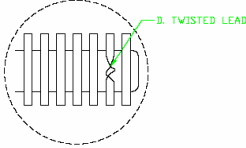
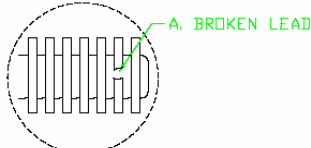
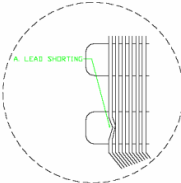
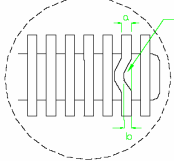
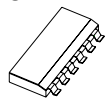
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Class	Item	Criteria																												
Minor	Segment deformation	1b. Pin hole on dot matrix display  <table><tr><th colspan="2">Acceptable quantity</th></tr><tr><th>Size</th><th></th></tr><tr><td>a,b<0.1</td><td>Any number</td></tr><tr><td>(a+b)/2<0.1</td><td>Any number</td></tr><tr><td>0.5<Ø<1.0</td><td>3</td></tr></table> Total acceptable quantity: 7 2. Segments / dots with different width  <table><tr><th colspan="2">Acceptable</th></tr><tr><td>a≥b</td><td>a/b≤4/3</td></tr><tr><td>a<b</td><td>a/b>4/3</td></tr></table> 3. Alignment layer defect Ø = (a+b)/2  <table><tr><th colspan="2">Acceptable quantity</th></tr><tr><th>Size</th><th></th></tr><tr><td>Ø≤0.4</td><td>Any number</td></tr><tr><td>0.4<Ø≤1.0</td><td>5</td></tr><tr><td>1.0<Ø≤1.5</td><td>3</td></tr><tr><td>1.5<Ø≤2.0</td><td>2</td></tr></table> Total acceptable quantity: 7	Acceptable quantity		Size		a,b<0.1	Any number	(a+b)/2<0.1	Any number	0.5<Ø<1.0	3	Acceptable		a≥b	a/b≤4/3	a<b	a/b>4/3	Acceptable quantity		Size		Ø≤0.4	Any number	0.4<Ø≤1.0	5	1.0<Ø≤1.5	3	1.5<Ø≤2.0	2
Acceptable quantity																														
Size																														
a,b<0.1	Any number																													
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0.4<Ø≤1.0	5																													
1.0<Ø≤1.5	3																													
1.5<Ø≤2.0	2																													
Minor	Panel Chipping	$X \leq 1/6$ Panel length $Y \leq 1$ $Z \leq T$ 																												
Minor	Panel Cracking	Cracks not allowed 																												
Minor	Copper exposed (pin or film)	Not allowed if visible by eye inspection																												
Minor	Film or Trace Damage	Not allowed if affect electrical function																												

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Class	Item	Criteria			
Minor	Contact Lead Twist	Not allowed			
Minor	Contact Lead Broken	Not allowed			
Minor	Contact Lead Bent	Not allowed if bent lead causes short circuit			
		Not allowed if bent lead extends horizontally more than 50% of its width			
Minor	Colour uniformity	Level of sample for approval set as limit sample			
Major	 PCB	No unmelted solder paste should be present on PCB			
Critical		Cold solder joints, missing solder connections, or oxidation are not allowed			
Minor		No residue or solder balls on PCB are allowed			
Critical		Short circuits on components are not allowed			
Minor	Tray particles		Size		Quantity
			On tray	$\varnothing < 0.2$	Any number
				$\varnothing > 0.25$	4
			On display	$\varnothing \geq 0.25$	2
				L = 3	1

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7.3 DEALING WITH CUSTOMER COMPLAINTS

7.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.
After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.

If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.

Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.

Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

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8 RELIABILITY SPECIFICATION

8.1 RELIABILITY TESTS

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	70°C, 240 hours	No abnormalities in function and appearance
Low Temperature Operation	-30°C, 240 hours	No abnormalities in function and appearance
High Temperature Storage	80°C, 240 hours	No abnormalities in function and appearance
Low Temperature Storage	-40°C, 240 hours	No abnormalities in function and appearance
High Temperature & High Humidity Storage	60°C, 90%RH, 240 hours	No abnormalities in function and appearance
Thermal Shock	24 cycle of -40°C 1 Hour, 85°C 1 Hour. 60 Mins dwell	No abnormalities in function and appearance

- The samples used for above tests do not include polarizer.
- No moisture condensation is observed during tests.

8.1.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5 °C; 55±15% RH

8.2 LIFE TIME

Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration more than 40,000 hours under 100 cd/m ² brightness and 50% Checkerboard, humidity (50% RH), and in area not exposed to direct sunlight.
2	End of lifetime is specified as 50% of initial brightness.

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9 HANDLING PRECAUTIONS

Safety

If the panel breaks, be careful not to get the organic substance in your mouth or in your eyes.
If the organic substance touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design

Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.

Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during OLED cleaning

Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotrifluoroethane.

Do not wipe the display surface with dry or hard materials that will damage the polariser surface.

Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge

As the display uses C-MOS LSI drivers, connect any unused input terminal to V_{DD} or V_{SS} . Do not input any signals before power is turned on.

Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging

Displays use OLED elements, and must be treated as such. Avoid strong shock and drop from a height.

To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation

It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.

Other Precautions

When a display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.

Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored.

Also, there will be no problem in the reliability of the module.

Storage

Store the display in a dark place where the temperature is $25^{\circ}\text{C} \pm 10^{\circ}\text{C}$ and the humidity below 50%RH.

Store the display in a clean environment, free from dust, organic solvents and corrosive gases.

Do not crash, shake or jolt the display (including accessories).

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