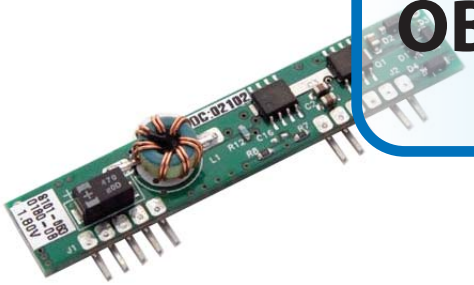
S101-084-S101-00

5.0v Input, 1.5 to 3.3v Output @ 7A

Murata Power Solutions

This product is not fuse protected. User is responsible for providing system protection. Consult factory for application information.

OBSOLETE PRODUCT



FEATURES

- Output Current up to 7A
- 5.0V ± 10% input
- Regulation ±0.4% Line and Load
- Industry Standard Pin Configuration
- High Efficiency To 90%
- Remote Sense, Trim and Enable
- Short Circuit Protection
- MTBF 3.9 million hours

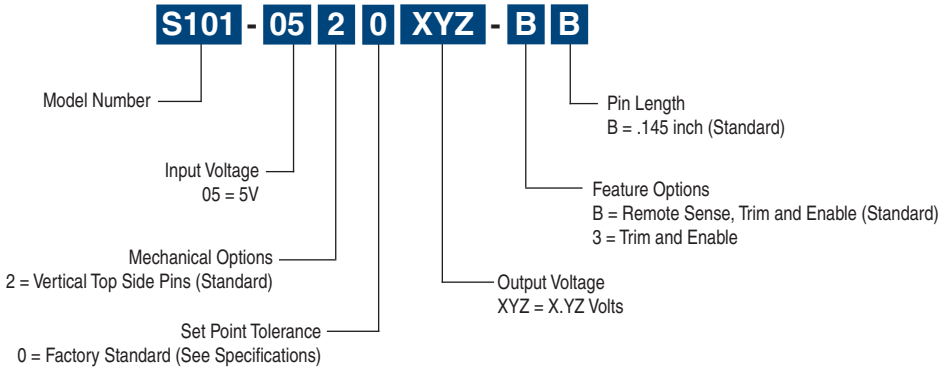
Specifications	S101-05	
INPUT SPECIFICATIONS		
Input voltage range	5.0V ± 10%	Measured at +Vin pin
External input capacitor	Minimum 330µF with adequate ripple current rating	See also note on pg 6 and chart on pg 4
OUTPUT SPECIFICATIONS		
Standard output voltages and output current	1.5V	Standard setpoint accuracy varies ±1.3%. Contact factory for tighter tolerances. See note on pg 5 for trimming to different voltages.
	1.8V	
	2.1V	
	2.5V	
	3.3V	
Output current	7A	100 LFM at 70°C
Load regulation	±0.4%	0 to 7A load
Line regulation	±0.4%	Over specified input voltage range
External output capacitor	>150µF with maxESR = 100mΩ	See also note on pg 6
Short circuit protection	200% of maximum rated current	
GENERAL SPECIFICATIONS		
Enable ***	ON - open or high / OFF - low	
Efficiency	90% for 3.3V	See efficiency curves on pg 4
Isolation	Non-isolated	
Switching frequency	300 kHz	Constant
Approvals and Standards	UL 94V-0	
Protection	Fusing	Unit is not fused.
Operating Temperature ****	0°C to 60°C	
Storage Temperature	-40°C to 125°C	Non-condensing
MTBF	4.1 million hours	Per RAC PRISM at 50°C ambient and 200 LFM

* All specifications are typical at nominal input, full load at 25°C unless otherwise stated.
*** Pull below 0.5V and sink greater than 1mA to disable the SIP; pull above 4V (do not exceed 12V) and source greater than 10µA or leave
open to enable the SIP.
**** The output capacitors must meet the max ESR = 100mΩ requirement over the operating temperature range.

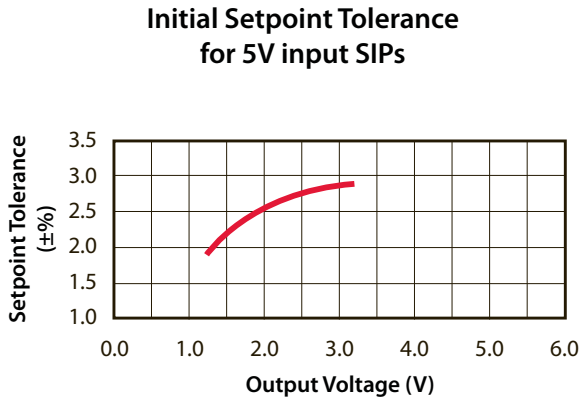
RoHS COMPLIANT 2002/95/EC

For full details go to www.murata-ps.com/rohs

PART NUMBER CODING



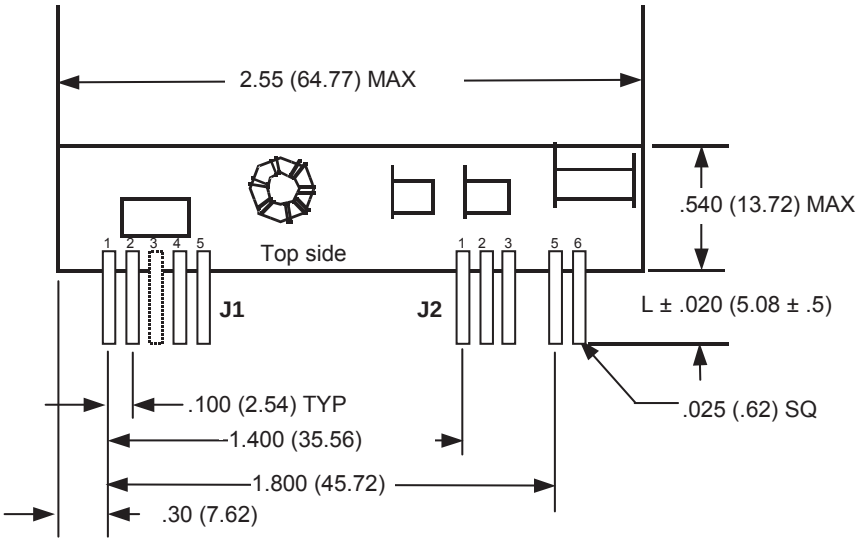
INITIAL SETPOINT TOLERANCE



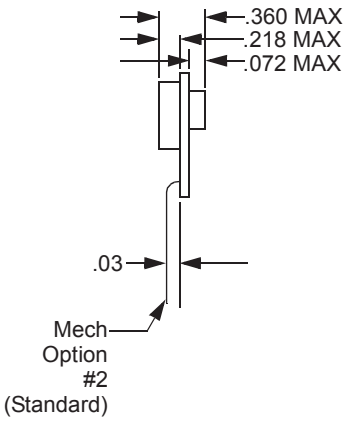
PIN ASSIGNMENT

CONNECTOR	PIN	FUNCTION	CONNECTOR	PIN	FUNCTION
J1	1	VOUT	J2	1	Ground
	2	VOUT		2	VIN
	3	Remote Sense		3	VIN
	4	VOUT		4	Empty
	5	Ground		5	Trim
				6	Enable

MECHANICAL DIMENSIONS



Mechanical Option 2

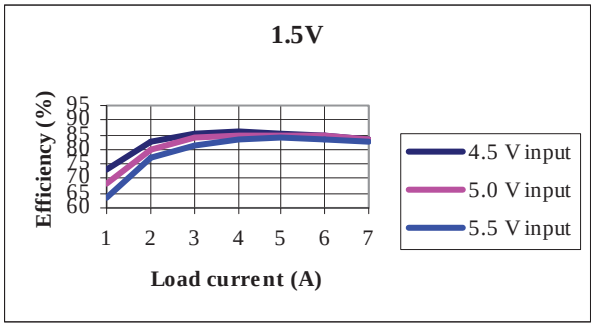


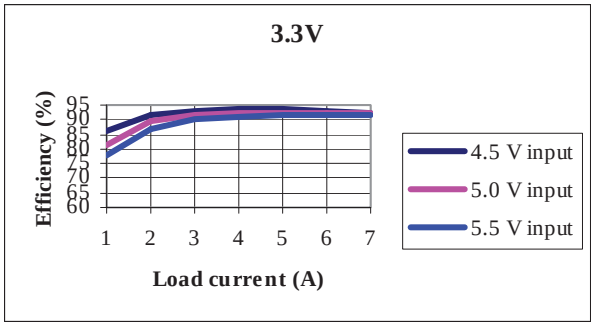
* Recommended Customer Hole Size 0.046 ±.003 with 0.070 pad both sides

1. Dimensions are in inches and (millimeters).
2. Tolerances: (unless otherwise noted)

	Inches	Millimeters
	.XX ± .020	.X ± 0.5
	.XXX ± .010	.XX ± 0.25
Pin:	± .002	± 0.05

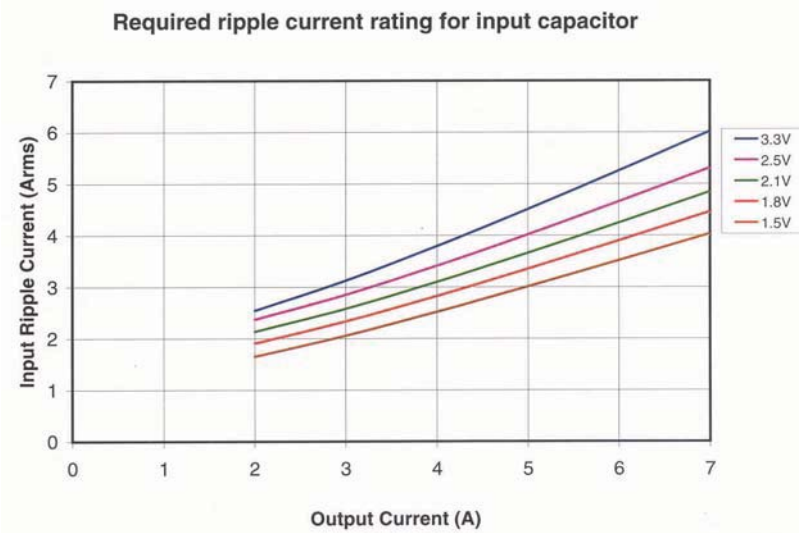
EFFICIENCY CURVES AT 25°C





INPUT RIPPLE CURRENT

Required ripple current ratings required for input bulk capacitor.



RESISTOR TRIM EQUATIONS

The S101 output voltage can be trimmed to a different value than the one set by the factory by using one external resistor. Check the following table for trimming range and use the appropriate trimming equation to calculate the value of the trim resistor.

V_{SET}	V_{REF}	R_8 (OHMS)	R_7 (OHMS)	TRIM RANGE
1.5V	1.3V	9760	63400	1.3V - 1.8V
1.8V	1.5V	10000	49900	1.5V - 2.1V
2.1V	1.7V	11500	48700	1.7V - 2.5V
2.5V	2.1V	12100	63400	2.1V - 3.3V
3.3V	2.5V	11500	35700	2.5V - 3.5V

Trimming Up ($V_{OutUp} > V_{Set}$)

Connect the Trim Up Resistor between the Trim pin (J1-5) and the Ground pin (J1-1).

$$R_{TrimUp} = \frac{1}{\left(\frac{V_{OutUp} - V_{Ref}}{R_8 * V_{Ref}} - \frac{1}{R_7} \right)}$$

Trimming Down ($V_{Ref} < V_{Out\ Down} < V_{Set}$)

Connect the Trim Down Resistor between the Trim pin (J1-5) and the Remote Sense pin (J1-3). If the sense pin is not present, use the Vout pin (J1-1 or J1-2 or J1-4).

$$R_{TrimDown} = \frac{1}{\frac{V_{Ref}}{R_7(V_{OutDown} - V_{Ref})} - \frac{1}{R_8}}$$

Where:

VSet:	the output setpoint (output voltage set by the factory, with no trim)
VOutUp:	the desired output voltage (higher than VSet)
VOutDown:	the desired output voltage (lower than VSet, but not lower than VRef)
VRef:	see table
R7, R8:	see table
RTrimUp, RTrimDown:	the resistance value of the trimming resistor

External Capacitance for SIP Products

All SIP products require external capacitance to be placed on the system board that the SIP will be designed into. This application note is an attempt to explain how to translate datasheet information and apply it to a system level board design.

INPUT CAPACITANCE
Although input capacitance value is not critical, the input capacitors must be capable of storing fairly large amounts of energy. This means, for example, small ceramic capacitors would be inappropriate. The primary criteria, though, for choosing the input capacitors is AC ripple current rating. The SIP datasheet contains a chart showing ripple current vs. output current (or output power). The system designer determines the maximum SIP output current required from the SIP. Based on that number, the chart will show a corresponding ripple current rating the designer needs to plan for when choosing input capacitors.

> Example using SIP S101:
> The designer knows the S101 is intended to provide 2.5V at maximum 5A. Using the S101 datasheet chart, this corresponds with 4A of ripple current. Also known is that the capacitor the designer hopes to use has a ripple current rating of 2.2A. Therefore, the designer must use two of the chosen capacitors in parallel for a total ripple current capability of 4.4A - which will be sufficient for the 4A requirement.

OUTPUT CAPACITANCE
The only requirement for capacitance value is for basic circuit stability of the SIP. That value is specified on the SIP datasheet—usually 150µF. The other consideration for output capacitance is the total effective ESR (Equivalent Series Resistance). As with ripple current, every capacitor has a specified ESR. When using multiple capacitors in parallel, this ESR is added exactly like parallel resistors. Therefore, more capacitors mean less ESR. The SIP datasheet specifies a maximum total ESR necessary for optimum SIP performance. The designer may also choose to add more capacitance to reduce output ripple and noise.

> Example using SIP S101:
> The S101 datasheet specifies a maximum ESR of 100mΩ for output capacitance. The system designer wants to use a capacitor with a specified ESR of 130mΩ. Since 130mΩ is more than the needed 100mΩ, two capacitors must be used in parallel for a total effective ESR of 65mΩ.

Generally, good, low ESR bulk capacitors will be used for both input and output capacitance so that fewer capacitors are needed since board real estate is usually an important factor in today's designs.

Impact on Output Voltage Ripple and Transient Response

If the customer's application requires a very low output voltage ripple and / or very low output voltage overshoot / undershoot during transients, then the guidelines previously shown need to be exceeded and good layout practices become mandatory.

By using four 330µF OSCON capacitors, each having ESR = 17mΩ, the output voltage ripple can be decreased to 50mVpk-pk on a 1.2V output SIP. Also during a transient load condition (load current steps from 20% to 100% and back, at 2 A / µsec) the output voltage does not overshoot / undershoot more than 100mV.

When fast and deep transient loads are expected, the input capacitor becomes important as well, especially if the SIP is far from its input voltage source. Capacitors having as much as 2000µF and combined ESR lower than 20mΩ might be needed.

Practical results heavily depend on physical layout and specific load conditions. For critical applications the customer is encouraged to consult with the manufacturer.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Murata:
S101-0520210-BB