

- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-IIIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$**
- **Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )**
- **Parity-Error Flag With Parity Generator/Checker**
- **Register for Storage of Parity-Error Flag**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

### description

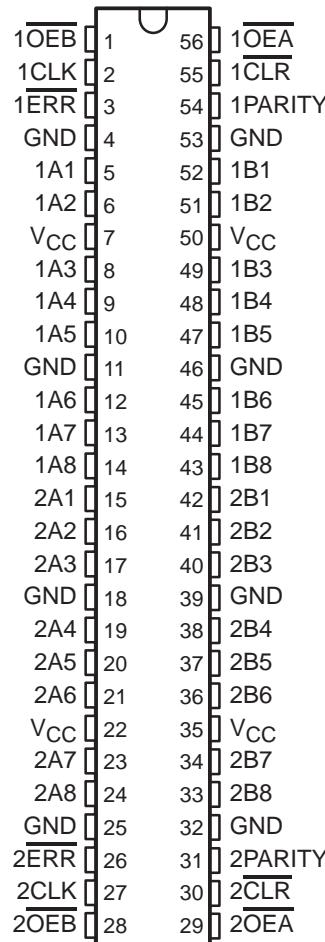
The 'ABT16833 consist of two noninverting 8-bit to 9-bit parity bus transceivers and are designed for communication between data buses. For each transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY). When data is transmitted from the B bus to the A bus, 1PARITY (or 2PARITY) is configured as an input and combined with the B-input data to generate an active-low error flag if odd parity is not detected.

The error ( $\overline{1ERR}$  or  $\overline{2ERR}$ ) output is configured as an open-collector output. The B-to-A parity-error flag is clocked into  $\overline{1ERR}$  (or  $\overline{2ERR}$ ) on the low-to-high transition of the clock (1CLK or 2CLK) input.  $\overline{1ERR}$  (or  $\overline{2ERR}$ ) is cleared (set high) by taking the clear ( $\overline{1CLR}$  or  $\overline{2CLR}$ ) input low.

The output-enable ( $\overline{OEA}$  and  $\overline{OEB}$ ) inputs can be used to disable the device so that the buses are effectively isolated. When both  $\overline{OEA}$  and  $\overline{OEB}$  are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ABT16833 . . . WD PACKAGE  
SN74ABT16833 . . . DGG OR DL PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus and EPIC-IIIB are trademarks of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1997, Texas Instruments Incorporated



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54ABT16833, SN74ABT16833 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS097D – FEBRUARY 1991 – REVISED JANUARY 1997

## description (continued)

The SN54ABT16833 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ABT16833 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
<u>OEB</u>	<u>OEA</u>	<u>CLR</u>	<u>CLK</u>	<u>Ai</u> $\Sigma$ OF H	<u>Bi</u> $\Sigma$ OF H	A	B	PARITY	<u>ERR</u> <sup>‡</sup>	
L	H	X	X	Odd	NA	NA	A	L	NA	A data to B bus and generate parity
				Even				H		
H	L	H	$\uparrow$	NA	Odd	B	NA	NA	H	B data to A bus and check parity
					Even				L	
X	X	L	X	X	X	X	NA	NA	H	Check error-flag register
									NC	
H	H	H	No $\uparrow$	X		Z	Z	Z	H	Isolation <sup>§</sup>
			No $\uparrow$	X	X				H	
			$\uparrow$	Odd					L	
			$\uparrow$	Even						
L	L	X	X	Odd	NA	NA	A	H	NA	A data to B bus and generate inverted parity
				Even				L		

NA = not applicable, NC = no change, X = don't care

<sup>†</sup> Summation of high-level inputs includes PARITY along with Bi inputs.

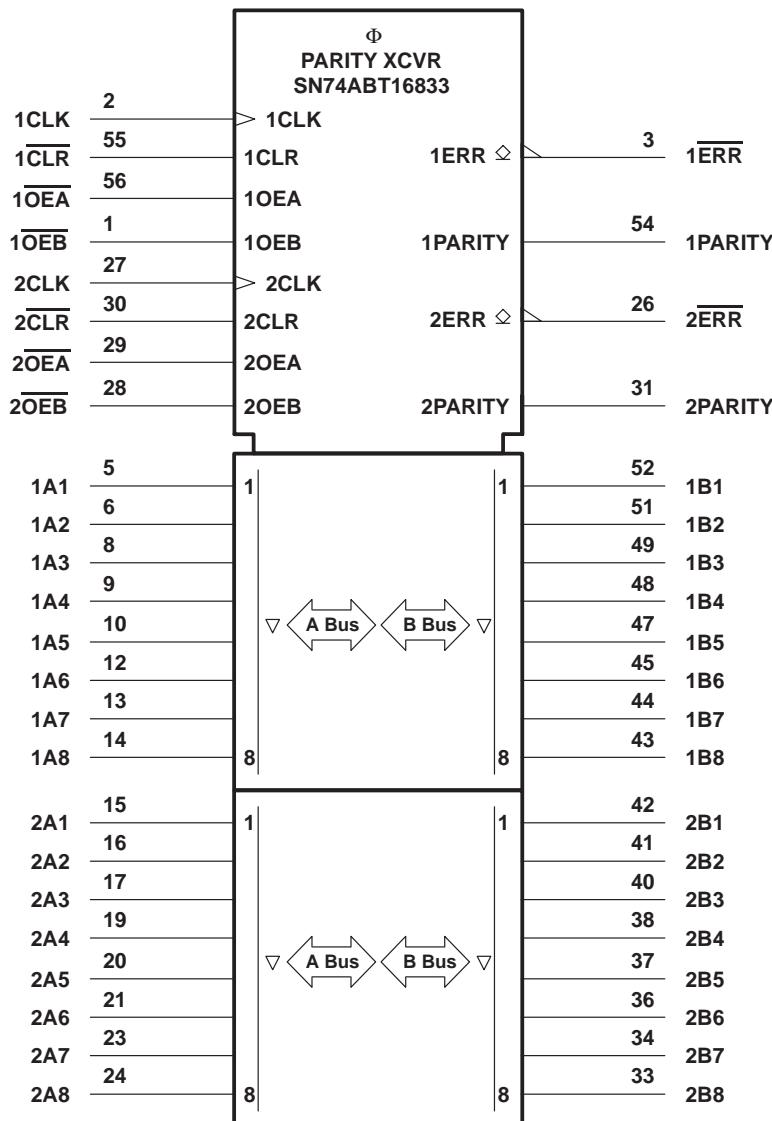
<sup>‡</sup> Output states shown assume ERR was previously high.

<sup>§</sup> In this mode, ERR (when clocked) shows inverted parity of the A bus.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic symbol†

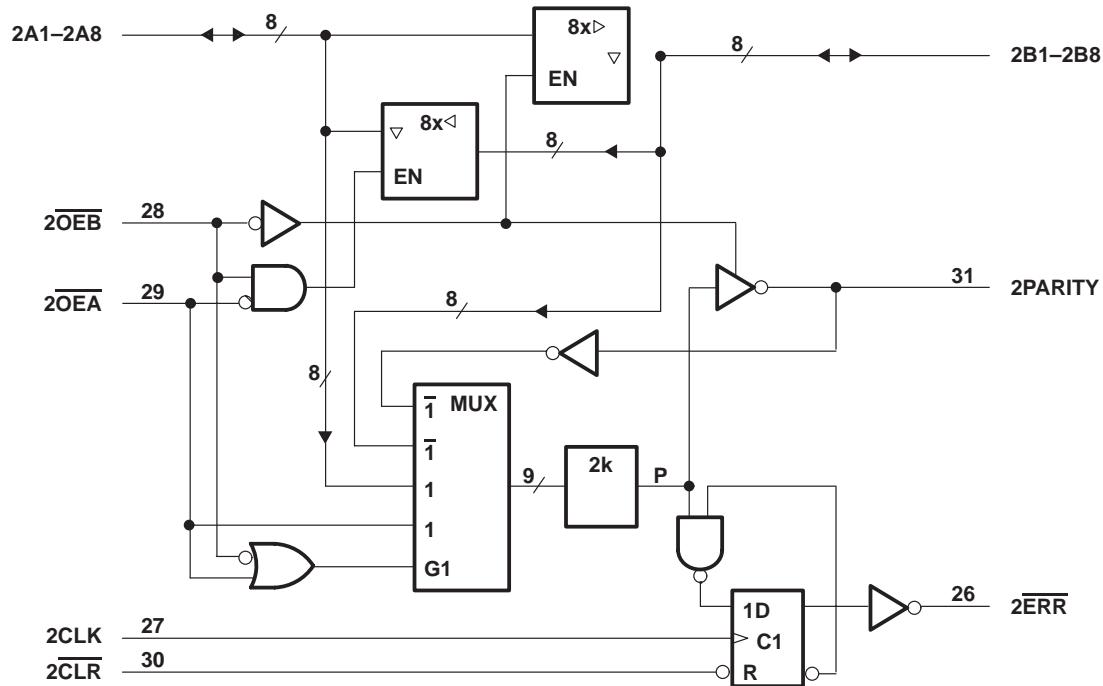
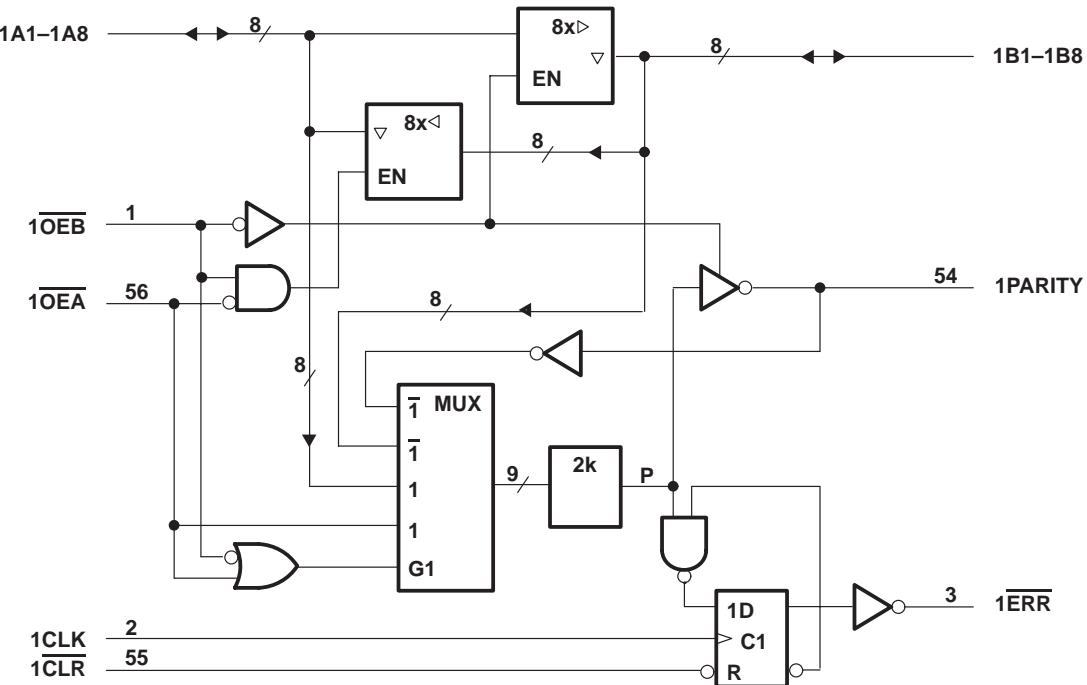


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54ABT16833, SN74ABT16833 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS097D – FEBRUARY 1991 – REVISED JANUARY 1997

## logic diagram (positive logic)

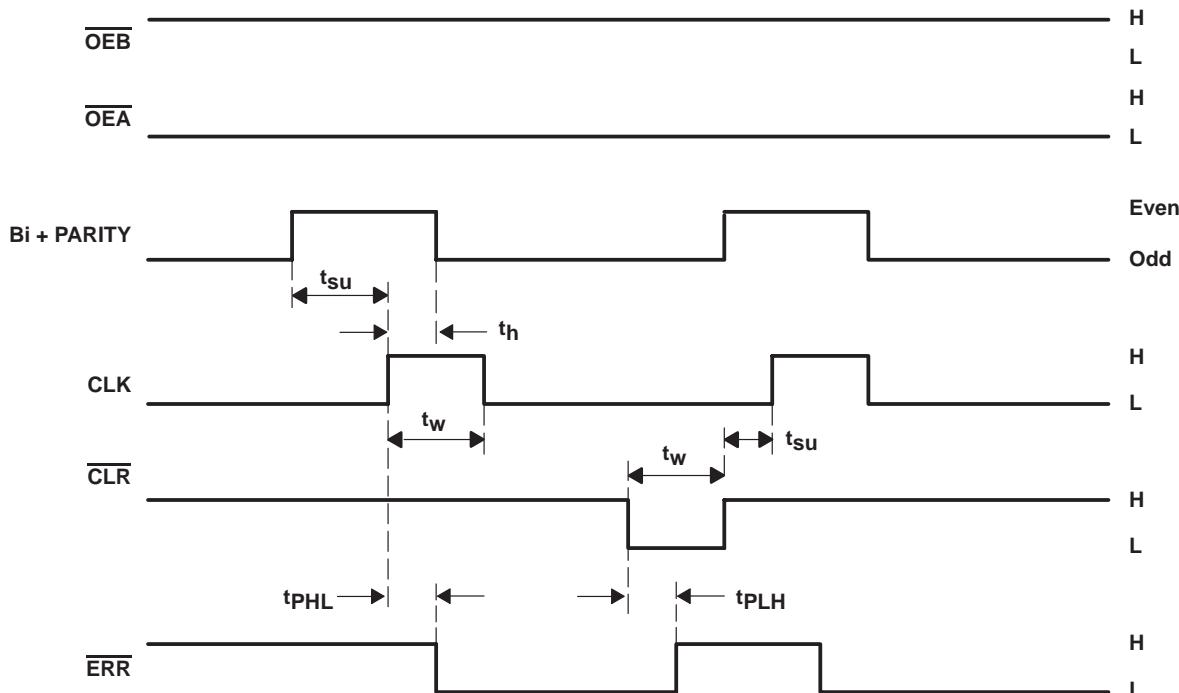


ERROR-FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT ERR	FUNCTION
CLR	CLK	POINT P	$\overline{ERR}_{n-1}^{\dagger}$		
H	↑	H	H	H	
H	↑	X	L	L	Sample
H	↑	L	X	L	
L	X	X	X	H	Clear

<sup>†</sup> State of  $\overline{ERR}$  before changes at CLR, CLK, or point P

### error-flag waveforms



# SN54ABT16833, SN74ABT16833 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS097D – FEBRUARY 1991 – REVISED JANUARY 1997

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

### **recommended operating conditions (see Note 3)**

		SN54ABT16833		SN74ABT16833		UNIT	
		MIN	MAX	MIN	MAX		
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V	
V <sub>IH</sub>	High-level input voltage	2		2		V	
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V	
V <sub>OH</sub>	High-level output voltage	ERR		5.5	5.5	V	
I <sub>OH</sub>	High-level output current	Except ERR		-24	-32	mA	
I <sub>OL</sub>	Low-level output current			48	64	mA	
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V	
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

**NOTE 3:** Unused pins (input or I/O) must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA = 25°C			SN54ABT16833		SN74ABT16833		UNIT	
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
VIK		VCC = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V	
V <sub>OH</sub>	All outputs except ERR	VCC = 4.5 V, I <sub>OH</sub> = -3 mA	2.5	3		2.5				V	
		VCC = 5 V, I <sub>OH</sub> = -3 mA	3	3.4		3		3			
		VCC = 4.5 V	I <sub>OH</sub> = -24 mA			2					
			I <sub>OH</sub> = -32 mA	2*	2.7			2			
V <sub>OL</sub>		VCC = 4.5 V	I <sub>OL</sub> = 24 mA	0.25	0.55		0.55			V	
			I <sub>OL</sub> = 64 mA	0.3	0.55*			0.55			
V <sub>hys</sub>				100						mV	
I <sub>OH</sub>	ERR	VCC = 4.5 V, V <sub>OH</sub> = 5.5 V			20		20		20	µA	
I <sub>off</sub>		VCC = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	µA	
I <sub>CEX</sub>	Outputs high	VCC = 5.5 V, V <sub>O</sub> = 5.5 V			50		50		50	µA	
I <sub>I</sub>	Control inputs	VCC = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND		±1		±1		±1		µA	
	A or B ports			±100		±100		±100			
I <sub>IL</sub>	A or B ports	VCC = 0, V <sub>I</sub> = GND			-50		-50		-50	µA	
I <sub>O</sub> ‡		VCC = 5.5 V, V <sub>O</sub> = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA	
I <sub>OZH</sub> §		VCC = 5.5 V, V <sub>O</sub> = 2.7 V			50		50		50	µA	
I <sub>OZL</sub> §		VCC = 5.5 V, V <sub>O</sub> = 0.5 V			-50		-50		-50	µA	
I <sub>CC</sub>	A or B ports	VCC = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high	1.5	2		2		2	mA	
			Outputs low	28	36		36		36		
			Outputs disabled	1	2		2		2		
ΔI <sub>CC</sub> ¶		VCC = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			50		50		50	µA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V		3						pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = 2.5 V or 0.5 V		9						pF	

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

# SN54ABT16833, SN74ABT16833 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS097D – FEBRUARY 1991 – REVISED JANUARY 1997

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			$V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$			SN54ABT16833		SN74ABT16833		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	
$t_W$	Pulse duration, CLK high or low		3		3		3		3	ns
$t_{SU}$	Setup time before CLK↑	A port	4.5		4.5		4.5		4.5	ns
		CLR	1		1		1		1	
		OE	5		5		5		5	
$t_h$	Hold time after CLK↑	A port or OE	0		0		0		0	ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

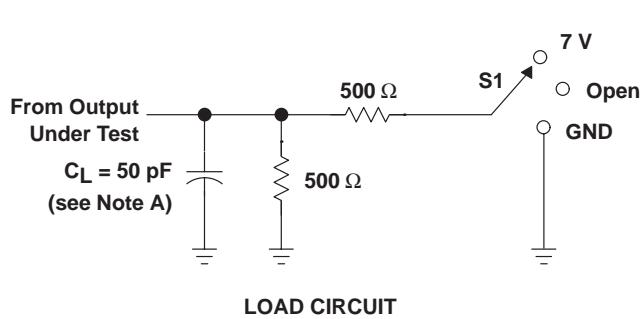
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$			SN54ABT16833		SN74ABT16833		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	1.5	2.5	3.3	1.5	4.2	1.5	4.1	ns
$t_{PHL}$			2	3.1	3.9	2	4.5	2	4.3	
$t_{PZH}$	OE	A or B	2	3.9	4.9	2	5.8	2	5.6	ns
$t_{PZL}$			2.5	4.3	5.1	2.5	6.2	2.5	6	
$t_{PHZ}$	OE	A or B	2	3.6	4.5	2	5.5	2	5.4	ns
$t_{PLZ}$			1.5	3	3.8	1.5	4.7	1.5	4.3	
$t_{PLH}$	A or OE	PARITY	2	4.6	5.4	2	7	2	6.7	ns
$t_{PHL}$			2	4.3	5.1	2	6.5	2	6.1	
$t_{PZH}$	OE	PARITY	2	3.6	5	2	5.8	2	5.7	ns
$t_{PZL}$			2.5	4.4	5.8	2.5	6.7	2.5	6.5	
$t_{PHZ}$	OE	PARITY	1.5	3.2	4	1.5	4.8	1.5	4.7	ns
$t_{PLZ}$			1.5	2.9	3.7	1.5	4.2	1.5	4.1	
$t_{PLH}$	CLK, CLR	ERR	2	3.4	4.2	2	4.8	2	4.6	ns
$t_{PHL}$	CLK		2	2.8	3.6	2	4.1	2	3.9	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



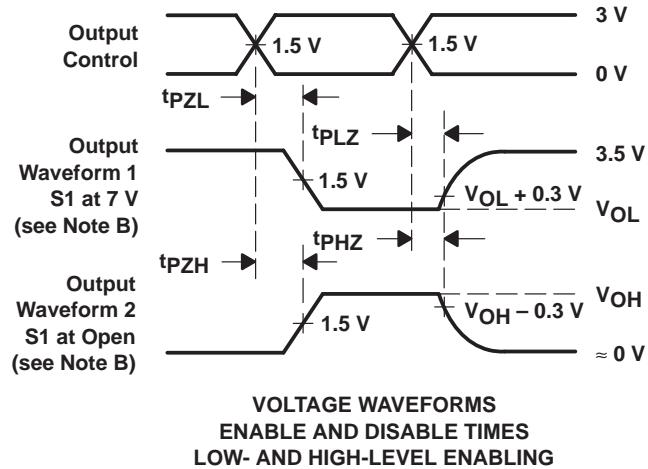
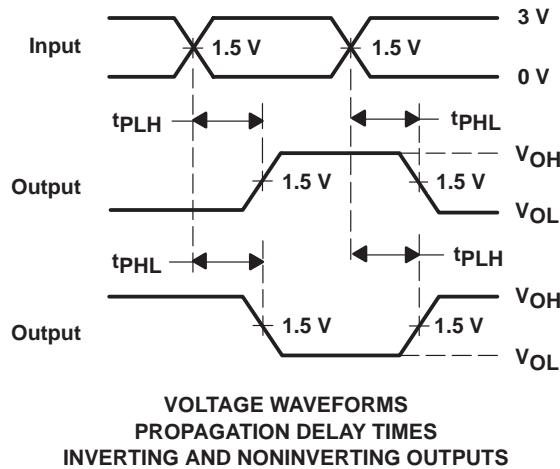
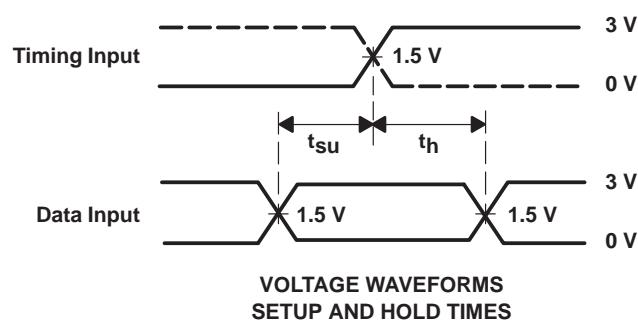
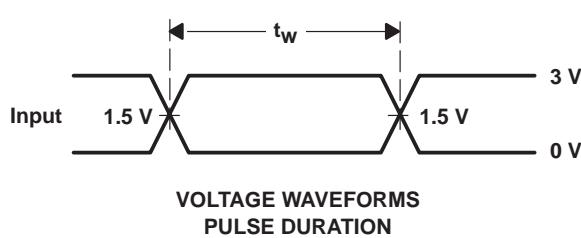
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open

ERR	S1
$t_{PHL}$ (see Note E)	7 V
$t_{PLH}$ (see Note F)	7 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .

D. The outputs are measured one at a time with one transition per measurement.

E.  $t_{PHL}$  is measured at 1.5 V.

F.  $t_{PLH}$  is measured at  $V_{OL} + 0.3 \text{ V}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74ABT16833DGGRE4	ACTIVE	TSSOP	DGG	56		TBD	Call TI	Call TI
74ABT16833DGGRG4	ACTIVE	TSSOP	DGG	56		TBD	Call TI	Call TI
SN74ABT16833DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16833DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16833DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16833DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

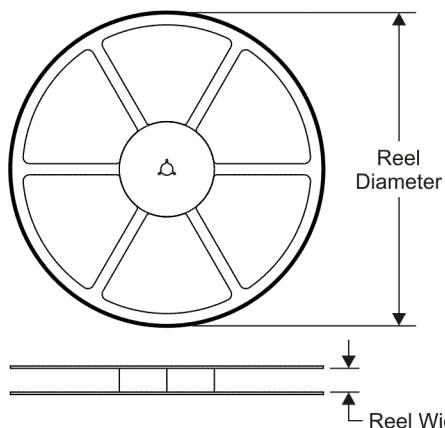
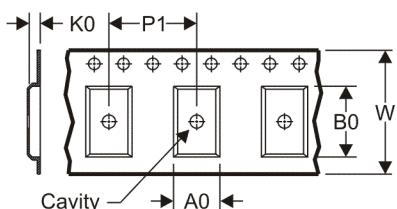
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

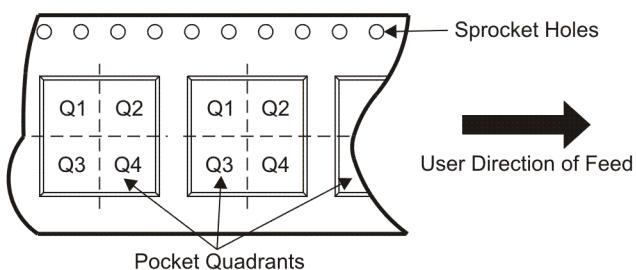
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16833DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16833DLR	SSOP	DL	56	1000	346.0	346.0	49.0

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2009, Texas Instruments Incorporated