SPEAr310

Embedded MPU with ARM926 core, flexible memory support, extended set of powerful connectivity features

Features

- ARM926EJ-S 333 MHz core
- High-performance 8-channel DMA
- Dynamic power-saving features
- Configurable peripheral functions multiplexed on 102 shared I/Os
- Memory:
  - 32 KB ROM and 8 KB internal SRAM
  - LPDDR-333/DDR2-666 external memory interface
  - Serial Flash Memory interface (SMI)
  - Flexible static memory controller (FSMC) up to 16-bit data bus width, supporting NAND Flash
  - External memory interface (EMI) up to 32-bit data bus width, supporting NOR Flash and FPGAs
- Connectivity
  - 2 x USB 2.0 Host
  - USB 2.0 Device
  - 1 x fast Ethernet MII port
  - 4 x fast Ethernet SMII ports
  - 1 x SSP Synchronous serial peripheral (SPI, Microwire or TI protocol) with 4 chip selects
  - 1 x I^2C
  - 1 x fast IrDA interface
  - 6 x UART interface
  - 1x TDM/E1 HDLC interface with 128/32 timeslots per frame respectively
  - 2x RS485 HDLC ports
- Security
  - C3 Cryptographic accelerator
- Miscellaneous functions
  - Integrated real time clock, watchdog, and system controller
  - 8-channel 10-bit ADC, 1 Msps

LFBGA289 (15 x 15 x 1.7 mm)

  - JPEG CODEC accelerator
  - Six 16-bit general purpose timers with programmable prescaler, 4 capture inputs
  - Up to 102 GPIOs with interrupt capability

Applications

The SPEAr310 embedded MPU is configurable for a range of telecom and networking applications such as:

- Routers, switches and gateways
- Remote apparatus control
- Metering concentrators

Table 1. Device summary

Order code	Temp range, °C	Package	Packing
SPEAR310-2	-40 to 85	LFBGA289 (15x15 mm, pitch 0.8 mm)	Tray

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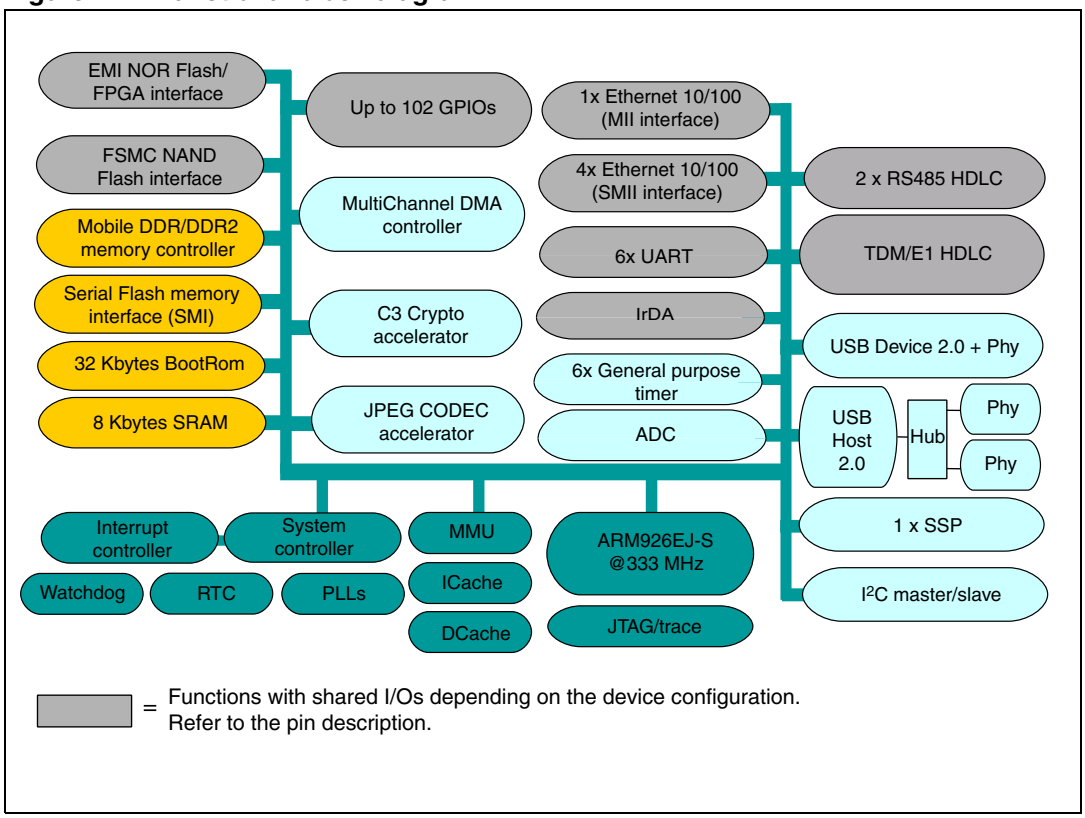
1 Description

The SPEAr310 is a member of the SPEAr family of embedded MPUs, optimized for telecom applications. It is based on the powerful ARM926EJ-S processor (up to 333 MHz), widely used in applications where high computation performance is required.

In addition, SPEAr310 has an MMU that allows virtual memory management -- making the system compliant with advanced operating systems, like Linux. It also offers 16 KB of data cache, 16 KB of instruction cache, JTAG and ETM (embedded trace macro-cell) for debug operations.

A full set of peripherals allows the system to be used in many applications, some typical applications being routers, switches and gateways as well as remote apparatus control and metering concentrators.

Figure 1. Functional block diagram



- ARM926EJ-S 32-bit RISC CPU, up to 333 MHz
  - 16 Kbytes of instruction cache, 16 Kbytes of data cache
  - 3 instruction sets: 32-bit for high performance, 16-bit (Thumb) for efficient code density, Java mode (Jazelle™) for direct execution of Java bytecode.
  - AMBA bus interface
- 32-KByte on-chip BootROM
- 8-KByte on-chip SRAM
- External DRAM memory interface:
  - 8/16-bit (mobile DDR@166 MHz)
  - 8/16-bit (DDR2@333 MHz)
- Serial memory interface
- 8/16-bits NAND Flash controller (FSMC)
- External memory interface (EMI) for connecting NOR Flash or FPGAs
- Boot capability from NAND Flash, serial/parallel NOR Flash
- Boot and field upgrade capability from USB
- High performance 8-channel DMA controller
- TDM/E1 HDLC, six-signal interface supporting duplex Tx/Rx communication
  - For TDM applications, up to 8 Mbps per Tx/Rx channel
    128 timeslots per frame (125 µs)
  - For E1 applications, up to 2 Mbps per Tx/Rx channel
    32 timeslots per frame (125 µs)
  - Compliant with ISO/IEC13239
  - Standard HDLC frame code/decode
- 2x RS485 HDLC ports:
  - Five interface signals
  - Supports duplex Tx/Rx communication
  - Maximum Tx/Rx data rate 3.88 Mbps
- 4x Ethernet MAC 10/100 Mbps with SMII PHY interface
- 1x Ethernet MAC 10/100 Mbps with MII PHY interface
- Two USB2.0 host (high-full-low speed) with integrated PHY transceiver
- One USB2.0 device (high-full-low speed) with integrated PHY transceiver
- Up to 102 GPIOs with interrupt capability
- Synchronous serial port (SSP), master/slave (supporting SPI, Microwire and TI sync protocols) up to 41.5 Mbps
- I^2C master/slave interface (slow-fast-high speed, up to 1.2 Mb/s)
- 1x UART with hardware flow control (up to 3 Mbps)
- 5x UARTs with software flow control (up to 5 Mbps)
- ADC 10-bit, 1 Msps 8 inputs
- JPEG CODEC accelerator 1 clock/pixel
- C3 Crypto accelerator (DES/3DES/AES/SHA1)
- Advanced power saving features
  - Normal, Slow, Doze and Sleep modes
  - CPU clock with software-programmable frequency

  - Enhanced dynamic power-domain management
  - Clock gating functionality
  - Low frequency operating mode
  - Automatic power saving controlled from application activity demands
- Vectored interrupt controller
- System and peripheral controller
  - 3 pairs of 16-bits general purpose timers with programmable prescaler
  - RTC with separate power supply allowing battery connection
  - Watchdog timer
  - Miscellaneous registers array for embedded MPU configuration
- Programmable PLL for CPU and system clocks
- JTAG IEEE 1149.1
- Boundary scan
- ETM functionality multiplexed on primary pins
- Supply voltages
  - 1.2 V core, 1.8 V/2.5 V DDR, 2.5 V PLLs, 1.5 V RTC and 3.3 V I/Os
- Operating temperature: - 40 to 85 °C
- LFBGA289 (15 x 15 mm, pitch 0.8 mm)

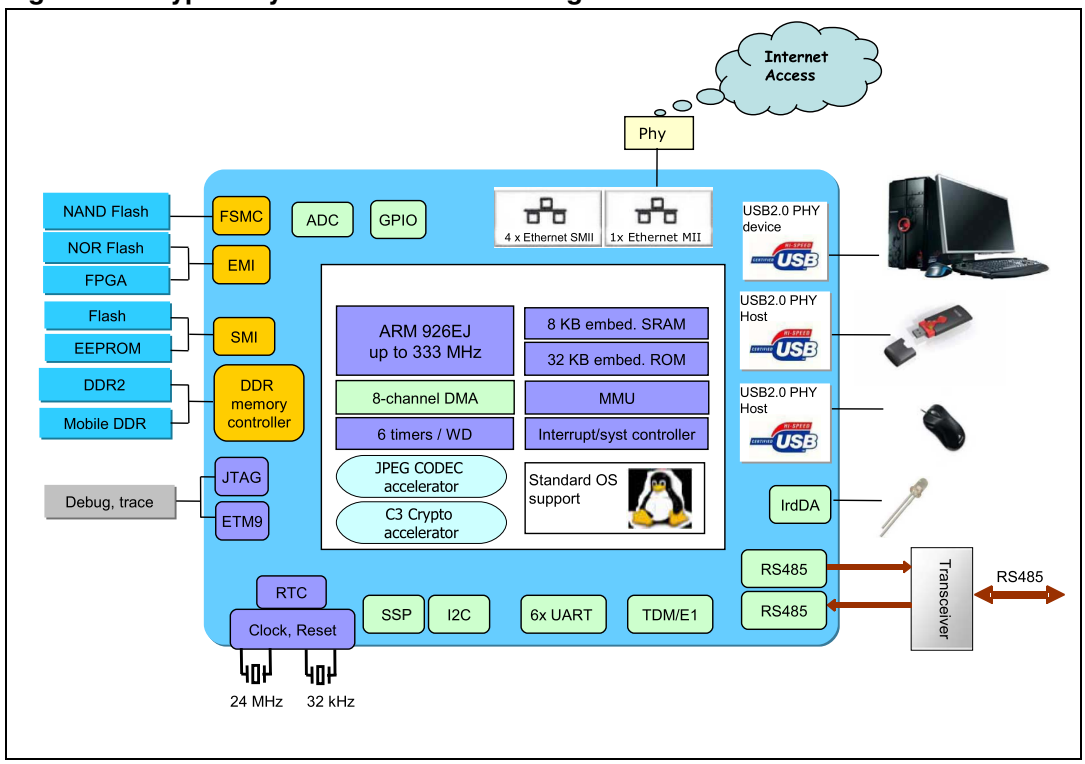
2 Architecture overview

The SPEAr310 internal architecture is based on several shared subsystem logic blocks interconnected through a multilayer interconnection matrix.

The switch matrix structure allows different subsystem dataflow to be executed in parallel improving the core platform efficiency.

High performance master agents are directly interconnected with the memory controller reducing the memory access latency. The overall memory bandwidth assigned to each master port can be programmed and optimized through an internal efficient weighted round-robin arbitration mechanism.

Figure 2. Typical system architecture using SPEAr310



2.1 CPU ARM 926EJ-S

The core of the SPEAr310 is an ARM926EJ-S reduced instruction set computer (RISC) processor.

It supports the 32-bit ARM and 16-bit Thumb instruction sets, enabling the user to trade off between high performance and high code density and includes features for efficient execution of Java byte codes.

The ARM CPU is clocked at a frequency up to 333 MHz. It has a 16-Kbyte instruction cache, a 16-Kbyte data cache, and features a memory management unit (MMU) which makes it fully compliant with Linux and WindowsCE operating systems.

It also includes an embedded trace module (ETM Medium+) for real-time CPU activity tracing and debugging. It supports 4-bit and 8-bit normal trace mode and 4-bit demultiplexed trace mode, with normal or half-rate clock.

2.2 System controller

The System Controller provides an interface for controlling the operation of the overall system.

Main features:

- Power saving system mode control
- Crystal oscillator and PLL control
- Configuration of system response to interrupts
- Reset status capture and soft reset generation
- Watchdog and timer module clock enable

2.2.1 Clock and reset system

The clock system is a fully programmable block that generates all the clocks necessary to the chip (see *Figure 3*).

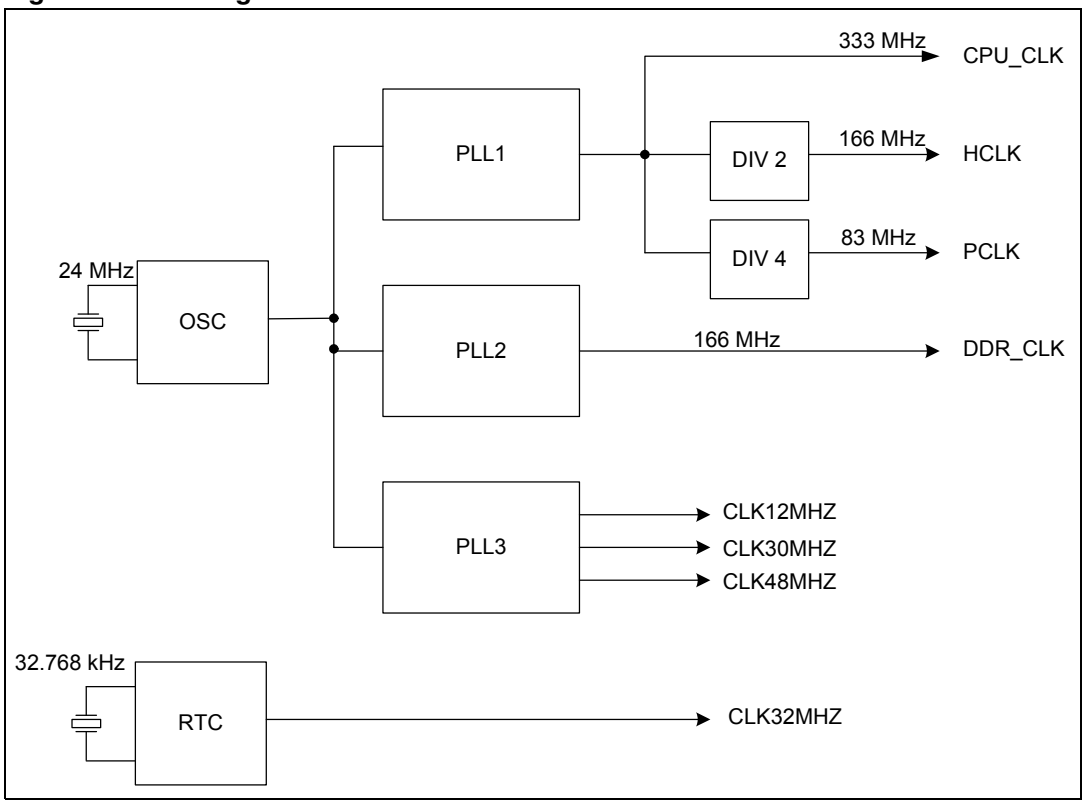
The default operating clock frequencies are:

- CPU_CLK @ 333 MHz for the CPU.
- HCLK @ 166 MHz for AHB bus and AHB peripherals.
- PCLK @ 83 MHz for, APB bus and APB peripherals.
- DDR_CLK @ 100-333 MHz for DDR memory interface.

The default values give the maximum allowed clock frequencies. The clock frequencies are fully programmable through dedicated registers.

The clock system consists of 2 main parts: a multi clock generator block and three internal PLLs.

Figure 3. Clock generator overview



The multi clock generator block, takes a reference signal (which is usually delivered by the PLL), generates all clocks for the IPs of SPEAr310 according to dedicated programmable registers.

Each PLL uses an oscillator input of 24 MHz to generate a clock signal at a frequency corresponding at the highest of the group. This is the reference signal used by the multi clock generator block to obtain all the other requested clocks for the group. Its main feature is electromagnetic interference reduction capability.

The user can set up the PLL in order to modulate the VCO with a triangular wave. The resulting signal has a spectrum (and power) spread over a small programmable range of frequencies centered on F0 (the VCO frequency), obtaining minimum electromagnetic emissions. This method replaces all the other traditional methods of EMI reduction, such as filtering, ferrite beads, chokes, adding power layers and ground planes to PCBs, metal shielding and so on. This gives the customer appreciable cost savings.

In sleep mode the SPEAr310 runs with the PLL disabled so the available frequency is 24 MHz or a sub-multiple (/2, /4, /8).

2.2.2 Power saving system mode control

Using three mode control bits, the system controller switch the SPEAr310 to any one of four different modes: DOZE, SLEEP, SLOW and NORMAL.

- **SLEEP mode**: In this mode the system clocks, HCLK and CPU_CLK, are disabled and the System Controller clock is driven by a low speed oscillator (nominally 32768 Hz). When either a FIQ or an IRQ interrupt is generated (through the VIC) the system enters

DOZE mode. Additionally, the operating mode setting in the system control register automatically changes from SLEEP to DOZE.

- **DOZE mode**: In this mode the system clocks, HCLK and CPU_CLK, and the System Controller clock are driven by a low speed oscillator. The System Controller moves into SLEEP mode from DOZE mode only when none of the mode control bits are set and the processor is in Wait-for-interrupt state. If SLOW mode or NORMAL mode is required the system moves into the XTAL control transition state to initialize the crystal oscillator.
- **SLOW mode**: During this mode, both the system clocks and the System Controller clock are driven by the crystal oscillator. If NORMAL mode is selected, the system goes into the "PLL control" transition state. If neither the SLOW nor the NORMAL mode control bits are set, the system goes into the "Switch from XTAL" transition state.
- **NORMAL mode**: In NORMAL mode, both the system clocks and the System Controller clock are driven by the PLL output. If the NORMAL mode control bit is not set, then the system goes into the "Switch from PLL" transition state.

2.2.3 Vectored interrupt controller (VIC)

The VIC allows the OS interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. There are 32 interrupt lines and the VIC uses a separate bit position for each interrupt source. Software controls each request line to generate software interrupts.

2.2.4 General purpose timers

SPEAr310 provides three general purpose timers (GPTs) acting as APB slaves. The timers can capture input signals from up to 4 external pins (enabled as PL_GPIO alternate functions).

Each GPT consists of 2 channels, each one made up of a programmable 16-bit counter and a dedicated 8-bit timer clock prescaler. The programmable 8-bit prescaler performs a clock division by 1 up to 256, and different input frequencies can be chosen through configuration registers (a frequency range from 3.96 Hz to 48 MHz can be synthesized).

Two different modes of operation are available :

- Auto-reload mode, an interrupt source is activated, the counter is automatically cleared and then it restarts incrementing.
- Single-shot mode, an interrupt source is activated, the counter is stopped and the GPT is disabled.

2.2.5 Watchdog timer

The ARM watchdog module consists of a 32-bit down counter with a programmable timeout interval that has the capability to generate an interrupt and a reset signal on timing out. The watchdog module is intended to be used to apply a reset to a system in the event of a software failure.

2.2.6 RTC oscillator

The RTC provides a 1-second resolution clock. This keeps time when the system is inactive and can be used to wake the system up when a programmed alarm time is reached. It has a

clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

Main features:

- Time-of-day clock in 24 hour mode
- Calendar
- Alarm capability
- Isolation mode, allowing RTC to work even if power is not supplied to the rest of the device.

2.3 Multichannel DMA controller

Within its basic subsystem, SPEAr310 provides an DMA controller (DMAC) able to service up to 8 independent DMA channels for sequential data transfers between single source and destination (i.e., memory-to-memory, memory-to-peripheral, peripheral to- memory, and peripheral-to-peripheral).

Each DMA channel can support a unidirectional transfer, with internal four-word FIFO per channel.

2.4 Embedded memory units

- 32 Kbytes of BootROM
- 8 Kbytes of SRAM

2.5 Mobile DDR/DDR2 memory controller

SPEAr310 integrates a high performance multi-channel memory controller able to support low power Mobile DDR and DDR2 double data rate memory devices. The multi-port architecture ensures memory is shared efficiently among different high-bandwidth client modules.

It has 6 internal ports. One of them is reserved for register access during the controller initialization while the other five are used to access the external memory.

It also includes the physical layer (PHY) and DLLs for fine tuning the timing parameters to maximize the data valid windows at different frequencies.

2.6 Serial memory interface

SPEAr310 provides a serial memory interface (SMI) to SPI-compatible off-chip memories.

These serial memories can be used either as data storage or for code execution.

Main features:

- Supports the following SPI-compatible Flash and EEPROM devices:
  - STMicroelectronics M25Pxxx, M45Pxxx
  - STMicroelectronics M95xxx, except M95040, M95020 and M95010
  - ATMEL AT25Fxx
  - YMC Y25Fxx
  - SST SST25LFxx
- Acts always as a SPI master and up to 2 SPI slave memory devices are supported (with seperate chip select signals), with up to 16 MB address space each
- SMI clock signal (SMICLK) is generated by SMI (and input to all slaves)
- SMICLK can be up to 50 MHz in fast read mode (or 20 MHz in normal mode). It can be controlled by a programmable 7-bit prescaler allowing up to 127 different clock frequencies.

2.7 External memory interface (EMI)

The EMI Controller provides a simple external memory interface that can be used for example to connect to NOR Flash memory or FPGA devices.

Main features:

- Multiplexed address and data bus.
- EMI bus master
- 32, 16, 8-bit transfers.
- Can access 6 different peripherals using CS#, one at a time.
- Supports single asynchronous transfers.
- Supports peripherals which use Byte Lane procedure

2.8 Flexible static memory controller (FSMC)

SPEAr310 provides a Flexible Static Memory Controller (FSMC) which interfaces the AHB bus to external parallel NAND Flash memories.

Main features:

- 8/16-bit wide data path
- FSMC performs only one access at a time and only one external device is accessed.
- Supports little-endian and big-endian memory architectures.
- AHB burst transfer handling to reduce access time to external devices.
- Supplies an independent configuration for each memory bank.
- Programmable timings to support a wide range of devices.
  - Programmable wait states (up to 31).
  - Programmable bus turnaround cycles (up to 15).
  - Programmable output enable and write enable delays (up to 15).
- Independent chip select control for each memory bank.
- Shares the address bus and the data bus with all the external peripherals.
- Only chips selects are unique for each peripheral.
- External asynchronous wait control.

2.9 UARTs

The SPEAr310 has 5 UARTs featuring software flow control and 1 UART featuring hardware and/or software flow control.

2.9.1 UART with hardware flow control

Main features:

- Separate 16 x 8 (16 locations deep x 8-bit wide) transmit and 16 x 12 receive FIFOs to reduce CPU interrupts
- Speed up to 3 Mbps
- Hardware and/or software flow control

2.9.2 UARTs with software flow control

Main features:

- Separate 16 x 8 (16 location deep x 8-bit wide) transmit and 16 x 12 receive FIFOs to reduce CPU interrupts
- Speed up to 5 Mbps.

2.10 Synchronous serial port (SSP)

SPEAr310 provides one synchronous serial port (SSP) block that offers a master or slave interface to enables synchronous serial communication with slave or master peripherals.

Main features:

- Master or slave operation.
- Programmable clock bit rate and prescale.
- Separate transmit and receive first-in, first-out memory buffers, 16-bits wide, 8 locations deep.
- Programmable choice of interface operation:
  - SPI (Motorola)
  - Microwire (National Semiconductor)
  - TI synchronous serial.
- Programmable data frame size from 4 to 16-bits.
- Independent masking of transmit FIFO, receive FIFO, and receive overrun interrupts.
- Internal loopback test mode available.
- DMA interface
- 4 chip selects available for non concurrent operations on 4 different devices.

2.11 I2C

Main features:

- Compliance to the I^2C bus specification (Philips)
- Supports three modes:
  - Standard (100 kbps)
  - Fast (400 kbps)
  - High-speed (3.4 Mbps)
- Clock synchronization
- Master and slave mode configuration possible
- Multi-master mode (bus arbitration)
- 7-bit or 10-bit addressing
- 7-bit or 10-bit combined format transfers
- Slave bulk transfer mode
- Ignores CBUS addresses (predessor to I2C that used to share the I2C bus)
- Transmit and receive buffers
- Interrupt or polled-mode operation
- handles bit and byte waiting at all bus speeds
- Digital filter for the received SDA and SCL lines
- Handles component parameters for configurable software driver support

2.12 TDM/E1 HDLC controller

SPEAr310 features a TDM/E1 HDLC controller which is composed of two main blocks: Time Division Multiplexing (TDM) and High-level Data Link Control (HDLC) engines.

The internal HDLC controller can service up to 128 Tx/Rx channels simultaneously in conventional HDLC mode and supports super-channel configuration. Each channel bit rate is programmable from 4 kbit/s to 64 kbit/s. The maximum bit rate of the TDM interface is 8 Mbps.

2.12.1 TDM interface

Main features:

- Six interface signals
- Duplex Tx/Rx communication
- 128 timeslots per frame (125 µs)
- Up to 8 Mbps per Tx/Rx channel
- Supports any timeslot banding on any Tx/Rx channel
- Tx/Rx Data sending/sampling time is configurable after/on the rising/falling edge of TxCLK/RxCLK.
- Delay between the bit 0 of TS0 and the SYNC signal is configurable (0 - up to 3 Tx/Rx clock cycles delay)
- The TDM/E1 interface is entirely dedicated to the HDLC protocol

2.12.2 E1 interface

Main features:

- Six interface signals
- Duplex Tx/Rx communication
- Up to 2 Mbps per Tx/Rx channel
- 32 timeslots / frame (125 µs)
- Supports any timeslot banding on any Tx/Rx channel
- Tx/Rx Data sending/sampling time is configurable after/on the rising/falling edge of TxCLK/RxCLK.
- Delay between the bit 0 of TS0 and the SYNC signal is configurable (0 - up to 3 Tx/Rx clock cycle delay)

2.13 RS485 HDLC ports

SPEAr310 features two RS485 HDLC ports.

Main features:

- Each RS485 interface has five signals
- Supports duplex Tx/Rx communication
- Maximum Tx/Rx data rate of RS485 HDLC is 3.88 Mbps
- Supports collision detection and automatic frame re-transmission
- Data sending/sampling timing is configurable:
  - Tx Data can be sent out after the rising/falling edge of TxCLK
  - Rx Data are sampled on the rising/falling edge of RxCLK
- No clock duty cycle constraints, data sending/receiving depends only on the rising/falling edge of Tx/Rx clock

2.13.1 HDLC controller

Main features:

- Compliant with ISO/IEC13239
- Standard HDLC frame code/decode
- Opening flag
- One or two bytes for address recognition (reception) and insertion (transmission)
- Payload with bit stuffing
- Frame check sequence: 16 bit CRC with polynomial G(x) = X16+X12+X5+1
- Closing flag

2.14 GPIOs

A maximum of 102 GPIOs are available when part of the embedded IPs are not needed (see "Pin description" table).

Within its basic subsystem, SPEAr310 provides twelve General Purpose Input/Output (GPIO) block. Each GPIO block provides 8 programmable inputs or outputs.

Main features of the GPIO are:

- Eight individually programmable input/output pins (default to input at reset)
- An APB slave acting as control interface in "software mode"
- Programmable interrupt generation capability on any number of pins.
- Hardware control capability of GPIO lines for different system configurations.
- Bit masking in both read and write operation through address lines.

2.15 8-channel ADC

Main features:

- Successive approximation conversion method
- 10-bit resolution @1 Msps
- Hardware supporting up to 13.5 bits resolution at 8 ksps by oversampling and accumulation
- Eight analog input (AIN) channels, ranging from 0 to 2.5 V
- INL ± 1 LSB, DNL ± 1 LSB
- Programmable conversion speed, (min. conversion time is 1 µs)
- Programmable averaging of results from 1 (No averaging) up to 128
- Programmable auto scan for all the eight channels.

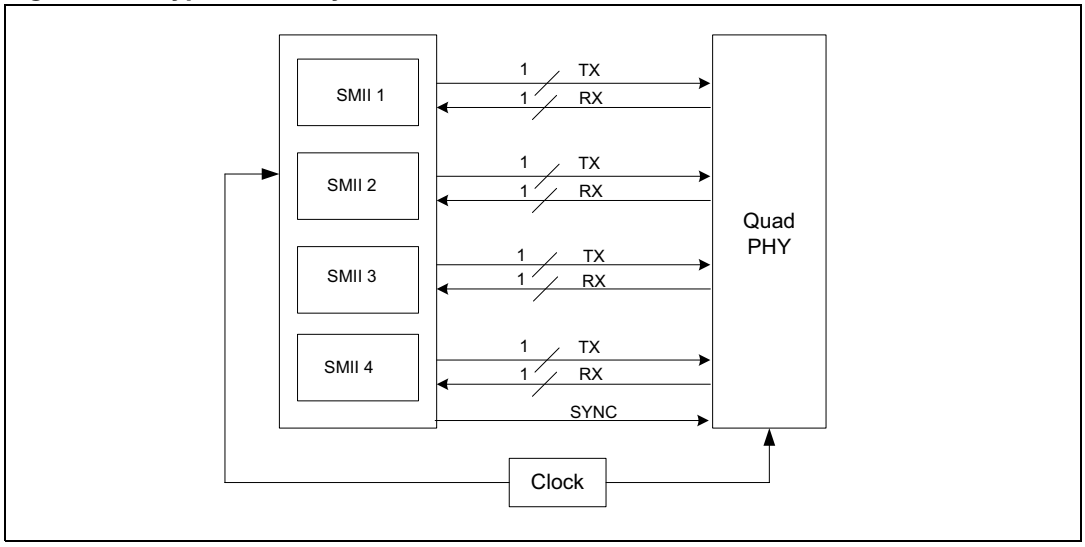
2.16 SMII Ethernet controller

SPEAr310 features four Ethernet MACs providing SMII interfaces.

Each MAC channel has dedicated TX/RX signals while synchronization and clock signals are common for PHY connection.

Figure 4 shows the typical SMII configuration (a generic example with four ports):

Figure 4. Typical SMII system



Each Ethernet port provides the following features:

- Compatible with IEEE Standard 802.3
- 10 and 100 Mbit/s operation
- Full and half duplex operation
- Statistics counter registers for RMON/MIB
- Interrupt generation to signal receive and transmit completion
- Automatic pad and CRC generation on transmitted frames
- Automatic discard of frames received with errors
- Address checking logic supports up to four specific 48-bit addresses
- Supports promiscuous mode where all valid received frames are copied to memory
- Hash matching of unicast and multicast destination addresses
- External address matching of received frames
- Physical layer management through MDIO interface
- Supports serial network interface operation
- Half duplex flow control by forcing collisions on incoming frames
- Full duplex flow control with recognition of incoming pause frames and hardware generation of transmitted pause frames
- Support for 802.1Q VLAN tagging with recognition of incoming VLAN and priority tagged frames
- Multiple buffers per receive and transmit frame
- Wake on LAN support
- Jumbo frames of up to 10240 bytes supported
- Configurable Endianess for the DMA Interface (AHB Master)

2.17 MII Ethernet controller

SPEAr310 provides an Ethernet MAC 10/100 Universal (commonly referred to as GMAC-UNIV), enabling to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard.

Note: GMAC is a hardware block implementing Ethernet MAC layer 2 processing. GMAC is configured for 10/100 Mbps operation on SPEAr3xx family and up to 1 Gbps on SPEAr600.

Main features:

- Supports the default Media Independent Interface (MII) defined in the IEEE 802.3 specifications.
- Supports 10/100 Mbps data transfer rates
- Local FIFO available (4 Kbyte RX, 2 Kbyte TX)
- Supports both half-duplex and full-duplex operation. In half-duplex operation, CSMA/CD protocol is provided
- Programmable frame length to support both standard and jumbo Ethernet frames with size up to 16 Kbyte
- A variety of flexible address filtering modes are supported
- A set of control and status registers (CSRs) to control MAC core operation
- Native DMA with single-channel transmit and receive engines
- DMA implements dual-buffer (ring) or linked-list (chained) descriptor chaining
- An AHB slave acting as programming interface to access all CSRs, for both DMA and MAC core subsystems
- A 32-bit AHB master for data transfer to system memory
- It supports both big-endian and little-endian.

2.18 USB2 host controller

SPEAr310 has two fully independent USB 2.0 hosts. Each consists of 5 major blocks:

- EHCI capable of managing high-speed transfers (HS mode, 480 Mbps)
- OHCI that manages the full and the low speed transfers (12 Mbps)
- Local 2-Kbyte FIFO
- Local DMA
- Integrated USB2 transceiver (PHY)

Both hosts can manage an external power switch, providing a control line to enable or disable the power, and an input line to sense any over-current condition detected by the external switch.

One host controller at time can perform high speed transfer.

2.19 USB2 device controller

Main features:

- Supports the 480 Mbps high-speed mode (HS) for USB 2.0, as well as the 12 Mbps full-speed (FS) and the 1.5 Mbps low-speed (LS modes) for USB 1.1
- Supports 16 physical endpoints, configurable as different logical endpoints
- Integrated USB transceiver (PHY)
- Local 4 Kbyte FIFO shared among all the endpoints
- DMA mode and slave-only mode are supported
- In DMA mode, the UDC supports descriptor-based memory structures in application memory
- In both modes, an AHB slave is provided by UDC-AHB, acting as programming interface to access to memory-mapped control and status registers (CSRs)
- An AHB master for data transfer to system memory is provided, supporting 8, 16, and 32-bit wide data transactions on the AHB bus
- A USB plug (UPD) detects the connection of a cable.

2.20 Cryptographic co-processor (C3)

SPEAr310 has an embedded Channel Control Coprocessor (C3). C3 is a high-performance instruction driven DMA based co-processor. It executes instruction flows generated by the host processor. After it has been set-up by the host it runs in a completely autonomous way (DMA data in, data processing, DMA data out), until the completion of all the requested operations.

C3 has been used to accelerate the processing of cryptographic, security and network security applications. It can be used for other types of data intensive applications as well.

Hardware cryptographic co-processor features are listed below:

- Supported cryptographic algorithms:
  - Advanced encryption standard (AES) cipher in ECB, CBC, CTR modes.
  - Data encryption standard (DES) cipher in ECB and CBC modes.
  - SHA-1, HMAC-SHA-1, MD5, HMAC-MD5 digests.
- Instruction driven DMA based programmable engine.
- AHB master port for data access from/to system memory.
- AHB slave port for co-processor register accesses and initial engine-setup.
- The co-processor is fully autonomous (DMA input reading, cryptographic operation execution, DMA output writing) after being set up by the host processor.
- The co-processor executes programs written by the host in memory, it can execute an unlimited list of programs.
- The co-processor supports hardware chaining of cryptographic blocks for optimized execution of data-flow requiring multiple algorithms processing over the same set of data (for example encryption + hashing on the fly).

2.21 JPEG CODEC

SPEAr310 provides a JPEG CODEC with header processing (JPGC), able to decode (or encode) image data contained in the SPEAr310 RAM, from the JPEG (or MCU) format to the MCU (or JPEG) format.

Main features:

- Compliance with the baseline JPEG standard (ISO/IEC 10918-1)
- Single-clock per pixel encoding/decoding
- Support for up to four channels of component color
- 8-bit/channel pixel depths
- Programmable quantization tables (up to four)
- Programmable Huffman tables (two AC and two DC)
- Programmable minimum coded unit (MCU)
- Configurable JPEG header processing
- Support for restart marker insertion
- Use of two DMA channels and of two 8 x 32-bits FIFO's (local to the JPEG) for efficient transferring and buffering of encoded/decoded data from/to the CODEC core.

3 Pin description

The following tables describe the pinout of the SPEAr310 listed by functional block.

List of abbreviations:

PU = Pull Up

PD = Pull Down

3.1 Required external components

- DDR_COMP_1V8: place an external 121 kΩ resistor between ball P4 and ball R4
- USB_TX_RTUNE: connect an external 43.2 kΩ pull-down resistor to ball K5
- DIGITAL_REXT: place an external 121 kΩ resistor between ball G4 and ball F4.

3.2 Dedicated pins

Table 2. Master clock, RTC, Reset and 3.3 V comparator pin descriptions

Group	Signal name	Ball	Direction	Function	Pin type
Master Clock	MCLK_XI	P1	Input	24 MHz (typical) crystal in	Oscillator 2.5 V capable
	MCLK_XO	P2	Output	24 MHz (typical) crystal out	
RTC	RTC_XI	E2	Input	32 kHz crystal in	Oscillator 1V5 capable
	RTC_XO	E1	Output	32 kHz crystal out	
Reset	MRESET	M17	Input	Main Reset	TTL Schmitt trigger input buffer, 3.3 V tolerant, PU
3.3 V Comp.	DIGITAL_REXT	G4	Output	Configuration	Analog, 3.3 V capable
	DIGITAL_GNDBG COMP	F4	Power	Power	Power

Table 3. Power supply pin description

Group	Signal name	Ball	Value
DIGITAL GROUND	GND	G6 G7 G8 G9 G10 G11 H6 H7 H8 H9 H10 H11 J6 J7 J8 J9 J10 J11 K6 K7 K8 K9 K10 K11 L6 L7 L8 L9 L10 M8 M9 M10	0 V
	USB_HOST1_HOST0_DEVICE_DVSS	L5	

Table 3. Power supply pin description (continued)

Group	Signal name	Ball	Value
ANALOG GROUND	RTC_GND	F2	0 V
	DITH_PLL_VSS_ANA	G1	
	USB_HOST1_VSSA	J2	
	USB_HOST0_VSSA	L1	
	USB_COMMON_VSSAC	L3	
	USB_DEVICE_VSSA	N2	
	DITH_VSS2V5	N4	
	MCLK_GND	P3	
	MCLK_GNDSUB	R3	
	ADC_AGND	N12	
I/O	DIGITAL_VDDE3V3	F5 F6 F7 F10 F11 F12 G5 J12 K12 L12 M12	3.3 V
CORE	VDD	F8 F9 G12 H5 H12 J5 L11 M6 M7 M11	1.2 V
USB HOST0 PHY	USB_HOST0_VDD2V5	L2	2.5 V
	USB_HOST0_VDD3V3	K4	3.3 V
USB HOST1 PHY	USB_HOST1_VDD2V5	K3	2.5 V
	USB_HOST1_VDD3V3	J1	3.3 V
USB DEVICE PHY	USB_DEVICE_VDD2V5	N1	2.5 V
	USB_DEVICE_VDD3V3	N3	3.3 V
	USB_HOST1_HOST0_DEVICE_DVDD1V2	M3	1.2 V
OSCI (master clock)	MCLK_VDD	R1	1.2 V
	MCLK_VDD2V5	R2	2.5 V
PLL1	DITH_PLL_VDD_ANA	G2	2.5 V
PLL2	DITH_VDD_2V5	M4	2.5 V
DDR I/O	DDR_VDDE1V8	M5 N5 N6 N7 N8 N9 N10 N11	1.8 V
ADC	ADC_AVDD	N13	2.5 V
OSCI RTC	RTC_VDD1V5	F1	1.5 V

Note: All the VDD 2V5 power supplies are analog VDD.

Table 4. Debug pin descriptions

Group	Signal name	Ball	Direction	Function	Pin type
DEBUG	TEST_0	K16	Input	Test_[4:0] configuration ports. For functional mode, they have to be set to 00110.	TTL input buffer, 3.3 V tolerant, PD
	TEST_1	K15			
	TEST_2	K14			
	TEST_3	K13			
	TEST_4	J15			
	BOOT_SEL	J14		Reserved, to be fixed at high level	
	nTRST	L16	Input	Test reset input	TTL Schmitt trigger input buffer, 3.3 V tolerant, PU
	TDO	L15	Output	Test data output	TTL output buffer, 3.3 V capable 4 mA
	TCK	L17	Input	Test clock	TTL Schmitt trigger input buffer, 3.3 V tolerant, PU
	TDI	L14	Input	Test data input	
	TMS	L13	Input	Test mode select	

Table 5. Serial memory interface (SMI) pin description

Group	Signal name	Ball	Direction	Function	Pin type
SMI	SMI_DATAIN	M13	Input	Serial Flash input data	TTL Input Buffer 3.3 V tolerant, PU
	SMI_DATAOUT	M14	Output	Serial Flash output data	TTL output buffer 3.3 V capable 4 mA
	SMI_CLK	N17	I/O	Serial Flash clock	
	SMI_CS_0	M15	Output	Serial Flash chip select	
	SMI_CS_1	M16			

Table 6. USB pin descriptions

Group	Signal name	Ball	Direction	Function	Pin type
USB DEV	USB_DEVICE_DP	M1	I/O	USB Device D+	Bidirectional analog buffer 5 V tolerant
	USB_DEVICE_DM	M2		USB Device D-	
	USB_DEVICE_VBUS	G3	Input	USB Device VBUS	TTL input buffer 3.3 V tolerant, PD

Table 6. USB pin descriptions (continued)

Group	Signal name	Ball	Direction	Function	Pin type
USB HOST	USB_HOST1_DP	H1	I/O	USB HOST1 D+	Bidirectional analog buffer 5 V tolerant
	USB_HOST1_DM	H2		USB HOST1 D-	
	USB_HOST1_VBUS	H3	Output	USBHOST1 VBUS	TTL output buffer 3.3 V capable, 4 mA
	USB_HOST1_OVERCUR	J4	Input	USB Host1 Over-Current	TTL input buffer 3.3 V tolerant, PD
	USB_HOST0_DP	K1	I/O	USB HOST0 D+	Bidirectional analog buffer 5 V tolerant
	USB_HOST0_DM	K2		USB HOST0 D-	
	USB_HOST0_VBUS	J3	Output	USB HOST0 VBUS	TTL output buffer 3.3 V capable, 4 mA
	USB_HOST0_OVERCUR	H4	Input	USB Host0 Over-current	TTL Input Buffer 3.3 V tolerant, PD
USB	USB_TXRTUNE	K5	Output	Reference resistor	Analog
	USB_ANALOG_TEST	L4	Output	Analog Test Output	Analog

Table 7. ADC pin description

Group	Signal name	Ball	Direction	Function	Pin type
ADC	AIN_0	N16	Input	ADC analog input channel	Analog buffer 2.5 V tolerant
	AIN_1	N15			
	AIN_2	P17			
	AIN_3	P16			
	AIN_4	P15			
	AIN_5	R17			
	AIN_6	R16			
	AIN_7	R15			
	ADC_VREFN	N14		ADC negative voltage reference	
	ADC_VREFP	P14		ADC positive voltage reference	

Table 8. DDR pin description

Group	Signal name	Ball	Direction	Function	Pin type
DDR	DDR_MEM_ADD_0	T2	Output	Address Line	SSTL_2/SSTL_18
	DDR_MEM_ADD_1	T1			
	DDR_MEM_ADD_2	U1			
	DDR_MEM_ADD_3	U2			
	DDR_MEM_ADD_4	U3			
	DDR_MEM_ADD_5	U4			
	DDR_MEM_ADD_6	U5			
	DDR_MEM_ADD_7	T5			
	DDR_MEM_ADD_8	R5			
	DDR_MEM_ADD_9	P5			
	DDR_MEM_ADD_10	P6			
	DDR_MEM_ADD_11	R6			
	DDR_MEM_ADD_12	T6			
	DDR_MEM_ADD_13	U6			
	DDR_MEM_ADD_14	R7			
	DDR_MEM_BA_0	P7	Output	Bank select	
	DDR_MEM_BA_1	P8			
	DDR_MEM_BA_2	R8			
	DDR_MEM_RAS	U8	Output	Row Add. Strobe	
	DDR_MEM_CAS	T8	Output	Col. Add. Strobe	
	DDR_MEM_WE	T7	Output	Write enable	
	DDR_MEM_CLKEN	U7	Output	Clock enable	
	DDR_MEM_CLKP	T9	Output	Differential clock	Differential SSTL_2/SSTL_18
	DDR_MEM_CLKN	U9			
	DDR_MEM_CS_0	P9	Output	Chip Select	SSTL_2/SSTL_18
	DDR_MEM_CS_1	R9			
	DDR_MEM_ODT_0	T3	I/O	On-Die Termination Enable lines	
	DDR_MEM_ODT_1	T4			

Table 8. DDR pin description (continued)

Group	Signal name	Ball	Direction	Function	Pin type
DDR	DDR_MEM_DQ_0	P11	I/O	Data Lines (Lower byte)	SSTL_2/SSTL_18
	DDR_MEM_DQ_1	R11			
	DDR_MEM_DQ_2	T11			
	DDR_MEM_DQ_3	U11			
	DDR_MEM_DQ_4	T12			
	DDR_MEM_DQ_5	R12			
	DDR_MEM_DQ_6	P12			
	DDR_MEM_DQ_7	P13			
	DDR_MEM__DQS_0	U10	Output	Lower Data Strobe	Differential SSTL_2/SSTL_18
	nDDR_MEM_DQS_0	T10			
	DDR_MEM_DM_0	U12	Output	Lower Data Mask	SSTL_2/SSTL_18
	DDR_MEM_GATE_OPEN_0	R10	I/O	Lower Gate Open	
	DDR_MEM_DQ_8	T17	I/O	Data Lines (Upper byte)	
	DDR_MEM_DQ_9	T16			
	DDR_MEM_DQ_10	U17			
	DDR_MEM_DQ_11	U16			
	DDR_MEM_DQ_12	U14			
	DDR_MEM_DQ_13	U13			
	DDR_MEM_DQ_14	T13			
	DDR_MEM_DQ_15	R13			
	DDR_MEM_DQS_1	U15	I/O	Upper Data Strobe	Differential SSTL_2/SSTL_18
	nDDR_MEM_DQS_1	T15			
	DDR_MEM_DM_1	T14	I/O	Upper Data Mask	SSTL_2/SSTL_18
	DDR_MEM_GATE_OPEN_1	R14		Upper Gate Open	
	DDR_MEM_VREF	P10	Input	Reference Voltage	Analog
	DDR_MEM_COMP2V5_GNDBGCOMP	R4	Power	Return for Ext. Resistors	Power
	DDR_MEM_COMP2V5_REXT	P4	Power	Ext. Resistor	Analog
	DDR2_EN	J13	Input	Configuration	TTL Input Buffer 3.3 V Tolerant, PU

3.3 Shared I/O pins (PL_GPIOs)

SPEAr3xx devices feature, in the Reconfigurable Array Subsystem (RAS), specific sets of IPs as well as groups of software controllable GPIOs (that can be used alternatively). In the SPEAr310 the following IPs are implemented in the RAS:

- External Memory Interface for external NOR Flash or other devices such as FPGAs
- FSMC NAND Flash interface
- TDM/E1 HDLC interface
- 2 RS485 ports
- 4 SMII interfaces for customized Ethernet MACs

The 98 PL_GPIO and 4 PL_CLK pins have the following characteristics:

- Output buffer: TTL 3.3 V capable up to 10 mA
- Input buffer: TTL, 3.3 V tolerant, selectable internal pull up/pull down (PU/PD)

3.3.1 PL_GPIO pin description

Table 9. PL_GPIO pin description

Group	Signal name	Ball	Direction	Function	Pin type
PL_GPIOs	PL_GPIO_97... PL_GPIO_0	(see the section *Table 10*)	I/O	General purpose I/O or multiplexed pins (see the section *Table 10*)	(see the introduction of the *Section 3.3* here above)
	PL_CLK1... PL_CLK4			programmable logic external clocks	

3.3.2 Configuration modes

RAS normal or RAS GPIO mode is selected by programming the RAS control registers. Details of each PL_GPIO pin are given in *Table 10: PL_GPIO multiplexing scheme on page 34*

RAS normal mode is the default mode for SPEAr310. It mainly provides:

- External Memory Interface (16 data bits, 24 address bits and 4 chip selects)
- FSMC NAND Flash interface (8-16 bits and 3 control lines shared with EMI)
- TDM/E1 HDLC interface
- 2 RS485 ports
- 4 SMII interfaces for customized Ethernet MACs,
- 6 UARTs, 1 with hardware flow control (up to 3 Mbps), 5 with software flow control (baud rate up to 5 Mbps)
- SSP port
- 1 independent I2C interface
- GPIOs with interrupt capabilities

3.3.3 Alternate functions

Other peripheral functions are listed in the Alternate Functions column of *Table 10: PL_GPIO multiplexing scheme* and can be individually enabled/disabled via RAS control register 1. Refer to the user manual for the register descriptions.

3.3.4 Boot pins

The status of the boot pins is read at startup by the BootROM. Refer to the description of the Boot register in the SPEAr310 user manual.

3.3.5 GPIOs

The PL_GPIO pins can be used as software controlled general purpose I/Os (GPIOs) if they are not used by the I/O functions of the SPEAr310 IPs.

To configure any PL_GPIO pin as GPIO, set the corresponding bit in the GPIO_Select(0 ..3) registers that are 102 bits write registers that select GPIO versus some IPs.

Please refer to the SPEAr310 user manual for more detail about these registers.

3.3.6 Multiplexing scheme

To provide the best I/O multiplexing flexibility and the higher number of GPIOs for ARM controlled input-output function, the following hierarchical multiplexing scheme has been implemented.

The two multiplexers shown in *Figure 5* are controlled by different registers. The first multiplexer selects the pin either as a software controllable GPIO or as an I/O signal controlled by one of the RAS IPs (see column “Function in RAS normal mode” in *Table 10*). This selection is programmable for each PL_GPIO pin via the PL_GPIO_EN register bits. The output multiplexer is controlled by the Function enable register and allows you to enable the alternate function of the embedded IPs, see column “Alternate function (enabled by Function Enable register)” in *Table 10*.

To get more information about these registers, please refer to the SPEAr310 user manual.

Figure 5. Hierarchical multiplexing scheme

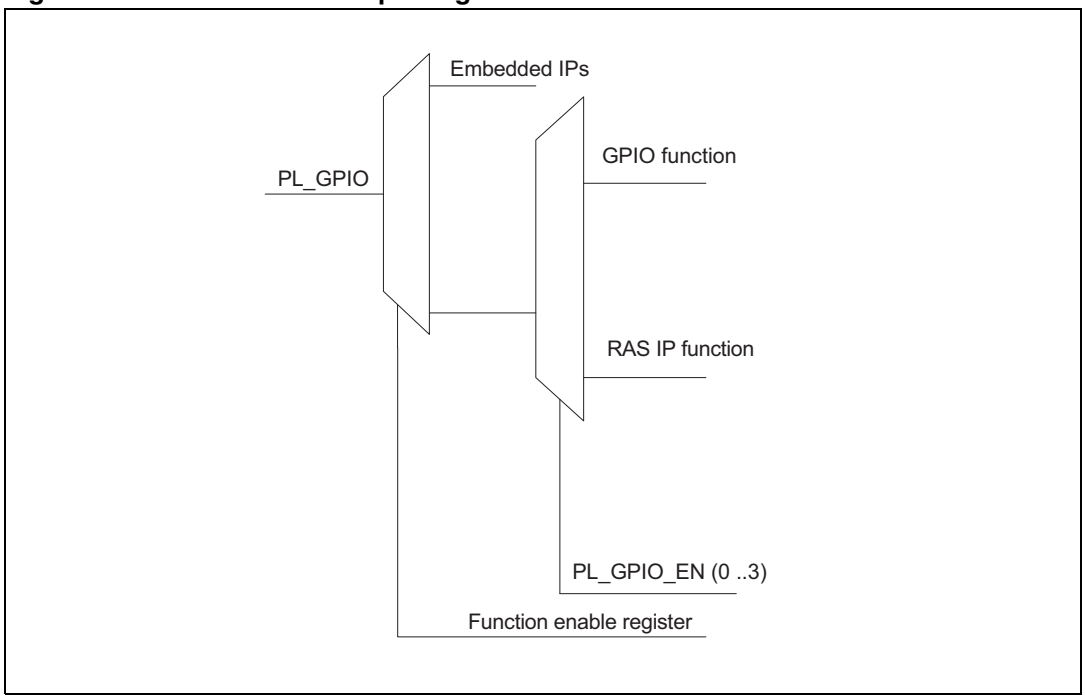


Table 10. PL_GPIO multiplexing scheme

PL / pin number	Function in RAS normal mode	Alternate function (enabled by Function Enable register)	Boot pins	Function in RAS GPIO mode
PL_GPIO_97/H16	ETH0_TX			GPIO12_7
PL_GPIO_96/H15	ETH0_RX			GPIO12_6
PL_GPIO_95/H14	ETH1_TX			GPIO12_5
PL_GPIO_94/H13	ETH1_RX			GPIO12_4
PL_GPIO_93/G17	ETH2_TX			GPIO12_3
PL_GPIO_92/G16	ETH2_RX			GPIO12_2
PL_GPIO_91/G15	ETH3_TX			GPIO12_1
PL_GPIO_90/G14	ETH3_RX			GPIO12_0
PL_GPIO_89/F17	ETH_SYNC			GPIO11_7
PL_GPIO_88/F16	SMII_MDIO			GPIO11_6
PL_GPIO_87/G13	SMII_MDC			GPIO11_5
PL_GPIO_86/E17	EMI_ADDB_0/FSMC_D0		B0	GPIO11_4
PL_GPIO_85/F15	EMI_ADDB_1/FSMC_D1		B1	GPIO11_3
PL_GPIO_84/D17	EMI_ADDB_2/FSMC_D2		B2	GPIO11_2
PL_GPIO_83/E16	EMI_ADDB_3/FSMC_D3		B3	GPIO11_1
PL_GPIO_82/E15	EMI_ADDB_4/FSMC_D4		B4	GPIO11_0
PL_GPIO_81/C17	EMI_ADDB_5/FSMC_D5		B5	GPIO10_7
PL_GPIO_80/D16	EMI_ADDB_6/FSMC_D6		B6	GPIO10_6

Table 10. PL_GPIO multiplexing scheme (continued)

PL / pin number	Function in RAS normal mode	Alternate function (enabled by Function Enable register)	Boot pins	Function in RAS GPIO mode
PL_GPIO_79/F14	EMI_ADDB_7/FSMC_D7			GPIO10_5
PL_GPIO_78/D15	EMI_ADDB_8/FSMC_D8			GPIO10_4
PL_GPIO_77/B17	EMI_ADDB_9/FSMC_D9			GPIO10_3
PL_GPIO_76/F13	EMI_ADDB_10/FSMC_D10			GPIO10_2
PL_GPIO_75/E14	EMI_ADDB_11/FSMC_D11			GPIO10_1
PL_GPIO_74/C16	EMI_ACK			GPIO10_0
PL_GPIO_73/A17	EMI_ADDB_13/FSMC_D13			GPIO9_7
PL_GPIO_72/B16	EMI_ADDB_14/FSMC_D14			GPIO9_6
PL_GPIO_71/D14	EMI_ADDB_15/FSMC_D15			GPIO9_5
PL_GPIO_70/C15	EMI_ADDB_16			GPIO9_4
PL_GPIO_69/A16	EMI_ADDB_17			GPIO9_3
PL_GPIO_68/B15	EMI_ADDB_18			GPIO9_2
PL_GPIO_67/C14	EMI_ADDB_19			GPIO9_1
PL_GPIO_66/E13	EMI_ADDB_20			GPIO9_0
PL_GPIO_65/B14	EMI_ADDB_21			GPIO8_7
PL_GPIO_64/D13	EMI_ADDLE/FSMC_AL			GPIO8_6
PL_GPIO_63/C13	EMI_ADDB_23			GPIO8_5
PL_GPIO_62/A15	EMI_ADDB_24			GPIO8_4
PL_GPIO_61/E12	EMI_ADDB_25			GPIO8_3
PL_GPIO_60/A14	EMI_ADDB_26			GPIO8_2
PL_GPIO_59/B13	EMI_ADDB_27			GPIO8_1
PL_GPIO_58/D12	EMI_ADDB_28			GPIO8_0
PL_GPIO_57/E11	EMI_ADDB_29			GPIO7_7
PL_GPIO_56/C12	EMI_ADDB_30			GPIO7_6
PL_GPIO_55/A13	EMI_ADDB_31			GPIO7_5
PL_GPIO_54/E10	EMI_ADDB_12/FSMC_D12			GPIO7_4
PL_GPIO_53/D11	EMI_ADDB_22			GPIO7_3
PL_GPIO_52/B12	EMI_OE/FSMC_/R			GPIO7_2
PL_GPIO_51/D10	EMI_WE/FSMC_/W			GPIO7_1
PL_GPIO_50/A12	EMI_CS[0]	TMR_CPTR4		GPIO7_0
PL_GPIO_49/C11	EMI_CS[1]	TMR_CPTR3		GPIO6_7
PL_GPIO_48/B11	EMI_CS[2]	TMR_CPTR2		GPIO6_6
PL_GPIO_47/C10	EMI_CS[3]	TMR_CPTR1		GPIO6_5
PL_GPIO_46/A11	EMI_CS[4]	TMR_CLK4		GPIO6_4
PL_GPIO_45/B10	EMI_CS[5]	TMR_CLK3		GPIO6_3
PL_GPIO_44/A10	UART2_TX	TMR_CLK2		GPIO6_2
PL_GPIO_43/E9	UART2_RX	TMR_CLK1		GPIO6_1

Table 10. PL_GPIO multiplexing scheme (continued)

PL / pin number	Function in RAS normal mode	Alternate function (enabled by Function Enable register)	Boot pins	Function in RAS GPIO mode
PL_GPIO_42/D9	UART5_TX	UART0_DTR		GPIO6_0
PL_GPIO_41/C9	UART5_RX	UART0_RI		GPIO5_7
PL_GPIO_40/B9	UART4_TX	UART0_DSR		GPIO5_6
PL_GPIO_39/A9	UART4_RX	UART0_DCD		GPIO5_5
PL_GPIO_38/A8	UART3_TX	UART0_CTS		GPIO5_4
PL_GPIO_37/B8	UART3_RX	UART0_RTS		GPIO5_3
PL_GPIO_36/C8	FSMC_/E1	SSP_CS4		GPIO5_2
PL_GPIO_35/D8	FSMC_CL	SSP_CS3		GPIO5_1
PL_GPIO_34/E8	FSMC_R/B	SSP_CS2		GPIO5_0
PL_GPIO_33/E7	0	BasGPIO5		BasGPIO5
PL_GPIO_32/D7	0	BasGPIO4		BasGPIO4
PL_GPIO_31/C7	0	BasGPIO3		BasGPIO3
PL_GPIO_30/B7	0	BasGPIO2		BasGPIO2
PL_GPIO_29/A7	0	BasGPIO1		BasGPIO1
PL_GPIO_28/A6	0	BasGPIO0		BasGPIO0
PL_GPIO_27/B6	0	MII_TX_CLK		GPIO4_7
PL_GPIO_26/A5	0	MII_TXD0		GPIO4_6
PL_GPIO_25/C6	0	MII_TXD1		GPIO4_5
PL_GPIO_24/B5	0	MII_TXD2		GPIO4_4
PL_GPIO_23/A4	RS0_IN	MII_TXD3		GPIO4_3
PL_GPIO_22/D6	RS0_OUT	MII_TX_EN		GPIO4_2
PL_GPIO_21/C5	RS0_RXCLK	MII_TX_ER		GPIO4_1
PL_GPIO_20/B4	RS0_TXCLK	MII_RX_CLK		GPIO4_0
PL_GPIO_19/A3	RS0_CTS	MII_RX_DV		GPIO3_7
PL_GPIO_18/D5	RS1_IN	MII_RX_ERR		GPIO3_6
PL_GPIO_17/C4	RS1_OUT	MII_RXD0		GPIO3_5
PL_GPIO_16/E6	RS1_RXCLK	MII_RXD1		GPIO3_4
PL_GPIO_15/B3	RS1_TXCLK	MII_RXD2		GPIO3_3
PL_GPIO_14/A2	RS1_CTS	MII_RXD3		GPIO3_2
PL_GPIO_13/A1	TDM0_DTOUT	MII_COL		GPIO3_1
PL_GPIO_12/D4	TDM0_RSYNC	MII_CRS		GPIO3_0
PL_GPIO_11/E5	TDM0_TSYNC	MII_MDC		GPIO2_7
PL_GPIO_10/C3	TDM0_DTIN	MII_MDIO		GPIO2_6
PL_GPIO_9/B2	SSP_MOSI	SSP_MOSI		GPIO2_5
PL_GPIO_8/C2	SSP_SCLK	SSP_SCLK		GPIO2_4
PL_GPIO_7/D3	SSP_SS0	SSP_SS0		GPIO2_3
PL_GPIO_6/B1	SSP_MISO	SSP_MISO		GPIO2_2

Table 10. PL_GPIO multiplexing scheme (continued)

PL / pin number	Function in RAS normal mode	Alternate function (enabled by Function Enable register)	Boot pins	Function in RAS GPIO mode
PL_GPIO_5/D2	I2C_SDA	I2C_SDA		GPIO2_1
PL_GPIO_4/C1	I2C_SCL	I2C_SCL		GPIO2_0
PL_GPIO_3/D1	UART0_RX	UART0_RX		GPIO1_7
PL_GPIO_2/E4	UART0_TX	UART0_TX		GPIO1_6
PL_GPIO_1/E3	UART1_TX	IrDA_RX		GPIO1_5
PL_GPIO_0/F3	UART1_RX	IrDA_TX		GPIO1_4
PL_CLK1/K17	ETH_CLKIN	PL_CLK1		GPIO1_3
PL_CLK2/J17	ETH_CLKREF	PL_CLK2		GPIO1_2
PL_CLK3/J16	TDM0_RCLK	PL_CLK3		GPIO1_1
PL_CLK4/H17	TDM0_TCLK	PL_CLK4		GPIO1_0

Note: 1 Table cells filled with '0' or '1' are unused and unless otherwise configured as Alternate function or GPIO, the corresponding pin is held at low or high level respectively by the internal logic.

2 Pins shared by EMI and FSMC: Depending on the AHB address to be accessed the pins are used for EMI or FSMC transfers.

Table 11. Table shading

Shading	Pin group
FSMC	FSMC pins: NAND Flash
EMI	EMI pins
UART	UART pins
Ethernet MAC	MII/SMII Ethernet Mac pins
GPT	Timer pins
IrDa	IrDa pins
SSP	SSP pins
I2C	I2C pins

Note: For the full description of the I/O functions related to each IP, please refer to the corresponding sections of the SPEAR310 user manual.

3.4 PL_GPIO pin sharing for debug modes

In some cases the PL_GPIO pins may be used in different ways for debugging purposes. There are three different cases (see also *Table 12*):

1. Case 1 - All the PL_GPIO get values from Boundary scan registers during Ex-test instruction of JTAG . Typically this configuration is used to verify correctness of the soldering process during the production flow .
2. Case 2 - All the PL_GPIO maintain their original meaning but the JTAG Interface is connected to the processor. This configuration is useful during the development phase but offers only "static" debug.
3. Case 3 - Some PL_GPIO, as shown in *Table 12: Ball sharing during debug*, are used to connect the ETM9 lines to an external box. This configuration is typically used only during the development phase. It offers a very powerful debug capability. When the processor reaches a breakpoint it is possible, by analyzing the trace buffer, to understand the reason why the processor has reached the break.

Table 12. Ball sharing during debug

Signal	Case 1 - Board Debug	Case 2 - Static Debug	Case 3 - Full Debug
Test[0]	0	1	0
Test[1]	0	0	1
Test[2]	0	0/1	0/1
Test[3]	0	0/1	0/1
Test[4]	1	0	0
nTRST	nTRST_bscan	nTRST_ARM	nTRST_ARM
TCK	TCK_bscan	TCK_ARM	TCK_ARM
TMS	TSM_bscan	TMS_ARM	TSM_ARM
TDI	TDI_bscan	TDI_ARM	TDI_ARM
TDO	TDO_bscan	TDO_ARM	TDO_ARM
PL_GPIO[97]	BSR Value	Functional I/O	ARM_TRACE_CLK
PL_GPIO[96]	BSR Value	Functional I/O	ARM_TRACE_PKTA[0]
PL_GPIO[95]	BSR Value	Functional I/O	ARM_TRACE_PKTA[1]
PL_GPIO[94]	BSR Value	Functional I/O	ARM_TRACE_PKTA[2]
PL_GPIO[93]	BSR Value	Functional I/O	ARM_TRACE_PKTA[3]
PL_GPIO[92]	BSR Value	Functional I/O	ARM_TRACE_PKTB[0]
PL_GPIO[91]	BSR Value	Functional I/O	ARM_TRACE_PKTB[1]
PL_GPIO[90]	BSR Value	Functional I/O	ARM_TRACE_PKTB[2]
PL_GPIO[89]	BSR Value	Functional I/O	ARM_TRACE_PKTB[3]
PL_GPIO[88]	BSR Value	Functional I/O	ARM_TRACE_SYNCA
PL_GPIO[87]	BSR Value	Functional I/O	ARM_TRACE_SYNCB
PL_GPIO[86]	BSR Value	Functional I/O	ARM_PIPESTATA[0]
PL_GPIO[85]	BSR Value	Functional I/O	ARM_PIPESTATA[1]
PL_GPIO[84]	BSR Value	Functional I/O	ARM_PIPESTATA[2]
PL_GPIO[83]	BSR Value	Functional I/O	ARM_PIPESTATB[0]
PL_GPIO[82]	BSR Value	Functional I/O	ARM_PIPESTATB[1]

Table 12. Ball sharing during debug (continued)

Signal	Case 1 - Board Debug	Case 2 - Static Debug	Case 3 - Full Debug
PL_GPIO[81]	BSR Value	Functional I/O	ARM_PIPESTATB[2]
PL_GPIO[80]	BSR Value	Functional I/O	ARM_TRACE_PKTA[4]
PL_GPIO[79]	BSR Value	Functional I/O	ARM_TRACE_PKTA[5]
PL_GPIO[78]	BSR Value	Functional I/O	ARM_TRACE_PKTA[6]
PL_GPIO[77]	BSR Value	Functional I/O	ARM_TRACE_PKTA[7]
PL_GPIO[76]	BSR Value	Functional I/O	ARM_TRACE_PKTB[4]
PL_GPIO[75]	BSR Value	Functional I/O	ARM_TRACE_PKTB[5]
PL_GPIO[74]	BSR Value	Functional I/O	ARM_TRACE_PKTB[6]
PL_GPIO[73]	BSR Value	Functional I/O	ARM_TRACE_PKTB[7]
PL_GPIO[72:0]			

4 Memory map

Table 13. SPEAr310 memory mapping

Start address	End address	Peripheral	Description
0x0000_0000	0x3FFF_FFFF	LP DDR/DDR2 external memory	
0x4000_0000	0x43FF_FFFF	FSMC	External NAND Flash memory
0x4400_0000	0x44FF_FFFF		FSMC configuration registers
0x4500_0000	0x4EFF_FFFF	Reserved	
0x4F00_0000	0x4FFF_FFFF	EMI	EMI configuration registers
0x5000_0000	0x5FFF_FFFF		256 MB Ext. memory EMI CS[0]/NOR_CS[0]
0x6000_0000	0x6FFF_FFFF		256 MB Ext. memory EMI CS[1]
0x7000_0000	0x7FFF_FFFF		256 MB Ext. memory EMI CS[2]
0x8000_0000	0x8FFF_FFFF		256 MB Ext. memory EMI CS[3]
0x9000_0000	0x9FFF_FFFF		256 MB Ext. memory EMI CS[4]
0xA000_0000	0xAFFF_FFFF		256 MB Ext. memory EMI CS[5]
0xB000_0000	0xB07F_FFFF	MACB 0 (SMII)	MACB configuration registers
0xB080_0000	0xB0FF_FFFF	MACB 1 (SMII)	MACB configuration registers
0xB100_0000	0xB17F_FFFF	MACB 2 (SMII)	MACB configuration registers
0xB180_0000	0xB1FF_FFFF	MACB 3 (SMII)	MACB configuration registers
0xB200_0000	0xB207_FFFF	UART 1	UART configuration registers
0xB208_0000	0xB20F_FFFF	UART 2	UART configuration registers
0xB210_0000	0xB217_FFFF	UART 3	UART configuration registers
0xB218_0000	0xB21F_FFFF	UART 4	UART configuration registers
0xB220_0000	0xB227_FFFF	UART 5	UART configuration registers
0xB228_0000	0xB27F_FFFF	Reserved	
0xB280_0000	0xB2FF_FFFF	TDM/E1 HDLC	TDM/E1 HDLC configuration registers
0xB300_0000	0xB37F_FFFF	RS485 HDLC 1	RS485 HDLC 1 configuration registers
0xB380_0000	0xB3FF_FFFF	RS485 HDLC 2	RS485 HDLC 2 configuration registers
0xB400_0000	0xB47F_FFFF	RAS	RAS configuration registers
0xB480_0000	0xCFFF_FFFF	Reserved	
0xD000_0000	0xD007_FFFF	UART 0	UART configuration registers
0xD008_0000	0xD00F_FFFF	ADC	ADC configuration registers
0xD010_0000	0xD017_FFFF	SSP	SSP configuration registers

Table 13. SPEAr310 memory mapping (continued)

Start address	End address	Peripheral	Description
0xD018_0000	0xD01F_FFFF	I2C	I2C configuration registers
0xD020_0000	0xD07F_FFFF	Reserved	
0xD080_0000	0xD0FF_FFFF	JPEG CODEC	JPEG configuration registers
0xD100_0000	0xD17F_FFFF	IrDA	IrDA configuration registers
0xD180_0000	0xD1FF_FFFF	Reserved	
0xD280_0000	0xD7FF_FFFF	SRAM	Static RAM shared memory (8 Kbytes)
0xD800_0000	0xE07F_FFFF	Reserved	
0xE080_0000	0xE0FF_FFFF	GMAC (MII)	GMAC configuration registers
0xE100_0000	0xE10F_FFFF	USB 2.0 device controller	FIFO
0xE110_0000	0xE11F_FFFF		Configuration registers
0xE120_0000	0xE12F_FFFF		Plug detect
0xE130_0000	0xE17F_FFFF	Reserved	
0xE180_0000	0xE18F_FFFF	USB2.0 hosts EHCI 0-1	Configuration registers
0xE190_0000	0xE19F_FFFF	USB2.0 hosts OHCI 0	Configuration registers
0xE1A0_0000	0xE20F_FFFF	Reserved	
0xE210_0000	0xE21F_FFFF	USB2.0 hosts OHCI 1	Configuration registers
0xE220_0000	0xE27F_FFFF	Reserved	
0xE280_0000	0xE28F_FFFF	ML USB ARB	Configuration registers
0xE290_0000	0xEFFF_FFFF	Reserved	
0xF000_0000	0xF00F_FFFF	Timer 1 (in CPU subsystem)	GPT Configuration registers
0xF010_0000	0xF10F_FFFF	Reserved	
0xF110_0000	0xF11F_FFFF	VIC	Configuration registers
0xF120_0000	0xF7FF_FFFF	Reserved	
0xF800_0000	0xFBFF_FFFF	SMI	Serial Flash actual memory
0xFC00_0000	0xFC1F_FFFF		SMI configuration registers
0xFC20_0000	0xFC3F_FFFF	Reserved	
0xFC40_0000	0xFC5F_FFFF	DMA Controller	DMAC configuration registers
0xFC60_0000	0xFC7F_FFFF	MPMC	MPMC configuration registers
0xFC80_0000	0xFC87_FFFF	Timer 2	GPT configuration registers
0xFC88_0000	0xFC8F_FFFF	Watchdog Timer	WDT configuration registers
0xFC90_0000	0xFC97_FFFF	Real-time Clock	RTC configuration registers

Table 13. SPEAr310 memory mapping (continued)

Start address	End address	Peripheral	Description
0xFC98_0000	0xFC9F_FFFF	General Purpose I/O	GPIO configuration registers
0xFCA0_0000	0xFCA7_FFFF	System Controller	SYS Ctrl configuration registers
0xFCA8_0000	0xFCAF_FFFF	MISC (Miscellaneous)	MISC configuration registers
0xFCB0_0000	0xFCB7_FFFF	Timer 3	GPT configuration registers
0xFCB8_0000	0xFEFF_FFFF	Reserved	
0xFF00_0000	0xFFFF_FFFF	Internal ROM	Boot ROM

5 Electrical characteristics

5.1 Absolute maximum ratings

This product contains devices to protect the inputs against damage due to high/low static voltages. However it is advisable to take normal precaution to avoid application of any voltage higher/lower than the specified maximum/minimum rated voltages.

The absolute maximum rating is the maximum stress that can be applied to a device without causing permanent damage. However, extended exposure to minimum/maximum ratings may affect long-term device reliability.

Table 14. Absolute maximum ratings

Symbol	Parameter	Minimum value	Maximum value	Unit
V_{DD} 1.2	Supply voltage for the core	- 0.3	1.44	V
V_{DD} 3.3	Supply voltage for the I/Os	- 0.3	3.9	V
V_{DD} 2.5	Supply voltage for the analog blocks	- 0.3	3	V
V_{DD} 1.8	Supply voltage for the DRAM interface	- 0.3	2.16	V
V_{DD} RTC	RTC supply voltage	-0.3	2.16	V
T_{STG}	Storage temperature	-55	150	°C
T_J	Junction temperature	-40	125	°C

5.2 Maximum power consumption

Note: These values take into consideration the worst cases of process variation and voltage range and must be used to design the power supply section of the board.

Table 15. Maximum power consumption

Symbol	Description	Max	Unit
V_{DD} 1.2	Supply voltage for the core	420	mA
V_{DD} 1.8	Supply voltage for the DRAM interface (1)	160	mA
V_{DD} RTC	RTC supply voltage	8	µA
V_{DD} 2.5	Supply voltage for the analog blocks	35	mA
V_{DD} 3.3	Supply voltage for the I/Os (2)	15	mA
P_D	Maximum power consumption	930(3)	mW

1. Peak current with Linux memory test (50% write and 50% read) plus DMA reading memory.
2. With 30 logic channels connected to the device and simultaneously switching at 10 MHz.

3. The maximum current and power values listed above, obtained with typical supply voltages, are not guaranteed to be the highest obtainable. These values are dependent on many factors including the type of applications running, clock rates, use of internal functional capabilities, external interface usage, case temperature, and the power supply voltages. Your specific application can produce significantly different results.

   1.2 V current and power are primarily dependent on the applications running and the use of internal chip functions (DMA, USB, Ethernet, and so on).

   3.3 V current and power are primarily dependent on the capacitive loading, frequency, and utilization of the external buses.

5.3 DC electrical characteristics

The recommended operating conditions are listed in the following table:

Table 16. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD} 1.2	Supply voltage for the core	1.14	1.2	1.3	V
V_{DD} 3.3	Supply voltage for the I/Os	3	3.3	3.6	V
V_{DD} 2.5	Supply voltage for the analog blocks	2.25	2.5	2.75	V
V_{DD} 1.8	Supply voltage for DRAM interface	1.70	1.8	1.9	V
V_{DD} RTC	RTC supply voltage	1.3	1.5	1.8	V
T_C	Case temperature	-40		85	°C

5.4 Overshoot and undershoot

This product can support the following values of overshoot and undershoot.

Table 17. Overshoot and undershoot specifications

Parameter	3V3 I/Os	2V5 I/Os	1V8 I/Os
Amplitude	500 mV	500 mV	500 mV
Ratio of overshoot (or undershoot) duration with respect to pulse width	1/3	1/3	1/3

If the amplitude of the overshoot/undershoot increases (decreases), the ratio of overshoot/undershoot width to the pulse width decreases (increases). The formula relating the two is:

Amplitude of OS/US = 0.75*(1- ratio of OS (or US) duration with respect to pulse width)

Note: The value of overshoot/undershoot should not exceed the value of 0.5 V. However, the duration of the overshoot/undershoot can be increased by decreasing its amplitude.

5.5 3.3V I/O characteristics

The 3.3 V I/Os are compliant with JEDEC standard JESD8b

Table 18. Low voltage TTL DC input specification (3 V< V_{DD} <3.6 V)

Symbol	Parameter	Min	Max	Unit
V_{IL}	Low level input voltage		0.8	V
V_{IH}	High level input voltage	2		V
V_{hyst}	Schmitt trigger hysteresis	300	800	mV

Table 19. Low voltage TTL DC output specification (3 V< V_{DD} <3.6 V)

Symbol	Parameter	Test condition	Min	Max	Unit
V_{OL}	Low level output voltage	I_{OL}= X mA (1)		0.3	V
V_{OH}	High level output voltage	I_{OH}= -X mA (1)	V_{DD} - 0.3		V

1. For the max current value (X mA) refer to *Section 3: Pin description*.

Table 20. Pull-up and pull-down characteristics

Symbol	Parameter	Test condition	Min	Max	Unit
R_{PU}	Equivalent pull-up resistance	V_I = 0 V	29	67	kΩ
R_{PD}	Equivalent pull-down resistance	V_I = V_{DDE}3V3	29	103	kΩ

5.6 LPDDR and DDR2 pin characteristics

Table 21. DC characteristics

Symbol	Parameter	Test condition	Min	Max	Unit
V_{IL}	Low level input voltage	SSTL2	-0.3	V_{REF}-0.15	V
		SSTL18	-0.3	V_{REF}-0.125	V
V_{IH}	High level input voltage	SSTL2	V_{REF}+0.15	V_{DDE}2V5+0.3	V
		SSTL18	V_{REF}+0.125	V_{DDE}1V8+0.3	V
V_{hyst}	Input voltage hysteresis		200		mV

Table 22. Driver characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R_O	Output impedance (strong value)	40.5	45	49.5	Ω
	Output impedance (weak value)	44.1	49	53.9	Ω

Table 23. On die termination

Symbol	Parameter	Min	Typ	Max	Unit
RT1*	Termination value of resistance for on die termination		75		Ω
RT2*	Termination value of resistance for on die termination		150		Ω

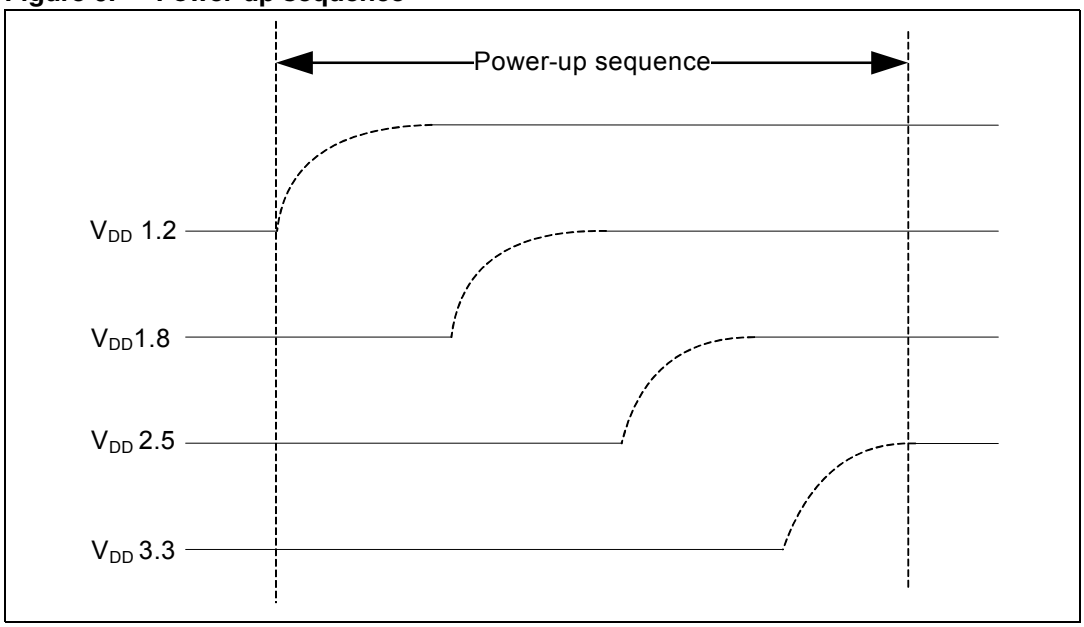
Table 24. Reference voltage

Symbol	Parameter	Min	Typ	Max	Unit
V_{REFIN}	Voltage applied to core/pad	0.49 * V_{DDE}	0.500 * V_{DDE}	0.51 * V_{DDE}	V

5.7 Power up sequence

It is recommended to power up the power supplies in the order shown in *Figure 6*. V_{DD} 1.2 is brought up first, followed by V_{DD} 1.8, then V_{DD} 2.5 and finally V_{DD} 3.3.

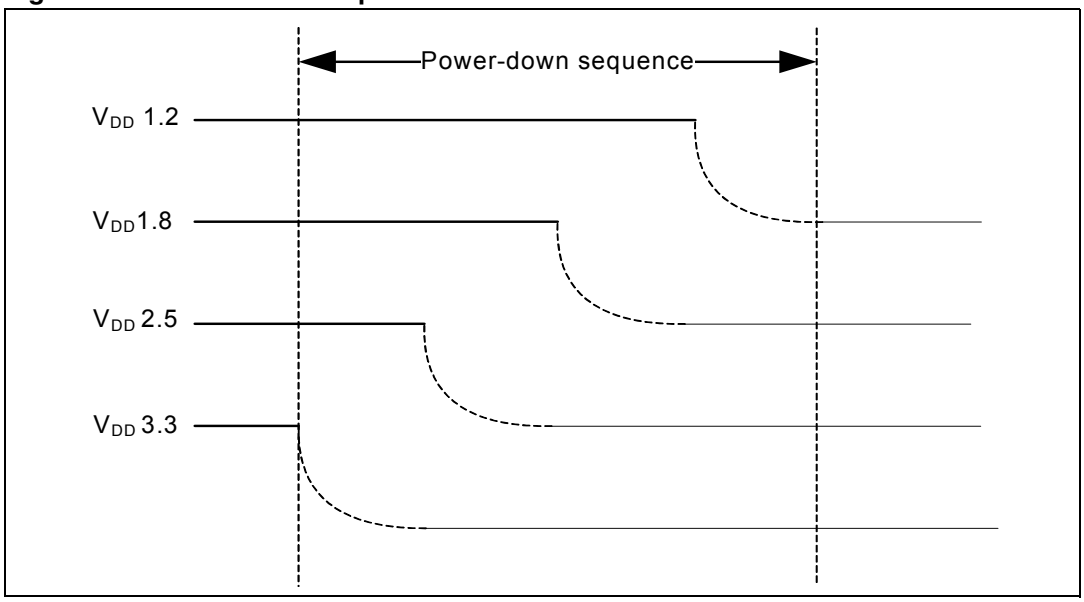
Figure 6. Power-up sequence



5.8 Removing power supplies for power saving

It is recommended to remove the the power supplies in the order shown in *Figure 7*. So V_{DD} 3.3 supply is to be removed first, then the V_{DD} 2.5 supply, followed by the V_{DD} 1.8 supply and last the V_{DD} 1.2.

Figure 7. Power-down sequence



5.9 Power on reset (MRESET)

The MRESET must remain active for at least 10 ms after all the power supplies are in the correct range and should become active in no more than 10 µs when one of the power supplies goes out of the correct range.

6 Timing requirements

6.1 DDR2 timing characteristics

The characterization timing is done considering an output load of 10 pF on all the DDR pads. The operating conditions are in worst case V = 0.90 V T_A = 125° C and in best case V=1.10 V T_A = 40° C.

6.1.1 DDR2 read cycle timings

Figure 8. DDR2 Read cycle waveforms

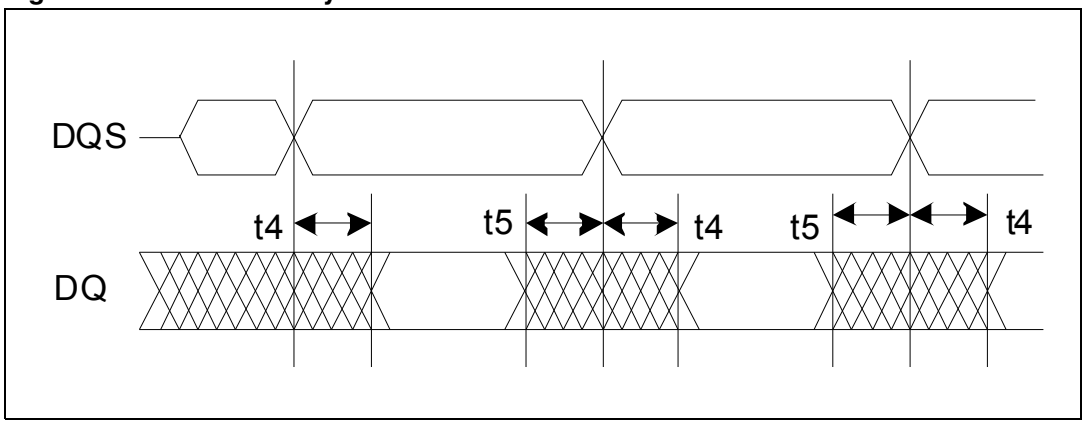


Figure 9. DDR2 Read cycle path

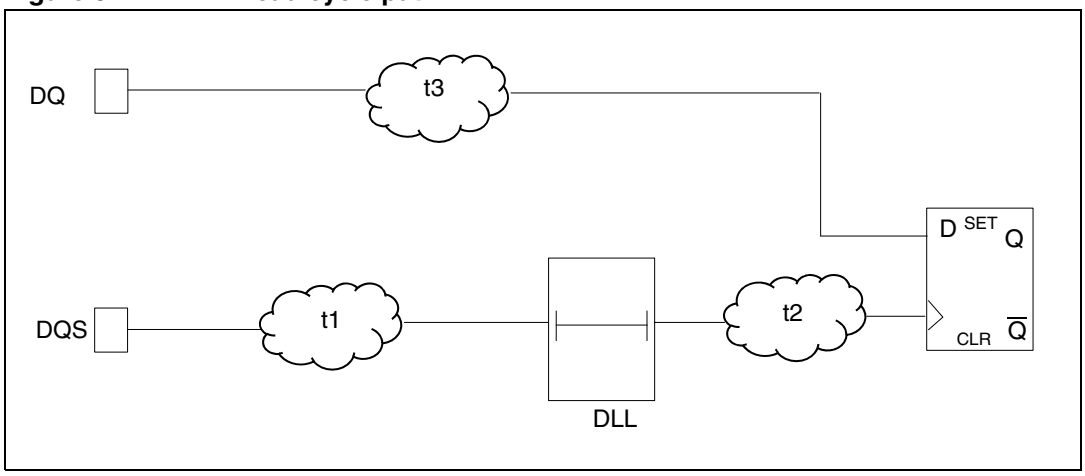


Table 25. DDR2 Read cycle timings

Frequency	t4 max	t5 max
333 MHz	1.24 ns	-495 ps
266 MHz	1.43 ns	-306 ps
200 MHz	1.74 ns	4 ps

Table 25. DDR2 Read cycle timings (continued)

Frequency	t4 max	t5 max
166 MHz	2.00 ns	260 ps
133 MHz	2.37 ns	634 ps

6.1.2 DDR2 write cycle timings

Figure 10. DDR2 Write cycle waveforms

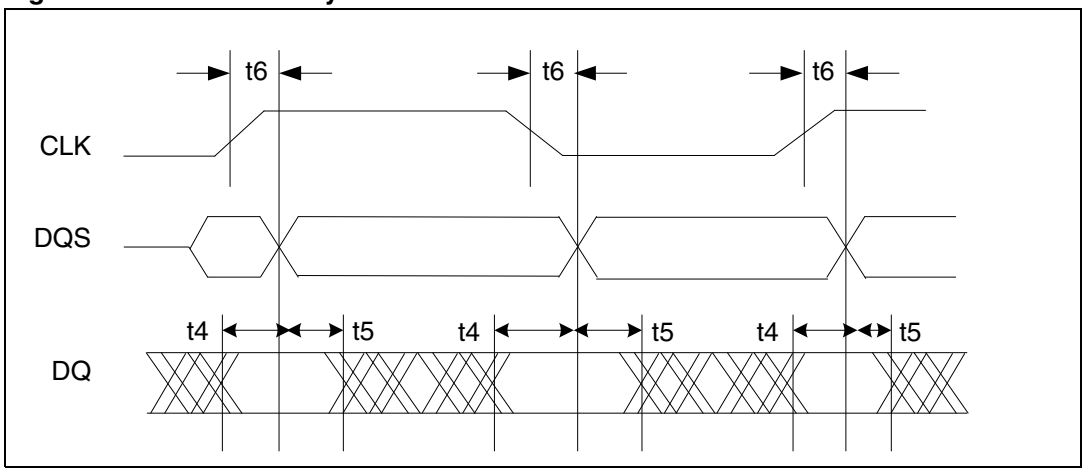


Figure 11. DDR2 Write cycle path

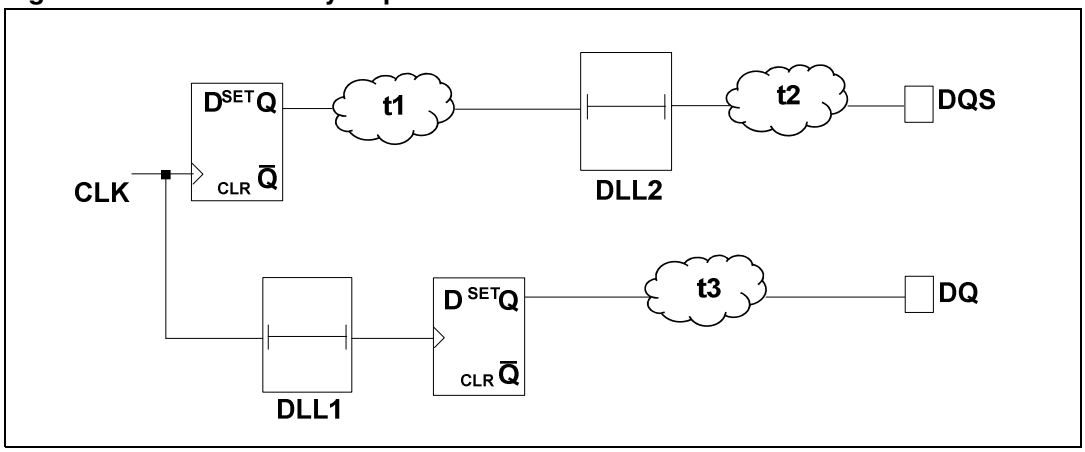


Table 26. DDR2 Write cycle timings

Frequency	t4 max	t5 max	Unit
333 MHz	1.36	-1.55	ns
266 MHz	1.55	-1.36	ns
200 MHz	1.86	-1.05	ns
166 MHz	2.11	- 794	ns
133 MHz	2.49	-420	ns

6.1.3 DDR2 command timings

Figure 12. DDR2 Command waveforms

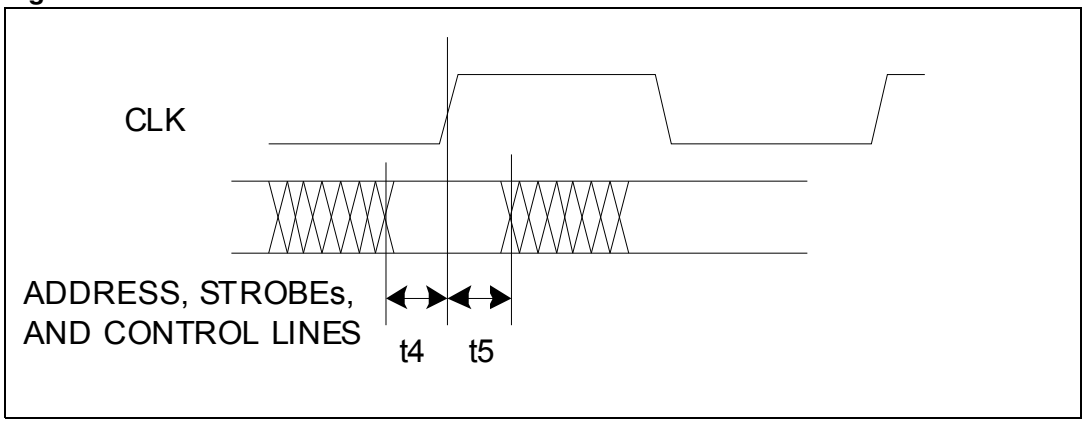


Figure 13. DDR2 Command path

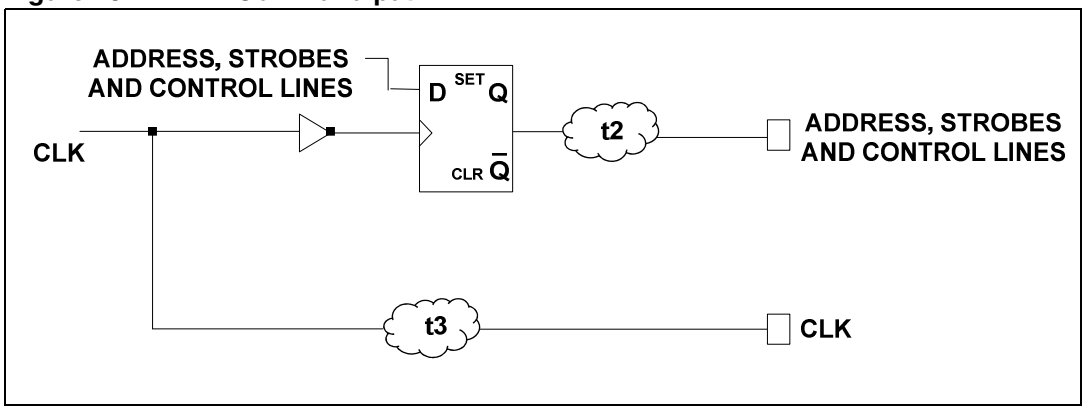


Table 27. DDR2 Command timings

Frequency	t4 max	t5 max	Unit
333 MHz	1.39	1.40	ns
266 MHz	1.77	1.78	ns
200 MHz	2.39	2.40	ns
166 MHz	2.90	2.91	ns
133 MHz	3.65	3.66	ns

6.2 I²C timing characteristics

The characterization timing is done considering an output load of 10 pF on SCL and SDA. The operating conditions are V = 0.90 V, T_A=125° C in worst case and V =1.10 V, T_A= 40° C in best case.

Figure 14. I²C output pins

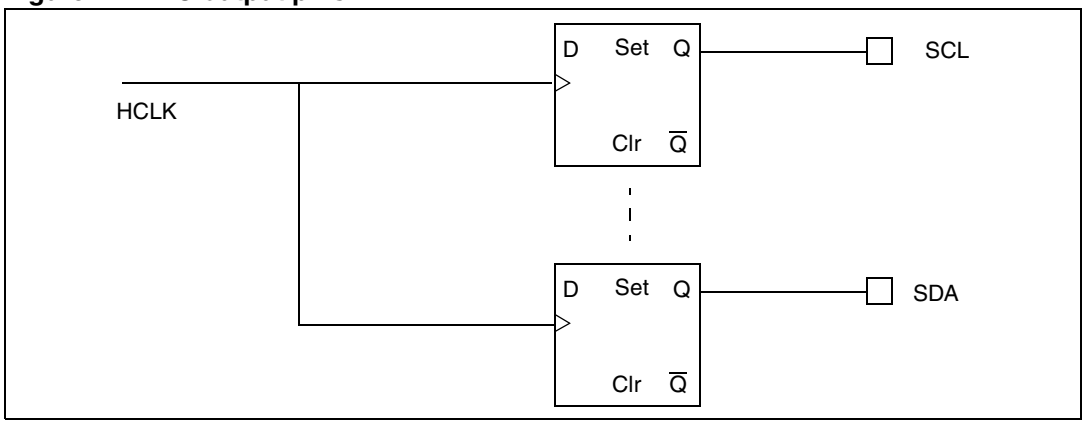
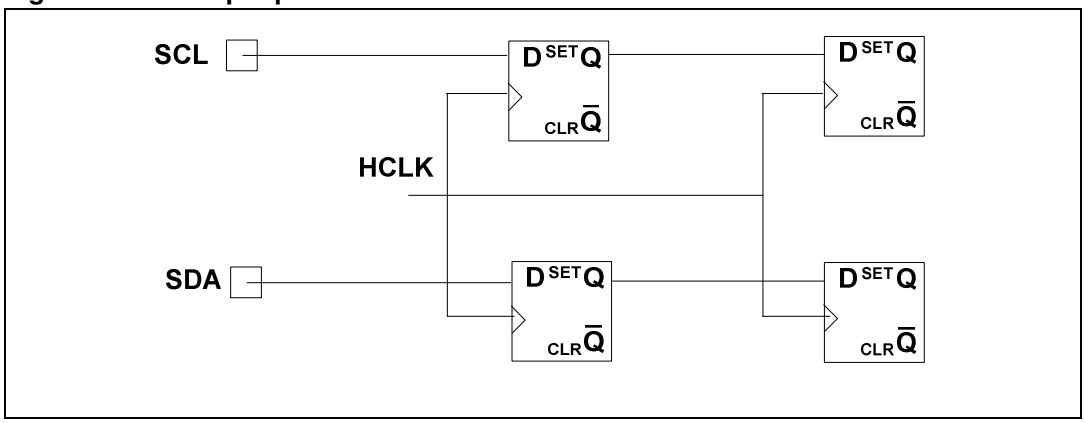


Figure 15. I²C input pins



The flip-flops used to capture the incoming signals are re-synchronized with the AHB clock (HCLK): so, no input delay calculation is required.

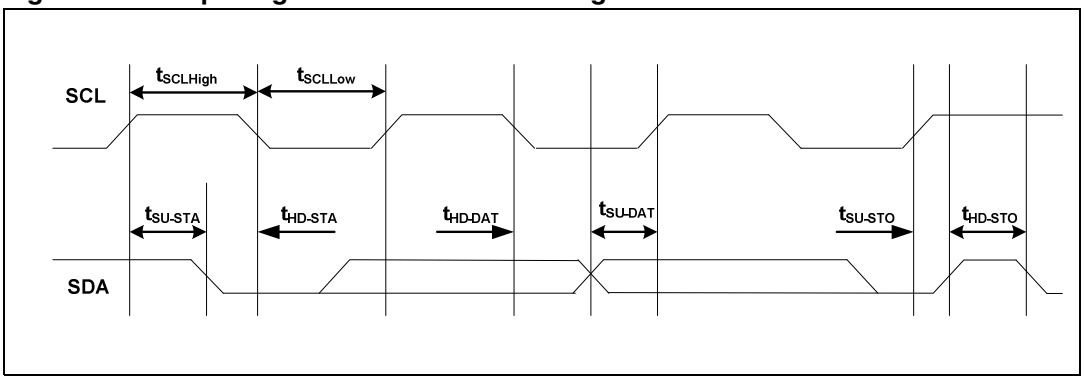
Table 28. Output delays for I²C signals

Parameter	Min	Max	Unit
$t_{HCLK->SCLH}$	8.1067	11.8184	ns
$t_{HCLK->SCLL}$	7.9874	12.6269	ns
$t_{HCLK->SDAH}$	7.5274	11.2453	ns
$t_{HCLK->SDAL}$	7.4081	12.0530	ns

Those values are referred to the common internal source clock which has a period of:

t_{HCLK} = 6 ns.

Figure 16. Output signal waveforms for I²C signals



The timing of high and low level of SCL ($t_{SCLHigh}$ and t_{SCLLow}) are programmable.

Table 29. Time characteristics for I²C in high-speed mode

Parameter	Min	Unit
t_{SU-STA}	157.5897	ns
t_{HD-STA}	325.9344	
t_{SU-DAT}	314.0537	
t_{HD-DAT}	0.7812	
t_{SU-STO}	637.709	
t_{HD-STO}	4742.1628	

Table 30. Time characteristics for I²C in fast speed mode

Parameter	Min	Unit
t_{SU-STA}	637.5897	ns
t_{HD-STA}	602.169	
t_{SU-DAT}	1286.0537	
t_{HD-DAT}	0.7812	
t_{SU-STO}	637.709	
t_{HD-STO}	4742.1628	

Table 31. Time characteristics for I²C in standard speed mode

Parameter	Min	Unit
t_{SU-STA}	4723.5897	ns
t_{HD-STA}	3991.9344	
t_{SU-DAT}	4676.0537	
t_{HD-DAT}	0.7812	
t_{SU-STO}	4027.709	
t_{HD-STO}	4742.1628	

Note: 1 The timings shown in Figure 16 depend on the programmed value of $T_{SCLHigh}$ and T_{SCLLow}, so the values present in the three tables here above have been calculated using the minimum programmable values of :

IC_HS_SCL_HCNT=19 and IC_HS_SCL_LCNT=53 registers (for High-Speed mode);

IC_FS_SCL_HCNT=99 and IC_FS_SCL_LCNT=215 registers (for Fast-Speed mode);

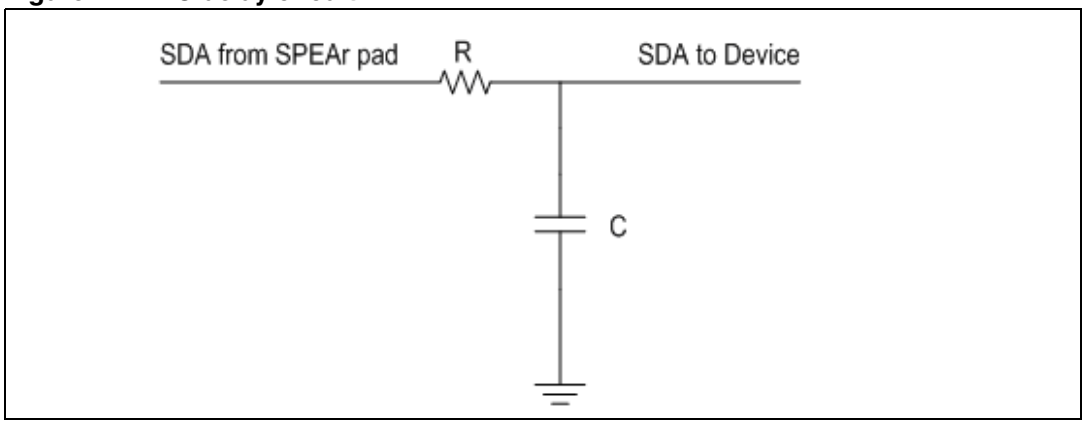
IC_SS_SCL_HCNT=664 and IC_SS_SCL_LCNT=780 registers (for Standard-Speed mode).

Note: 1 These minimum values depend on the AHB clock (HCLK) frequency, which is 166 MHz.

2 A device may internally require a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL (Please refer to the I^2C Bus Specification v3-0 Jun 2007). However, the SDA data hold time in the I^2C controller of SPEAr310 is one-clock cycle based (6 ns with the HCLK clock at 166 MHz). This time may be insufficient for some slave devices. A few slave devices may not receive the valid address due to the lack of SDA hold time and will not acknowledge even if the address is valid. If the SDA data hold time is insufficient, an error may occur.

*3 **Workaround:** If a device needs more SDA data hold time than one clock cycle, an RC delay circuit is needed on the SDA line as illustrated in the following figure:*

Figure 17. RC delay circuit



For example, R= K and C = 200 pF.

6.3 FSMC timing characteristics

The characterization timing is done considering an output load of 3 pF on the data, 15 pF on NF_CE, NF_RE and NF_WE and 10 pF on NF_ALE and NF_CLE.

The operating conditions are V= 0.90 V, T=125 °C in worst case and V=1.10 V, T= 40 °C in best case.

6.3.1 8-bit NAND Flash configuration

Figure 18. Output pads for 8-bit NAND Flash configuration

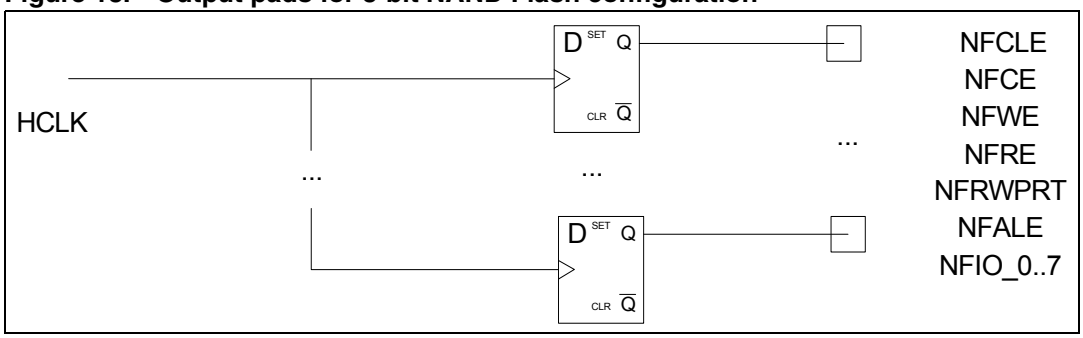


Figure 19. Input pads for 8-bit NAND Flash configuration

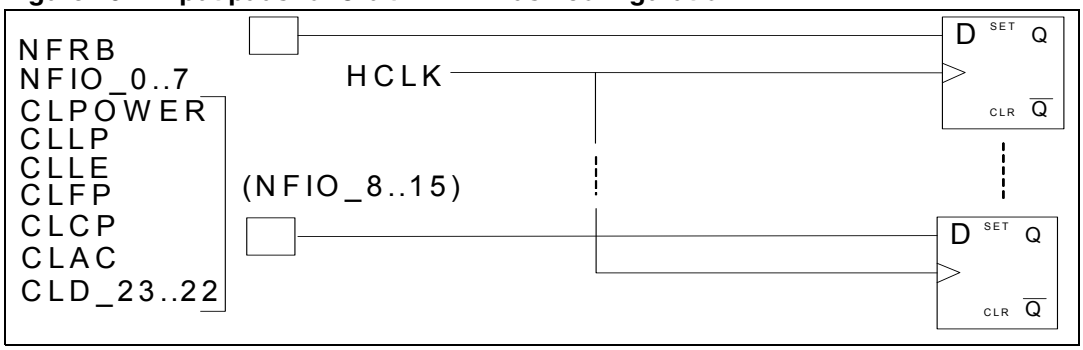


Figure 20. Output command signal waveforms for 8-bit NAND Flash configuration

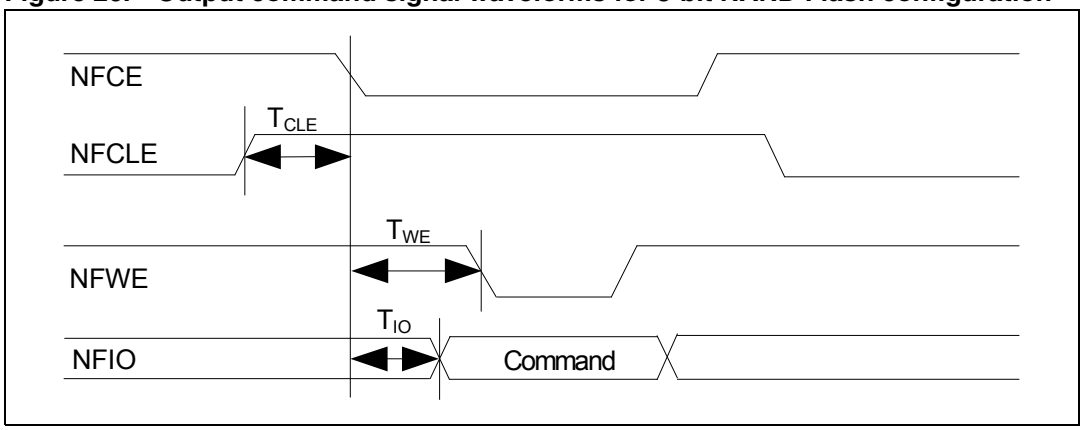


Figure 21. Output address signal waveforms for 8-bit NAND Flash configuration

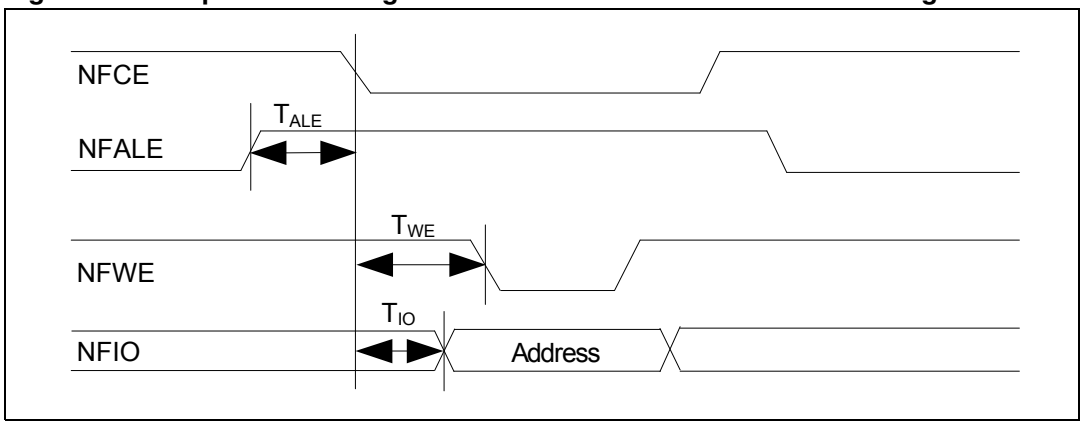


Figure 22. In/out data address signal waveforms for 8-bit NAND Flash configuration

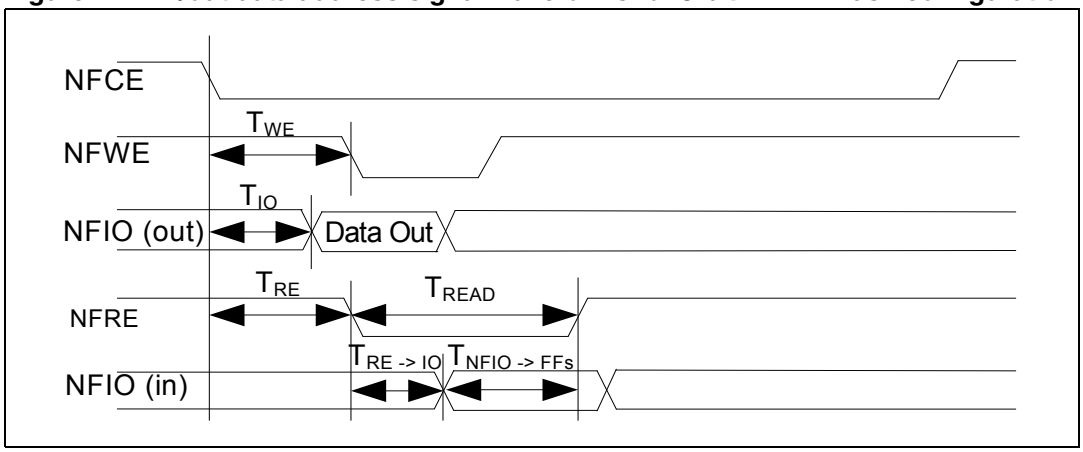


Table 32. Time characteristics for 8-bit NAND Flash configuration

Parameter	Min	Max
TCLE	-16.85 ns	-19.38 ns
TALE	-16.84 ns	-19.37 ns
TWE (s=1)	11.10 ns	13.04 ns
TRE (s=1)	11.18 ns	13.05 ns
TIO (h=1)	3.43 ns	8.86 ns

Note: Values in Table 32 are referred to the common internal source clock which has a period of THCLK = 6 ns.

6.3.2 16-bit NAND Flash configuration

Figure 23. Output pads for 16-bit NAND Flash configuration

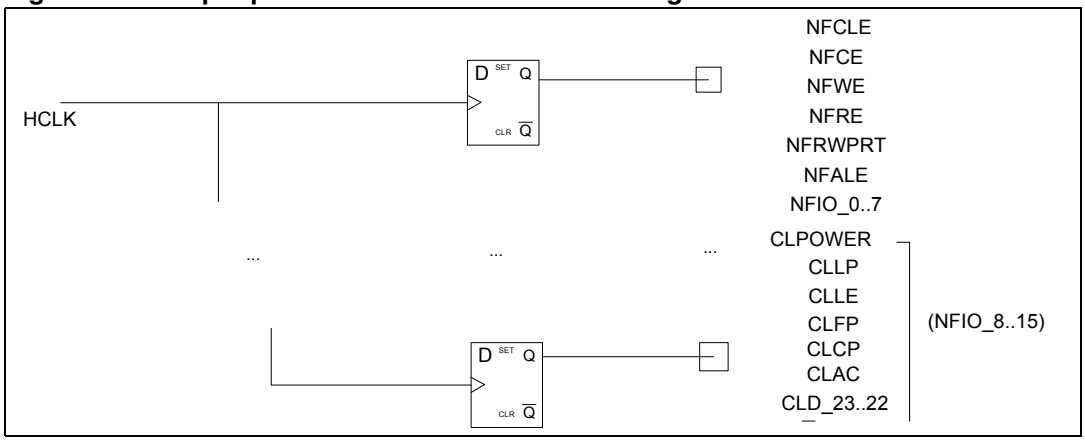


Figure 24. Input pads for 16-bit NAND Flash configuration

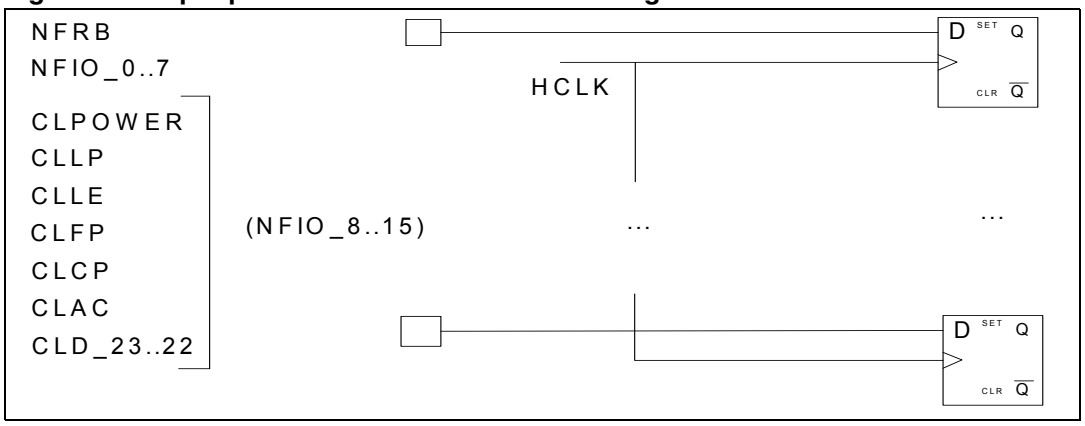


Figure 25. Output command signal waveforms 16-bit NAND Flash configuration

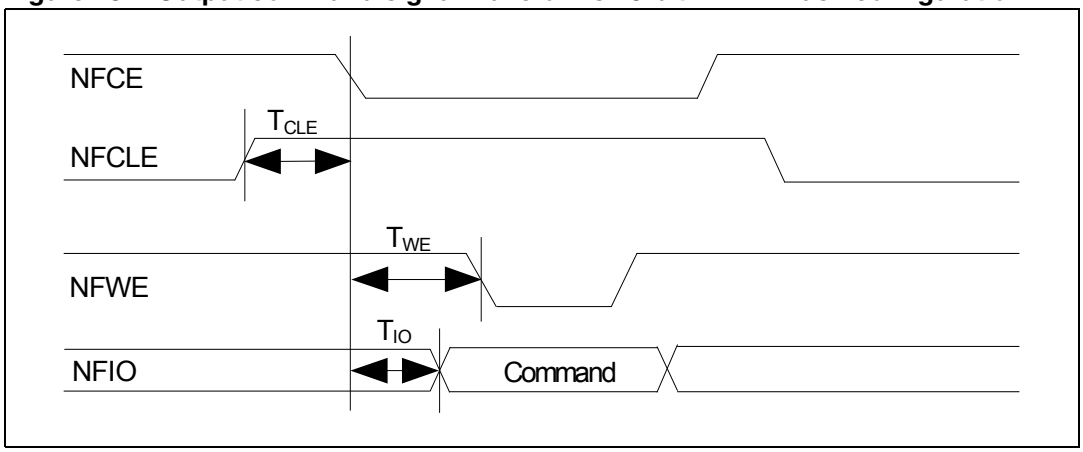


Figure 26. Output address signal waveforms 16-bit NAND Flash configuration

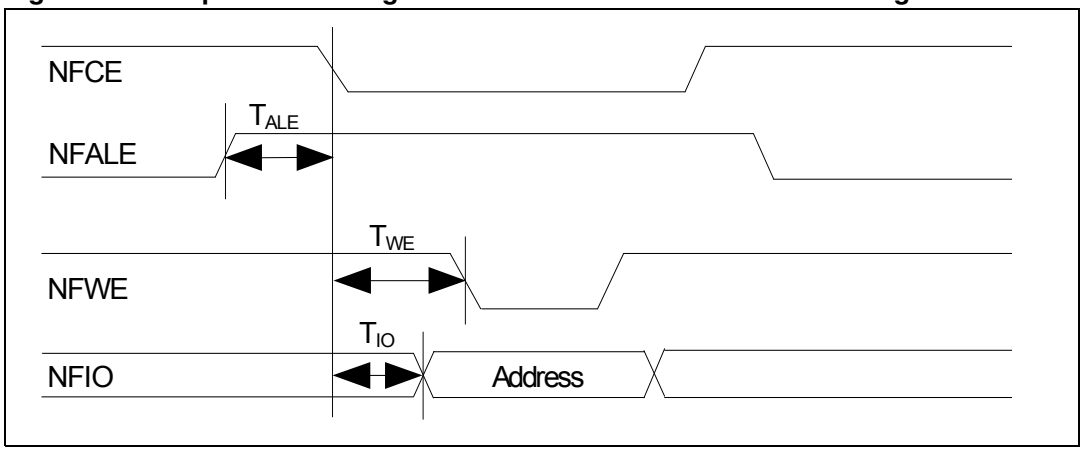


Figure 27. In/out data signal waveforms for 16-bit NAND Flash configuration

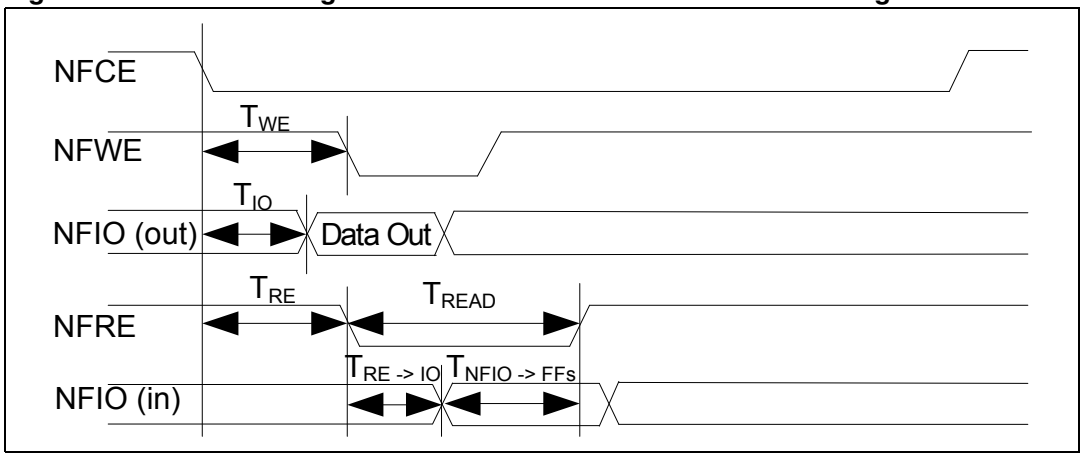


Table 33. Time characteristics for 16-bit NAND Flash configuration

Parameter	Min	Max
TCLE	-16.85 ns	-19.38 ns
TALE	-16.84 ns	-19.37 ns
TWE (s=1)	11.10 ns	13.04 ns
TRE (s=1)	11.18 ns	13.05 ns
TIO (h=1)	3.27 ns	11.35 ns

Note: Values in Table 33 are referred to the common internal source clock which has a period of THCLK = 6 ns.

6.4 Ether MAC 10/100 Mbps timing characteristics

The characterization timing is given for an output load of 5 pF on the MII TX clock and 10 pF on the other pads. The operating conditions are in worst case V=0.90 V, T=125 °C and in best case V=1.10 V, T= 40° C.

6.4.1 MII transmit timing specifications

Figure 28. MII TX waveforms

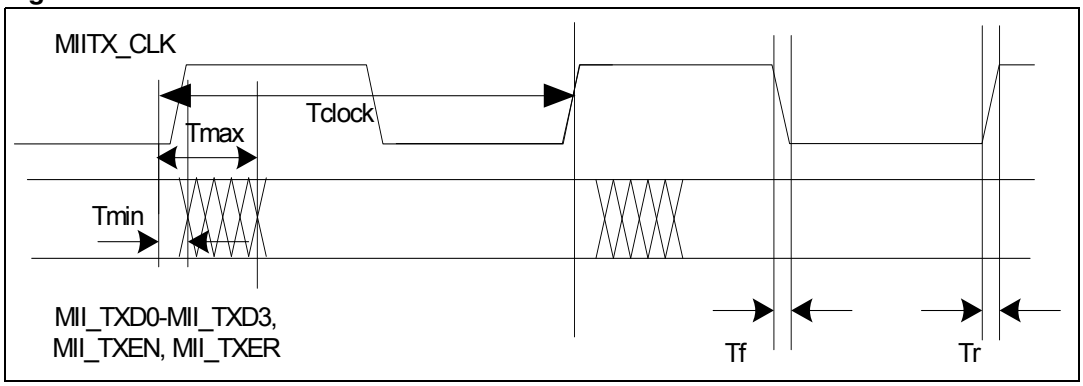


Figure 29. Block diagram of MII TX pins

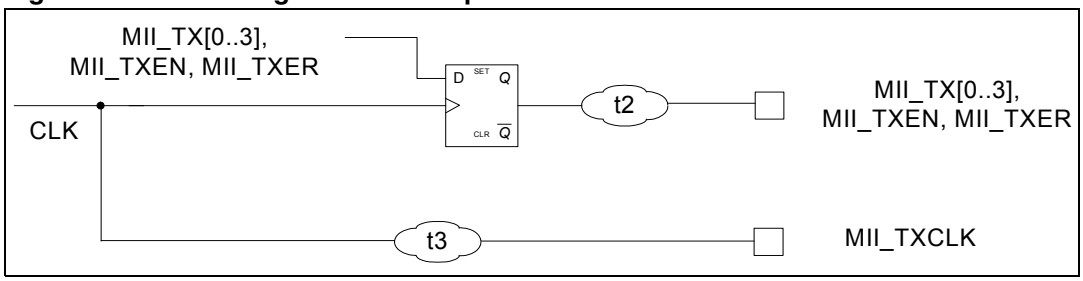


Table 34. MII TX timings

Parameter	Value using MII 100 Mb = 25 MHz	Value using MII 10 Mb = 2.5 MHz
t_{max}= $t2_{max}$- $t3_{min}$	6.8 ns	6.8 ns
t_{min}= $t2_{min}$- $t3_{max}$	2.9 ns	2.9 ns
t_{SETUP}	33.2 ns	393.2 ns

Note: To calculate the t_{SETUP} value for the PHY you have to consider the next t_{CLK} rising edge, so you have to apply the following formula: $t_{SETUP} = t_{CLK} - t_{max}$

6.4.2 MII receive timing specifications

Figure 30. MII RX waveforms

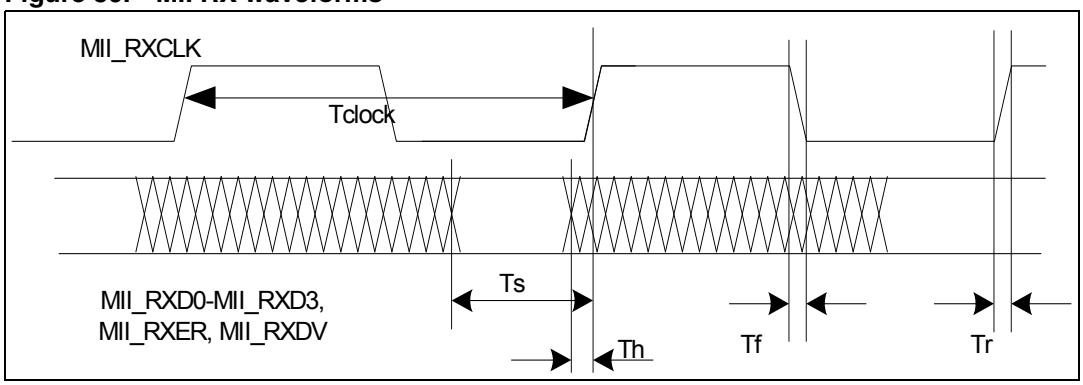
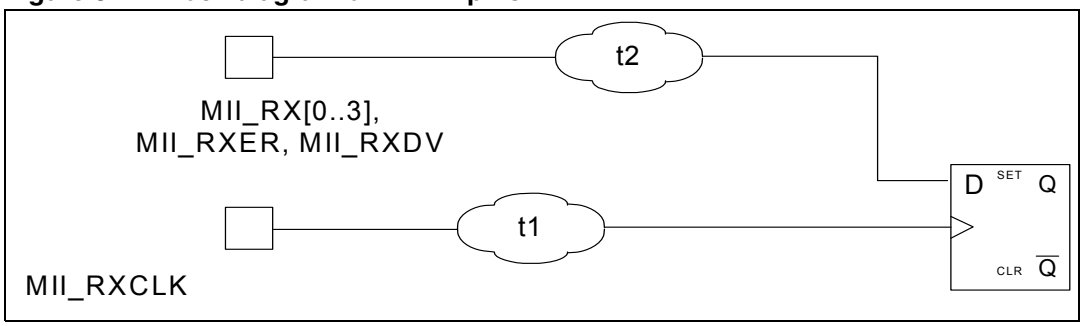


Figure 31. Block diagram of MII RX pins



6.4.3 MDIO timing specifications

Figure 32. MDC waveforms

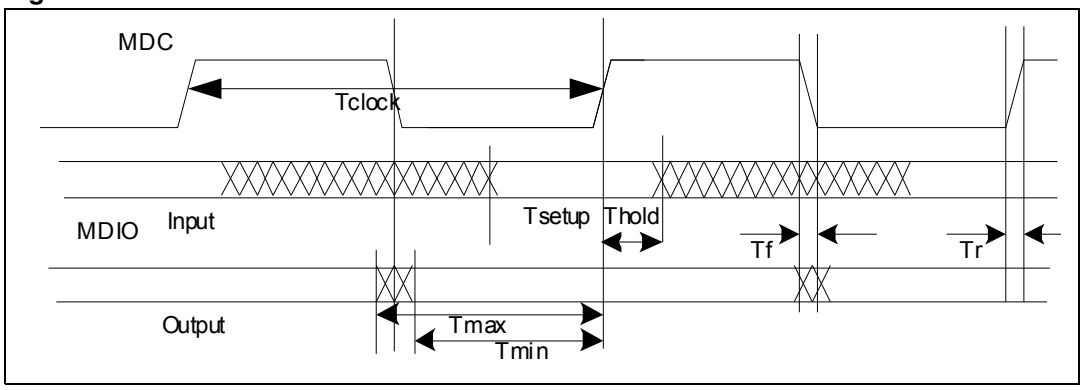


Figure 33. Paths from MDC/MDIO pads

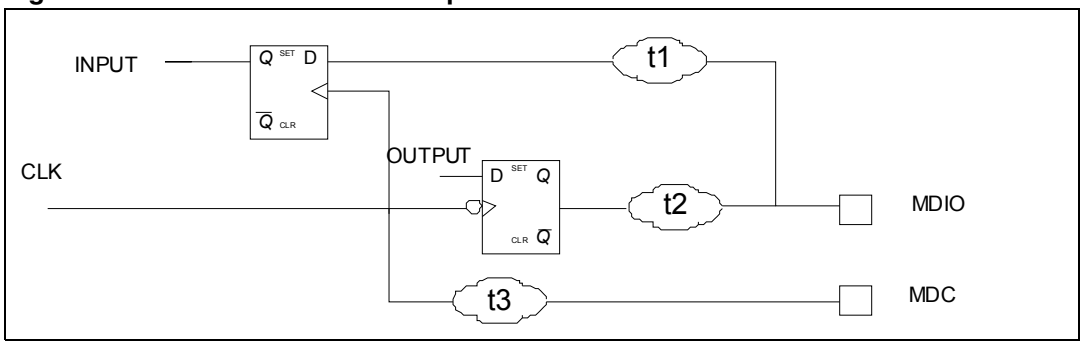


Table 35. MDC/MDIO timing

Parameter	Value	Frequency
t_{CLK} period	614.4 ns	1.63 MHz
t_{CLK} fall (t_f)	1.18 ns	
t_{CLK} rise (t_r)	1.14 ns	
Output		
$t_{max} = \sim t_{CLK}/2$	307 ns	
$t_{min} = \sim t_{CLK}/2$	307 ns	
Input		
$t_{SETUPmax} = t1_{max} - t3_{min}$	6.88 ns	
$t_{HOLDmin} = t1_{min} - t3_{max}$	-1.54 ns	

Note: When MDIO is used as output the data are launched on the falling edge of the clock as shown in Figure 32.

6.5 SMI - Serial memory interface timing characteristics

Figure 34. SMI_DATAIN data path

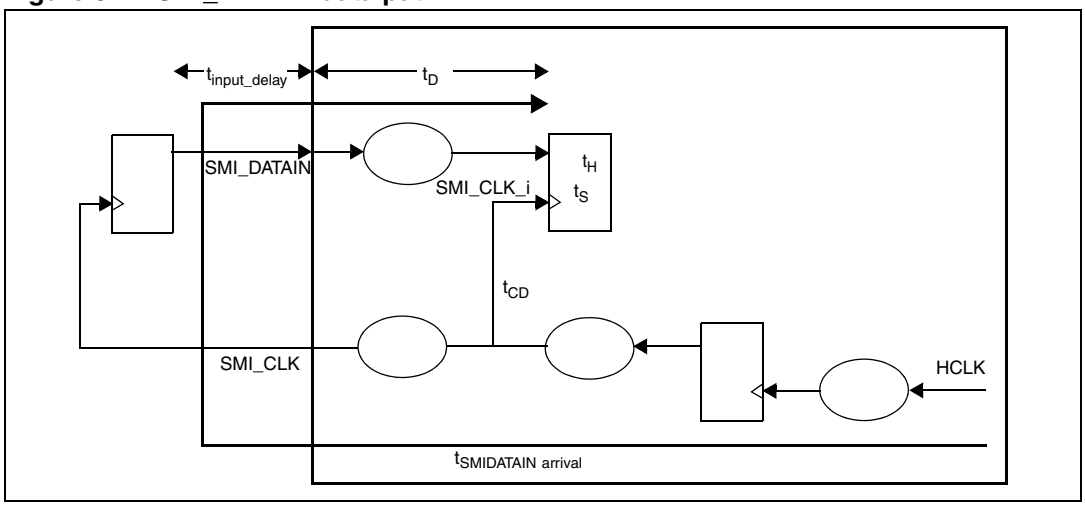


Table 36. SMI_DATAIN timings

Signal	Parameter	Value
SMI_DATAIN	t_{d_max}	$t_{SMIDATAIN\_arrival\_max} - t_{input\_delay}$
	t_{d_min}	$t_{SMIDATAIN\_arrival\_min} - t_{input\_delay}$
	t_{cd_min}	$t_{SMI\_CLK\_i\_arrival\_min}$
	t_{cd_max}	$t_{SMI\_CLK\_i\_arrival\_max}$
	t_{SETUP_max}	$t_s + t_{d\_max} - t_{cd\_min}$
	t_{HOLD_min}	$t_h - t_{d\_min} + t_{cd\_max}$

Figure 35. SMI_DATAOUT/SMI_CSn data paths

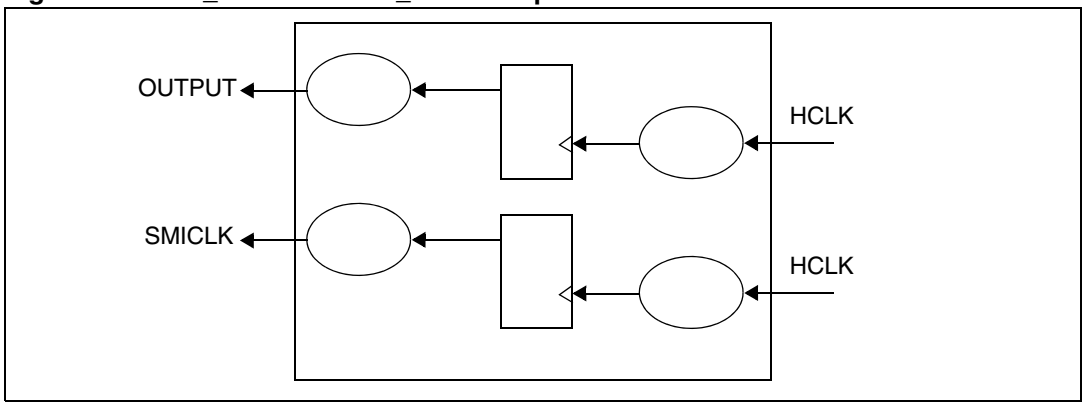


Figure 36. SMI_DATAOUT timings

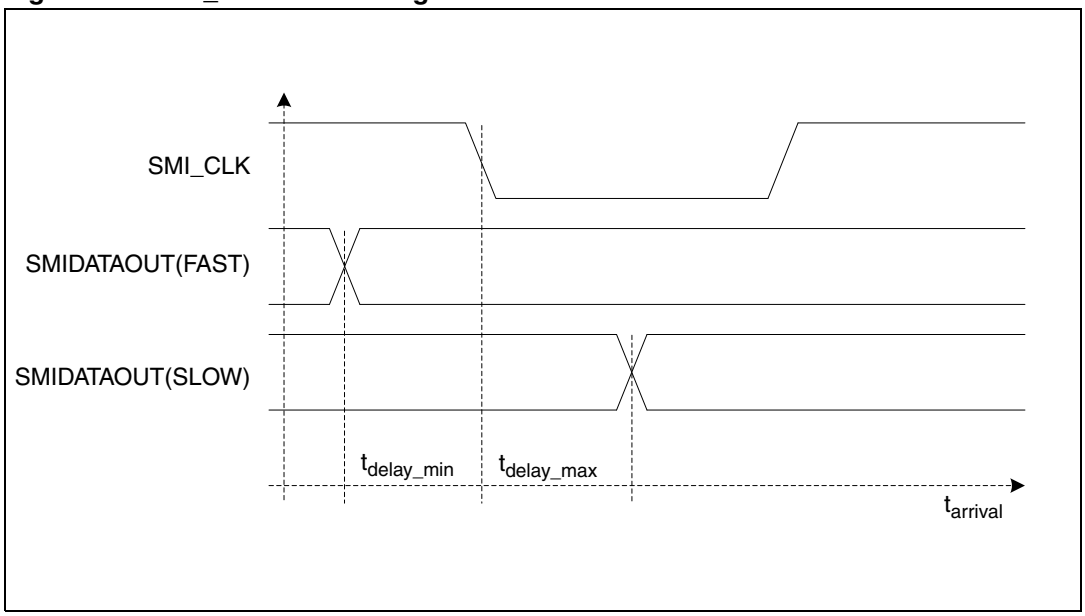


Table 37. SMI_DATAOUT timings

Signal	Parameter	Value
SMI_DATAOUT	t_{delay_max}	$t_{arrivalSMIDATAOUT\_max} - t_{arrival\_SMI\_CLK\_min}$
	t_{delay_min}	$t_{arrivalSMIDATAOUT\_min} - t_{arrival\_SMI\_CLK\_max}$

Figure 37. SMICSn fall timings

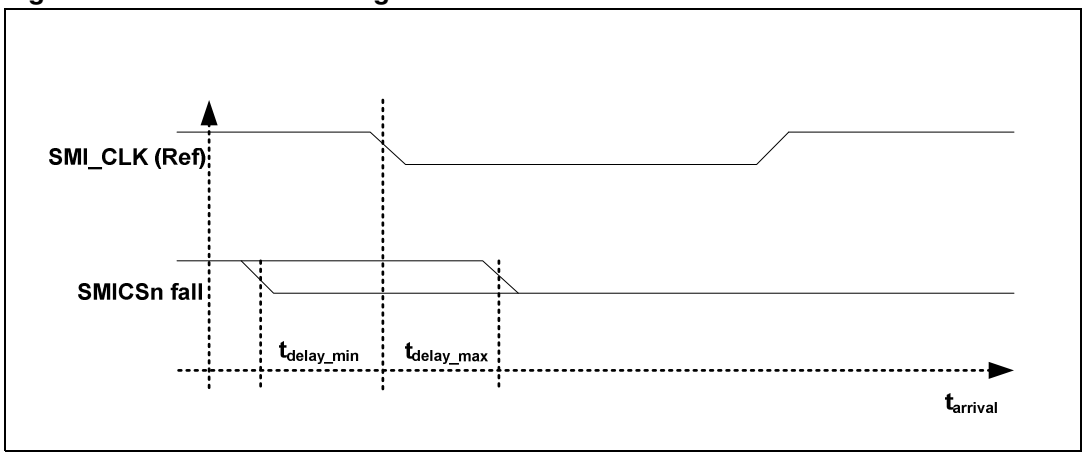


Table 38. SMI_CSn fall timings

Signal	Parameter	Value
SMI_CSn fall	t_{delay_max}	$t_{arrivalSMICSn\_max\_fall} - t_{arrival\_SMI\_CLK\_min\_fall}$
	t_{delay_min}	$t_{arrivalSMICSn\_min\_fall} - t_{arrival\_SMI\_CLK\_max\_fall}$

Figure 38. SMI_CSn rise timings

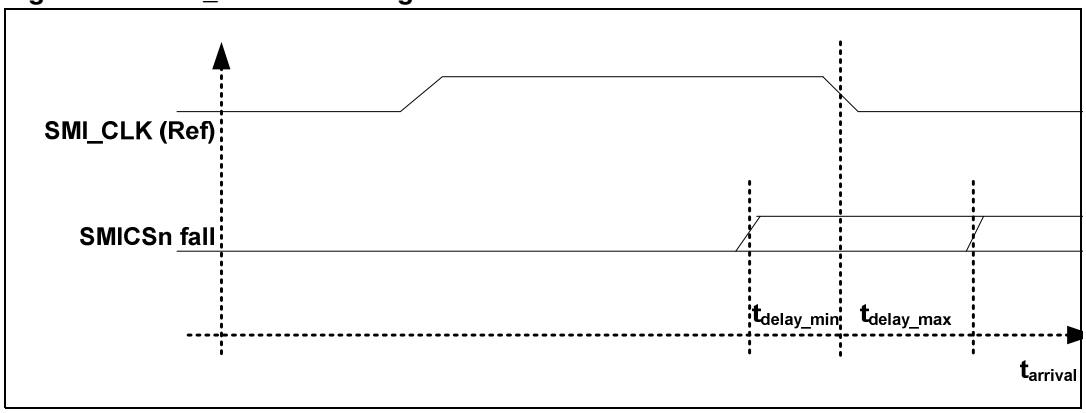


Table 39. SMI_CSn rise timings

Signal	Parameter	Value
SMI_CSn rise	t_{delay_max}	$t_{arrivalSMICSn\_max\_rise}$ - $t_{arrival\_SMI\_CLK\_min\_fall}$
	t_{delay_min}	$t_{arrivalSMICSn\_min\_rise}$ - $t_{arrival\_SMI\_CLK\_max\_fall}$

Table 40. Timing requirements for SMI

Parameter		Input setup-hold/output delay		
		Max	Min	Unit
SMI_CLK	Fall time	1.82	1.40	ns
	Rise time	1.63	1.19	
SMIDATAIN	Input setup time	8.27		
	Input hold time	-2.59		
SMIDATAOUT Output valid time		2.03		
SMICS_0 Output valid time	fall	1.92		
	rise	1.69		
SMICS_1Output valid time	fall	1.78		
	rise	1.63		

6.6 SSP timing characteristics

This module provides a programmable length shift register which allows serial communication with other SSP devices through a 3 or 4 wire interface (SSP_CLK, SSP_MISO, SSP_MOSI and SSP_CSn). The SSP supports the following features:

- Master/Slave mode operations
- Chip-selects for interfacing to multiple slave SPI devices.
- 3 or 4 wire interface (SSP_SCK, SSP_MISO, SSP_MOSI and SSP_CSn)
- Single interrupt
- Separate DMA events for SPI Receive and Transmit
- 16-bit shift register
- Receive buffer register
- Programmable character length (2 to 16 bits)
- Programmable SSP clock frequency range
- 8-bit clock pre-scaler
- Programmable clock phase (delay or no delay)
- Programmable clock polarity

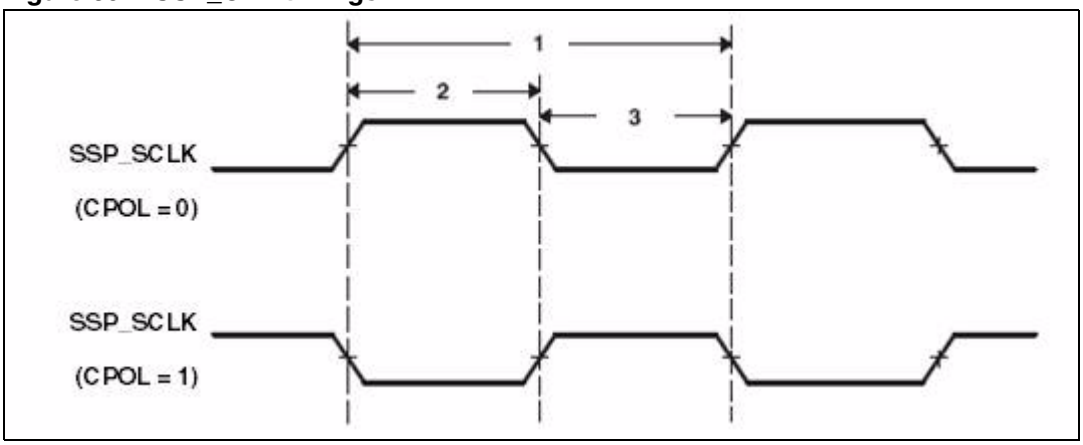
Note: The following tables and figures show the characterization of the SSP using the SPI protocol.

Table 41. Timing requirements for SSP (all modes)

No.	Parameters		Value	Unit
1	$T_{c(CLK)}$	Cycle time, SSP_CLK	24	ns
2	$T_{w(CLKH)}$	Pulse duration, SSP_CLK high	0.49T - 0.51T	ns
3	$T_{w(CLKL)}$	Pulse duration, SSP_CLK low	0.51T - 0.49T	ns

T = Tc(CLK) = SSP_CLK period is equal to the SSP module master clock divided by a configurable divider.

Figure 39. SSP_CLK timings



6.6.1 SPI master mode timings (clock phase = 0)

Table 42. Timing requirements for SPI master mode (clock phase = 0)

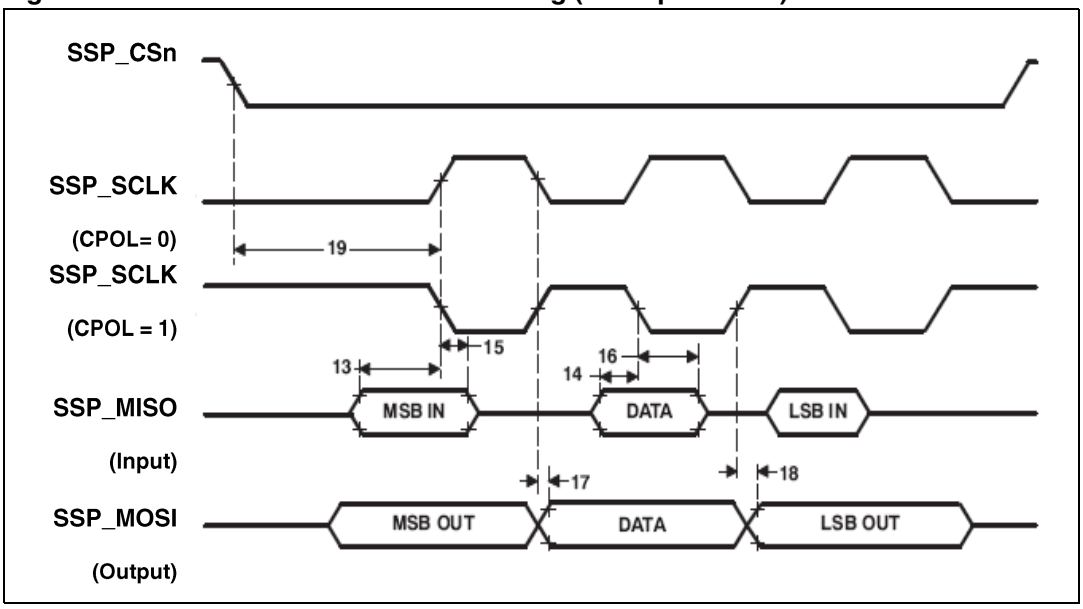
No.	Parameters			Min	Max	Unit
13	$t_{su(DIV-CLKL)}$	Setup time, MISO (input) valid before SSP_CLK (output) rising edge	Clock Polarity = 0	-0.411	-0.342	ns
14	$t_{su(DIV-CLKH)}$	Setup time, MISO (input) valid before SSP_CLK (output) falling edge	Clock Polarity = 1	-0.411	-0.342	ns
15	$t_{h(CLKL-DIV)}$	Hold time, MISO (input)valid after SSP_CLK (output) rising edge	Clock Polarity = 0	0.912	1.720	ns
16	$t_{h(CLKH-DIV)}$	Hold time, MISO (input) valid after SSP_CLK (output) falling edge	Clock Polarity = 1	0.912	1.720	ns

P = 1/SSP_CLK in nanoseconds (ns). For example, if the SSP_CLK frequency is 83 MHz, use P = 12.048 ns

Table 43. Switching characteristics over recommended operating conditions for SPI master mode (clock phase = 0)

No.	Parameters			Min	Max	Unit
17	$t_{d(CLKH-DOV)}$	Delay time, SSP_CLK (output) falling edge to MOSI (output) transition	Clock Polarity = 0	-3.138	2.175	ns
18	$t_{d(CLKL-DOV)}$	Delay time, SSP_CLK (output) rising edge to MOSI (output) transition	Clock Polarity = 1	-3.138	2.175	ns
19	$t_{d(ENL-CLKH/L)}$	Delay time, SSP_CSn (output) falling edge to first SSP_CLK (output) rising or falling edge		T/2		ns
20	$t_{d(CLKH/L-ENH)}$	Delay time, SSP_CLK (output) rising or falling edge to SSP_CSn (output) rising edge		T		ns

Figure 40. SPI master mode external timing (clock phase = 0)



6.6.2 SPI master mode timings (clock phase = 1)

Table 44. Timing requirements for SPI master mode (clock phase = 1)

No.	Parameters			Min	Max	Unit
4	$t_{su(DIV-CLKL)}$	Setup time, MISO (input) valid before SSP_CLK (output) falling edge	Clock polarity = 0	-0.411	-0.342	ns
5	$t_{su(DIV-CLKH)}$	Setup time, MISO (input) valid before SSP_CLK (output) rising edge	Clock polarity = 1	-0.411	-0.342	ns
6	$t_{h(CLKL-DIV)}$	Hold time, MISO (input) valid after SSP_CLK (output) falling edge	Clock polarity = 0	0.912	1.720	ns
7	$t_{h(CLKH-DIV)}$	Hold time, MISO (input) valid after SSP_CLK (output) rising edge	Clock polarity = 1	0.912	1.720	ns

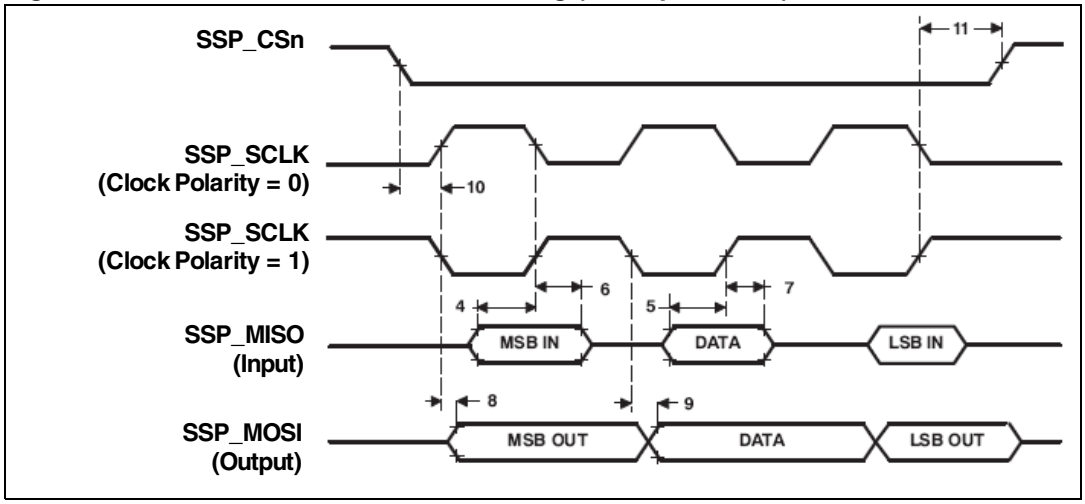
Table 45. Switching characteristics over recommended operating conditions for SPI master mode (clock phase = 1)

No.	Parameters			Min	Max	Unit
8	$t_{d(CLKH-DOV)}$	Delay time, SSP_CLK (output) rising edge to MOSI (output) transition	Clock Polarity = 0	-3.138	2.175	ns
9	$t_{d(CLKL-DOV)}$	Delay time, SSP_CLK (output) falling edge to MOSI (output) transition	Clock Polarity = 1	-3.138	2.175	ns

Table 45. Switching characteristics over recommended operating conditions for SPI master mode (clock phase = 1) (continued)

No.	Parameters		Min	Max	Unit
10	$t_{d(ENL-CLKH/L)}$	Delay time, SSP_CSn (output) falling edge to first SSP_CLK (output) rising or falling edge	T		ns
11	$td_{(CLKH/L-ENH)}$	Delay time, SSP_CLK (output) rising or falling edge to SSP_CSn (output) rising edge	T/2		ns

Figure 41. SPI master mode external timing (clock phase = 1)



6.7 UART (Universal asynchronous receiver/transmitter) timing characteristics

Figure 42. UART transmit and receive timings

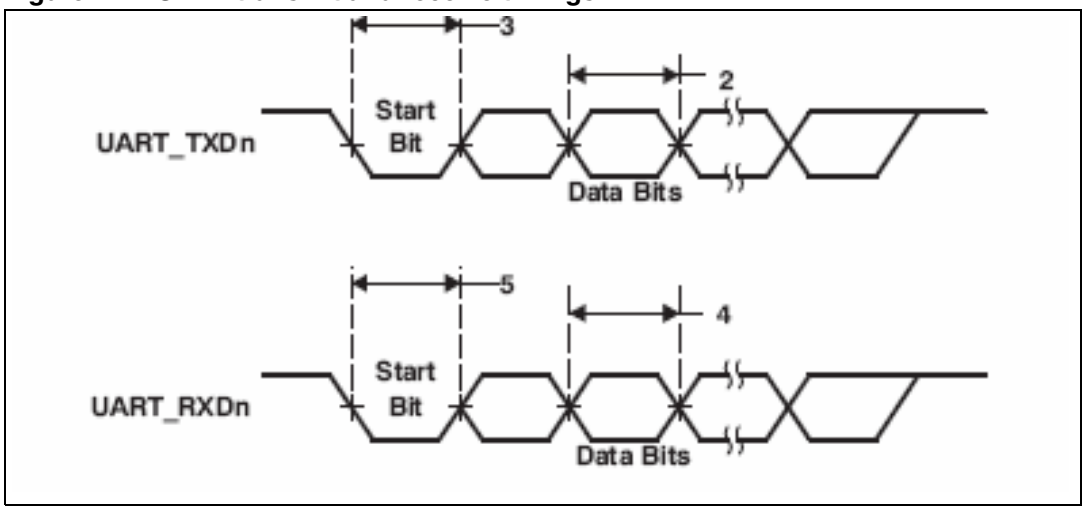


Table 46. UART transmit timing characteristics

S.No.	Parameters	Min	Max	Unit
1	UART Maximum Baud Rate		3	Mbps
2	UART Pulse Duration Transmit Data (TxD)	$0.99B_{(1)}$	$B_{(1)}$	ns
3	UART Transmit Start Bit	$0.99B_{(1)}$	$B_{(1)}$	ns

Table 47. UART receive timing characteristics

S.No.	Parameters	Min	Max	Units
4	UART Pulse Duration Receive Data (RxD)	$0.97B_{(1)}$	$1.06B_{(1)}$	ns
5	UART Receive Start Bit	$0.97B_{(1)}$	$1.06B_{(1)}$	ns

where (1) B = UART baud rate

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 48. LFBGA289 (15 x 15 x 1.7 mm) mechanical data

Dim.	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.700			0.0669
A1	0.270			0.0106		
A2		0.985			0.0387	
A3		0.200			0.0078	
A4			0.800			0.0315
b	0.450	0.500	0.550	0.0177	0.0197	0.0217
D	14.850	15.000	15.150	0.5846	0.5906	0.5965
D1		12.800			0.5039	
E	14.850	15.000	15.150	0.5846	0.5906	0.5965
E1		12.800			0.5039	
e		0.800			0.0315	
F		1.100			0.0433	
ddd			0.200			0.0078
eee			0.150			0.0059
fff			0.080			0.0031

Figure 43. LFBGA289 package dimensions

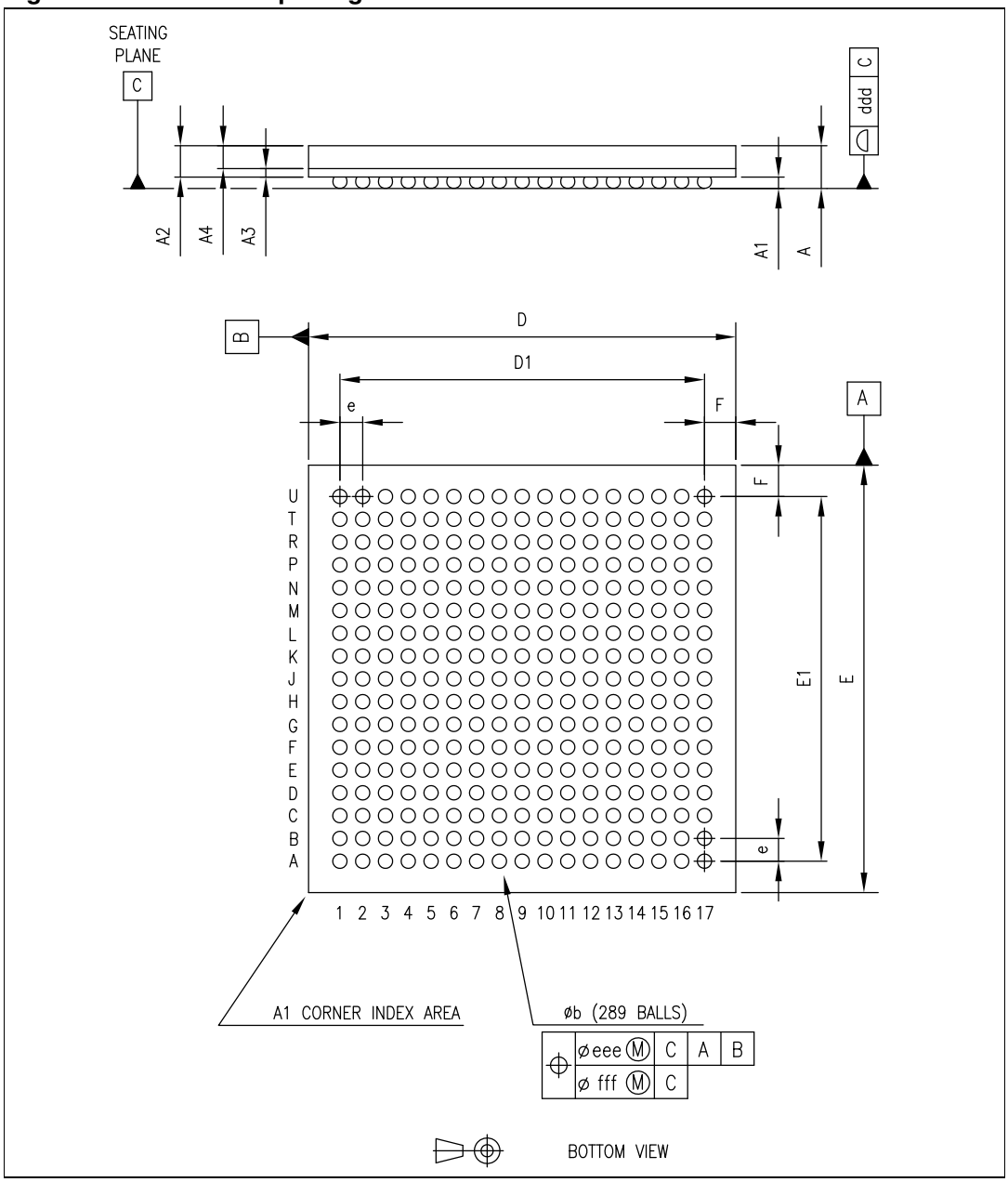


Table 49. Thermal resistance characteristics

Package	Θ_{JC} (°C/W)	Θ_{JB} (°C/W)
LFBGA289	18.5	24.5

8 Revision history

Table 50. Document revision history

Date	Revision	Changes
16-Oct-2009	1	Initial release.
02-Mar-2010	2	Changed “SPI” to “SSP” where applicable. Updated features list on coverpage. Updated *Figure 1: Functional block diagram* and *Figure 2: Typical system architecture using SPEAr310* Corrected *Figure 4: Typical SMII system* Updated *Section 3.3: Shared I/O pins (PL_GPIOs)*: – Added *Section 3.3.1: PL_GPIO pin description*, *Section 3.3.5: GPIOs* and *Section 3.3.6: Multiplexing scheme* – Updated *Table 10: PL_GPIO multiplexing scheme* and *Table 11: Table shading* Added *Section 3.4: PL_GPIO pin sharing for debug modes* Added V_{DD} RTC lines in *Table 14: Absolute maximum ratings* and *Table 15: Maximum power consumption* Updated *Table 16: Recommended operating conditions* Changed title of *Section 5.5: 3.3V I/O characteristics* Updated *Table 22: Driver characteristics* (difference made between strong and weak values of output independance) Updated *Section 5.7: Power up sequence* Added *Section 5.8: Removing power supplies for power saving* Separated *Electrical characteristics* and *Timing requirements* into two sections. Deleted “1000 Mbps” from title of *Section 6.4: Ether MAC 10/100 Mbps timing characteristics* Corrected signal names in *Section 6.5: SMI - Serial memory interface timing characteristics* Updated *Section 6.6: SSP timing characteristics* (SPI replaced by SSP where applicable). Minor text corrections.

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