LCD Segment Driver series

Multifunction Segment Drivers

BU97930MUV,BU97931FV,BU9798KV,BU9798GUW,BU97500KV

No.10044EAT04

●Description

New released Multi-function type segment drivers support GPO function, LED driving function, static-driving mode, and Blink function that can blink each segment individually.
ROHM Multi-function segment driver series contribute to reduction in cost of system and easy software development.

●Features (BU97930MUV, BU97931FV, BU9798KV/GUW)

1) LCD drive output
   Common output : 4, Segment output : 27 (BU97930MUV)
   Common output : 4, Segment output : 28 (BU97931FV)
   Common output : 4, Segment output : 49 (BU9798KV/GUW)
2) Integrated Display data RAM (DDRAM)
   RAM: 28*4 =112 bit (BU97930MUV, BU97931FV)
   RAM: 49*4 =196 bit (BU9798KV/GUW)
3) 3-wire Serial interface (SD, SCL, CSB)
4) Integrated Oscillator circuit
5) Integrated LCD Voltage generator circuit
   Support: 1/3 Bias, 1/3 or 1/4 Duty
   Support: 1/1 Bias, 1/1Duty (Static Driving)
   Integrated buffer amp
   Integrated regulator for LCD drive: 3.2, 3.3, 3.4, 4.4, 4.5, 4.6, 5.0V selectable (BU9798KV/GUW)
6) Support Split Supply for Logic (VDD) and LCD (VLCD)
7) Integrated LED driver circuit
8) Segment terminals operation, segment output mode/GPO output mode selectable
9) Segment terminals operation, segment output mode/LED output mode selectable (BU9798KV/GUW)
10) Support PWM source select, external clock or internal clock
    Resolution 8bit mode/12bit mode selectable (BU9798KV/GUW)
    Resolution 8bit mode (BU97930MUV, BU97931FV)
11) Low power consumption design
12) Support standby mode
13) Integrated Power-On-Reset circuit (POR).
14) No external component
15) Support Independent blink function
    Blink frequency 1.6, 2.0, 2.6, 4.0Hz selectable
16) Operating power supply : 1.8 ~ 3.6V
17) LCD drive power supply : 2.7 ~ 5.5V (BU97930MUV, BU97931FV)
    : 3.3 ~ 5.5V (BU9798KV/GUW)

●**Features (BU97500KV)**

1) LCD drive output:
   Common output : 4, Segment output : 51
2) Integrated Display data RAM (DDRAM)
   RAM: 51*4 =204 bit
3) 3-wire Serial interface (SD, SCL, CSB)
4) Integrated Oscillator circuit
5) Integrated Power supply circuit for LCD driving:
   Support 1/2 and 1/3 Bias
   Support 1/3 and 1/4 Duty
   Integrated Buffer AMP
6) Support Split Supply for Logic (VDD) and LCD (VLCD)
7) Segment terminals operation, segment output mode/GPO output mode selectable
8) Low power consumption design
9) Support standby mode
10) Integrated Power-on Reset circuit
11) No external components
12) Operating power supply: VDD = 2.7 ~ 5.5V
13) LCD drive power supply: VLCD=4.5 ~ 5.5V

●**Applications**

Telephone, FAX, Portable equipment (POS, ECR, PDA etc.),
DSC, DVC, Car Audio, Home electrical appliance, Meter equipment, Healthcare equipment etc.

●**Line up matrix**

Parameter	BU97930MUV	BU97931FV	BU9798KV/GUW	BU97500KV
Segment output	27	28	49	52 (1/3Duty) 51 (1/4Duty)
Common output	1 / 3 / 4	1 / 3 / 4	1 / 3 / 4	3 (1/3Duty) 4 (1/4Duty)
Total display dot number	108	112	196	156 (1/3Duty) 204 (1/4Duty)
Adjustable contrast function	-	-	YES	-
Support split voltage supply	YES	YES	YES	YES
Interface	3wireSPI	3wire SPI	3wire SPI	3wire SPI
Package	VQFN040V6060	SSOP-B40	VQFP64 / VBGA063W050	VQFP64

●Absolute maximum ratings (VSS = 0V)

Parameter	BU97930MUV	BU97931FV	BU9798KV /GUW	BU97500KV	Unit	Remarks
Power Supply Voltage1 (VDD)	-0.3 ~ +4.5			-0.5 ~ +7.0	V	Power supply
Power Supply Voltage 2 (VLCD)	-0.5 ~ +7.0				V	LCD drive Voltage
Allowable Loss (Pd)	0.8*1		1.0*2 (KV) / 0.8*3 (GUW)	1.0*2	W	
Input Voltage Range (VIN)	-0.5 ~ VDD+0.5				V	
Operational Temperature Range (Topr)	-40 ~ +85		-30 ~ +75	-40 ~ +85	℃	
Storage Temperature Range (Tstg)	-55 ~ +125				℃	
Output Current (Iout1)	5			-	mA	SEG output
Output Current (Iout2)	5			-	mA	COM output
Output Current (Iout3)	10			-	mA	GPO output
Output Current (Iout4)	50			-	mA	LED output

*1 When use more than Ta=25°C,, subtract 8.0mW per degree. (using ROHM standard board)
(board size: 74.2mm×74.2mm×1.6mm material: FR4 board copper foil: land pattern only)
*2 When use more than Ta=25°C,, subtract 10mW per degree. (using ROHM standard board)
(board size: 70mm×70mm×1.6mm material: FR4 board copper foil: land pattern only)
*3 When use more than Ta=25°C,, subtract 8.0mW per degree. (using ROHM standard board)
(board size: 114.3mm×76.2mm×1.6mm)

●Recommended operating conditions

(BU9798KV/GUW : Ta=-30 ~ 75°C, VSS = 0V)
(BU97930MUV, BU97931FV, BU97500KV : Ta=-40 ~ 85°C,VSS = 0V)

Parameter	BU97930MUV			BU97931FV			BU9798KV/GUW			BU97500KV*4			Unit	Remarks
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
Power Supply Voltage 1 (VDD)	1.8	-	3.6	1.8	-	3.6	1.8	-	3.6	2.7	-	5.5	V	Power supply
Power Supply Voltage 2 (VLCD)	2.7	-	5.5	2.7	-	5.5	3.3	-	5.5	4.5	-	5.5	V	Power supply for LCD
LED Supply Voltage (VLED)	-	-	-	-	-	-	1.0	-	VLCD	-	-	-	V	Power supply for LED
Output Current (Iout4)	-	-	20	-	-	20	-	-	20	-	-	-	mA	Per LED port 1ch
Output Current (Iout4)	-	-	-	-	-	-	-	-	60	-	-	-	mA	Total LED port current

*4 The power supply condition shall be met VLCD ≥ VDD.
○ This product is not designed against radioactive ray

●Electrical Characteristics

<BU97930MUV>

DC characteristics (Ta=-40 ~ 85 °C, VDD=1.8V ~ 3.6V, VLCD=2.7V ~ 5.5V, VSS=0)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
“H” level input voltage	VIH	0.8VDD	-	VDD	V	SD, SCL, CSB, CLKIN, INHb
“L” level input voltage	VIL	VSS	-	0.2VDD	V	SD, SCL, CSB, CLKIN, INHb
Hysteresis width	VH	-	0.2	-	V	SCL, INHb, VDD=3.3V, Ta=25°C
“H” level input current	IIH1	-	-	5	μA	SD, SCL, CSB, CLKIN, INHb, VI=3.6V
“L” level input current	IIL1	-5	-	-	μA	SD, SCL, CSB, CLKIN, INHb, VI=0V
“H” level output voltage (*2)	VOH1	VLCD -0.4	-	-	V	Iload=-50μA, VLCD=5.0V SEG0 ~ SEG26
	VOH2	VLCD -0.4	-	-	V	Iload=-50μA, VLCD=5.0V, COM0 ~ COM3
	VOH3	VLCD -0.6	-	-	V	Iload=-1mA,VLCD=5.0V, SEG23 ~ SEG26(GPO mode)
“L” level output voltage (*2)	VOL1	-	-	0.4	V	Iload= 50μA, VLCD=5.0V, SEG0 ~ SEG26
	VOL2	-	-	0.4	V	Iload= 50μA, VLCD=5.0V, COM0 ~ COM3
	VOL3	-	-	0.5	V	Iload=1mA, VLCD=5.0V, SEG23 ~ SEG26(GPO mode)
	VOL4	-	0.34	0.5	V	Iload=20mA, VLCD=5.0V, LED
Current consumption (*1)	IstVDD	-	3	10	μA	Input terminal ALL’L’, Display off, Oscillation off
	IstVLCD	-	0.5	5	μA	Input terminal ALL’L’, Display off, Oscillation off
	IVDD1	-	8	15	μA	VDD=3.3V, Ta=25°C, 1/3bias, fFR=64Hz, PWM generate off, All output pin open
	IVDD2	-	30	45	μA	VDD=3.3V, Ta=25°C, 1/3bias, fFR=64Hz, PWM Frequency=500Hz setting, All output pin open
	IVLCD1	-	10	15	μA	VDD=5.0V, Ta=25°C, 1/3bias, fFR=64Hz, LED generate off, All output pin open
	IVLCD2	-	30	48	μA	VDD=5.0V, Ta=25°C, 1/3bias, fFR=64Hz, PWM Frequency=500Hz setting, All output pin open

*1 Power save mode 1 and frame inversion setting

*2 Iload: In case, load current from only one port

Oscillation Frequency Characteristics (Ta=-40 ~ 85 °C, VDD=1.8V ~ 3.6V, VLCD=2.7V ~ 5.5V, VSS=0)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	MIN	MIN		
Frame frequency 1	fFR1	57.6	64	70.4	Hz	VDD=3.3V, Ta=25°C, fFR=64Hz setting
Frame frequency 2	fFR2	51.2	64	73.0	Hz	VDD=2.5 ~ 3.6V FR=64Hz setting
Frame frequency 3	fFR3	45.0	-	64	Hz	VDD=1.8 ~ 2.5V fFR=64Hz setting

MPU interface Characteristics (Ta=-40 ~ 85 °C, VDD=1.8V ~ 3.6V, VLCD=2.7V ~ 5.5V, VSS=0)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
Input rise time	tr	-	-	50	ns	
Input fall time	tf	-	-	50	ns	
SCL cycle time	tSCYC	250	-	-	ns	
“H” SCL pulse width	tSHW	50	-	-	ns	
“L” SCL pulse width	tSLW	50	-	-	ns	
SD setup time	tSDS	50	-	-	ns	
SD hold time	tSDH	50	-	-	ns	
CSB setup time	tCSS	50	-	-	ns	
CSB hold time	tCSH	50	-	-	ns	
“H” CSB pulse width	tCHW	50	-	-	ns	

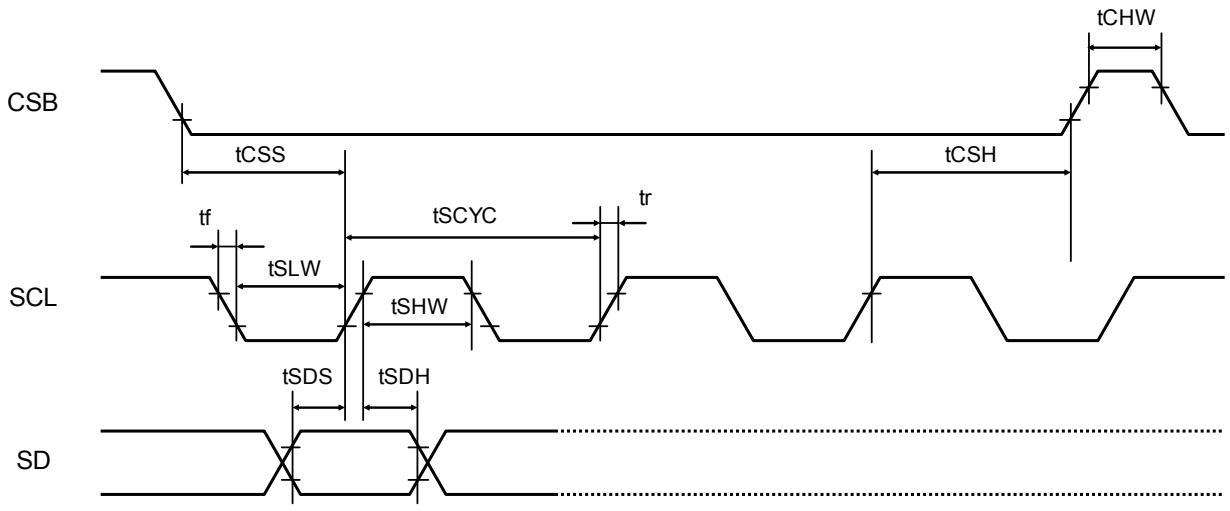


Fig.1 Serial Interface Timing

<BU97931FV>

DC characteristics (Ta=-40 ~ 85 °C, VDD=1.8V ~ 3.6V, VLCD=3.3V ~ 5.5V, VSS=0)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
"H" level input voltage	VIH	0.8VDD	-	VDD	V	SD, SCL, CSB, CLKIN
"L" level input voltage	VIL	VSS	-	0.2VDD	V	SD, SCL, CSB, CLKIN
Hysteresis width	VH	-	0.2	-	V	SCL, VDD=3.3V, Ta=25°C
"H" level input current	IIH1	-	-	5	μA	SD, SCL, CSB, CLKIN, VI=3.6V
"L" level input current	IIL1	-5	-	-	μA	SD, SCL, CSB, CLKIN, VI=0V
"H" level output voltage(*2)	VOH1	VLCD -0.4	-	-	V	Iload=-50μA, VLCD=5.0V SEG0 ~ SEG27
	VOH2	VLCD -0.4	-	-	V	Iload=-50μA, VLCD=5.0V, COM0 ~ COM3
	VOH3	VLCD -0.6	-	-	V	Iload=-1mA,VLCD=5.0V, SEG23 ~ SEG27(GPO mode)
"L" level output voltage(*2)	VOL1	-	-	0.4	V	Iload= 50μA, VLCD=5.0V, SEG0 ~ SEG27
	VOL2	-	-	0.4	V	Iload= 50μA, VLCD=5.0V, COM0 ~ COM3
	VOL3	-	-	0.5	V	Iload=1mA, VLCD=5.0V, SEG23 ~ SEG27(GPO mode)
	VOL4	-	0.34	0.5	V	Iload=20mA, VLCD=5.0V, LED
Current consumption (*1)	IstVDD	-	3	10	μA	Input terminal ALL'L', Display off, Oscillation off
	IstVLCD	-	0.5	5	μA	Input terminal ALL'L', Display off, Oscillation off
	IVDD1	-	8	15	μA	VDD=3.3V, Ta=25°C, 1/3bias, fFR=64Hz, PWM generate off, All output pin open
	IVDD2	-	30	45	μA	VDD=3.3V, Ta=25°C, 1/3bias, fFR=64Hz, PWM Frequency=500Hz setting, All output pin open
	IVLCD1	-	10	15	μA	VLCD=5.0V, Ta=25°C, 1/3bias, fFR=64Hz, LED generate off, All output pin open
	IVLCD2	-	30	48	μA	VLCD=5.0V, Ta=25°C, 1/3bias, fFR=64Hz, PWM Frequency=500Hz setting, All output pin open

*1 Power save mode 1 and frame inversion setting

*2 Iload: In case, load current from only one port

Oscillation Frequency Characteristics (Ta=-40 ~ 85°C, VDD=1.8V ~ 3.6V, VLCD=2.7V ~ 5.5V, VSS=0)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	MIN	MIN		
Frame frequency 1	fFR1	57.6	64	70.4	Hz	VDD=3.3V, Ta=25°C, fFR=64Hz setting
Frame frequency 2	fFR2	51.2	64	73.0	Hz	VDD=2.5 ~ 3.6V fFR=64Hz setting
Frame frequency 3	fFR3	45.0	-	64	Hz	VDD=1.8 ~ 2.5V fFR=64Hz setting

MPU interface Characteristics (Ta=-40 ~ 85°C, VDD=1.8V ~ 3.6V, VLCD=2.7V ~ 5.5V, VSS=0)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
Input rise time	tr	-	-	50	ns	
Input fall time	tf	-	-	50	ns	
SCL cycle time	tSCYC	250	-	-	ns	
“H” SCL pulse width	tSHW	50	-	-	ns	
“L” SCL pulse width	tSLW	50	-	-	ns	
SD setup time	tSDS	50	-	-	ns	
SD hold time	tSDH	50	-	-	ns	
CSB setup time	tCSS	50	-	-	ns	
CSB hold time	tCSH	50	-	-	ns	
“H” CSB pulse width	tCHW	50	-	-	ns	

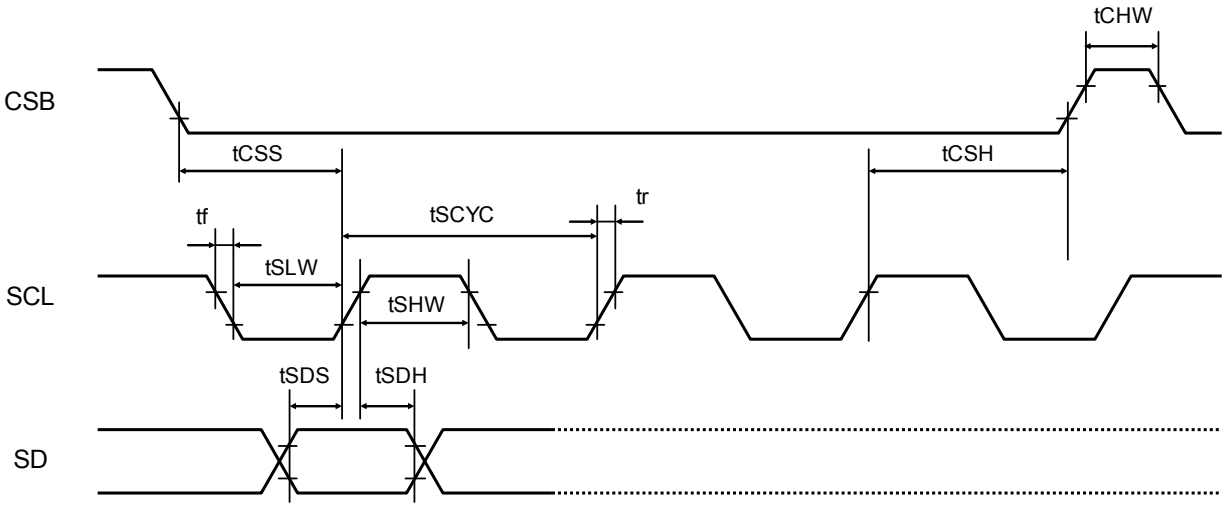


Fig.2 Serial Interface Timing

<BU9798KV/GUW>

DC characteristics (Ta=-30 ~ 75°C, VDD=1.8V ~ 3.6V, VLCD=3.3V ~ 5.5V, VSS=0)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
"H" level input voltage	VIH	0.8VDD	-	VDD	V	SD, SCL, CSB, TEST1,CLKIN, INHb
"L" level input voltage	VIL	VSS	-	0.2VDD	V	SD, SCL, CSB, TEST1,CLKIN, INHb
Hysteresis width	VH	-	0.2	-	V	SCL, INHb, VDD=3.3V, Ta=25°C
"H" level input current	IIH1	-	-	5	µA	SD, SCL, CSB, CLKIN, INHb, VI=3.6V
"L" level input current	IIL1	-5	-	-	µA	SD, SCL, CSB, CLKIN, INHb, TEST1 VI=0V
"H" level output voltage(*1, *3)	VOH1	VLCD -0.4	-	-	V	Iload=-50µA, VLCD=5.0V SEG0 ~ SEG48, Unused integrated regulator
	VOH2	VLCD -0.4	-	-	V	Iload=-50µA, VLCD=5.0V, COM0 ~ COM3, Unused integrated regulator
	VOH3	VLCD -0.6	-	-	V	Iload=-1mA,VLCD=5.0V, SEG15 ~ SEG45(GPO mode) Unused integrated regulator
	VOH4	VDD -0.6	-	-	V	Iload=-1mA, VDD=3.0V, PWMOUT
"L" level output voltage (*3)	VOL1	-	-	0.4	V	Iload=50µA, VLCD=5.0V, SEG0 ~ SEG48
	VOL2	-	-	0.4	V	Iload=50µA, VLCD=5.0V, COM0 ~ COM3
	VOL3	-	-	0.5	V	Iload=1mA, VLCD=5.0V, SEG15 ~ SEG45(GPO mode), PWMOUT
	VOL4	-	0.11	0.5	V	Iload=20mA, VLCD=5.0V, SEG46 ~ 48 (LED drive mode)
Current consumption (*2)	IstVDD	-	3	10	µA	Input terminal ALL'L', Display off, Oscillation off
	IstVLCD	-	0.5	5	µA	Input terminal ALL'L', Display off, Oscillation off
	IVDD1	-	8	15	µA	VDD=3.3V, Ta=25°C, 1/3bias, fFR=64Hz, PWM generate off, All output pin open
	IVDD2	-	90	130	µA	VDD=3.3V, Ta=25°C, 1/3bias, fFR=64Hz, PWM Frequency=500Hz setting, All output pin open
	IVLCD1	-	10	15	µA	VLCD=5.0V, Ta=25°C, 1/3bias, fFR=64Hz Unused Integrated regulator, LED generate off, All output pin open
	IVLCD2	-	25	40	µA	VLCD=5.0V, Ta=25°C, 1/3bias, fFR=64Hz Used Integrated regulator, LED generate off, All output pin open
	IVLCD3	-	30	48	µA	VLCD=5.0V, Ta=25°C,1/3bias, fFR=64Hz, Used Integrated regulator, PWM Frequency=500Hz setting, All output pin open

*1 Integrated regulator using case, please add load regulation value to output voltage listed above.
*2 Power save mode 1 and frame inversion setting
*3 Iload: In case, load current from only one port

Integrated Regulator Characteristics (Ta=-30 ~ 75°C, VDD=1.8V ~ 3.6V, VLCD=3.3V ~ 5.5V, VSS=0)
(BU9798KV)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
Output voltage 1	Vreg1	4.35	4.5	4.65	V	4.5V setting (VLCD=5.5V, Ta=-30 ~ 75°C)
Output voltage 2	Vreg2	4.42	4.5	4.58	V	4.5V setting (VLCD=5.5V, Ta=25°C)
Load regulation (**)	delta Vreg	-	-	0.3	V	Iout = -300μA

(BU9798GUW)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
Output voltage 1	Vreg1	4.25	4.5	4.70	V	4.5V setting (VLCD=5.5V, Ta=-30 ~ 75°C)
Output voltage 2	Vreg2	4.38	4.5	4.62	V	4.5V setting (VLCD=5.5V, Ta=25°C)
Load regulation (**)	delta Vreg	-	-	0.3	V	Iout = -300μA

* In case integrated regulator using, please satisfy condition that Vreg output lower than VLCD – 0.5V.
(**) Load regulation: Vreg block load regulation only. Do not include other block ability.

Oscillation Frequency Characteristics (Ta=-30 ~ 75°C, VDD=1.8V ~ 3.6V, VLCD=3.3V ~ 5.5V, VSS=0)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
Frame frequency 1	fFR1	57.6	64	70.4	Hz	VDD=3.3V, Ta=25°C, fFR=64Hz setting
Frame frequency 2	fFR2	51.2	64	73.0	Hz	VDD=2.5 ~ 3.6V fFR=64Hz setting
Frame frequency 3	fFR3	45.0	-	64	Hz	VDD=1.8 ~ 2.5V fFR=64Hz setting
CLKIN Input frequency	fCLK	-	2	4	MHz	

MPU interface Characteristics (Ta=-30 ~ 75°C, VDD=1.8V ~ 3.6V, VLCD=3.3V ~ 5.5V, VSS=0)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
Input rise time	tr	-	-	50	ns	
Input fall time	tf	-	-	50	ns	
SCL cycle time	tSCYC	250	-	-	ns	
“H” SCL pulse width	tSHW	50	-	-	ns	
“L” SCL pulse width	tSLW	50	-	-	ns	
SD setup time	tSDS	50	-	-	ns	
SD hold time	tSDH	50	-	-	ns	
CSB setup time	tCSS	50	-	-	ns	
CSB hold time	tCSH	50	-	-	ns	
“H” CSB pulse width	tCHW	50	-	-	ns	

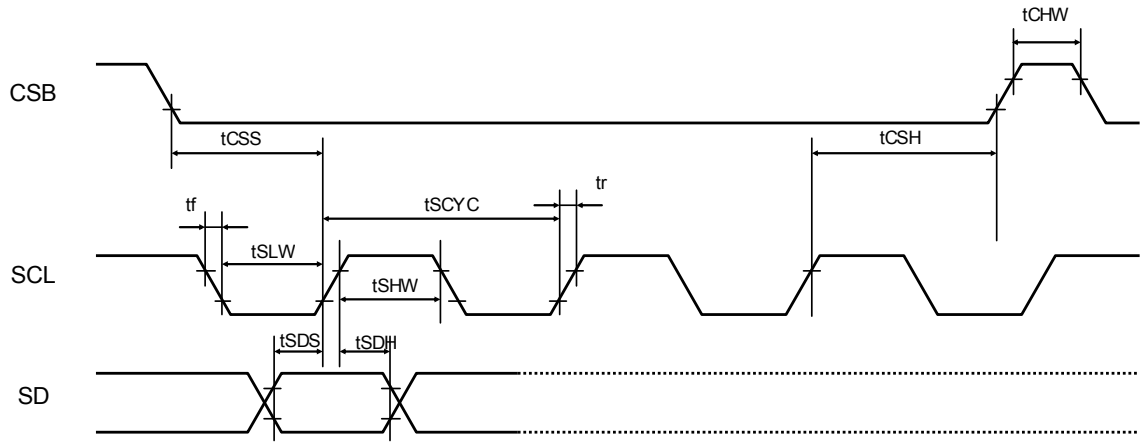


Fig.3 Serial Interface Timing

<BU97500KV>

DC Characteristics (Unless otherwise indicated, VDD=2.7 ~ 5.5V, VLCD=4.5 ~ 5.5V, VSS=0V, Ta=-40 ~ 85°C)

Parameters	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
“H” Input Voltage	VIH	0.7VDD	-	VDD	V	SD, SCL, CSB, RESB, OSC
“L” Input Voltage	VIL	VSS	-	0.3VDD	V	SD, SCL, CSB, RESB, OSC
“H” Input Current	IIH			5.0	μA	SD,SCL,CSB,RESB, OSC VI=5.5V
“L” Input Current	IIL	-5.0			μA	SD,SCL,CSB,RESB, OSC VI=0V
“H” Level Output Voltage	VOH1	VLCD -1.0			V	P1 ~ P4, Io=1mA
	VOH2	VLCD -1.0				S1 ~ S52, Io=20μA
	VOH3	VLCD -1.0				COM1 ~ COM4, Io=100μA
“L” Level Output Voltage	VOL1	-	-	1.0	V	P1 ~ P4, Io=1mA
	VOL2	-	-	1.0		S1 ~ S52, Io=20μA
	VOL3	-	-	1.0		COM1 ~ COM4, Io=100μA
LCD Bias Voltage	VMID1	1/2VLCD -1.0	-	1/2VLCD +1.0	V	S1 ~ S52 1/2 Bias, Io=±100μA
	VMID2	1/2VLCD -1.0	-	1/2VLCD +1.0		COM1 ~ COM4 1/2 Bias, Io=±100μA
	VMID3	2/3VLCD -1.0	-	2/3VLCD +1.0		S1 ~ S52 1/3 Bias, Io=±20μA
	VMID4	1/3VLCD -1.0	-	1/3VLCD +1.0		S1 ~ S52 1/3 Bias, Io=±20μA
	VMID5	2/3VLCD -1.0	-	2/3VLCD +1.0		COM1 ~ COM4 1/3Bias, Io=±100μA
	VMID6	1/3VLCD -1.0	-	1/3VLCD +1.0		COM1 ~ COM4 1/3 Bias, Io=±100μA
Current consumption	IstVDD	-	1	5	μA	Input Pin ALL ”L” Display off, Disable oscillator
	IstVLCD	-	1	5		Input Pin ALL ”L” Display off, Disable oscillator
	ILCD1	-	2	10		VDD=VLCD=5.0V Output unloaded fFR=80Hz
	ILCD2	-	40	95		VDD=VLCD=5.0V Output unloaded 1/2 Bias, fFR=80Hz
	ILCD3	-	65	140		VDD=VLCD=5.0V Output unloaded 1/3 Bias, fFR=80Hz

Oscillation Characteristics (Ta=-40 ~ 85°C, VDD=2.7 ~ 5.5V, VLCD=4.5 ~ 5.5V , VSS=0V)

Parameters	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
Frame Frequency	fCLK	56	80	104	Hz	fFR = 80Hz setting, 1/4 Duty setting

MPU interface Characteristics (Ta=-40 ~ 85°C, VDD=2.7V ~ 5.5V, VLCD=4.5 ~ 5.5V , VSS=0V)

Parameters	Symbol	Limits			Unit	Conditions
		MIN.	TYP.	MAX.		
Input Rise Time	tr	-	-	80	ns	
Input Fall Time	tf	-	-	80	ns	
SCL Cycle Time	tSCYC	400	-	-	ns	
“H” SCL Pulse Width	tSHW	100	-	-	ns	
“L” SCL Pulse Width	tSLW	100	-	-	ns	
SD Setup Time	tSDS	20	-	-	ns	
SD Hold Time	tSDH	20	-	-	ns	
CSB Setup Time	tCSS	50	-	-	ns	
CSB Hold Time	tCSH	50	-	-	ns	
“H” CSB Pulse Time	tCHW	50	-	-	ns	

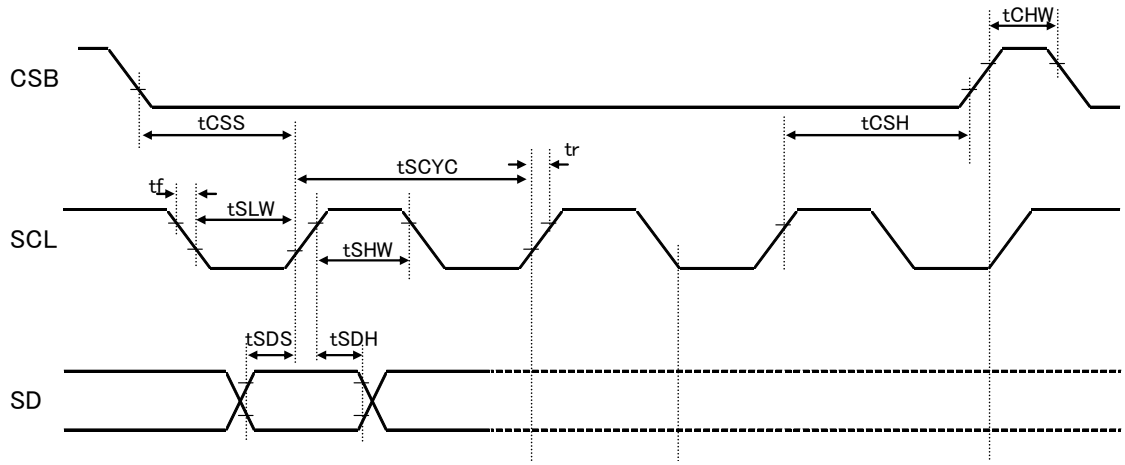


Fig.4 Serial interface Timing

●Block diagrams / Pin arrangement / Terminal description

<BU97930MUV>

●Block diagrams

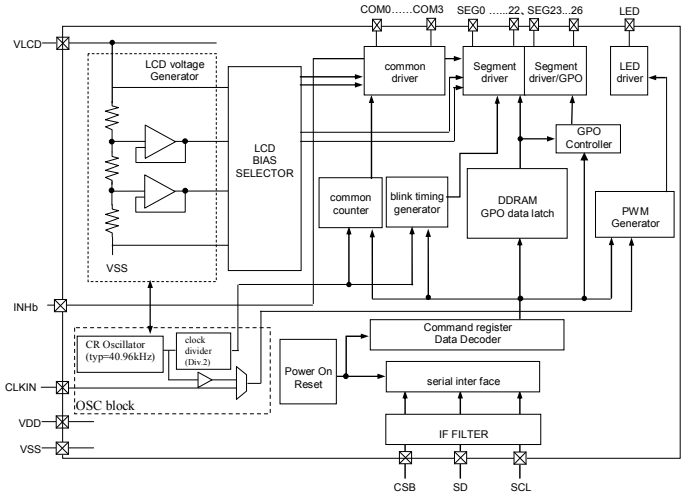


Fig.5 Block Diagram (BU97930MUV)

●Pin arrangement

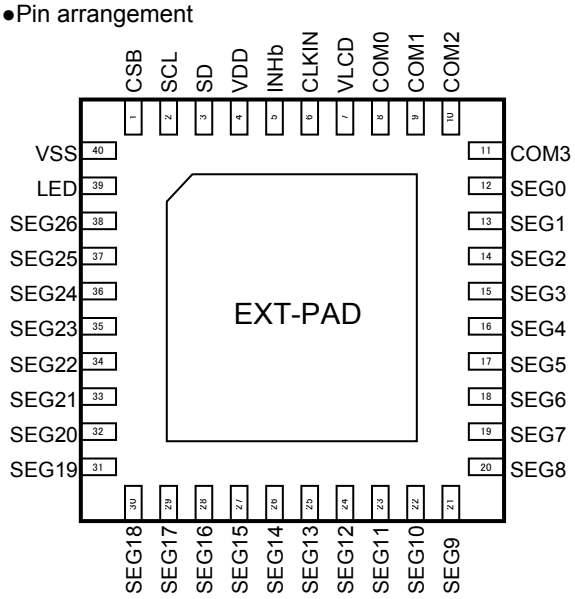


Fig.6 Pin Arrangement (BU97930MUV)

●Terminal description

Terminal	Terminal number	I/O	unused case	Function
CSB	1	I	VDD	Chip select: "L" active
SCL	2	I	VSS	Serial data transfer clock
SD	3	I	VSS	Input serial data
VDD	4	-	-	Power supply for LOGIC
CLKIN	6	I	OPEN / VSS	External clock input terminal (for display/PWM using selectable) Support Hi-Z input mode at internal clock mode
VSS	40	-	-	GND
VLCD	7	-	-	Power supply for LCD
INHb	5	I	VDD	Display turning on/off select terminal H: turning on display, L: turning off display INHb = "L": All SEG/COM terminal : output VSS level GPO terminal : output VSS level LED drive terminal : output Hi-Z
COM0 ~ 3	8-11	O	OPEN	COMMON output for LCD
SEG0 ~ 22	12-34	O	OPEN	SEGMENT output for LCD
SEG23 ~ 26	35-38	O	OPEN	SEGMENT output for LCD/GPO
LED	39	O	OPEN	LED driver output
EXT-PAD	-	-	VSS	substrate

<BU97931FV>

●Block diagrams

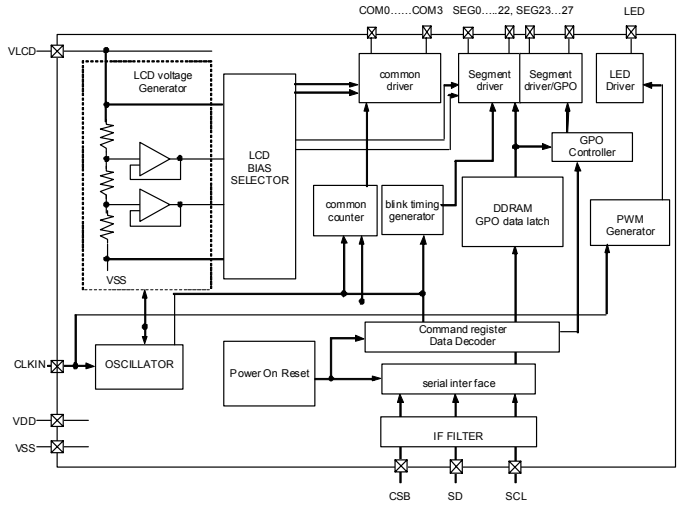


Fig.7 Block Diagram (BU97931FV)

●Pin arrangement

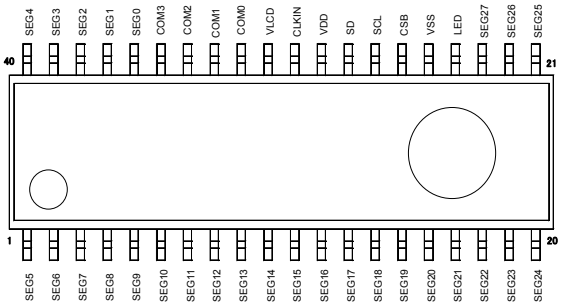


Fig.8 Pin Arrangement (BU97931FV)

●Terminal description

Terminal	Terminal number	I/O	unused case	Function
CSB	26	I	VDD	Chip select: "L" active
SCL	27	I	VSS	Serial data transfer clock
SD	28	I	VSS	Input serial data
VDD	29	-	-	Power supply for LOGIC
CLKIN	30	I	OPEN / VSS	External clock input terminal (for display/PWM using selectable) Support Hi-Z input mode at internal clock mode
VSS	25	-	-	GND
VLCD	31	-	-	Power supply for LCD
COM0 ~ 3	32-35	O	OPEN	COMMON output for LCD
SEG0 ~ 22	36-40 1-18	O	OPEN	SEGMENT output for LCD
SEG23 ~ 27	19-23	O	OPEN	SEGMENT output for LCD/GPO
LED	24	O	OPEN	LED driver output

<BU9798KV>

●Block diagrams

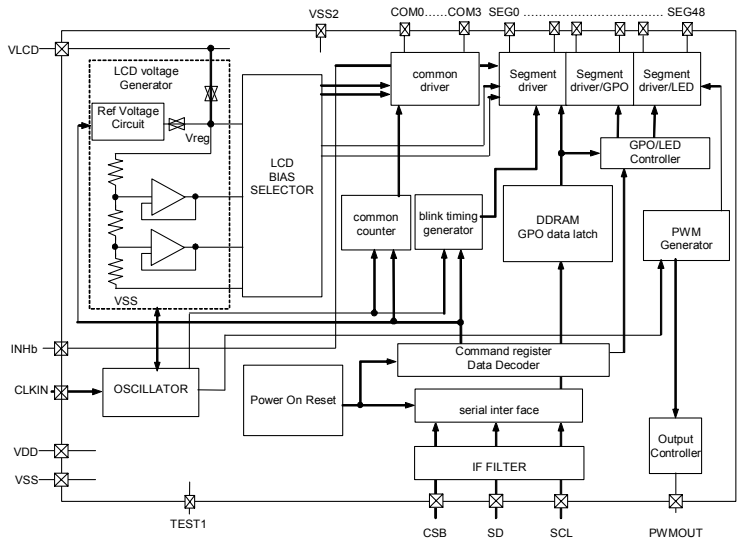


Fig.9 Block Diagram (BU9798KV)

●Pin arrangement

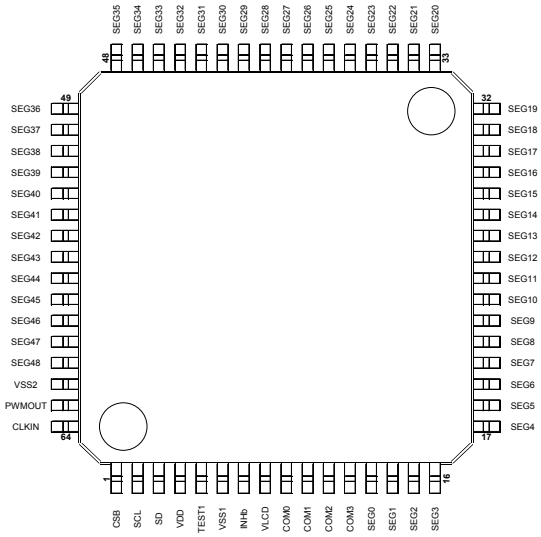


Fig.10 Pin Arrangement (BU9798KV)

●Terminal description

Terminal	Terminal number	I/O	unused case	Function
CSB	1	I	VDD	Chip select: "L" active
SCL	2	I	VSS	Serial data transfer clock
SD	3	I	VSS	Input serial data
VDD	4	-	-	Power supply for LOGIC
CLKIN	64	I	OPEN / VSS	External clock input terminal (for display/PWM using selectable) Support Hi-Z input mode at internal clock mode
TEST1	5	I	-	TEST terminal (Please connect VSS terminal)
VSS1	6	-	-	GND
VLCD	8	-	-	Power supply for LCD
INHb	7	I	VDD	Display turning on/off select terminal H: turning on display, L: turning off display INHb = "L": All SEG/COM terminal : output VSS level GPO terminal : output VSS level LED drive terminal : output Hi-Z
PWMOUT	63	O	OPEN	PWM output for LED2 group
COM0 ~ 3	9-12	O	OPEN	COMMON output for LCD
SEG0 ~ 14	13-27	O	OPEN	SEGMENT output for LCD
SEG15 ~ 45	28-58	O	OPEN	SEGMENT output for LCD/GPO
SEG46 ~ 48	59-61	O	OPEN	SEGMENT output for LCD/LED driver
VSS2	62	-	GND	GND (for SEG46-48 / LED driver)

<BU9798GUW>

●Block diagrams

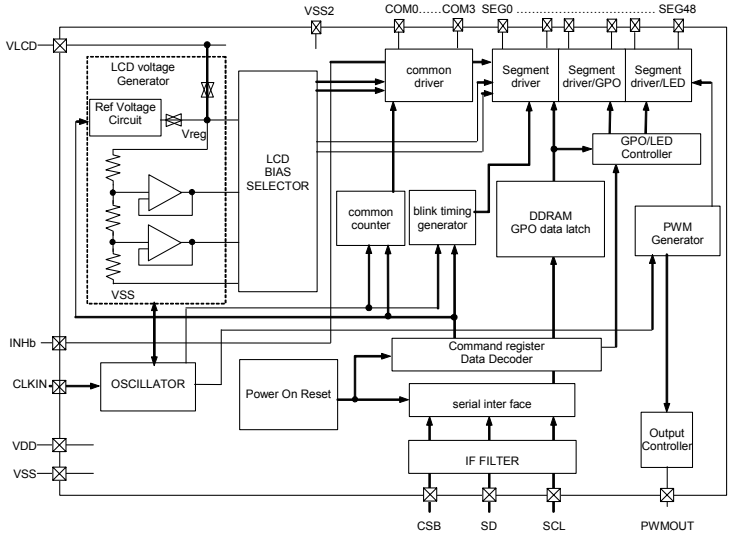


Fig.11 Block Diagram (BU9798GUW)

●Pin arrangement

	1	2	3	4	5	6	7	8
H	SEG 4	SEG 5	SEG 9	SEG 11	SEG 14	SEG 16	SEG 18	SEG 20
G	SEG 2	SEG 3	SEG 7	SEG 8	SEG 12	SEG 17	SE G19	SEG 21
F	SEG 0	SEG 1	SEG 6	SEG 10	SEG 13	SEG 22	SEG 23	SEG 25
E	COM 2	COM 0	COM 1	COM 3	SEG 15	SEG 26	SEG 24	SEG 27
D	VLCD	VDD	INHB	SEG 47	SEG 31	SEG 29	SEG 28	SEG 30
C	VSS1	SDA	SCL	SEG 45	SEG 42	SEG 38	SEG 33	SEG 32
B	(NC)	CLK IN	VSS2	SEG 44	SEG 40	SEG 39	SEG 35	SEG 34
A	CSB	PWM OUT	SEG 48	SEG 46	SEG 43	SEG 41	SEG 37	SEG 36

Fig.12 Pin Arrangement (BU9798GUW)

●Terminal description

Terminal	I/O	Unused case	Function
CSB	I	VDD	Chip select: "L" active
SCL	I	VSS	Serial data transfer clock
SD	I	VSS	Input serial data
VDD	-	-	Power supply for LOGIC
CLKIN	I	OPEN / VSS	External clock input terminal (for display/PWM using selectable) Support Hi-Z input mode at internal clock mode
VSS1	-	-	GND
VLCD	-	-	Power supply for LCD
INHb	I	VDD	Display turning on/off select terminal H: turning on display, L: turning off display INHb = "L": All SEG/COM terminal : output VSS level GPO terminal : output VSS level LED drive terminal : output Hi-Z
PWMOUT	O	OPEN	PWM output for LED2 group
COM0 ~ 3	O	OPEN	COMMON output for LCD
SEG0 ~ 14	O	OPEN	SEGMENT output for LCD
SEG15 ~ 45	O	OPEN	SEGMENT output for LCD/GPO
SEG46 ~ 48	O	OPEN	SEGMENT output for LCD/LED driver
VSS2	-	GND	GND (for SEG46-48 / LED driver)

<BU97500KV>

●Block diagrams

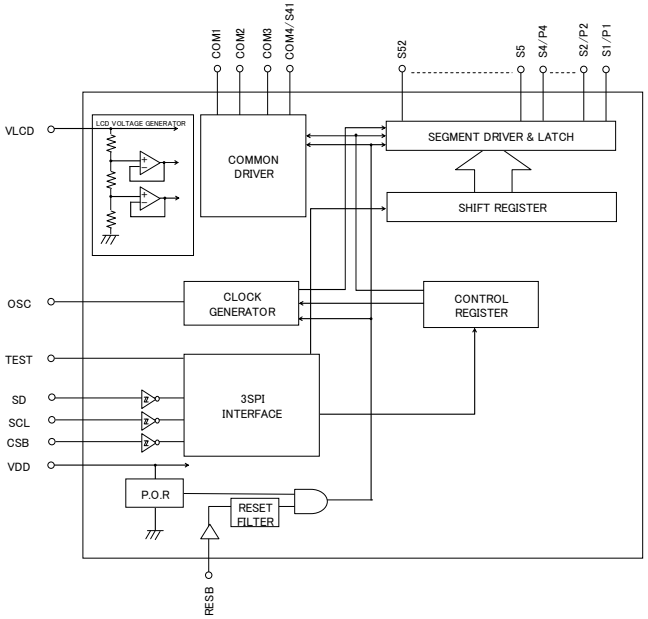


Fig.13 Block Diagram (BU97500KV)

●Pin arrangement

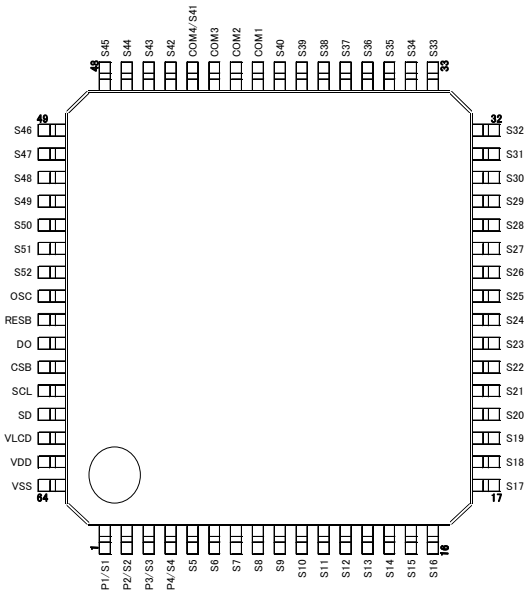


Fig.14 Pin Arrangement (BU97500KV)

●Terminal description

Terminal	Terminal No.	I/O	Unused case	Function
CSB	59	I	VDD	Chip select : “L”active
SCL	60	I	VSS	Serial data transfer clock
SD	61	I	VSS	Input Serial data
VDD	63	-	-	Power Supply for the logic
OSC	56	I/O	OPEN / VSS	External clock input terminal Supported Hi-Z input if the internal clock mode.
VSS	64	-	-	GND
VLCD	62	-	-	Power Supply for the LCD driver
COM1 ~ 3	41-43	O	OPEN	COMMON output for LCD driving
COM4/S41	44	O	OPEN	COMMON / SEGMENT output for LCD driving Assigned as SEGMENT output if 1/3Duty mode.
S1/P1 ~ S4/P4	1-4	O	OPEN	SEGMENT output for LCD driving / General Purpose output
S5 ~ S40 S42 ~ S52	5-40 45-55	O	OPEN	SEGMENT output for LCD driving
RESB	57	I	VDD	Reset Input: RESB=“L” : Display is disabled RESB=“H” : Display is controllable NOTE) 3-SPI is NOT available if RESET is “L”.
DO	58	O	OPEN	Output for manufacturing test:

●I/O equivalent circuit

<BUI97930MUV>

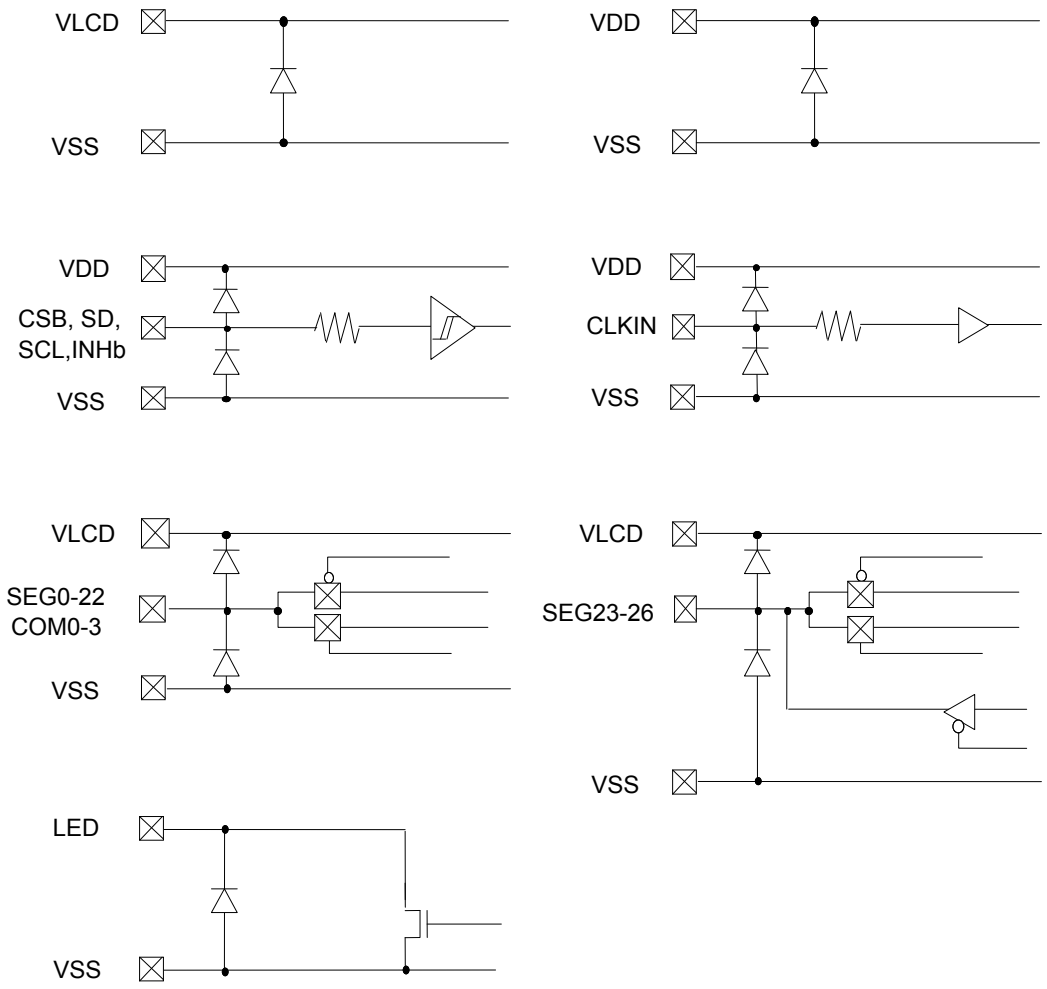


Fig.15 I/O equivalent circuit

<BU97931FV>

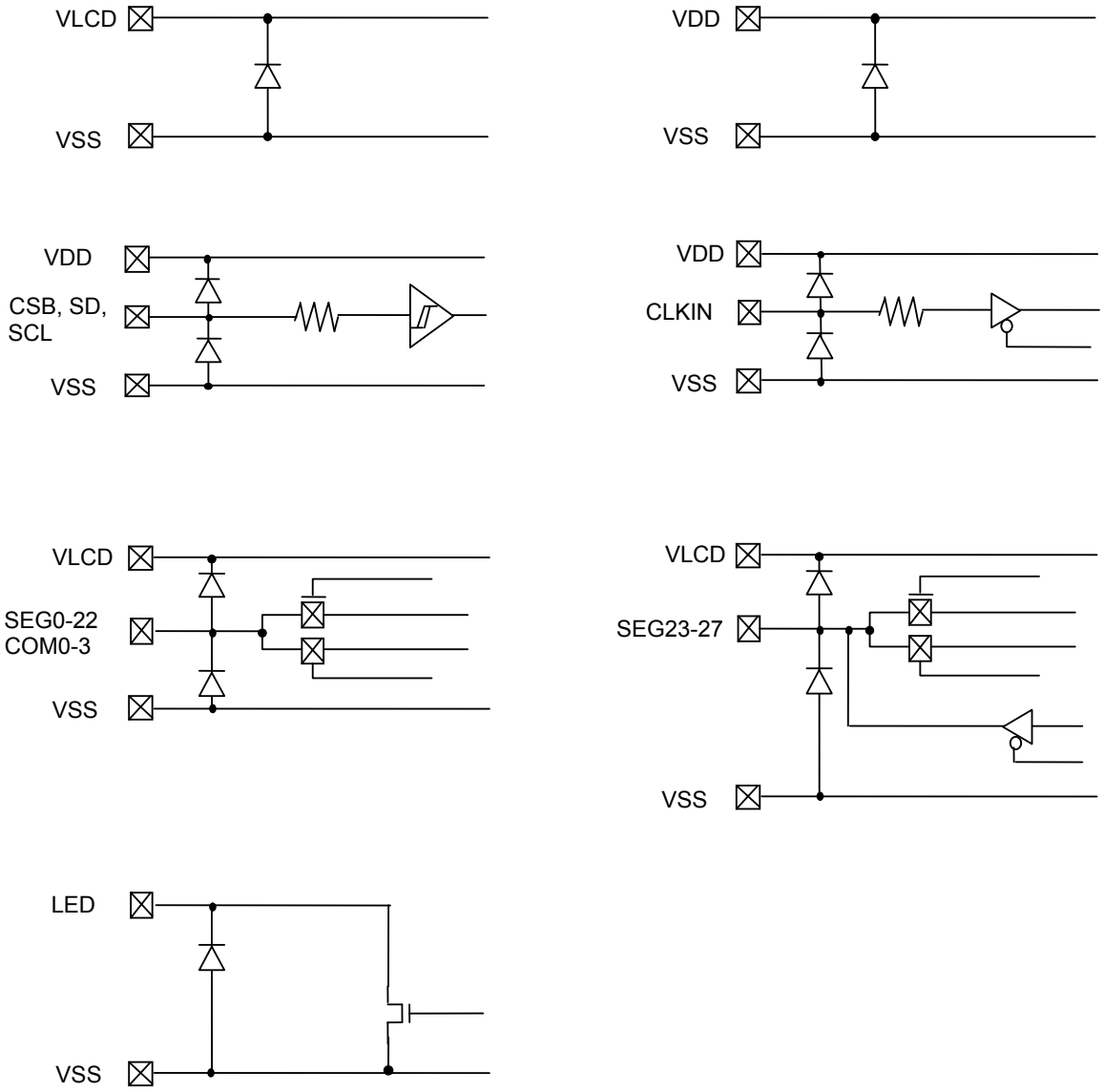


Fig.16 I/O equivalent circuit

<BU9798KV>

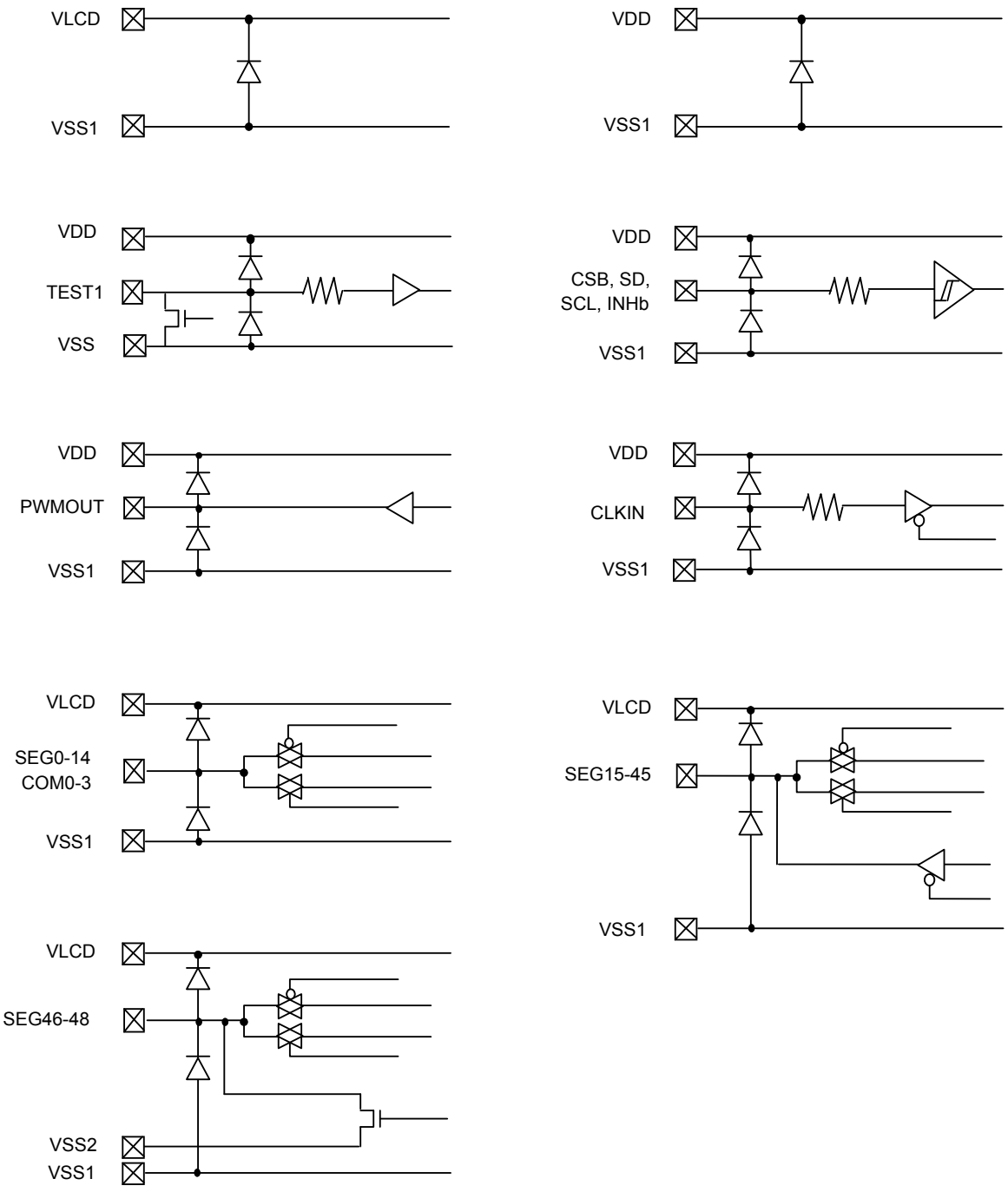


Fig.17 I/O equivalent circuit

<BU9798GUW>

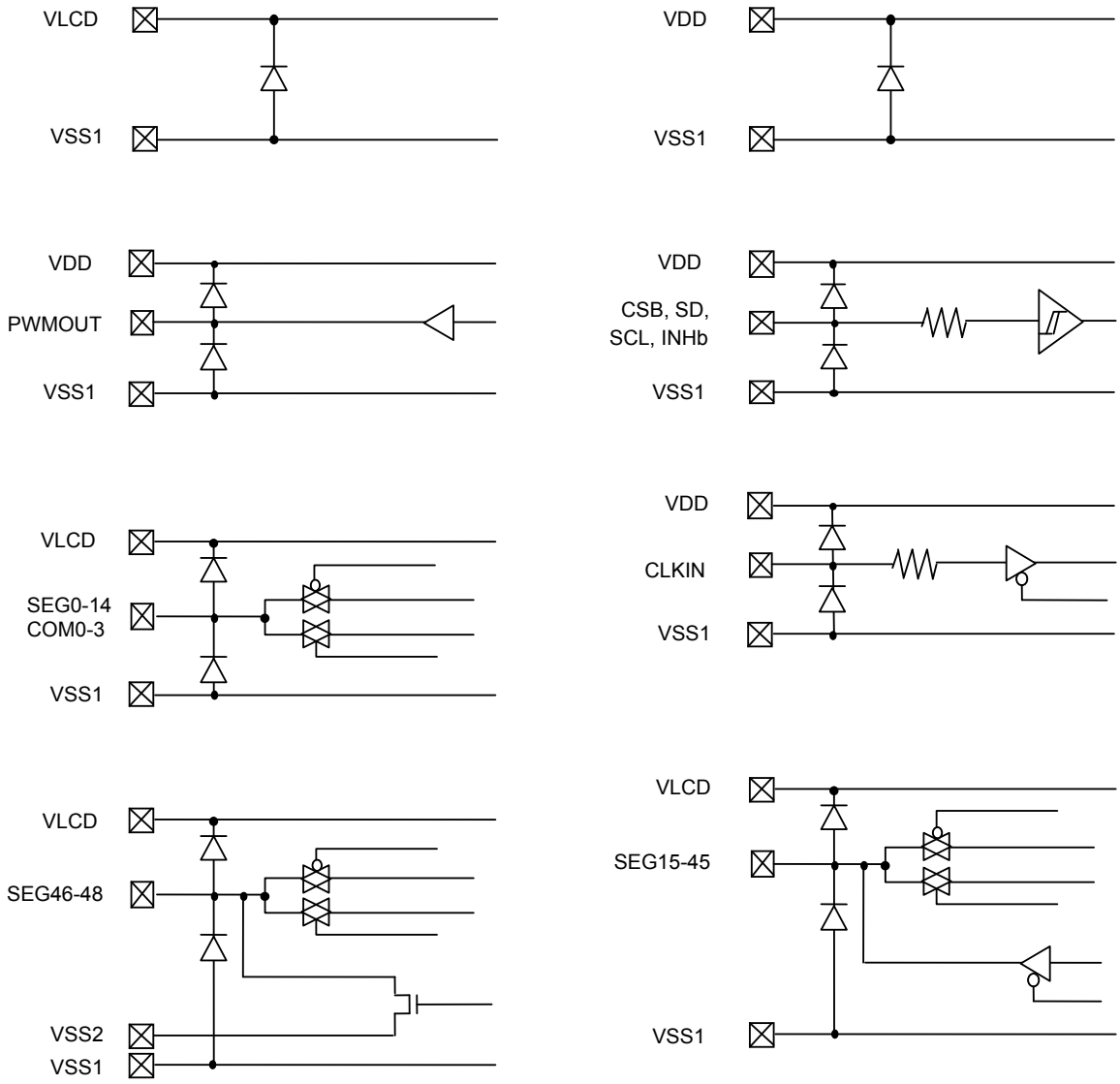


Fig.18 I/O equivalent circuit

<BU97500KV>

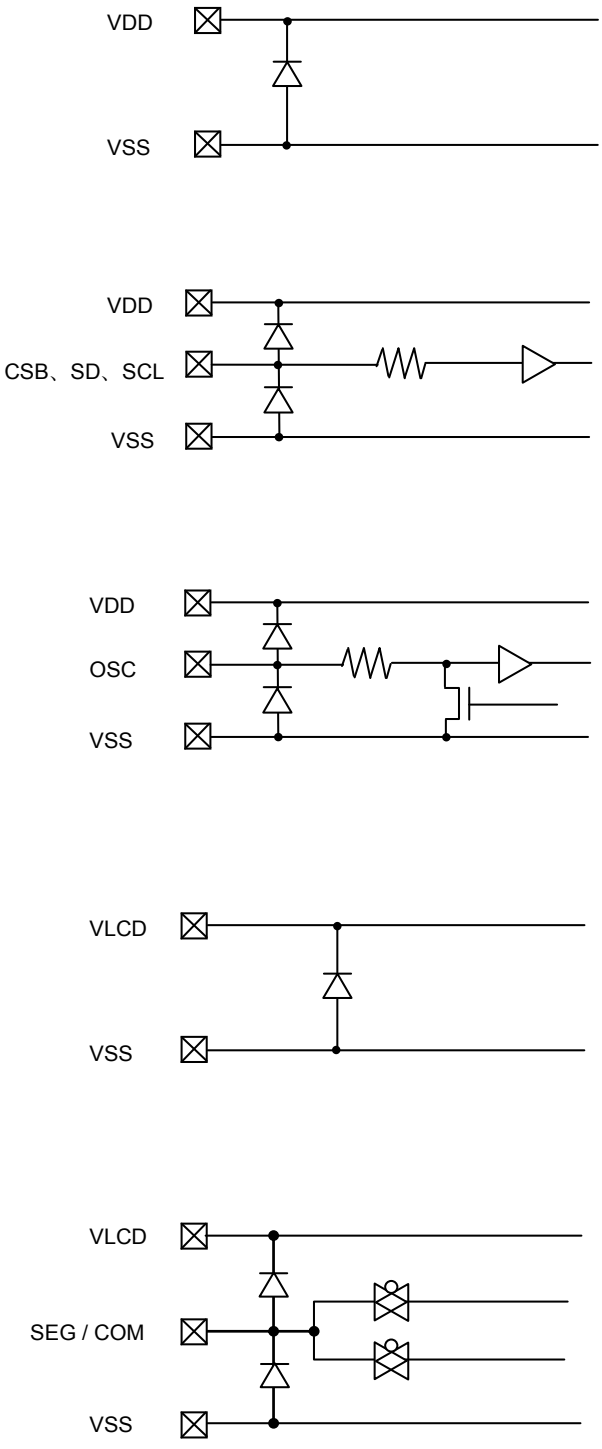


Fig.19 I/O equivalent circuit

●**Ordering part number**

B	U	9	7	9	3	0	M	U	V	-	E	2

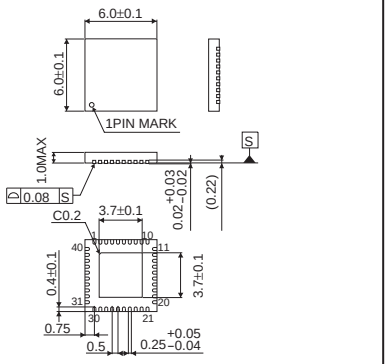
Part No.

Part No.
BU97930
BU97931
BU9798
BU97500

Package
MUV : VQFN040V6060
FV : SSOP-B40
KV : VQFP64
GUW : VBGA063W050

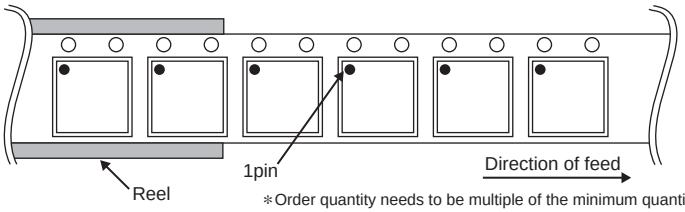
Packaging and forming specification
E2: Embossed tape and reel

VQFN040V6060



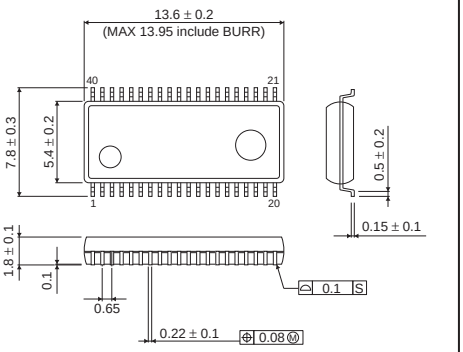
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



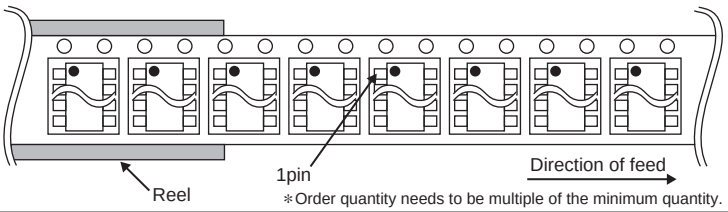
∗Order quantity needs to be multiple of the minimum quantity.

SSOP-B40



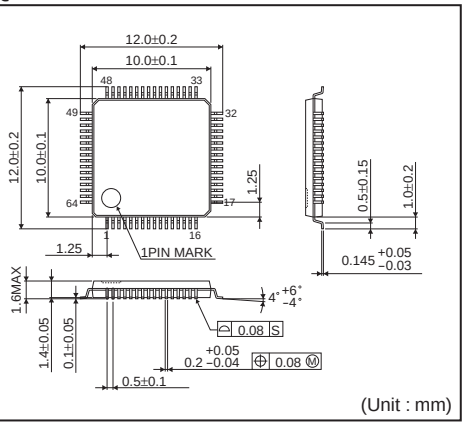
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



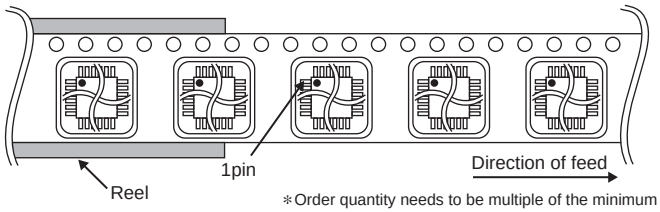
∗Order quantity needs to be multiple of the minimum quantity.

VQFP64



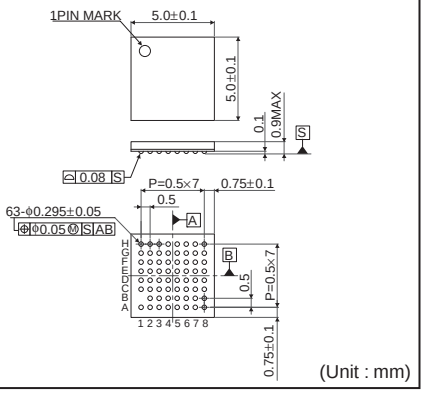
<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



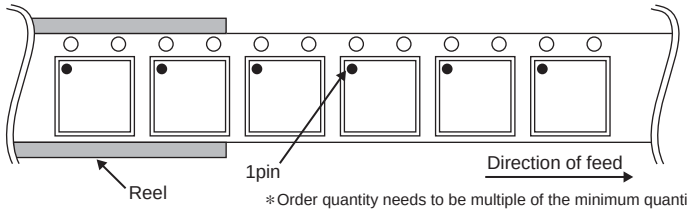
∗Order quantity needs to be multiple of the minimum quantity.

VBGA063W050



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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