

SN54LS638, SN54LS639, SN74LS638, SN74LS639 OCTAL BUS TRANSCEIVERS

SDLS188 – JANUARY 1981 – REVISED MARCH 1988

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- A Bus Outputs are Open-Collector, B Bus Outputs are 3-State

description

These octal bus transceivers are designed for asynchronous two-way communication between open-collector and 3-state buses. The devices transmit data from the A bus (open-collector) to the B bus (3-state) or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\bar{G}$) can be used to disable the device so the buses are isolated.

FUNCTION TABLE

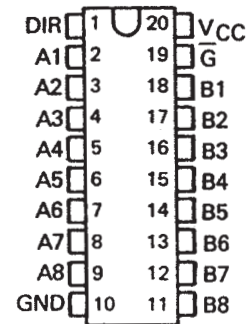
CONTROL INPUTS		OPERATION	
		'LS638	'LS639
$\bar{G}$	DIR	$\bar{B}$ data to A bus	B data to A bus
L	L	$\bar{A}$ data to B bus	A data to B bus
L	H	Isolation	Isolation
H	X	Isolation	Isolation

H = high level, L = low level, X = irrelevant

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'LS638	Open-Collector	3-State	Inverting
'LS639	Open-Collector	3-State	True

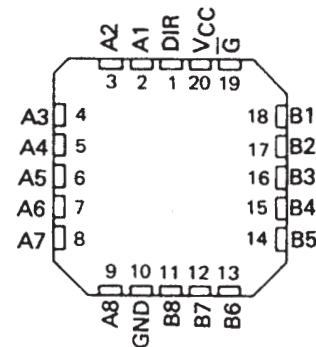
SN54LS638, SN54LS639 . . . J PACKAGE SN74LS638, SN74LS639 . . . DW OR N PACKAGE

(TOP VIEW)

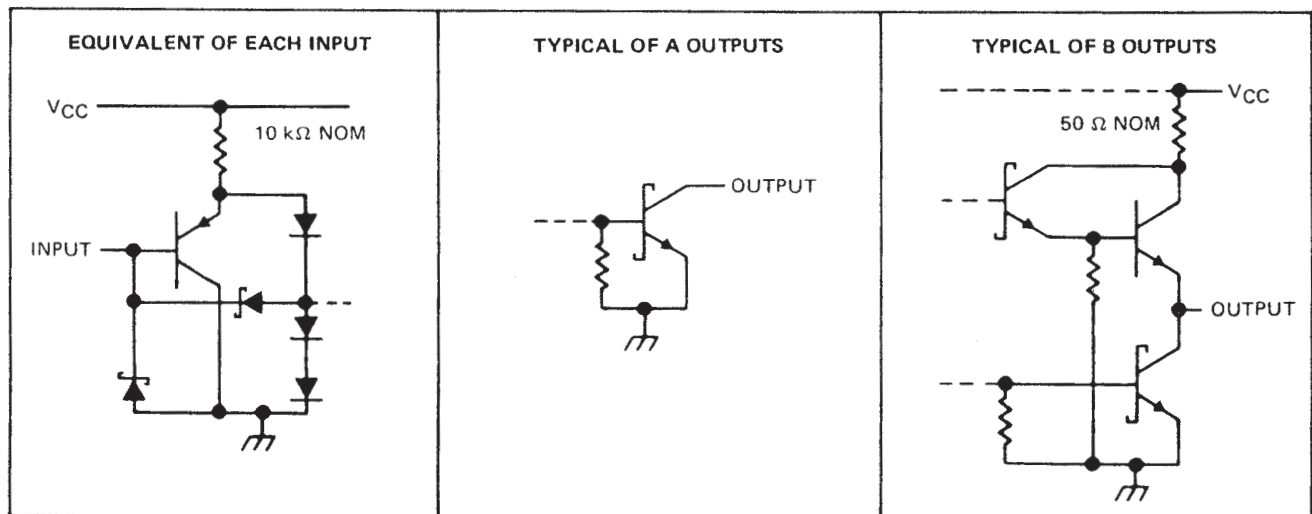


SN54LS638, SN54LS639 . . . FK PACKAGE

(TOP VIEW)



schematics of inputs and outputs



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

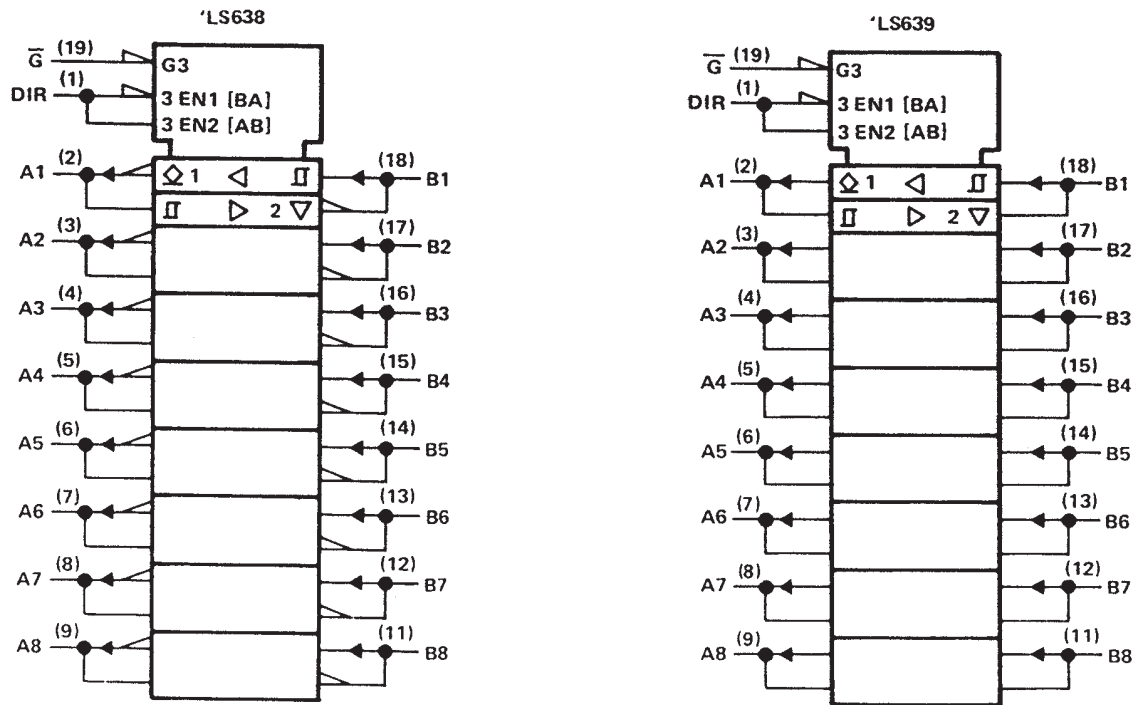
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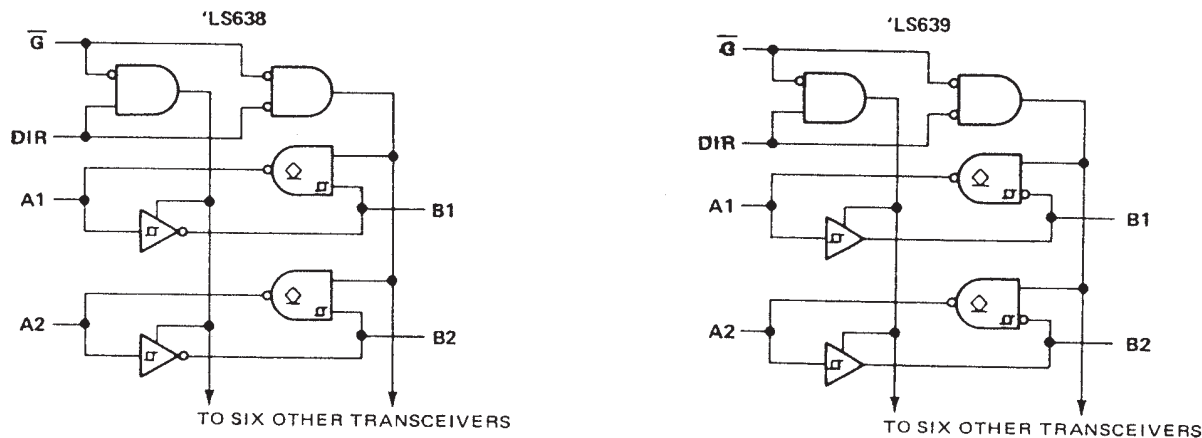
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logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (DIR or $\overline{G}$)	7 V
Off-state output voltage (A or B)	5.5 V
Operating free-air temperature range: SN54LS638, SN54LS639	-55°C to 125°C
SN74LS638, SN74LS639	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.



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recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH} (A bus)			5.5			5.5	V
High-level output current, I_{OH} (B bus)			-12			-15	mA
Low-level output current, I_{OL} (A or B bus)			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT	
			MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IH}	High-level input voltage		2			2			V	
V _{IL}	Low-level input voltage				0.5			0.6	V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V	
Hysteresis (V _{T+} - V _{T-})		V _{CC} = MIN	0.1	0.4		0.2	0.4		V	
I _{OH}	High-level output current	A	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, V _{OH} = 5.5 V			0.1			mA	
V _{OH}	High-level output voltage	B	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OH} = -3 mA	2.4	2.4		V		
				I _{OH} = MAX	2	2				
V _{OL}	Low-level output voltage	A or B	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V	
				I _{OL} = 24 mA			0.35	0.5		
I _{OZH}	Off-state output current, high-level voltage applied	B	V _{CC} = MAX, $\overline{G}$ at 2 V, V _O = 2.7 V			20			μA	
I _{OZL}	Off-state output current low-level voltage applied	A or B	V _{CC} = MAX, $\overline{G}$ at 2 V, V _O = 0.4 V			- 0.4			mA	
I _I	Input current at maximum input voltage	A or B	V _{CC} = MAX	V _I = 5.5 V	0.1		0.1		mA	
		D1R or $\overline{G}$		V _I = 7 V	0.1		0.1			
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7 V			20			μA	
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.4 V			-0.4			mA	
I _{OS}	Short-circuit output current§	B	V _{CC} = MAX			-40	-225	-40	-225	mA
I _{CCH}	Supply current, outputs high		V _{CC} = MAX, Outputs open			48	70	48	70	mA
I _{CCL}	Supply current, outputs low		V _{CC} = MAX, Outputs open			62	90	62	90	mA
I _{CCZ}	Supply current, outputs off		V _{CC} = MAX, Outputs open			64	95	64	95	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS638			'LS639			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	B	$C_L = 45 \text{ pF}, R_L = 667 \Omega$	6	10		8	15		ns
	B	A		17	25		19	25		
t_{PHL}	A	B		8	15		11	15		ns
	B	A		14	25		16	25		
t_{PLH}	$\bar{G}$	A		26	40		23	40		ns
t_{PHL}	$\bar{G}$	A		43	60		34	50		ns
t_{PZH}	$\bar{G}$	B		23	40		26	40		ns
t_{PZL}	$\bar{G}$	B		31	40		31	40		ns
t_{PHZ}	$\bar{G}$	B	$C_L = 5 \text{ pF}, R_L = 667 \Omega$	15	25		15	25		ns
t_{PLZ}	$\bar{G}$	B		15	25		15	25		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



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TYPICAL CHARACTERISTICS

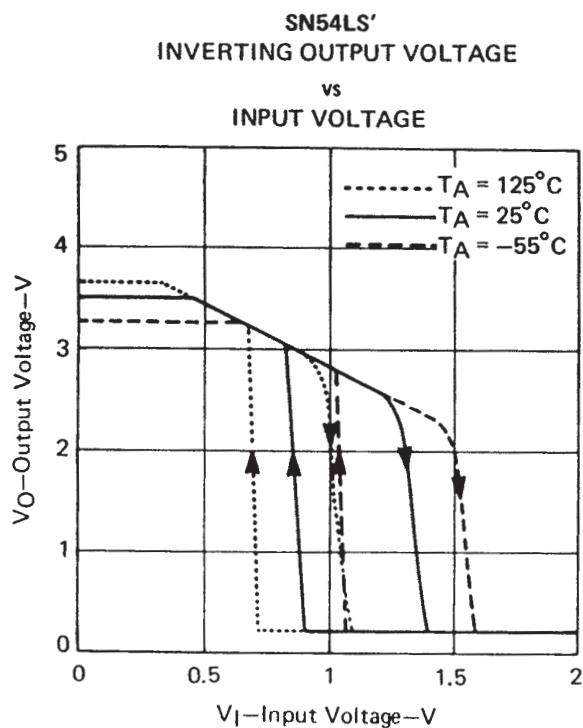


FIGURE 1

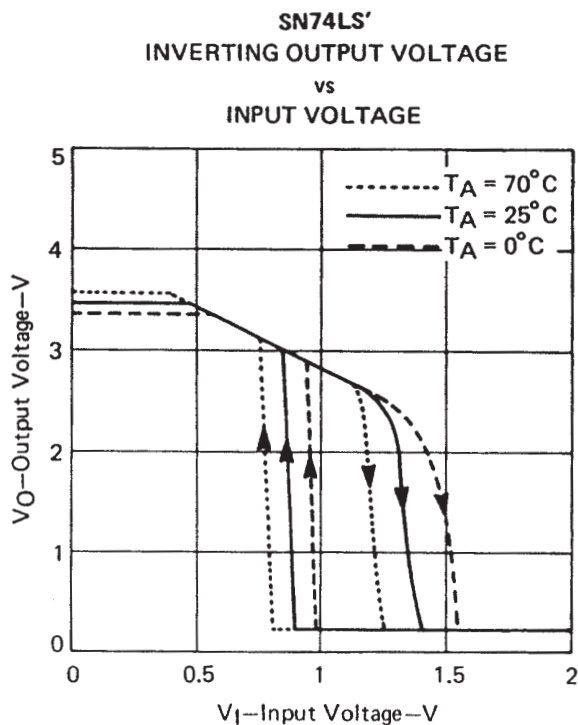


FIGURE 2

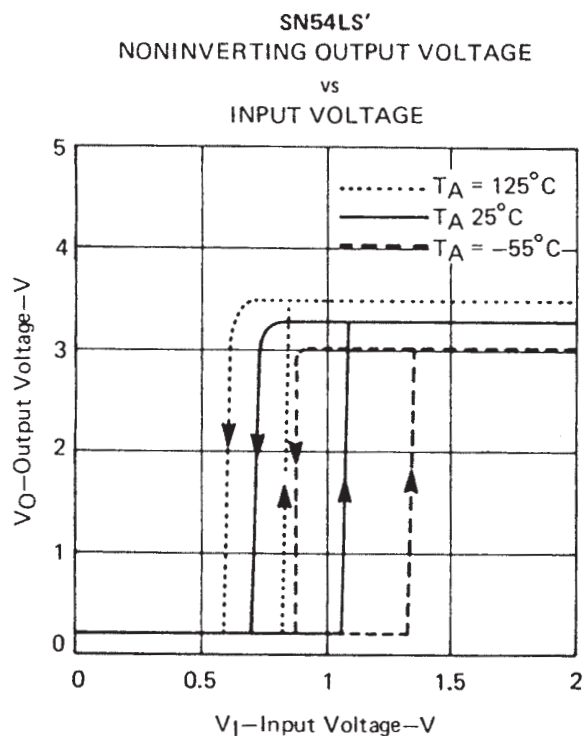


FIGURE 3

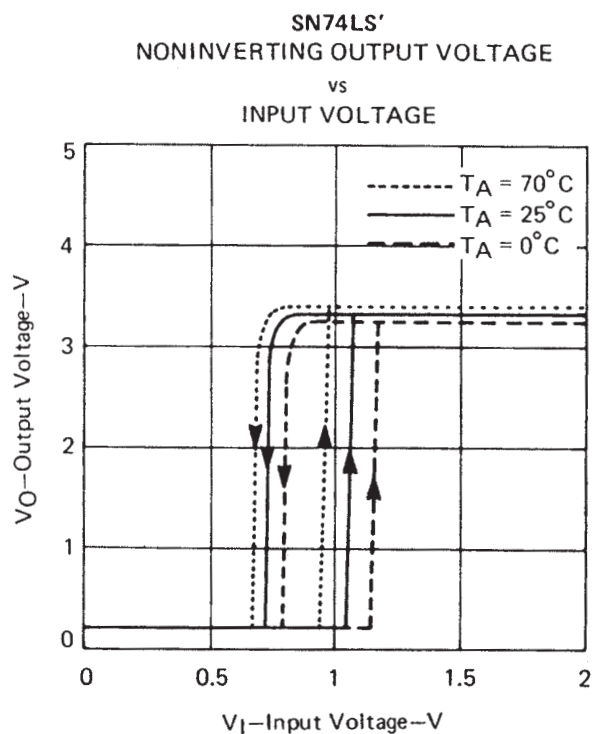


FIGURE 4

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