SHARC Processors

Preliminary Technical Data

ADSP-21462W/ADSP-21465W/ADSP-21467/ADSP-21469/ADSP-21469W

SUMMARY

Note: This datasheet is preliminary. This document contains material that is subject to change without notice.

High performance 32-bit/40-bit floating point processor optimized for high performance audio processing

Single-instruction, multiple-data (SIMD) computational architecture

On-chip memory—5 Mbits of on-chip RAM, 4 Mbits of on-chip ROM

Up to 450 MHz operating frequency

Automotive applications—several models are available for automotive products with special manufacturing. See Automotive Products on Page 68

Code compatible with all other members of the SHARC family

The ADSP-2146x processors are available with unique audio-centric peripherals such as the digital applications interface, DTCP (digital transmission content protection protocol), serial ports, precision clock generators, S/PDIF transceiver, asynchronous sample rate converters, input data port, and more.

For complete ordering information, see Automotive Products on Page 68 and Ordering Guide on Page 68.

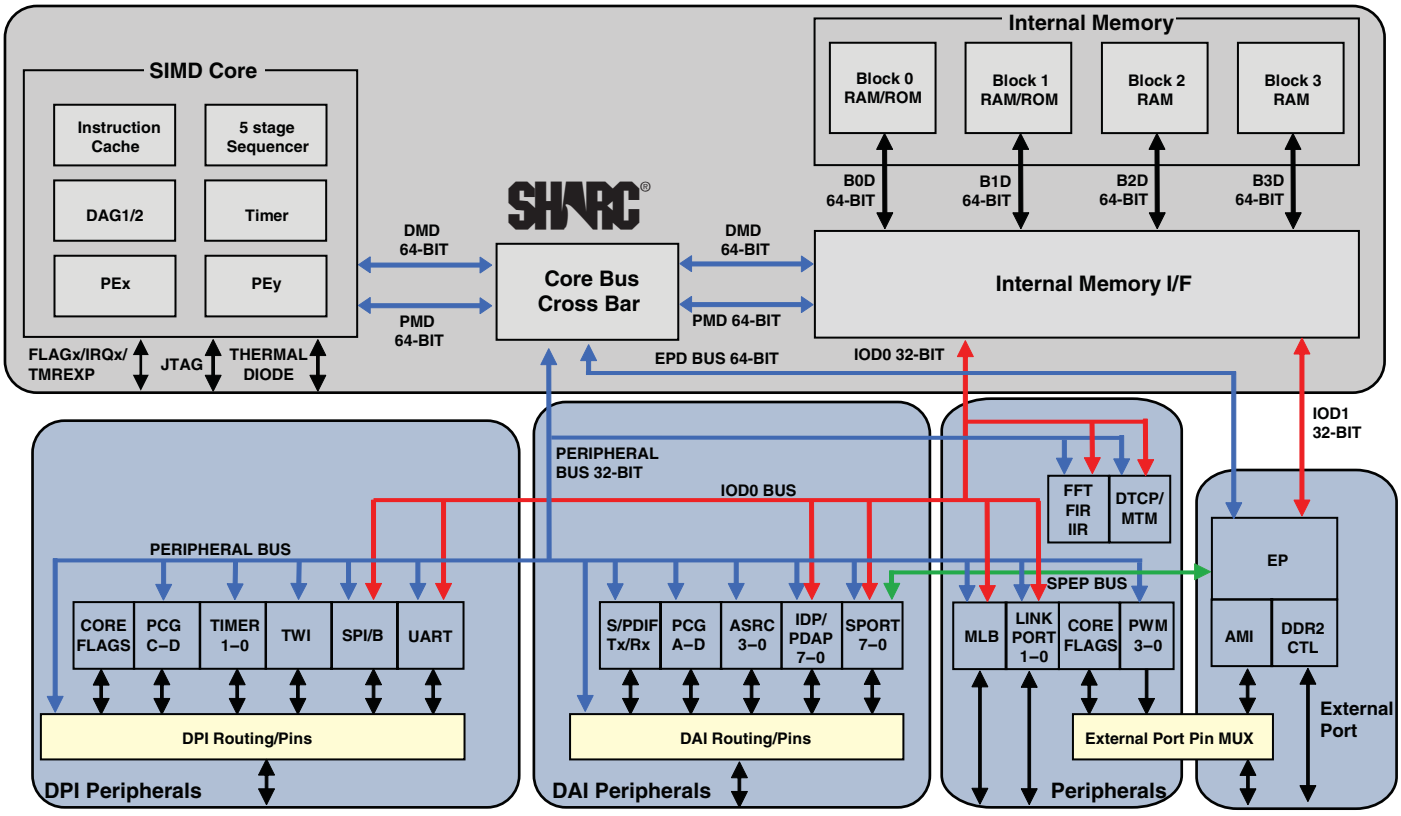

Figure 1. Functional Block Diagram

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GENERAL DESCRIPTION

The ADSP-21462W/ADSP-21465W/ADSP-21467/ADSP-21469/ADSP-21469W SHARC® processors are members of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. The processors are source code compatible with the ADSP-2126x, ADSP-2136x, ADSP-2137x, and ADSP-2116x DSPs as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. These new processors are 32-bit/40-bit floating point processors optimized for high performance audio applications with its large on-chip SRAM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital applications interface (DAI).

Table 1 shows performance benchmarks for the ADSP-2146x processors. Table 2 shows the features of the individual product offerings.

Table 1. Processor Benchmarks

Benchmark Algorithm	Speed (at 450 MHz)
1024 Point Complex FFT (Radix 4, With Reversal)	20.44 µs
FIR Filter (per Tap)[1]	1.11 ns
IIR Filter (per Biquad)[1]	4.43 ns
Matrix Multiply (Pipelined)	
[3 × 3] × [3 × 1]	10.0 ns
[4 × 4] × [4 × 1]	17.78 ns
Divide (y/x)	6.67 ns
Inverse Square Root	10.0 ns

[1] Assumes two files in multichannel SIMD mode

Table 2. SHARC Family Features[1]

Feature	ADSP-21462W	ADSP-21465W	ADSP-21467	ADSP-21469	ADSP-21469W
Frequency	400 MHz	400 MHz	450 MHz	450 MHz	400 MHz
RAM	5M bits				
ROM	N/A	4M bits	4M bits	N/A	N/A
Audio Decoders in ROM[2]	No	Yes	Yes	No	No
Pulse-Width Modulation	Yes				
S/PDIF	Yes				
DTCP[3]	Yes	Yes	No	No	No
DDR2 Memory Interface	Yes				
DDR2 Memory Bus Width	16 bits				
Direct DMA from SPORTs to External Memory	Yes				
FIR, IIR, FFT Accelerator	Yes				
MLB Interface	Yes	Yes	No	No	Yes
IDP	Yes				
Serial Ports	8				
DAI (SRU)/DPI (SRU2)	20/14 pins				
UART	1				
Link Ports	2				
S/PDIF Transceiver	1				
AMI Interface with 8-bit Support	Yes				
SPI	2				
TWI	Yes				
SRC Performance	–128 dB				
Package	324-Ball CSP_BGA				

[1] W = Automotive grade product. See Automotive Products on Page 68 for more information.

[2] Audio decoding algorithms include PCM, Dolby Digital EX, Dolby Prologic IIx, DTS 96/24, Neo:6, DTS ES, MPEG-2 AAC, MP3, and functions like bass management, delay, speaker equalization, graphic equalization, and more. Decoder/post-processor algorithm combination support varies depending upon the chip version and the system configurations. Please visit www.analog.com for complete information.

[3] The ADSP-21462W and ADSP-21465W processors provide the Digital Transmission Content Protection protocol, a proprietary security protocol. Contact your Analog Devices sales office for more information.

The diagram on Page 1 shows the two clock domains that make up the ADSP-2146x processors. The core clock domain contains the following features.

- Two processing elements (PEx, PEy), each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- One periodic interval timer with pinout

- PM and DM buses capable of supporting 2x64-bit data transfers between memory and the core at every core processor cycle
- On-chip SRAM (5M bit)
- On-chip mask-programmable ROM (4M bit)
- JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints which allows flexible exception handling.

The block diagram of the ADSP-2146x on Page 1 also shows the peripheral clock domain (also known as the I/O processor) and contains the following features:

- IOD0 (peripheral DMA) and IOD1 (external port DMA) buses for 32-bit data transfers
- Peripheral and external port buses for core connection
- External port with an AMI and DDR2 controller
- 4 units for PWM control
- 1 MTM unit for internal-to-internal memory transfers
- Digital applications interface that includes four precision clock generators (PCG), a input data port (IDP) for serial and parallel interconnect, an S/PDIF receiver/transmitter, four asynchronous sample rate converters, eight serial ports, a flexible signal routing unit (DAI SRU).
- Digital peripheral interface that includes two timers, a 2-wire interface, two UARTs, two serial peripheral interfaces (SPI), 2 precision clock generators (PCG) and a flexible signal routing unit (DPI SRU).

As shown in the functional block diagram on Page 1, the processor uses two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. Fabricated in a state-of-the-art, high speed, CMOS process, the processor achieves an instruction cycle time of 2.22 ns at 450 MHz and 2.5 ns at 400 MHz. With its SIMD computational hardware, the processors can perform 2.7 GFLOPS running at 450 MHz and 2.4 GFLOPS running at 400 MHz.

FAMILY CORE ARCHITECTURE

The ADSP-2146x is code compatible at the assembly level with the ADSP-2137x, ADSP-2136x, ADSP-2126x, ADSP-21160, and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-2146x shares architectural features with the ADSP-2126x, ADSP-2136x, ADSP-2137x, and ADSP-2116x SIMD SHARC processors, as shown in Figure 2 and detailed in the following sections.

SIMD Computational Engine

The ADSP-2146x contains two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Timer

A core timer that can generate periodic software Interrupts. The core timer can be configured to use FLAG3 as a timer expired signal.

Data Register File

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the processor's enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0-R15 and in PEY as S0-S15.

Context Switch

Many of the processor's registers have secondary registers that can be activated during interrupt servicing for a fast context switch. The data registers in the register file, the DAG registers, and the multiplier result registers all have secondary registers. The primary registers are active at reset, while the secondary registers are activated by control bits in a mode control register.

Universal Registers

These registers can be used for general-purpose tasks. The USTAT (4) registers allow easy bit manipulations (Set, Clear, Toggle, Test, XOR) for all system registers (control/status) of the core.

The data bus exchange register (PX) permits data to be passed between the 64-bit PM data bus and the 64-bit DM data bus, or between the 40-bit register file and the PM data bus. These registers contain hardware to handle the data width difference.

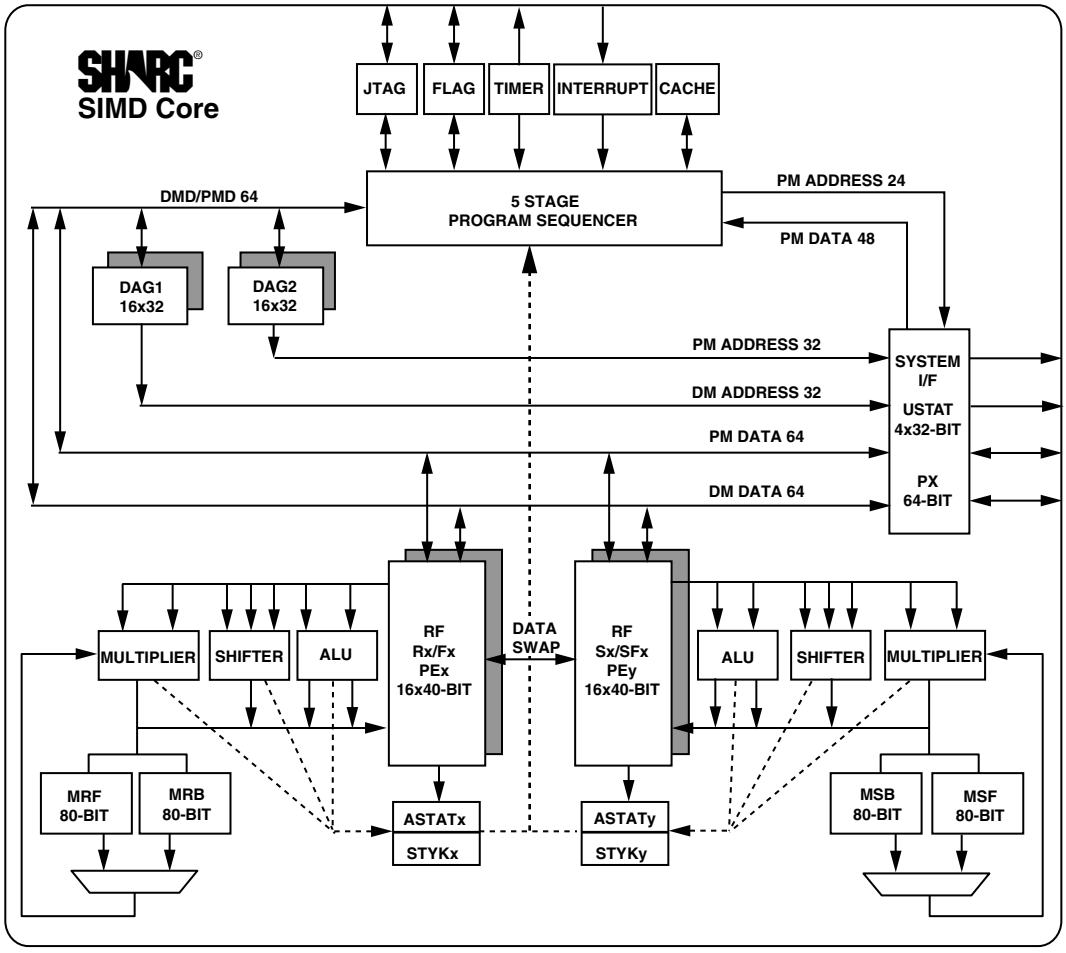


Figure 2. SHARC Core Block Diagram

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-2146x features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 2). With the its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-2146x includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators With Zero-Overhead Hardware Circular Buffer Support

The ADSP-2146x's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the processors contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-2146x can conditionally execute a multiply, an add, and a

subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

Variable Instruction Set Architecture (VISA)

In addition to supporting the standard 48-bit instructions from previous SHARC processors, the ADSP-2146x supports new instructions of 16 and 32 bits. This feature, called Variable Instruction Set Architecture (VISA), drops redundant/unused bits within the 48-bit instruction to create more efficient and compact code. The program sequencer supports fetching these 16-bit and 32-bit instructions from both internal and external DDR2 memory. Source modules need to be built using the VISA option, in order to allow code generation tools to create these more efficient opcodes.

On-Chip Memory

The processors contain 5 Mbits of internal RAM. Each block can be configured for different combinations of code and data storage (see Table 4). Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The ADSP-2146x memory architecture, in combination with its separate on-chip buses, allow two data transfers from the core and one from the I/O processor, in a single cycle.

The processor's SRAM can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5 megabit. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

The memory map in Table 3 displays the internal memory address space of the ADSP-21462W, ADSP-21469 and ADSP-21469W processors.

The memory map in Table 4 displays the internal memory address space of the ADSP-21465W and ADSP-21467 processors.

The 48-bit space section describes what this address range looks like to an instruction that retrieves 48-bit memory. The 32-bit section describes what this address range looks like to an instruction that retrieves 32-bit memory.

On-Chip Memory Bandwidth

The internal memory architecture allows programs to have four accesses at the same time to any of the four blocks (assuming there are no block conflicts). The total bandwidth is realized using the DMD and PMD buses (2 x 64-bits, CCLK speed) and the IOD0/1 buses (2 x 32-bit, PCLK speed).

Table 3. ADSP-21462W/ADSP-21469/ADSP-21469W Internal Memory Space

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 bits)	**Extended Precision Normal or Instruction Word (48 bits)**	**Normal Word (32 bits)**	**Short Word (16 bits)**
BLOCK 0 RAM 0x0004 9000–0x0004 EFFF	BLOCK 0 RAM 0x0008 C000-0x0009 3FFF	BLOCK 0 RAM 0x0009 2000-0x0009 DFFF	BLOCK 0 RAM 0x0012 4000–0x0013 BFFF
Reserved 0x0004 F000–0x0005 8FFF	Reserved 0x0009 4000–0x0009 5554	Reserved 0x0009 E000–0x000B 1FFF	Reserved 0x0013 C000–0x0016 3FFF
BLOCK 1 RAM 0x0005 9000–0x0005 EFFF	BLOCK 1 RAM 0x000A C000-0x000B 3FFF	BLOCK 1 RAM 0x000B 2000-0x000B DFFF	BLOCK 1 RAM 0x0016 4000-0x0017 BFFF
Reserved 0x0005 F000–0x0005 FFFF	Reserved 0x000B 4000–0x000B 5554	Reserved 0x000B E000–0x000B FFFF	Reserved 0x0017 C000–0x0017 FFFF
BLOCK 2 RAM 0x0006 0000–0x0006 3FFF	BLOCK 2 RAM 0x000C 0000–0x000C 5554	BLOCK 2 RAM 0x000C 0000-0x000C 7FFF	BLOCK 2 RAM 0x0018 0000–0x0018 FFFF
Reserved 0x0006 4000–0x0006 FFFF	Reserved 0x000C 5555–0x000D 5554	Reserved 0x000C 8000–0x000D FFFF	Reserved 0x0019 0000–0x001B FFFF
BLOCK 3 RAM 0x0007 0000–0x0007 3FFF	BLOCK 3 RAM 0x000E 0000–0x000E 5554	BLOCK 3 RAM 0x000E 0000–0x000E 7FFF	BLOCK 3 RAM 0x001C 0000–0x001C FFFF
Reserved 0x0007 4000–0x0007 FFFF	Reserved 0x000E 5555–0x000F 5554	Reserved 0x000E 8000–0x000F FFFF	Reserved 0x001D 0000–0x001F FFFF

Table 4. ADSP-21465W/ADSP-21467 Internal Memory Space

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 bits)	**Extended Precision Normal or Instruction Word (48 bits)**	**Normal Word (32 bits)**	**Short Word (16 bits)**
BLOCK 0 ROM 0x0004 0000–0x0004 7FFF	BLOCK 0 ROM 0x0008 0000–0x0008 AAA9	BLOCK 0 ROM 0x0008 0000–0x0008 FFFF	BLOCK 0 ROM 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 8FFF	Reserved 0x0008 AAAA–0x0008 BFFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0012 0000–0x0012 3FFF
BLOCK 0 RAM 0x0004 9000–0x0004 EFFF	BLOCK 0 RAM 0x0008 C000-0x0009 3FFF	BLOCK 0 RAM 0x0009 2000-0x0009 DFFF	BLOCK 0 RAM 0x0012 4000–0x0013 BFFF
Reserved 0x0004 F000–0x0004 FFFF	Reserved 0x0009 4000–0x0009 5554	Reserved 0x0009 E000–0x0009 FFFF	Reserved 0x0013 C000–0x0013 FFFF
BLOCK 1 ROM 0x0005 0000–0x0005 7FFF	BLOCK 1 ROM 0x000A 0000–0x000A AAA9	BLOCK 1 ROM 0x000A 0000–0x000A FFFF	BLOCK 1 ROM 0x0014 0000-0x0015 FFFF
Reserved 0x0005 8000–0x0005 8FFF	Reserved 0x000A AAAA–0x000A BFFF	Reserved 0x000B 0000–0x000B 1FFF	Reserved 0x0016 0000-0x0016 3FFF
BLOCK 1 RAM 0x0005 9000–0x0005 EFFF	BLOCK 1 RAM 0x000A C000-0x000B 3FFF	BLOCK 1 RAM 0x000B 2000-0x000B DFFF	BLOCK 1 RAM 0x0016 4000-0x0017 BFFF
Reserved 0x0005 F000–0x0005 FFFF	Reserved 0x000B 4000–0x000B 5554	Reserved 0x000B E000–0x000B FFFF	Reserved 0x0017 C000–0x0017 FFFF
BLOCK 2 RAM 0x0006 0000–0x0006 3FFF	BLOCK 2 RAM 0x000C 0000–0x000C 5554	BLOCK 2 RAM 0x000C 0000-0x000C 7FFF	BLOCK 2 RAM 0x0018 0000–0x0018 FFFF
Reserved 0x0006 4000–0x0006 FFFF	Reserved 0x000C 5555–0x000D 5554	Reserved 0x000C 8000–0x000D FFFF	Reserved 0x0019 0000–0x001B FFFF
BLOCK 3 RAM 0x0007 0000–0x0007 3FFF	BLOCK 3 RAM 0x000E 0000–0x000E 5554	BLOCK 3 RAM 0x000E 0000–0x000E 7FFF	BLOCK 3 RAM 0x001C 0000–0x001C FFFF
Reserved 0x0007 4000–0x0007 FFFF	Reserved 0x000E 5555–0x0000F 5554	Reserved 0x000E 8000–0x000F FFFF	Reserved 0x001D 0000–0x001F FFFF

ROM Based Security

The ADSP-2146x has a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code when enabled. When using this feature, the processor does not boot-load any external code, executing exclusively from internal ROM. Additionally, the processor is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or Test Access Port will be assigned to each customer. The device ignores a wrong key. Emulation features and external boot modes are only available after the correct key is scanned.

Digital Transmission Content Protection

The DTCP specification defines a cryptographic protocol for protecting audio entertainment content from illegal copying, intercepting, and tampering as it traverses high performance digital buses, such as the IEEE 1394 standard. Only legitimate entertainment content delivered to a source device via another approved copy protection system (such as the DVD content scrambling system) is protected by this copy protection system. This feature is available on the ADSP-21462W and ADSP-21465W processors only. Licensing through DTLA is required for these products. Visit www.dtcp.com for more information.

FAMILY PERIPHERAL ARCHITECTURE

The ADSP-2146x family contains a rich set of peripherals that support a wide variety of applications including high quality audio, medical imaging, communications, military, test equipment, 3D graphics, speech recognition, motor control, imaging, and other applications.

External Port

The external port interface supports access to the external memory through core and DMA accesses. The external memory address space is divided into four banks. Any bank can be programmed as either asynchronous or synchronous memory. The external ports are comprised of the following modules.

- An Asynchronous Memory Interface which communicates with SRAM, FLASH, and other devices that meet the standard asynchronous SRAM access protocol. The AMI

supports 14M words of external memory in bank 0 and 16M words of external memory in bank 1, bank 2, and bank 3.

- A DDR2 DRAM controller. External memory devices up to 2 Gbits in size can be supported.
- Arbitration Logic to coordinate core and DMA transfers between internal and external memory over the external port.

External Memory

The external port on the ADSP-2146x SHARC provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The external port may be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal DDR2 memory controller. The 16-bit DDR2 DRAM controller connects to industry-standard synchronous DRAM devices, while the second 8-bit asynchronous memory controller is intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types. Non DDR2 DRAM external memory address space is shown in Table 5.

Table 5. External Memory for Non DDR2 DRAM Addresses

Bank	Size in Words	Address Range
Bank 0	14M	0x0020 0000 – 0x00FF FFFF
Bank 1	16M	0x0400 0000 – 0x04FF FFFF
Bank 2	16M	0x0800 0000 – 0x08FF FFFF
Bank 3	16M	0x0C00 0000 – 0x0CFF FFFF

SIMD Access to External Memory

The DDR2 controller on the ADSP-2146x processor supports SIMD access on the 64-bit EPD (external port data bus) which allows to access the complementary registers on the PEy unit in the normal word space (NW). This improves performance since there is no need to explicitly load the complimentary registers as in SISD mode.

VISA and Non VISA Access to External Memory

The DDR2 controller on the ADSP-2146x processor supports VISA code operation which reduces the memory load since the VISA instructions are compressed. Moreover, bus fetching is reduced because in the best case one 48-bit fetch contains 3 valid instructions. Code execution from the traditional non-VISA operation is also supported. Note that code execution is only supported from bank 0 regardless of VISA/non-VISA.

DDR2 Support

The ADSP-2146x supports a 16-bit DDR2 interface operating at a maximum frequency of half the core clock. Execution from external memory is supported. External memory devices up to 2 Gbits in size can be supported.

DDR2 DRAM Controller

The DDR2 DRAM controller provides an 16-bit interface to up to four separate banks of industry-standard DDR2 DRAM devices. Fully compliant with the DDR2 DRAM standard, each bank can has its own memory select line (DDR2_CS3 – DDR2_CS0), and can be configured to contain between 32M bytes and 256M bytes of memory. DDR2 DRAM external memory address space is shown in Table 6

A set of programmable timing parameters is available to configure the DDR2 DRAM banks to support memory devices.

Table 6. External Memory for DDR2 DRAM Addresses

Bank	Size in Words	Address Range
Bank 0	62M	0x0020 0000 – 0x03FF FFFF
Bank 1	64M	0x0400 0000 – 0x07FF FFFF
Bank 2	64M	0x0800 0000 – 0x0BFF FFFF
Bank 3	64M	0x0C00 0000 – 0x0FFF FFFF

Note that the external memory bank addresses shown are for normal-word (32-bit) accesses. If 48-bit instructions as well as 32-bit data are both placed in the same external memory bank, care must be taken while mapping them to avoid overlap. In case of 16-bit wide external memory, two 48-bit instructions are stored in six 32-bit wide memory locations. For example, if 2k instructions are placed in 16-bit wide external memory starting at the bank 0 normal-word base address 0x0030 0000 (corresponding to instruction address 0x0020 0000) and ending at address 0x0030 0BFF (corresponding to instruction address 0x0020 07FF), then data buffers can be placed starting at an address that is offset by 3k 32-bit words (for example, starting at 0x0030 0C00).

Asynchronous Memory Controller

The asynchronous memory controller provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 14M word window and banks 1, 2, and 3 occupy a 16M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic.

External Port Throughput

The throughput for the external port, based on a 400 MHz clock, is 66 M bytes/s for the AMI and 800 M bytes/s for DDR2.

Link Ports

Two 8-bit wide link ports can connect to the link ports of other DSPs or peripherals. Link ports are bidirectional ports having eight data lines, an acknowledge line and a clock line. Link ports can operate at a maximum frequency of 166 MHz.

MediaLB

The ADSP-21462W, ADSP-21465W and ADSP-21469W have a MLB interface which allows the processor to function as a media local bus device. It includes support for both 3-pin as well as 5-pin media local bus protocols. It supports speeds up to 1024 FS (49.25 Mbits/sec, FS = 48.1 kHz) and up to 31 logical channels, with up to 124 bytes of data per media local bus frame.

The MLB interface on ADSP-2146x supports MOST25 and MOST50 data rates. The isochronous mode of transfer is not supported in ADSP-2146x processor.

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs each. Therefore, this module generates 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the mid-point of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the mid-point of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters.

Digital Applications Interface (DAI)

The digital applications interface (DAI) provides the ability to connect various peripherals to any of the DAI pins (DAI_P20–1).

Programs make these connections using the signal routing unit (SRU), shown in Figure 1.

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI also includes eight serial ports, four precision clock generators (PCG), S/PDIF transceiver, four ASRCs, and an input data port (IDP). The IDP provides an additional input path to the SHARC core, configurable as either eight channels of serial data, or a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

Serial Ports

The ADSP-2146x features eight synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports can support up to 16 transmit or 16 receive channels of audio data when all eight SPORTs are enabled, or four full duplex TDM streams of 128 channels per frame.

The serial ports operate at a maximum data rate of $f_{PCLK}/4$. Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode

Left-justified mode is a mode where in each frame sync cycle two samples of data are transmitted/received—one sample on the high segment of the frame sync, the other on the low segment of the frame sync. Programs have control over various attributes of this mode.

Each of the serial ports supports the left-justified and I^2S protocols (I^2S is an industry-standard interface commonly used by audio codecs, ADCs, and DACs such as the Analog Devices AD183x family), with two data pins, allowing four left-justified or I^2S channels (using two stereo devices) per serial port, with a maximum of up to 32 I^2S channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For the left-justified and I^2S modes, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional µ-law or A-law companding selection on a per channel basis. Serial port clocks and frame syncs can be internally or externally generated.

The serial ports also contain frame sync error detection logic where the serial ports detect frame syncs that arrive early (for example frame syncs that arrive while the transmission/reception of the previous word is occurring). All the serial ports also share one dedicated error interrupt.

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left justified, I^2S or right justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCGs), and are controlled by the SRU control registers.

Asynchronous Sample Rate Converter

The sample rate converter (ASRC) contains four ASRC blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter and provides up to 128 dB SNR. The ASRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the ASRC can be used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

Input Data Port

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive audio channels in I2S, left-justified sample pair, or right-justified mode. One frame sync cycle indicates one 64-bit left/right pair, but data is sent to the FIFO as 32-bit words (that is, one-half of a frame at a time). The processor supports 24- and 32-bit I^2S, 24- and 32-bit left-justified, and 24-, 20-, 18- and 16-bit right-justified formats.

Precision Clock Generators

The precision clock generators (PCG) consist of four units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A B, C, and D, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

Digital Peripheral Interface (DPI)

The digital peripheral interface provides connections to two serial peripheral interface ports (SPI), one universal asynchronous receiver-transmitter (UART), 12 flags, a 2-wire interface (TWI), and two general-purpose timers.

Serial Peripheral (Compatible) Interface

The ADSP-2146x SHARC processors contain two serial peripheral interface ports (SPIs). The SPI is an industry-standard synchronous serial link, enabling the SPI-compatible port to communicate with other SPI compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The SPI-compatible peripheral implementation also features programmable baud rate and clock phase and polarities. The SPI-compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

UART Port

The processors provide a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{PCLK}/ 1,048,576) to (f_{PCLK}/16) bits per second.
- Supporting data formats from 7 to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

In conjunction with the general-purpose timer functions, autobaud detection is supported.

Timers

The ADSP-2146x has a total of three timers: a core timer that can generate periodic software interrupts and two general purpose timers that can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

The core timer can be configured to use FLAG3 as a timer expired signal, and each general-purpose timer has one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables both general-purpose timers independently.

2-Wire Interface Port (TWI)

The TWI is a bidirectional 2-wire, serial bus used to move 8-bit data while maintaining compliance with the I^2C bus protocol. The TWI master incorporates the following features:

- 7-bit addressing
- Simultaneous master and slave operation on multiple device systems with support for multi master data arbitration
- Digital filtering and timed event processing
- 100 kbps and 400 kbps data rates
- Low interrupt rate

I/O Processor Features

The ADSP-21462W, ADSP-21465W and ADSP-21469W I/O processors provide 67 channels of DMA, while ADSP-21467 and ADSP-21469 I/O processors provide 36 channels of DMA as well as an extensive set of peripherals. These include a 20 lead digital applications interface, which controls:

DMA Controller

The processor's on-chip DMA controller allows data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the ADSP-2146x's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the parallel data acquisition port (PDAP) or the UART.

Up to 67 channels of DMA are available on the ADSP-2146x processors as shown in Table 7.

Programs can be downloaded to the ADSP-2146x using DMA transfers. Other DMA features include interrupt generation upon completion of DMA transfers, and DMA chaining for automatic linked DMA transfers.

Delay Line DMA

The ADSP-2146x processor provides delay line DMA functionality. This allows processor reads and writes to external delay line buffers (and hence to external memory) with limited core interaction.

Scatter/Gather DMA

The ADSP-2146x processor provides scatter/gather DMA functionality.

This allows processor DMA reads/writes to/from non-contingeous memory blocks.

IIR Accelerator

The IIR (infinite impulse response) accelerator consists of a 1440 word coefficient memory for storage of biquad coefficients, a data memory for storing the intermediate data and one MAC unit. A controller manages the accelerator. The IIR accelerator runs at the peripheral clock frequency.

Table 7. DMA Channels

Peripheral	DMA Channels	
	ADSP-21462W ADSP-21465W ADSP-21469W	**ADSP-21467 ADSP-21469**
SPORTs	16	16
PDAP	8	8
SPI	2	2
UART	2	2
External Port	2	2
Link Port	2	2
Accelerators	2	2
Memory-to-Memory	2	2
MLB	31	0

FFT Accelerator

FFT accelerator implements radix-2 complex/real input, complex output FFT with no core intervention.

FIR Accelerator

The FIR (finite impulse response) accelerator consists of a 1024 word coefficient memory, a 1024 word deep delay line for the data, and four MAC units. A controller manages the accelerator. The FIR accelerator runs at the peripheral clock frequency.

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory of the ADSP-2146x boots at system power-up from an 8-bit EPROM via the external port, link port, an SPI master, or an SPI slave. Booting is determined by the boot configuration (BOOTCFG2–0) pins in Table 8.

Table 8. Boot Mode Selection

BOOTCFG2–0	Booting Mode
000	SPI Slave Boot
001	SPI Master Boot
010	AMI Boot (for 8-bit Flash boot)
011	Reserved
100	Link Port 0 Boot
101	Reserved

The "Running Reset" feature allows a user to perform a reset of the processor core and peripherals, but without resetting the PLL and DDR2 DRAM controller, or performing a Boot. The functionality of the $\overline{\text{RESETOUT}}$ pin also acts as the input for initiating a Running Reset. For more information, see the *ADSP-2146x SHARC Processor Hardware Reference*.

Power Supplies

The processors have separate power supply connections for the internal (V_{DD_INT}), external (V_{DD_EXT}), and analog (V_{DD_A}/AGND) power supplies. The internal and analog supplies must meet the V_{DD_INT} specifications. The external supply must meet the V_{DD_EXT} specification. All external supply pins must be connected to the same power supply.

Note that the analog supply pin (V_{DD_A}) powers the processor's internal clock generator PLL. To produce a stable clock, it is recommended that PCB designs use an external filter circuit for the V_{DD_A} pin. Place the filter components as close as possible to the V_{DD_A}/AGND pins. For an example circuit, see Figure 3. (A recommended ferrite chip is the muRata BLM18AG102SN1D).

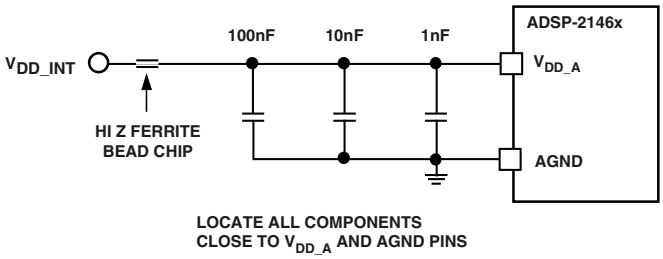


Figure 3. Analog Power (V_{DD_A}) Filter Circuit

To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DD_INT} and GND. Use wide traces to connect the bypass capacitors to the analog power (V_{DD_A}) and ground (AGND) pins. Note that the V_{DD_A} and AGND pins specified in Figure 3 are inputs to the processor and not the analog ground plane on the board—the AGND pin should connect directly to digital ground (GND) at the chip

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-2146x processors to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate "Emulator Hardware User's Guide".

DEVELOPMENT TOOLS

The ADSP-2146x processors are supported with a complete set of CROSSCORE® software and hardware development tools, including Analog Devices emulators and VisualDSP++® development environment. The same emulator hardware that supports other SHARC processors also fully emulates the ADSP-2146x processors.

EZ-KIT Lite Evaluation Board

For evaluation of the processors, use the EZ-KIT Lite® board being developed by Analog Devices. The board comes with on-chip emulation capabilities and is equipped to enable software development. Multiple daughter cards are available.

Designing an Emulator-Compatible DSP Board (Target)

The Analog Devices family of emulators are tools that every DSP developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG Test Access Port (TAP) on each JTAG DSP. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing. The emulator uses the TAP to access the internal features of the processor, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The processor must be halted to send data and commands, but once an operation has been completed by the emulator, the DSP system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

Evaluation Kit

Analog Devices offers a range of EZ-KIT Lite® evaluation platforms to use as a cost effective method to learn more about developing or prototyping applications with Analog Devices processors, platforms, and software tools. Each EZ-KIT Lite includes an evaluation board along with an evaluation suite of the VisualDSP++® development and debugging environment with the C/C++ compiler, assembler, and linker. Also included are sample application programs, power supply, and a USB cable. All evaluation versions of the software tools are limited for use only with the EZ-KIT Lite product.

The USB controller on the EZ-KIT Lite board connects the board to the USB port of the user's PC, enabling the VisualDSP++ evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also allows in-circuit programming of the on-board Flash device to store user-specific boot code, enabling the board to run as a standalone unit without being connected to the PC.

With a full version of VisualDSP++ installed (sold separately), engineers can develop software for the EZ-KIT Lite or any custom defined system. Connecting one of Analog Devices JTAG emulators to the EZ-KIT Lite board enables high speed, nonintrusive emulation.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-2146x architecture and functionality. For detailed information on the ADSP-2146x family core architecture and instruction set, refer to the *ADSP-2136x/ADSP-2146x SHARC Processor Programming Reference*.

PIN FUNCTION DESCRIPTIONS

UNUSED DDR2 PINS

When the DDR2 controller is not used:

- Leave the DDR2 signal pins floating.
- Internally, three-state the DDR2 I/O signals. This can be done by setting the DIS_DDTCL bit of DDR2CTL0 register.
- Power down the receive path by setting the PWD bits of the DDR2PADCTLx register.
- Connect the V_{DD_DDR2} pins to the V_{DD_INT} supply.
- Leave V_{REF} floating/unconnected.

Table 9. Pin Descriptions

Name	Type	State During/ After Reset	Description
AMI_ADDR$_{23-0}$	I/O/T (ipu)	High-Z/driven low (boot)	**External Address.** The processor outputs addresses for external memory and peripherals on these pins. The data pins can be multiplexed to support the PDAP (I) and PWM (O). After reset, all AMI_ADDR$_{23-0}$ pins are in external memory interface mode and FLAG(0–3) pins are in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the AMI_ADDR$_{23-0}$ pins for parallel input data.
AMI_DATA$_{7-0}$	I/O/T (ipu)	High-Z	**External Data.** The data pins can be multiplexed to support the external memory interface data (I/O), the PDAP (I), FLAGS (I/O) and PWM (O). After reset, all AMI_DATA pins are in EMIF mode and FLAG(0-3) pins are in FLAGS mode (default).
AMI_ACK	I (ipu)		**Memory Acknowledge (AMI_ACK).** External devices can deassert AMI_ACK (low) to add wait states to an external memory access. AMI_ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{\text{AMI_MS}}_{0-1}$	O/T (ipu)	High-Z	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory on the AMI interface. The $\overline{\text{MS}}_{1-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{\text{MS}}_{1-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, whether or not the condition is true. The $\overline{\text{MS1}}$ pin can be used in EPORT/FLASH boot mode. For more information, see the *ADSP-2146x SHARC Processor Hardware Reference*.
$\overline{\text{AMI_RD}}$	O/T (ipu)	High-Z	**AMI Port Read Enable.** $\overline{\text{AMI_RD}}$ is asserted whenever the processor reads a word from external memory.
$\overline{\text{AMI_WR}}$	O/T (ipu)	High-Z	**External Port Write Enable.** $\overline{\text{AMI_WR}}$ is asserted when the processor writes a word to external memory.
FLAG[0]/$\overline{\text{IRQ0}}$	I/O (ipu)	FLAG[0] INPUT	**FLAG0/Interrupt Request0.**
FLAG[1]/$\overline{\text{IRQ1}}$	I/O (ipu)	FLAG[1] INPUT	**FLAG1/Interrupt Request1.**
FLAG[2]/$\overline{\text{IRQ2}}$/ $\overline{\text{AMI_MS2}}$	I/O (ipu)	FLAG[2] INPUT	**FLAG2/Interrupt Request2/Async Memory Select2.**
FLAG[3]/TMREXP/ $\overline{\text{AMI_MS3}}$	I/O (ipu)	FLAG[3] INPUT	**FLAG3/Timer Expired/Async Memory Select3.**

The following symbols appear in the Type column of Table 9: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26k–63k Ω. The range of an ipd resistor can be between 31k–85k Ω.
In this table, the DDR2 pins are SSTL18 compliant. All other pins are LVTTL compliant.

Table 9. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
DDR2_ADDR$_{15–0}$	O/T	High-Z/Driven low	**DDR2 Address.** DDR2 address pins.
DDR2_BA$_{2-0}$	O/T	High-Z/Driven low	**DDR2 Bank Address Input.** Defines which internal bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied to. BA$_{2–0}$define which mode registers, including MR, EMR, EMR(2), and EMR(3) are loaded during the LOAD MODE REGISTER command.
$\overline{\text{DDR2_CAS}}$	O/T	High-Z/Driven high	**DDR2 Column Address Strobe.** Connect to $\overline{\text{DDR2_CAS}}$ pin, in conjunction with other DDR2 command pins, defines the operation for the DDR2 to perform.
DDR2_CKE	O/T	High-Z/Driven low	**DDR2 Clock Enable Output to DDR2.** Active high signal. Connect to DDR2 CKE signal.
$\overline{\text{DDR2_CS}}_{3-0}$	O/T	High-Z/Driven high	**DDR2 Chip Select.** All commands are masked when $\overline{\text{DDR2_CS}}_{3-0}$ is driven high. $\overline{\text{DDR2_CS}}_{3-0}$ are decoded memory address lines. Each $\overline{\text{DDR2_CS}}_{3-0}$lines select the corresponding external bank.
DDR2_DATA$_{15-0}$	I/O/T	High-Z	**DDR2 Data In/Out.** Connect to corresponding DDR2_DATA pins.
DDR2_DM$_{1-0}$	O/T	High-Z/Driven high	**DDR2 Input Data Mask.** Mask for the DDR2 write data if driven high. Sampled on both edges of DDR2_DQS at DDR2 side. DM0 corresponds to DDR2_DATA 7–0 and DM1 corresponds to DDR2_DATA15–8.
DDR2_DQS$_{1-0}$ $\overline{\text{DDR2_DQS}}_{1-0}$	I/O/T (Differential)	High-Z	**Data Strobe.** Output with Write Data. Input with Read Data. DQS0 corresponds to DDR2_DATA 7–0 and DQS1 corresponds to DDR2_DATA 15–8. Based on software control via the DDR2CTL3 register, this pin can be single-ended or differential.
$\overline{\text{DDR2_RAS}}$	O/T	High-Z/Driven high	**DDR2 Row Address Strobe.** Connect to $\overline{\text{DDR2_RAS}}$ pin, in conjunction with other DDR2 command pins, defines the operation for the DDR2 to perform.
$\overline{\text{DDR2_WE}}$	O/T	High-Z/Driven high	**DDR2 Write Enable.** Connect to $\overline{\text{DDR2_WE}}$ pin, in conjunction with other DDR2 command pins, defines the operation for the DDR2 to perform.
DDR2_CLK0, $\overline{\text{DDR2_CLK0}}$, DDR2_CLK1, $\overline{\text{DDR2_CLK1}}$	O/T (Differential)	High-Z/Driven low	**DDR2 Memory Clocks.** Two differential outputs available via software control (DDR2CTL0 register). Free running, minimum frequency not guaranteed during reset.
DDR2_ODT	O/T	High-Z/Driven low	**DDR2 On Die Termination.** ODT pin when driven high (along with other requirements) enables the DDR2 termination resistances. ODT is enabled/disabled regardless off read or write commands.

The following symbols appear in the Type column of Table 9: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26k–63k Ω. The range of an ipd resistor can be between 31k–85k Ω.
In this table, the DDR2 pins are SSTL18 compliant. All other pins are LVTTL compliant.

Table 9. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
DAI _P_{20-1}	I/O/T (ipu)	High-Z	**Digital Applications Interface**. These pins provide the physical interface to the DAI SRU. The DAI SRU configuration registers define the combination of on-chip audio-centric peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determine the exact behavior of the pin. Any input or output signal present in the DAI SRU may be routed to any of these pins. The DAI SRU provides the connection from the serial ports, the S/PDIF module, input data ports (2), and the precision clock generators (4), to the DAI_P20–1 pins.
DPI _P_{14-1}	I/O/T (ipu)	High-Z	**Digital Peripheral Interface.** These pins provide the physical interface to the DPI SRU. The DPI SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DPI SRU may be routed to any of these pins. The DPI SRU provides the connection from the timers (2), SPIs (2), UART (1), flags (12), and general-purpose I/O (9) to the DPI_P14–1 pins.
$LDAT0_{7-0}$ $LDAT1_{7-0}$	I/O/T (ipd)	High-Z	**Link Port Data (Link Ports 0–1)**. When configured as a transmitter, the port drives both the data lines.
LCLK0 LCLK1	I/O/T (ipd)	High-Z	**Link Port Clock (Link Ports 0–1).** Allows asynchronous data transfers. When configured as a transmitter, the port drives LCLKx lines. An external 25kΩ pull-down resistor is required for the proper operation of this pin.
LACK0 LACK1	I/O/T (ipd)	High-Z	**Link Port Acknowledge (Link Port 0–1).** Provides handshaking. When the link ports are configured as a receiver, the port drives the LACKx line. An external 25kΩ pull-down resistor is required for the proper operation of this pin.
THD_P	I		**Thermal Diode Anode**. If unused, can be left floating.
THD_M	O		**Thermal Diode Cathode**. If unused, can be left floating.
MLBCLK[1]	I (ipd)		**Media Local Bus Clock.** This clock is generated by the MLB controller that is synchronized to the MOST network and provides the timing for the entire MLB interface. 49.152 MHz at Fs=48 kHz. If unused, can be left floating.
MLBDAT[1]	I/O/T (ipd) in 3 pin mode. I/T (ipd) in 5 pin mode.	High-Z	**Media Local Bus Data.** The MLBDAT line is driven by the transmitting MLB device and is received by all other MLB devices including the MLB controller. The MLBDAT line carries the actual data. In 5-pin MLB mode, this pin is an input only. If unused, can be left floating.
MLBSIG[1]	I/O/T in 3 pin mode. I/T in 5 pin mode	High-Z	**Media Local Bus Signal.** This is a multiplexed signal which carries the Channel/Address generated by the MLB Controller, as well as the Command and RxStatus bytes from MLB devices. In 5-pin mode, this pin is an input only. If unused, can be left floating.
MLBDO[1]	O/T (ipd)	High-Z	**Media Local Bus Data Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output data pin in 5-pin mode. If unused, can be left floating.
MLBSO[1]	O/T (ipd)	High-Z	**Media Local Bus Signal Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output signal pin in 5-pin mode. If unused, can be left floating.

The following symbols appear in the Type column of Table 9: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26k–63k Ω. The range of an ipd resistor can be between 31k–85k Ω.
In this table, the DDR2 pins are SSTL18 compliant. All other pins are LVTTL compliant.

Table 9. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
TDI	I (ipu)		**Test Data Input (JTAG).** Provides serial data for the boundary scan logic.
TDO	O /T	High-Z	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
TMS	I (ipu)		**Test Mode Select (JTAG).** Used to control the test state machine.
TCK	I		**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the device.
$\overline{\text{TRST}}$	I (ipu)		**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the processor.
$\overline{\text{EMU}}$	O/T (ipu)	High-Z	**Emulation Status.** Must be connected to the ADSP-2146x Analog Devices DSP Tools product line of JTAG emulators target board connector only.
CLK_CFG_{1-0}	I		**Core to CLKIN Ratio Control.** These pins set the start up clock frequency. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset. The allowed values are: 00 = 6:1 01 = 32:1 10 = 16:1 11 = reserved
CLKIN	I		**Local Clock In.** Used in conjunction with XTAL. CLKIN is the clock input. It configures the processors to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the processors to use the external clock source such as an external clock oscillator. CLKIN may not be halted, changed, or operated below the specified frequency.
XTAL	O		**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to drive an external crystal.
$\overline{\text{RESET}}$	I		**Processor Reset.** Resets the processor to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
$\overline{\text{RESETOUT}}$/ $\overline{\text{RUNRSTIN}}$	I/O (ipu)		**Reset Out/Running Reset In.** The default setting on this pin is reset out. This pin also has a second function as RUNRSTIN which is enabled by setting bit 0 of the RUNRSTCTL register. For more information, see the *ADSP-2146x SHARC Processor Hardware Reference*.
BOOT_CFG_{2-0}	I		**Boot Configuration Select.** These pins select the boot mode for the processor. The BOOT_CFG pins must be valid before $\overline{\text{RESET}}$ (hardware and software) is de-asserted.

The following symbols appear in the Type column of Table 9: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26k–63k Ω. The range of an ipd resistor can be between 31k–85k Ω.
In this table, the DDR2 pins are SSTL18 compliant. All other pins are LVTTL compliant.

[1] The MLB pins are only available on the AD21462W/AD21465W and AD21469W processors. These pins are NC (no connect) on the ADSP-21467 and ADSP-21469 processors. For more information, see CSP_BGA Ball Assignment – ADSP-21462W/ADSP-21465W/ADSP-21469W on Page 61, and CSP_BGA Ball Assignment - ADSP-21467/ADSP-21469 on Page 64.

Table 10. Pin List, Power and Ground

Name	Type	Description
V_{DD_INT}	P	Internal Power
V_{DD_EXT}	P	External Power
V_{DD_A}	P	Analog Power for PLL
V_{DD_THD}	P	Thermal Diode Power
V_{DD_DDR2}[1]	P	DDR2 Interface Power
V_{REF}		DDR2 Input Voltage Reference
GND	G	Ground
AGND	G	Analog Ground

[1] Applies to DDR2 signals.

SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	450 MHz		400 MHz		Unit
		Min	Max	Min	Max	
V_{DD_INT}	Internal (Core) Supply Voltage	1.05	1.15	TBD[2]	TBD[2]	V
V_{DD_EXT}	External (I/O) Supply Voltage	3.13	3.47	3.13	3.47	V
V_{DD_A}[3]	Analog Power Supply Voltage	1.05	1.15	TBD[2]	TBD[2]	V
V_{DD_DDR2}[4, 5]	DDR2 Controller Supply Voltage	1.7	1.9	1.7	1.9	V
V_{DD_THD}	Thermal Diode Supply Voltage	3.13	3.47	3.13	3.47	V
V_{REF}	DDR2 Reference Voltage	0.84	0.96	0.84	0.96	V
V_{IH}[6]	High Level Input Voltage @ V_{DD_EXT} = Max	2.0	V_{DD_EXT} + 0.5	2.0	V_{DD_EXT} + 0.5	V
V_{IL}[6]	Low Level Input Voltage @ V_{DD_EXT} = Min	–0.3	0.8	–0.3	0.8	V
V_{IH_CLKIN}[7]	High Level Input Voltage @ V_{DD_EXT} = Max	2.0	V_{DD_EXT} + 0.5	2.0	V_{DD_EXT} + 0.5	V
V_{IL_CLKIN}[7]	Low Level Input Voltage @ V_{DD_EXT} = Min	–0.5	1.32	–0.5	1.32	V
V_{IL_DDR2} (DC)	DC Low Level Input Voltage	-0.3	V_{REF} – 0.12	-0.3	V_{REF} – 0.12	V
V_{IH_DDR2} (DC)	DC High Level Input Voltage	V_{REF} + 0.13	V_{DD_DDR2} + 0.3	V_{REF} + 0.13	V_{DD_DDR2} + 0.3	V
V_{IL_DDR2} (AC)	AC Low Level Input Voltage		V_{REF} – 250		V_{REF} – 250	mV
V_{IH_DDR2} (AC)	AC High Level Input Voltage	V_{REF} + 250		V_{REF} + 250		mV
T_J	Junction Temperature 324-Lead CSP_BGA @ $T_{AMBIENT}$ 0°C to +70°C	0	125	0	TBD	°C
T_J	Junction Temperature 324-Lead CSP_BGA @ $T_{AMBIENT}$ –40°C to +85°C	N/A	N/A	–40	TBD	°C

[1] Specifications subject to change without notice.
[2] The expected nominal value is 1.05 V and initial customer designs should design with a programmable regulator that can be adjusted from 0.95 V to 1.15 V +/-50mV
[3] See Figure 3 on page 12 for an example filter circuit.
[4] Applies to DDR2 signals.
[5] If unused, see Unused DDR2 Pins on Page 14.
[6] Applies to input and bidirectional pins: AMI_ADDR23–0, AMI_DATA7–0, FLAG3–0, DAI_Px, DPI_Px, $\overline{SPIDS}$, BOOTCFGx, CLKCFGx, ($\overline{RUNRSTIN}$), $\overline{RESET}$, TCK, TMS, TDI, $\overline{TRST}$.
[7] Applies to input pin CLKIN.

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	450 MHz			400 MHz			Unit
			Min	Typical	Max	Min	Typical	Max	
V_{OH}[2]	High Level Output Voltage	@ V_{DD_EXT} = Min, I_{OH} = –1.0 mA[3]	2.4			2.4			V
V_{OL}[2]	Low Level Output Voltage	@ V_{DD_EXT} = Min, I_{OL} = 1.0 mA[3]			0.4			0.4	V
V_{OH_DDR2}	High Level Output Voltage for DDR2	@ V_{DD_DDR} = Min, IOH = –13.4 mA	1.4			1.4			V
V_{OL_DDR2}	Low Level Output Voltage for DDR2	@ V_{DD_DDR} = Min, IOL = 13.4 mA			0.29			0.29	V
I_{IH}[4, 5]	High Level Input Current	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max			10			10	µA
I_{IL}[4]	Low Level Input Current	@ V_{DD_EXT} = Max, V_{IN} = 0 V			10			10	µA
I_{ILPU}[5]	Low Level Input Current Pull-up	@ V_{DD_EXT} = Max, V_{IN} = 0 V			200			200	µA
I_{IHPD}[6]	High Level Input Current Pull-down	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max			200			200	µA
I_{OZH}[7, 8]	Three-State Leakage Current	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max			10			10	µA
I_{OZL}[7]	Three-State Leakage Current	@ V_{DD_EXT} = Max, V_{IN} = 0 V			10			10	µA
I_{OZLPU}[8]	Three-State Leakage Current Pull-up	@ V_{DD_EXT} = Max, V_{IN} = 0 V			200			200	µA
I_{OZLPD}[9]	Three-State Leakage Current Pull-down	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max			200			200	µA
$I_{DD\text{-}INTYP}$[10, 11]	Supply Current (Internal)	TBD			TBD			TBD	mA
C_{IN}[12, 13]	Input Capacitance	TBD			TBD			TBD	pF

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins: AMI_ADDR23-0, AMI_DATA7-0, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, FLAG3–0, DAI_Px, DPI_Px, $\overline{\text{EMU}}$, TDO.
[3] See Output Drive Currents on Page 59 for typical drive current capabilities.
[4] Applies to input pins: BOOTCFGx, CLKCFGx, TCK, $\overline{\text{RESET}}$, CLKIN.
[5] Applies to input pins with internal pull-ups: $\overline{\text{TRST}}$, TMS, TDI.
[6] Applies to input pins with internal pull-downs: MLBCLK
[7] Applies to three-statable pins: all DDR2 pins.
[8] Applies to three-statable pins with pull-ups: DAI_Px, DPI_Px, $\overline{\text{EMU}}$.
[9] Applies to three-statable pins with pull-downs: MLBCLK, MLBDAT, MLBSIG, MLBDO, MLBSO, LDAT07-0, LDAT17-0, LCLK0, LCLK1, LACK0, LACK1.
[10] Typical internal current data reflects nominal operating conditions.
[11] See Engineer-to-Engineer Note “Estimating Power Dissipation for ADSP-2146x SHARC Processors” for further information.
[12] Applies to all signal pins.
[13] Guaranteed, but not tested.

PACKAGE INFORMATION

The information presented in Figure 4 provides details about the package branding for the ADSP-2146x processors. For a complete listing of product availability, see Ordering Guide on Page 68.

Figure 4. Typical Package Brand

Table 11. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Option
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

POWER DISSIPATION

See Table 12 and Engineer-to-Engineer Note "Estimating Power Dissipation for ADSP-2146x SHARC Processors" for detailed thermal and power information regarding maximum power dissipation. For information on package thermal specifications, see Thermal Characteristics on Page 60.

Table 12. Power Dissipation

Parameter	Min	Typ	Max	Unit
Typical activity at 1.0 V, T_J = 125°C		682		mW

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 13 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 13. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DD_INT})	–0.3 V to +1.32 V
Analog (PLL) Supply Voltage (V_{DD_A})	–0.3 V to +1.15 V
External (I/O) Supply Voltage (V_{DD_EXT})	–0.3 V to +4.6 V
Thermal Diode Supply Voltage (V_{DD_THD})	–0.3 V to +4.6 V
DDR2 Controller Supply Voltage (V_{DD_DDR2})	–0.3 V to +2.7 V
DDR2 Input Voltage	–0.5 V to +2.7 V
Input Voltage	–0.5 V to +3.8 V
Output Voltage Swing	–0.5 V to V_{DD_EXT} +0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C
Junction Temperature under Bias	125°C

TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. See Figure 46 on page 59 under Test Conditions for voltage reference levels.

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Core Clock Requirements

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, and serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 pins.

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL, see Figure 5). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

Voltage Controlled Oscillator

In application designs, the PLL multiplier value should be selected in such a way that the VCO frequency never exceeds f_{VCO} specified in Table 16.

- The product of CLKIN and PLLM must never exceed 1/2 of f_{VCO} (max) in Table 16 if the input divider is not enabled (INDIV = 0).
- The product of CLKIN and PLLM must never exceed f_{VCO} (max) in Table 16 if the input divider is enabled (INDIV = 1).

The VCO frequency is calculated as follows:

$f_{VCO} = 2 \times PLLM \times f_{INPUT}$
$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div (PLLD)$

where:

f_{VCO} = VCO output

PLLM = Multiplier value programmed in the PMCTL register. During reset, the PLLM value is derived from the ratio selected using the CLK_CFG pins in hardware.

PLLD = Divider value 2, 4, 8, or 16 based on the PLLD value programmed on the PMCTL register. During reset this value is 2.

f_{INPUT} = is the input frequency to the PLL.

f_{INPUT} = CLKIN when the input divider is disabled or

f_{INPUT} = CLKIN ÷ 2 when the input divider is enabled

Note the definitions of the clock periods that are a function of CLKIN and the appropriate ratio control shown in and Table 14. All of the timing specifications for the ADSP-2146x peripherals are defined in relation to t_{PCLK}. See the peripheral specific section for each peripheral's timing information.

Table 14. Clock Periods

Timing Requirements	Description
t_{CK}	CLKIN Clock Period
t_{CCLK}	Processor Core Clock Period
t_{PCLK}	Peripheral Clock Period = 2 × t_{CCLK}

Figure 5 shows core to CLKIN relationships with external oscillator or crystal. The shaded divider/multiplier blocks denote where clock ratios can be set through hardware or software using the power management control register (PMCTL). For more information, see the *ADSP-2146x SHARC Processor Hardware Reference*.

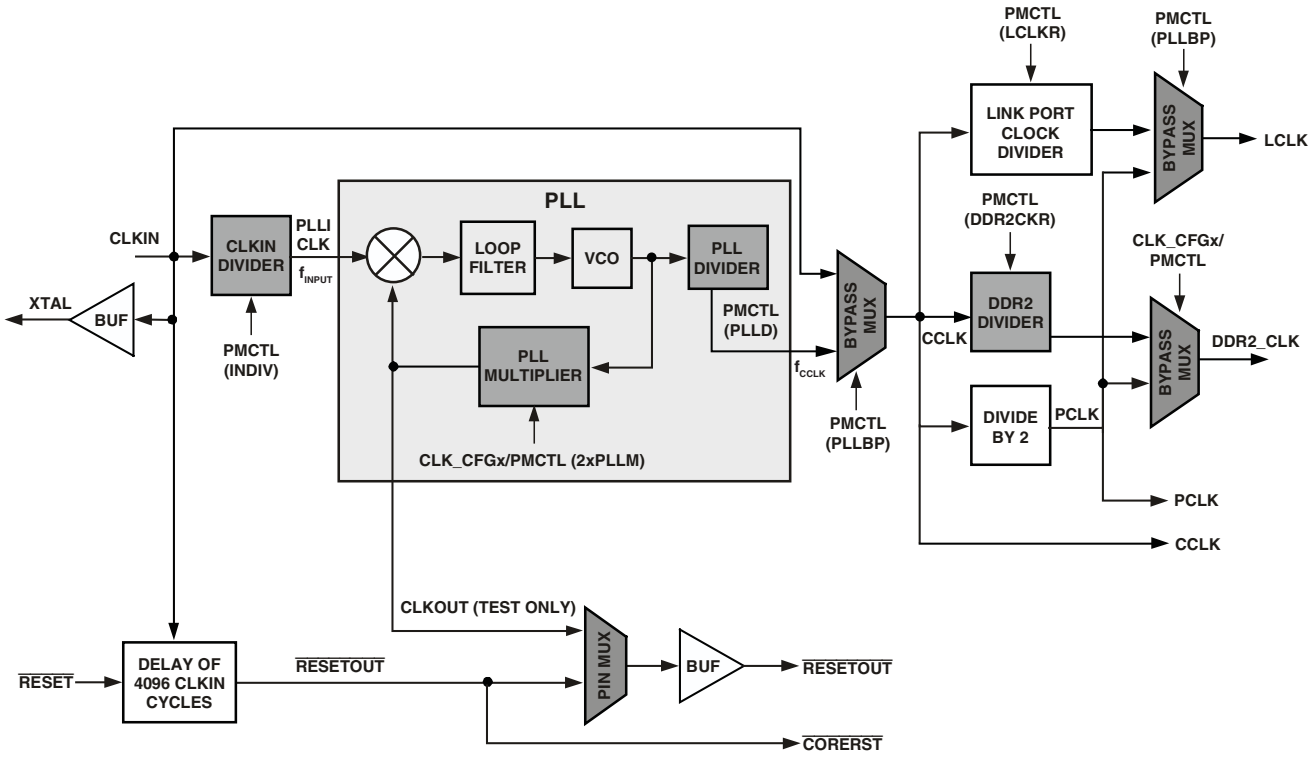


Figure 5. Core Clock and System Clock Relationship to CLKIN

Power-Up Sequencing

The timing requirements for processor startup are given in Table 15. While no specific power-up sequencing is required between V_{DD_EXT}, V_{DD_DDR2}, and V_{DD_INT}, there are some considerations that the system designs should take into account.

- No power supply should be powered up for an extended period of time (> 200 ms) before another supply starts to ramp up.
- If V_{DD_INT} power supply comes up after V_{DD_EXT}, any pin, such as $\overline{\text{RESETOUT}}$ and $\overline{\text{RESET}}$ may actually drive momentarily until the V_{DD_INT} rail has powered up. Systems sharing these signals on the board must determine if there are any issues that need to be addressed based on this behavior.

Note that during power-up, when the V_{DD_INT} power supply comes up after V_{DD_EXT}, a leakage current of the order of three-state leakage current pull-up, pull-down, may be observed on any pin, even if that is an input only (for example the $\overline{\text{RESET}}$ pin) until the V_{DD_INT} rail has powered up.

Table 15. Power Up Sequencing Timing Requirements (Processor Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DD_INT} or V_{DD_EXT} or V_{DD_DDR2} On	0		ms
$t_{IVDD-EVDD}$	V_{DD_INT} on Before V_{DD_EXT}	–200	+200	ms
$t_{EVDD_DDR2VDD}$	V_{DD_EXT} on Before V_{DD_DDR2}	–200	+200	ms
t_{CLKVDD} [1]	CLKIN Valid After V_{DD_INT} or V_{DD_EXT} or V_{DD_DDR2} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10[2]		ms
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20[3]		ms
Switching Characteristic				
$t_{CORERST}$	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096 \times t_{CK} + 2 \times t_{CCLK}$ [4, 5]		ms

[1] Valid V_{DD_INT} assumes that the supply is fully ramped to its nominal value. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to your crystal oscillator manufacturer's datasheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Based on CLKIN cycles.

[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of four CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[5] The 4096 cycle count depends on t_{SRST} specification in Table 17. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

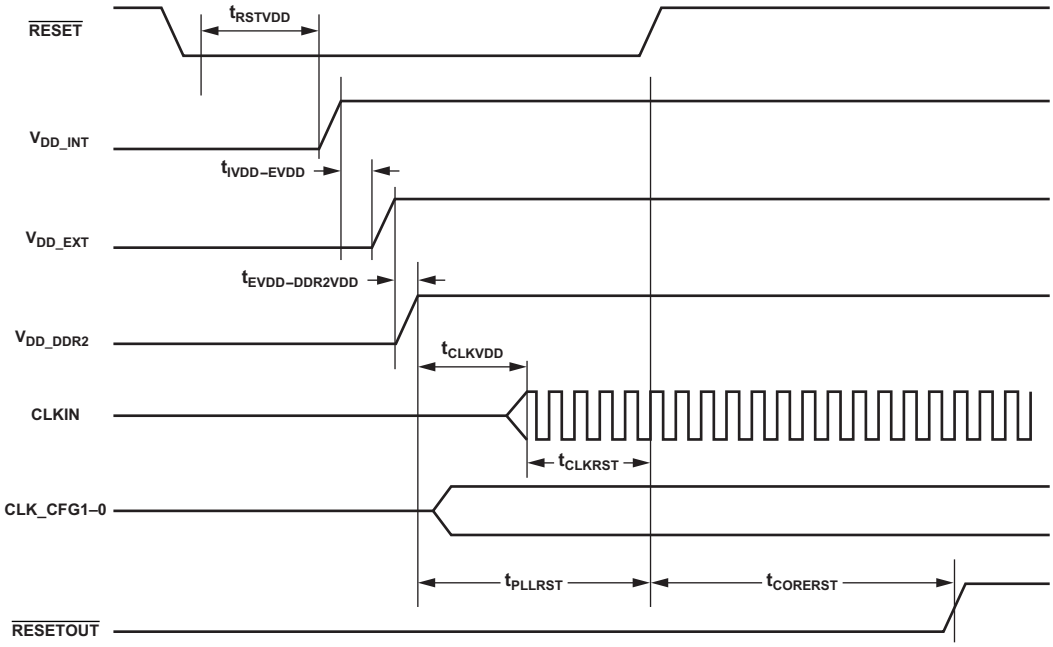


Figure 6. Power-Up Sequencing

Clock Input

Table 16. Clock Input

Parameter		400 MHz[1] Min	400 MHz[1] Max	Unit
Timing Requirements				
t_{CK}	CLKIN Period	15[2]	100	ns
t_{CKL}	CLKIN Width Low	7.5[1]	45	ns
t_{CKH}	CLKIN Width High	7.5[1]	45	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3	ns
t_{CCLK}[3]	CCLK Period	2.5[6]	10	ns
f_{VCO}[4]	VCO Frequency	200	2000 ÷ t_{CCLK}	MHz
t_{CKJ}[5, 6]	CLKIN Jitter Tolerance	–250	+250	ps

[1] Applies to all 400 MHz models. See Ordering Guide on Page 68.
[2] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in PMCTL.
[3] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.
[4] See Figure 5 on page 22 for VCO diagram.
[5] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[6] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

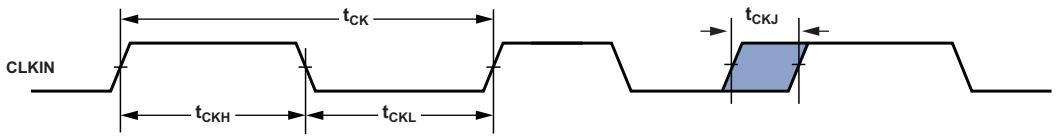
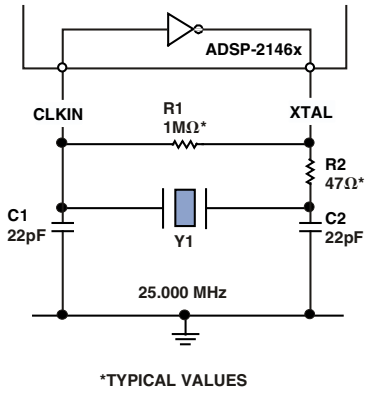


Figure 7. Clock Input

Clock Signals

The ADSP-2146x can use an external clock or a crystal. See the CLKIN pin description in Table 9. Programs can configure the processor to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 8 shows the component connections used for a crystal operating in fundamental mode. Note that the clock rate is achieved using a 25.000 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 400 MHz).

To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register. In case of the ADSP-21462W, ADSP-21465W, and ADSP-21469W, the maximum clock speed of 400 MHz is arrived at by using a 25 MHz crystal with the default multiplier of 16:1.



R2 SHOULD BE CHOSEN TO LIMIT CRYSTAL DRIVE POWER. REFER TO CRYSTAL MANUFACTURER'S SPECIFICATIONS

Figure 8. 450 MHz Operation (Fundamental Mode Crystal)

Reset

Table 17. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}[1]	$\overline{\text{RESET}}$ Pulse Width Low	$4 \times t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 ms while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

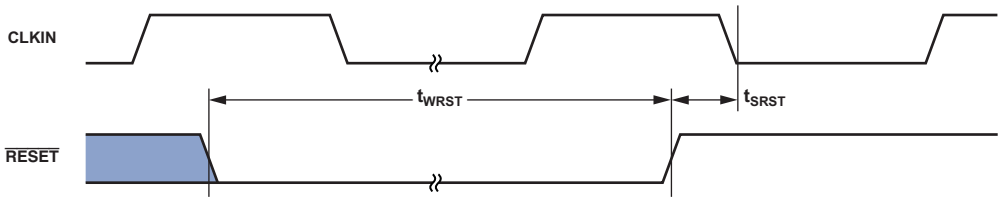


Figure 9. Reset

Running Reset

The following timing specification applies to $\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$ pin when it is configured as $\overline{\text{RUNRSTIN}}$.

Table 18. Running Reset

Parameter		Min	Max	Unit
Timing Requirements				
$t_{WRUNRST}$	Running $\overline{\text{RESET}}$ Pulse Width Low	$4 \times t_{CK}$		ns
$t_{SRUNRST}$	Running $\overline{\text{RESET}}$ Setup Before CLKIN High	8		ns

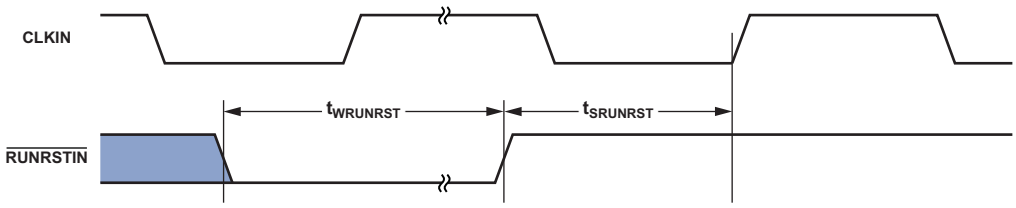


Figure 10. Running Reset

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts as well as the DAI_P20–1 and DPI_P14–1 pins when they are configured as interrupts.

Table 19. Interrupts

Parameter		Min	Max	Unit
Timing Requirement				
t_{IPW}	$\overline{\text{IRQx}}$ Pulse Width	$2 \times t_{PCLK} + 2$		ns

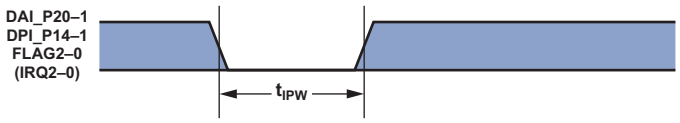


Figure 11. Interrupts

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP).

Table 20. Core Timer

Parameter		Min	Max	Unit
Switching Characteristic				
t_{WCTIM}	TMREXP Pulse Width	$4 \times t_{PCLK} - 1$		ns

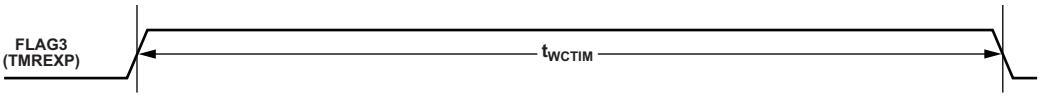


Figure 12. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to Timer0 and Timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 21. Timer PWM_OUT Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{PCLK} - 1.2$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

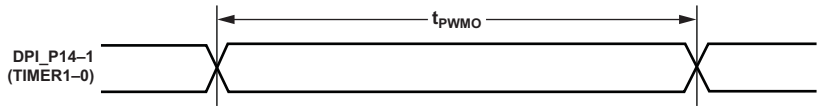


Figure 13. Timer PWM_OUT Timing

Timer WDTH_CAP Timing

The following timing specification applies to timer0 and timer1, and in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the SRU. Therefore, the timing specification provided below is valid at the DPI_P14–1 pins.

Table 22. Timer Width Capture Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{PWI}	Timer Pulse Width	$2 \times t_{PCLK}$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

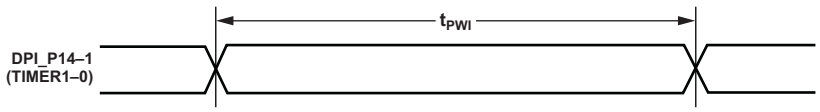


Figure 14. Timer Width Capture Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example DAI_PB01_I to DAI_PB02_O).

Table 23. DAI and DPI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI/DPI Pin Input Valid to DAI/DPI Output Valid	1.5	12	ns

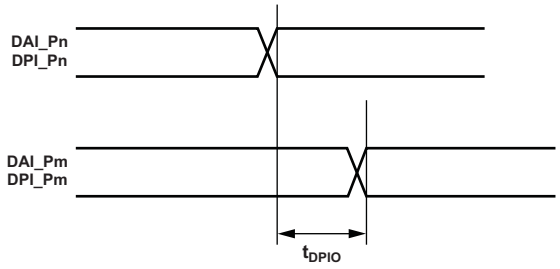


Figure 15. DAI and DPI Pin to Pin Direct Routing

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 – DAI_P20).

Table 24. Precision Clock Generator (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIW}	Input Clock Period	$t_{PCLK} \times 4$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$10 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$10 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOW}[1]	Output Clock Period	$2 \times t_{PCGIP} - 1$		ns

D = FSxDIV, PH = FSxPHASE. For more information, see the ADSP-2146x SHARC Processor Hardware Reference, "Precision Clock Generators" chapter.

[1] Normal mode of operation.

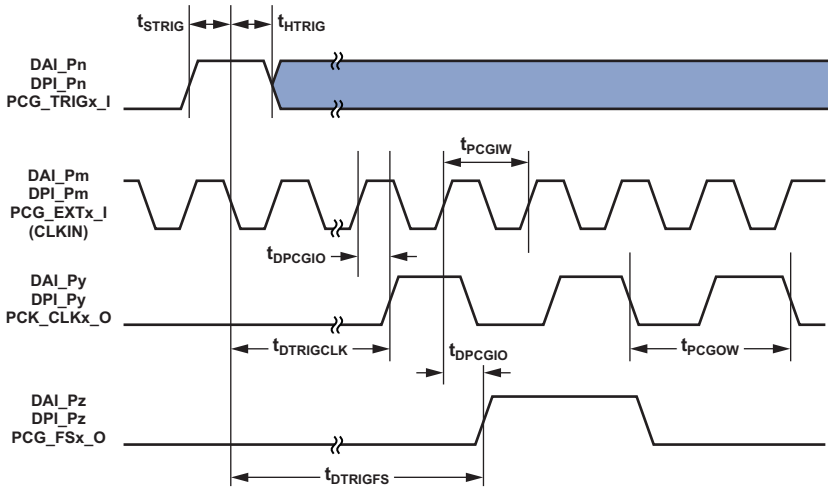


Figure 16. Precision Clock Generator (Direct Pin Routing)

Flags

The timing specifications provided below apply to AMI_ADDR23–0 and AMI_DATA7–0 when configured as FLAGS. See Table 9 on page 14 for more information on flag use.

Table 25. Flags

Parameter		Min	Max	Unit
Timing Requirement				
t_{FIPW}	DPI_P14–1, AMI_ADDR23–0, AMI_DATA7–0, FLAG3–0 IN Pulse Width	$2 \times t_{PCLK} + 3$		ns
switching characteristic				
t_{FOPW}	DPI_P14–1, AMI_ADDR23–0, AMI_DATA7–0, FLAG3–0 OUT Pulse Width	$2 \times t_{PCLK} - 1.5$		ns

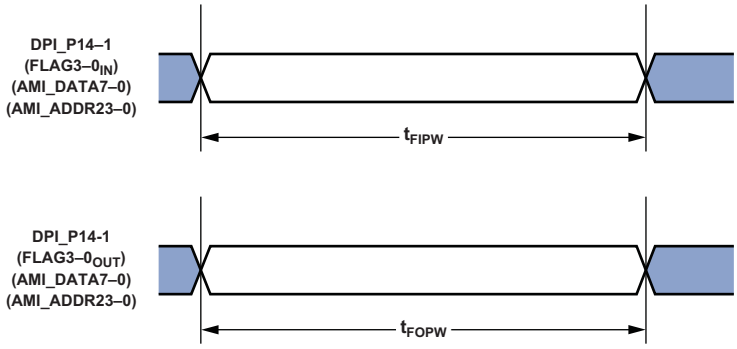


Figure 17. Flags

DDR2 SDRAM Read Cycle Timing

Table 26. DDR2 SDRAM Read Cycle Timing, $V_{DD\text{-}DDR2}$ nominal 1.8V

Parameter		Min	Max	Unit
Timing Requirements				
t_{AC}	DQ Output Access Time From CK/$\overline{CK}$	–1.0	0.7	ns
t_{DQSCK}	DQS Output Access Time From CK/$\overline{CK}$	–1.0	0.7	ns
t_{DQSQ}	DQS-DQ Skew for DQS and Associated DQ Signals		0.450	ns
t_{QH}	DQ, DQS Output Hold Time From DQS	1.5		ns
t_{RPRE}	Read Preamble	0.25		t_{CK}
t_{RPST}	Read Postamble	0.25		t_{CK}
Switching Characteristics				
t_{CK}	Clock Cycle Time, CL= x	5		ns
t_{CH}	Minimum Clock Pulse Width	2.35	2.65	ns
t_{CL}	Maximum Clock Pulse Width	2.35	2.65	ns
t_{AS}	Address Setup Time	2.6		ns
t_{AH}	Address Hold Time	1.0		ns

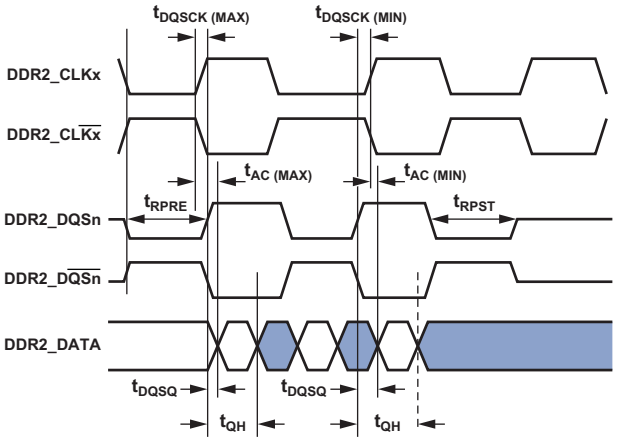


Figure 18. DDR2 SDRAM Controller Input AC Timing

DDR2 SDRAM Write Cycle Timing

Table 27. DDR2 SDRAM Read Cycle Timing, $V_{DD-DDR2}$ nominal 1.8V

Parameter		Min	Max	Unit
Switching Characteristics				
t_{CK}	Clock Cycle Time	5		ns
t_{CH}	Minimum Clock Pulse Width	2.35	2.65	ns
t_{CL}	Maximum Clock Pulse Width	2.35	2.65	ns
t_{DQSS}[1]	DQS Latching Rising Transitions to Associated Clock Edges	0	0.20	ns
t_{DS}	Last Data Valid to DQS Delay	1.0		ns
t_{DH}	DQS to First Data Invalid Delay	0.95		ns
t_{DSS}	DQS Falling Edge to Clock Setup Time	2.35		ns
t_{DSH}	DQS Falling Edge Hold Time From CK	2.60		ns
t_{DQSH}	DQS Input HIGH Pulse Width	0.48		t_{CK}
t_{DQSL}	DQS Input LOW Pulse Width	0.48		t_{CK}
t_{WPRE}	Write Preamble	0.8		t_{CK}
t_{WPST}	Write Postamble	0.5		t_{CK}
t_{AS}	Control/address Maximum Delay From DDCK Rise	2.6		ns
t_{AH}	Control/Address Minimum Delay From DDCK Rise	1.0		ns

[1] Write command to first DQS delay = WL × t_{CK} + t_{DQSS}.

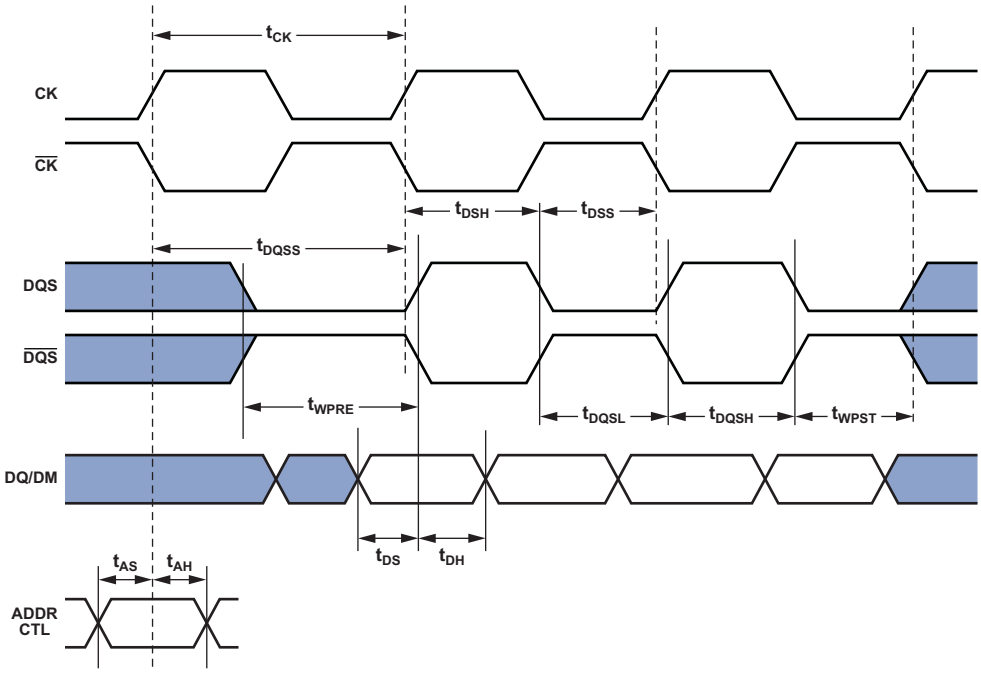


Figure 19. DDR2 SDRAM Controller Output AC Timing

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, AMI_DATA, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 28. Memory Read—Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}	Address, Selects Delay to Data Valid[1, 2]		W + t_{DDR2_CLK} – 5.12	ns
t_{DRLD}	$\overline{\text{AMI_RD}}$ Low to Data Valid[1]		W – 3.2	ns
t_{SDS}	Data Setup to $\overline{\text{AMI_RD}}$ High	2.5		ns
t_{HDRH}	Data Hold from $\overline{\text{AMI_RD}}$ High[3, 4]	0		ns
t_{DAAK}	AMI_ACK Delay from Address, Selects[2, 5]		t_{DDR2_CLK} – 9.5 + W	ns
t_{DSAK}	AMI_ACK Delay from $\overline{\text{AMI_RD}}$ Low[4]		W – 7.0	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{\text{AMI_RD}}$ High	RH + 0.20		ns
t_{DARL}	Address Selects to $\overline{\text{AMI_RD}}$ Low[2]	t_{DDR2_CLK} – 3.3		ns
t_{RW}	$\overline{\text{AMI_RD}}$ Pulse Width	W – 1.4		ns
t_{RWR}[6]	$\overline{\text{AMI_RD}}$ High to $\overline{\text{AMI_RD}}$ Low	HI + t_{DDR2_CLK} – 0.8		ns

W = (number of wait states specified in AMICTLx register) × t_{DDR2_CLK}.
HI = RHC + IC (RHC = (number of Read Hold Cycles specified in AMICTLx register) x t_{DDR2_CLK}
IC = (number of idle cycles specified in AMICTLx register) x t_{DDR2_CLK}).
H = (number of hold cycles specified in AMICTLx register) x t_{DDR2_CLK}.

[1] Data delay/setup: System must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{\text{AMI_MS}}$x, is referenced.
[3] Note that timing for AMI_ACK, AMI_DATA, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, and strobe timing parameters only apply to asynchronous access mode.
[4] Data hold: User must meet t_{HDRH} in asynchronous access mode. See Test Conditions on Page 59 for the calculation of hold times given capacitive and dc loads.
[5] AMI_ACK delay/setup: User must meet t_{DAAK}, or t_{DSAK}, for deassertion of AMI_ACK (low). For asynchronous assertion of AMI_ACK (high) user must meet t_{DAAK} or t_{DSAK}.
[6] For Read to Read: Same bank = (1 + RHC) × DDR2CLK if IC is not programmed. For Read to Read: Different bank = t_{RWR}. For Read to Write: 5 DDR2CLK cycles + (IC – 4), at least 5 DDR2CLK cycles for both the same bank and different banks.

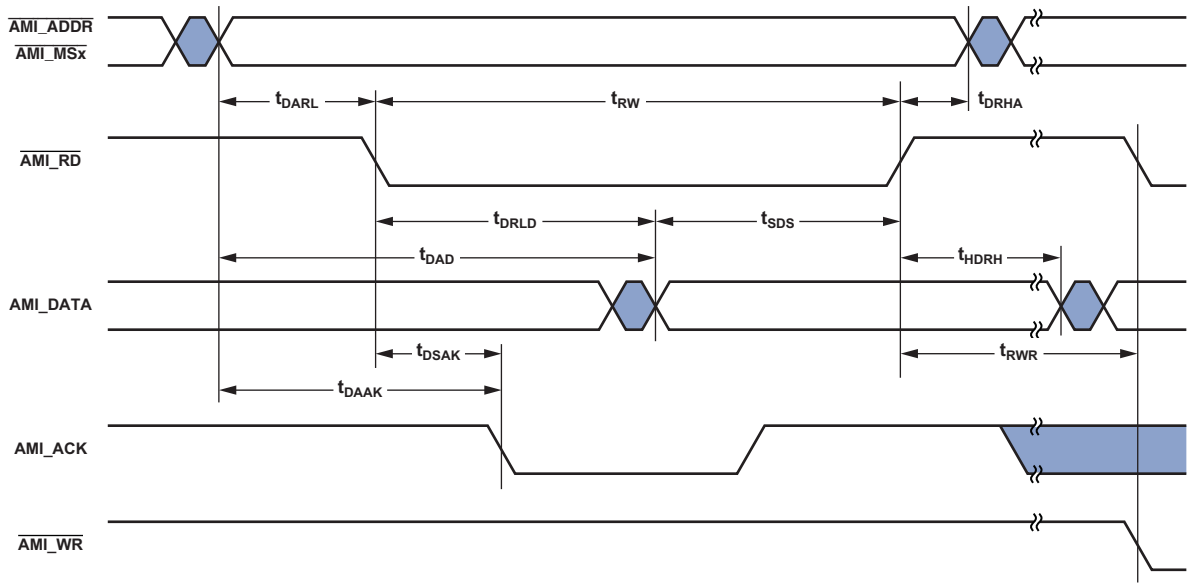


Figure 20. Memory Read—Bus Master

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, AMI_DATA, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 29. Memory Write—Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	AMI_ACK Delay from Address, Selects[1, 2]		t_{DDR2_CLK} – 9.7 + W	ns
t_{DSAK}	AMI_ACK Delay from $\overline{\text{AMI_WR}}$ Low [1, 3]		W – 4.9	ns
Switching Characteristics				
t_{DAWH}	Address, Selects to $\overline{\text{AMI_WR}}$ Deasserted[2]	t_{DDR2_CLK} – 3.1 + W		ns
t_{DAWL}	Address, Selects to $\overline{\text{AMI_WR}}$ Low[2]	t_{DDR2_CLK} – 2.7		ns
t_{WW}	$\overline{\text{AMI_WR}}$ Pulse Width	W – 1.3		ns
t_{DDWH}	Data Setup Before $\overline{\text{AMI_WR}}$ High	t_{DDR2_CLK} – 3.0 + W		ns
t_{DWHA}	Address Hold After $\overline{\text{AMI_WR}}$ Deasserted	H + 0.15		ns
t_{DWHD}	Data Hold After $\overline{\text{AMI_WR}}$ Deasserted	H + 0.02		ns
t_{DATRWH}	Data Disable After $\overline{\text{AMI_WR}}$ Deasserted[4]	t_{DDR2_CLK} – 1.37 + H	t_{DDR2_CLK} + 4.9 + H	ns
t_{WWR}	$\overline{\text{AMI_WR}}$ High to $\overline{\text{AMI_WR}}$ Low[5]	t_{DDR2_CLK} – 1.5 + H		ns
t_{DDWR}	Data Disable Before $\overline{\text{AMI_RD}}$ Low	$2t_{DDR2_CLK}$ – 4.11		ns
t_{WDE}	$\overline{\text{AMI_WR}}$ Low to Data Enabled	t_{DDR2_CLK} – 3.5		ns

W = (number of wait states specified in AMICTLx register) × t_{SDDR2_CLK} H = (number of hold cycles specified in AMICTLx register) x t_{DDR2_CLK}

[1] AMI_ACK delay/setup: System must meet t_{DAAK}, or t_{DSAK}, for deassertion of AMI_ACK (low). For asynchronous assertion of AMI_ACK (high) user must meet t_{DAAK} or t_{DSAK}.
[2] The falling edge of $\overline{\text{AMI_MSx}}$ is referenced.
[3] Note that timing for AMI_ACK, AMI_DATA, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, and strobe timing parameters only applies to asynchronous access mode.
[4] See Test Conditions on Page 59 for calculation of hold times given capacitive and dc loads.
[5] For Write to Write: 1 + HC, for both same bank and different bank. For Write to Read: 3 DDR2CLK cycles + HC , for the same bank and different banks.

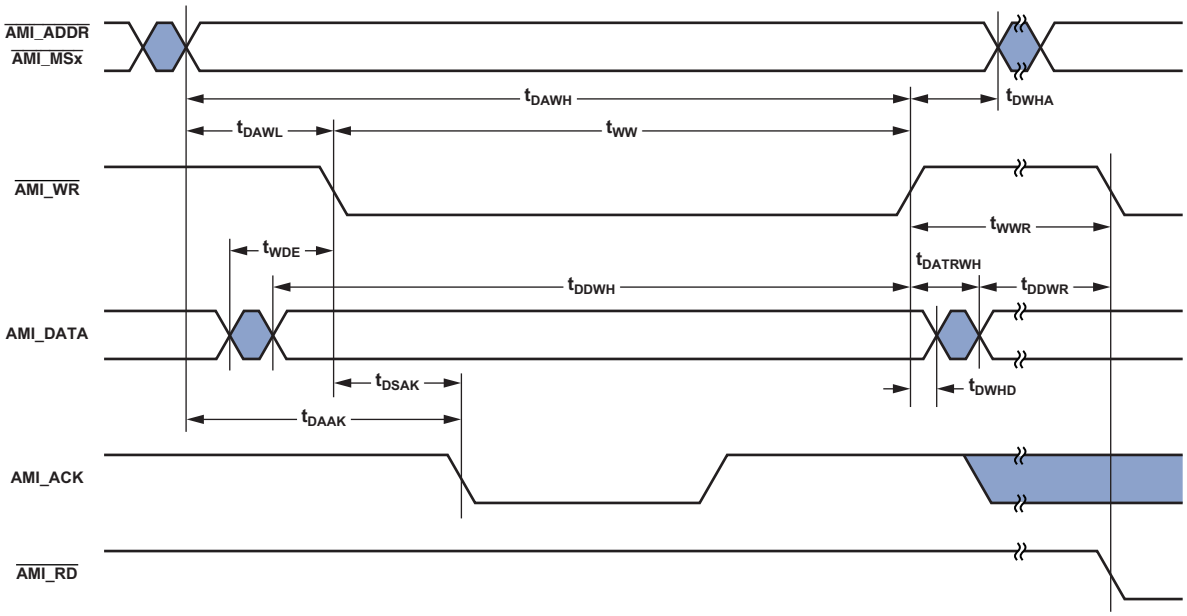


Figure 21. Memory Write—Bus Master

Link Ports

Calculation of link receiver data setup and hold relative to link clock is required to determine the maximum allowable skew that can be introduced in the transmission path between LDATA and LCLK. Setup skew is the maximum delay that can be introduced in LDATA relative to LCLK: (setup skew = $t_{LCLKTWH}$ min – t_{DLDCH} – t_{SLDCL}). Hold skew is the maximum delay that can be introduced in LCLK relative to LDATA, (hold skew = $t_{LCLKTWL}$ min – t_{HLDCH} – t_{HLDCL}). Calculations made directly from speed specifications will result in unrealistically small skew times because they include multiple tester guardbands. The setup and hold skew times shown below are calculated to include only one tester guardband.

Setup Skew = TBD ns max

Hold Skew = TBD ns max

Note that there is a two-cycle effect latency between the link port enable instruction and the link port actually being enabled by the processor.

Table 30. Link Ports – Receive

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLDCL}	Data Setup Before LCLK Low	0.5		ns
t_{HLDCL}	Data Hold After LCLK Low	1.5		ns
t_{LCLKIW}	LCLK Period	t_{LCLK} (6ns)		ns
$t_{LCLKRWL}$	LCLK Width Low	2.6		ns
$t_{LCLKRWH}$	LCLK Width High	2.6		ns
Switching Characteristics				
t_{DLALC}	LACK Low Delay After LCLK Low[1]	5	12	ns

[1] LACK goes low with t_{DLALC} relative to rise of LCLK after first byte, but does not go low if the receiver's link buffer is not about to fill.

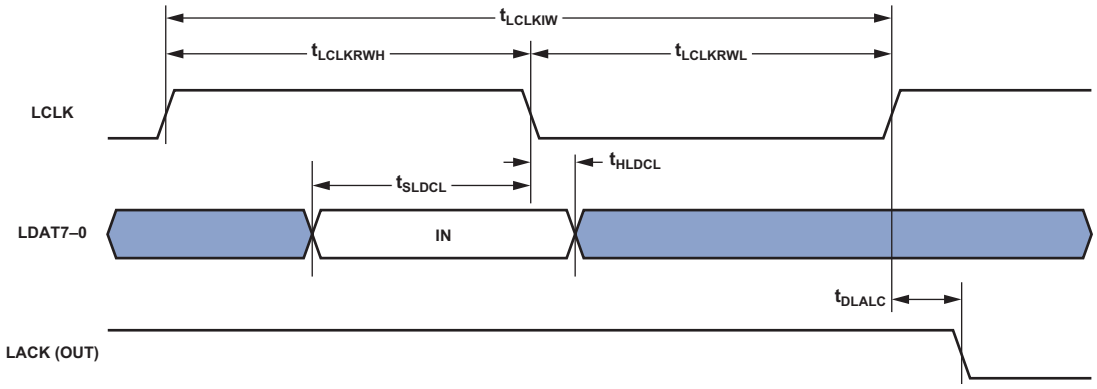


Figure 22. Link Ports—Receive

Table 31. Link Ports – Transmit

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLACH}	LACK Setup Before LCLK Low	8.5		ns
t_{HLACH}	LACK Hold After LCLK Low	–3		ns
Switching Characteristics				
t_{DLDCH}	Data Delay After LCLK High		1	ns
t_{HLDCH}	Data Hold After LCLK High	0		ns
$t_{LCLKTWL}$	LCLK Width Low	$0.5 \times t_{LCLK} - 0.1$	$0.6 \times t_{LCLK} + 0.1$[1]	ns
$t_{LCLKTWH}$	LCLK Width High	$0.4 \times t_{LCLK} - 0.1$[1]	$0.5 \times t_{LCLK} + 0.1$	ns
t_{DLACLK}	LCLK Low Delay After LACK High	4	$t_{LCLK} + 8$	ns

[1] For 1:2.5 ratio. For other ratios this specification is $0.5 \times t_{LCLK}$

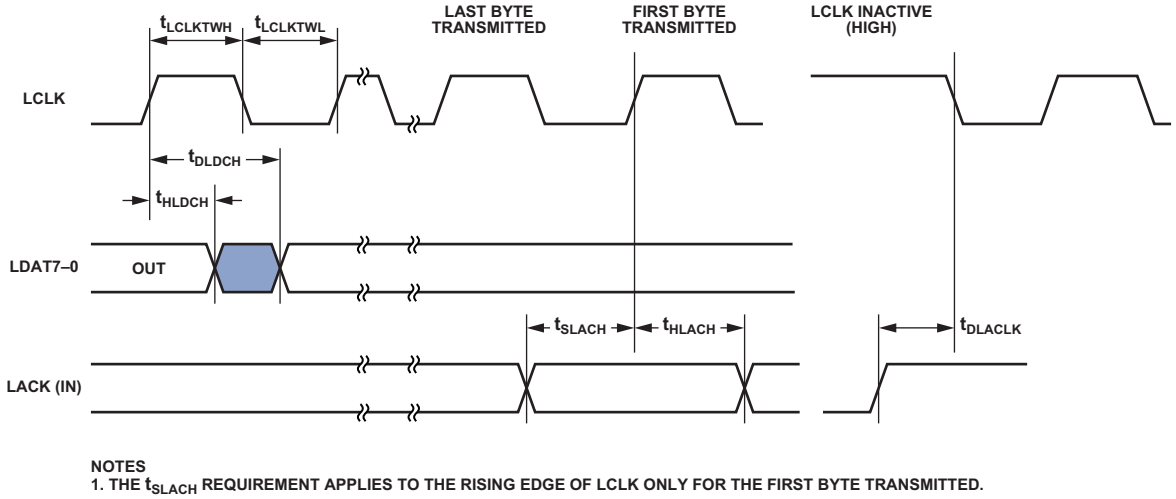


Figure 23. Link Ports—Transmit

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) Serial clock (SCLK) width.

Serial port signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 32. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		ns
t_{HFSE}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	1.9		ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5		ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 0.5$		ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{DFSE}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode)		10.25	ns
t_{HOFSE}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode)	2		ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		7.8	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 33. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	7		ns
t_{HFSI}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	7		ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5		ns
Switching Characteristics				
t_{DFSI}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)		4	ns
t_{HOFSI}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)	–1.0		ns
t_{DFSIR}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)		9.75	ns
t_{HOFSIR}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)	–1.0		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		3.25	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.0		ns
t_{SCKLIW}	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

Table 34. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}[1]	Data Enable from External Transmit SCLK	2		ns
t_{DDTTE}[1]	Data Disable from External Transmit SCLK		10	ns
t_{DDTIN}[1]	Data Enable from Internal Transmit SCLK	–1		ns

[1] Referenced to drive edge.

Table 35. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit Frame Sync or External Receive Frame Sync with MCE = 1, MFD = 0		7.75	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified as well as DSP serial mode, and MCE = 1, MFD = 0.

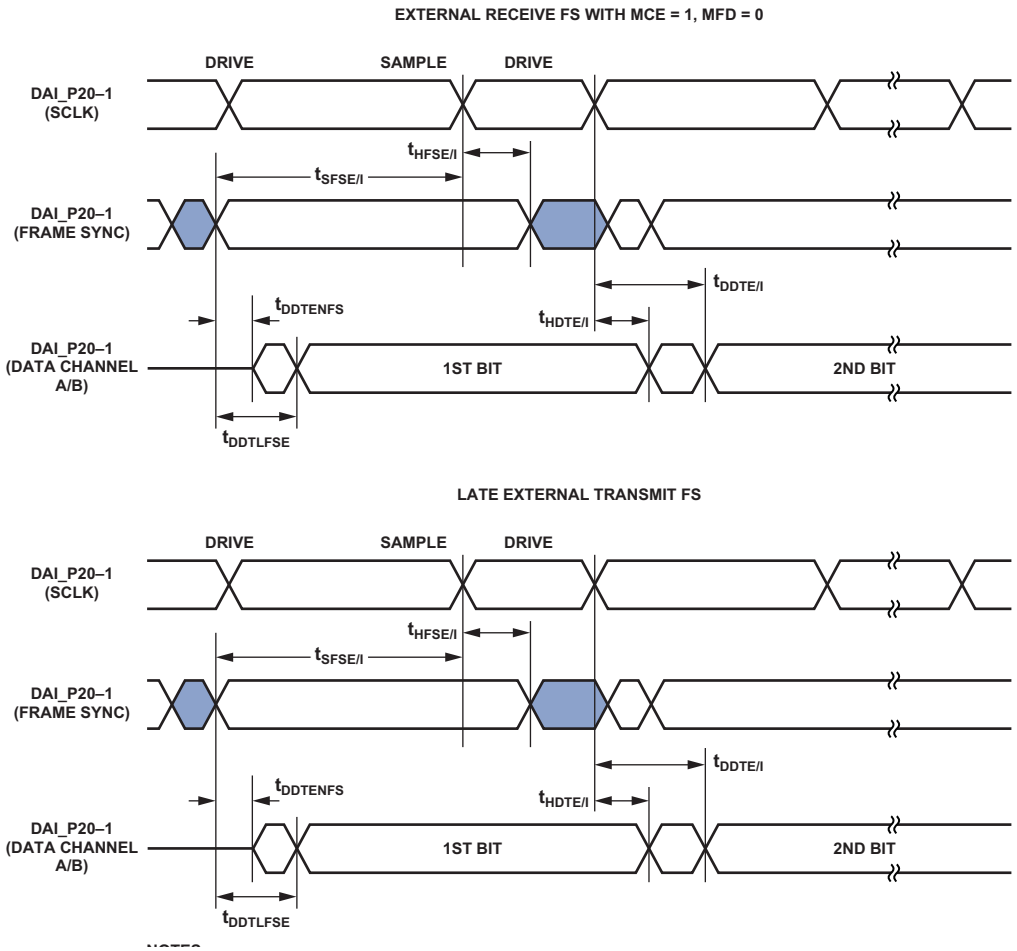
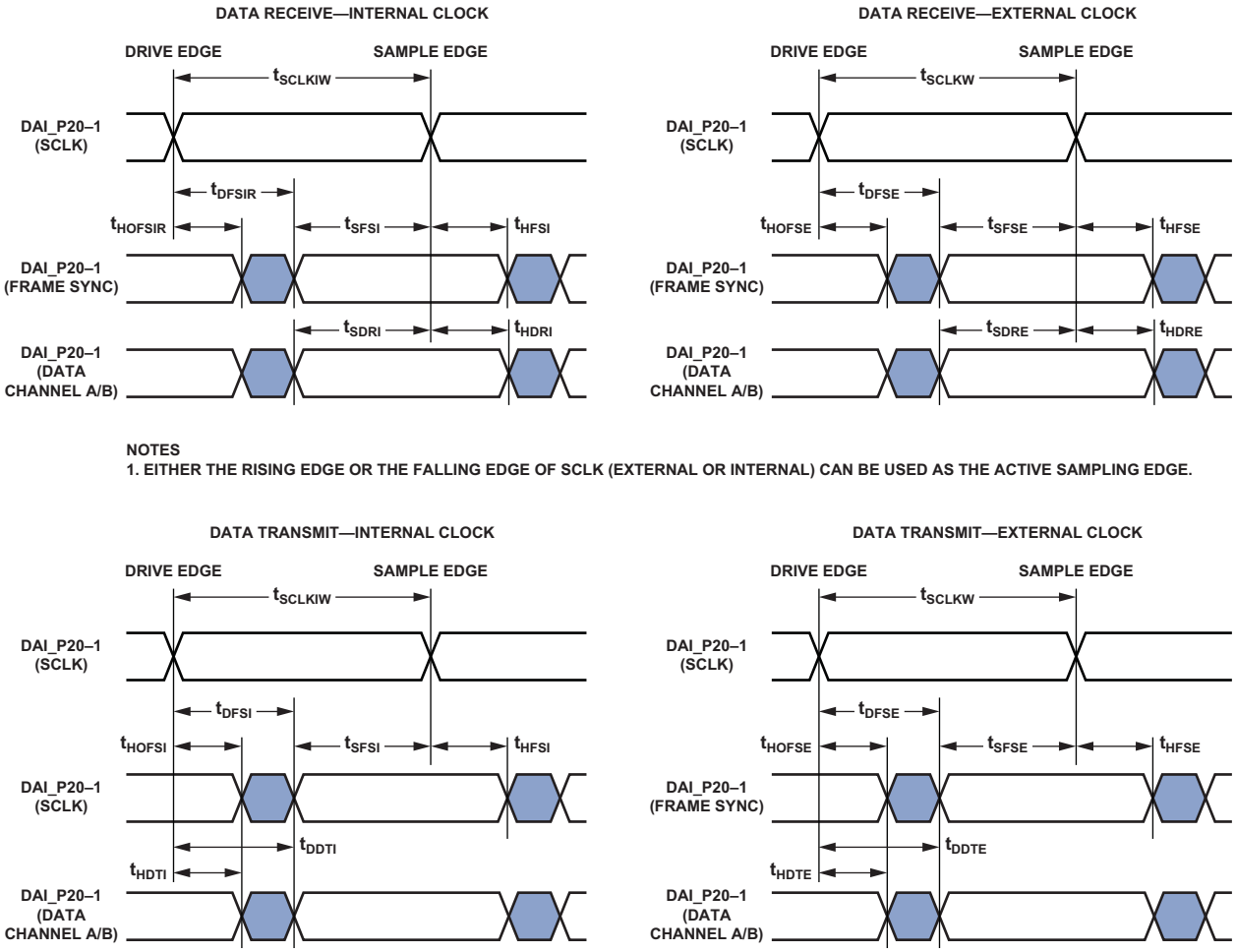


Figure 24. External Late Frame Sync[1]

[1] This figure reflects changes made to support left-justified mode.



NOTES
1. EITHER THE RISING EDGE OR THE FALLING EDGE OF SCLK (EXTERNAL OR INTERNAL) CAN BE USED AS THE ACTIVE SAMPLING EDGE.

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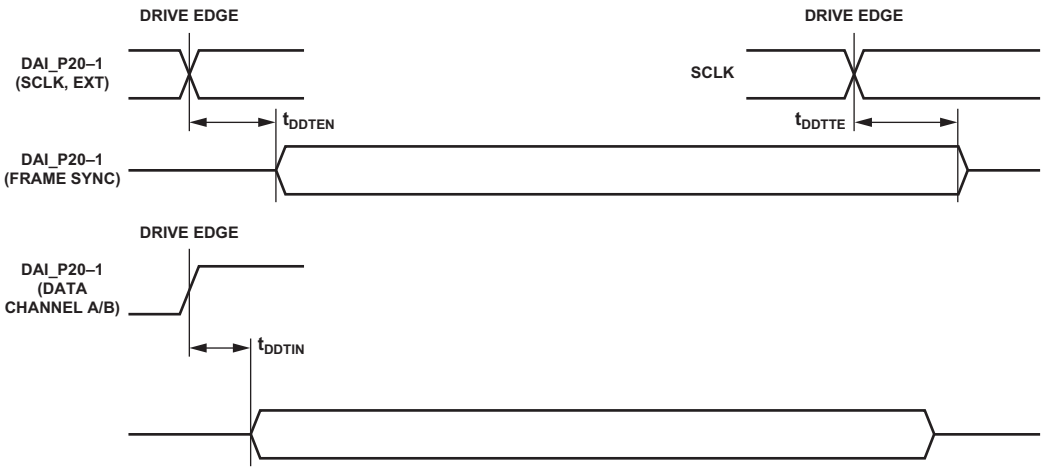


Figure 25. Serial Ports

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 36. IDP signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 36. Input Data Port (IDP)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	2.5		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	2.5		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	2.5		ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] The serial clock, data and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

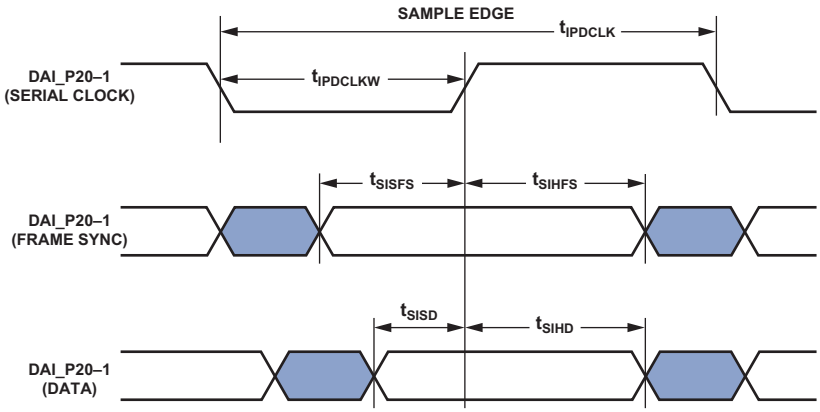


Figure 26. IDP Master Timing

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 37. PDAP is the parallel mode operation of channel 0 of the IDP. For details on the operation of the PDAP, see the PDAP chapter of the *ADSP-2146x SHARC Processor Hardware Reference*. Note that the 20-bits of external PDAP data can be provided through the AMI_ADDR23–4 pins or over the DAI pins.

Table 37. Parallel Data Acquisition Port (PDAP)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPHOLD}[1]	PDAP_HOLD Setup Before PDAP_CLK Sample Edge	2.5		ns
t_{HPHOLD}[1]	PDAP_HOLD Hold After PDAP_CLK Sample Edge	2.5		ns
t_{PDSD}[1]	PDAP_DAT Setup Before Serial Clock PDAP_CLK Sample Edge	3.85		ns
t_{PDHD}[1]	PDAP_DAT Hold After Serial Clock PDAP_CLK Sample Edge	2.5		ns
t_{PDCLKW}	Clock Width	$(t_{PCLK} \times 4) \div 2 - 3$		ns
t_{PDCLK}	Clock Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} + 3$		ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1$		ns

[1] Data source pins are AMI_ADDR23–4 or DAI pins. Source pins for serial clock and frame sync are: 1) AMI_ADDR3–2 pins, 2) DAI pins.

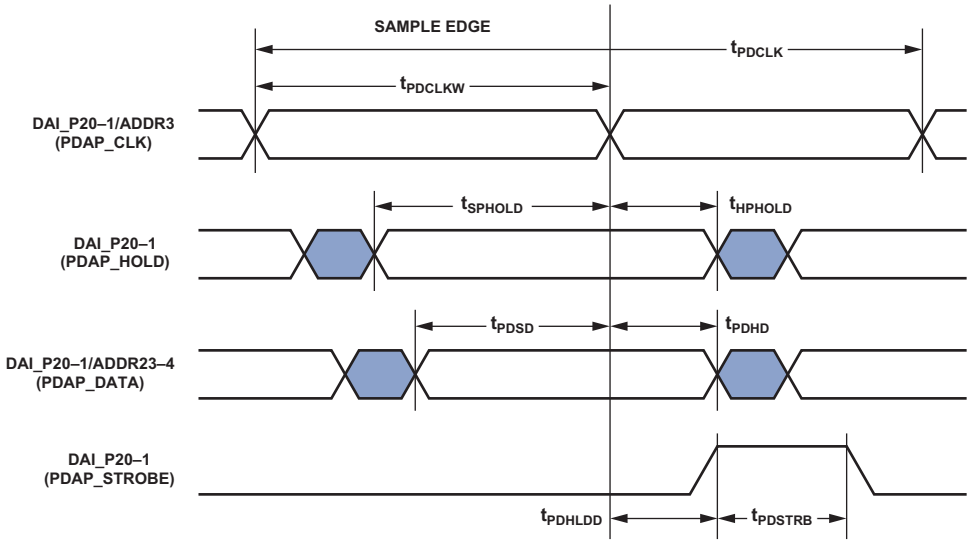


Figure 27. PDAP Timing

Sample Rate Converter—Serial Input Port

The ASRC input signals are routed from the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided in Table 38 are valid at the DAI_P20–1 pins.

Table 38. ASRC, Serial Input Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	5.5		ns
t_{SRCSD}[1]	Data Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHD}[1]	Data Hold After Serial Clock Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] The serial clock, data and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

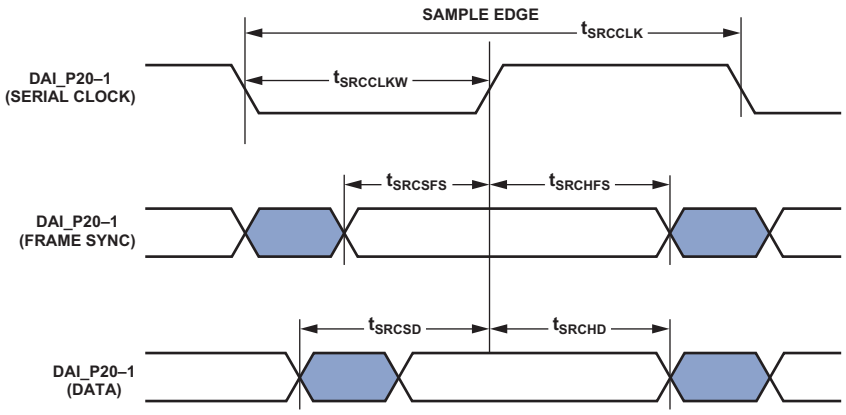


Figure 28. ASRC Serial Input Port Timing

Sample Rate Converter—Serial Output Port

For the serial output port, the frame-sync is an input and it should meet setup and hold times with regard to the serial clock on the output port. The serial data output, has a hold time and delay specification with regard to serial clock. Note that serial clock rising edge is the sampling edge and the falling edge is the drive edge.

Table 39. ASRC, Serial Output Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{SRCTDD}[1]	Transmit Data Delay After Serial Clock Falling Edge		9.9	ns
t_{SRCTDH}[1]	Transmit Data Hold After Serial Clock Falling Edge	1		ns

[1] The serial clock, data and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

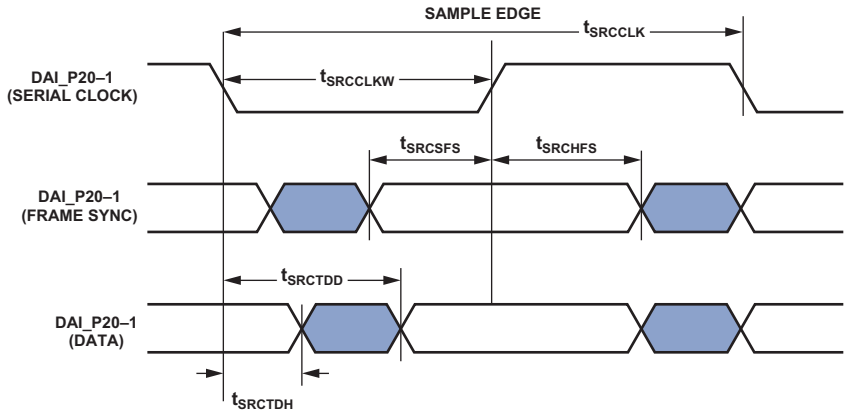


Figure 29. ASRC Serial Output Port Timing

Pulse-Width Modulation Generators (PWM)

The following timing specifications apply when the AMI_ADDR23–8 pins are configured as PWM.

Table 40. Pulse-Width Modulation (PWM) Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMW}	PWM Output Pulse Width	$t_{PCLK} - 2$	$(2^{16} - 2) \times t_{PCLK} - 2$	ns
t_{PWMP}	PWM Output Period	$2 \times t_{PCLK} - 1.5$	$(2^{16} - 1) \times t_{PCLK} - 1.5$	ns

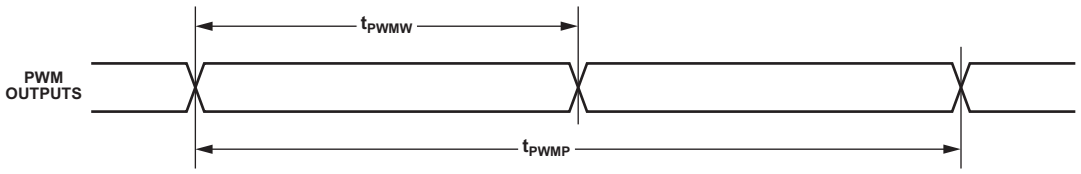


Figure 30. PWM Timing

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left-justified, I²S, or right-justified with word widths of 16-, 18-, 20-, or 24-bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter-Serial Input Waveforms

Figure 31 shows the right-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of Serial Clock. The MSB is delayed 12-bit clock periods (in 20-bit output mode) or 16-bit clock periods (in 16-bit output mode) from an LRCLK transition, so that when there are 64 Serial clock periods per LRCLK period, the LSB of the data will be right-justified to the next LRCLK transition.

Figure 32 shows the default I²S-justified mode. LRCLK is low for the left channel and HI for the right channel. Data is valid on the rising edge of Serial Clock. The MSB is left-justified to an LRCLK transition but with a single Serial Clock period delay.

Figure 33 shows the left-justified mode. LRCLK is high for the left channel and LO for the right channel. Data is valid on the rising edge of Serial Clock. The MSB is left-justified to an LRCLK transition with no MSB delay.

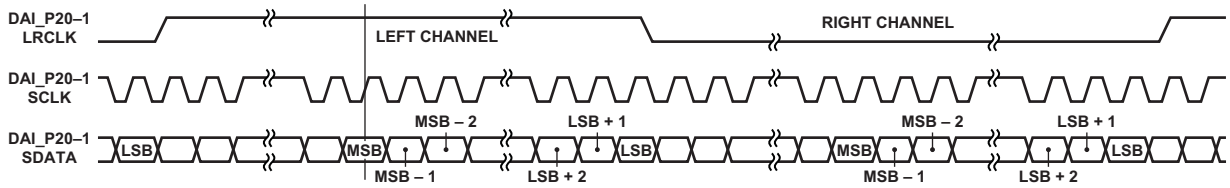


Figure 31. Right-Justified Mode

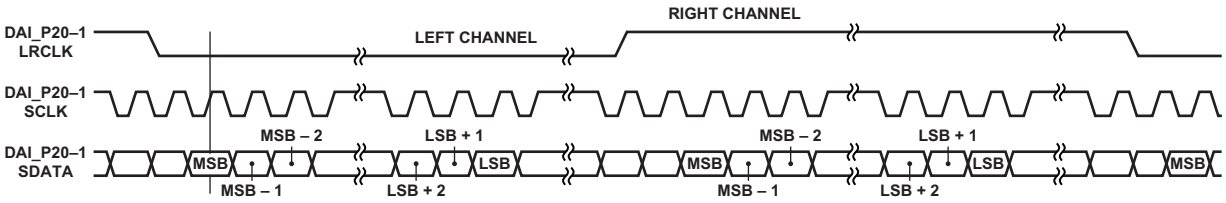


Figure 32. I²S-Justified Mode

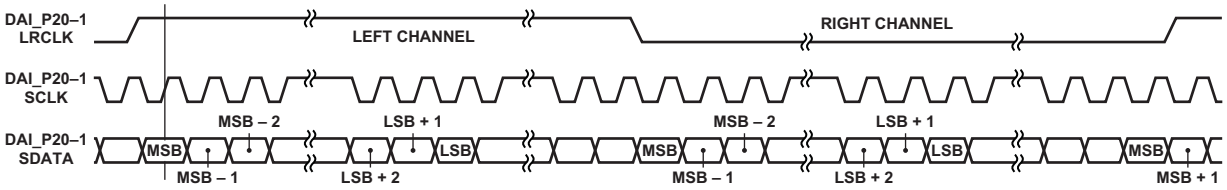


Figure 33. Left-Justified Mode

S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 41. Input signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 41. S/PDIF Transmitter Input Data Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	3		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	3		ns
$t_{SIHFCLKW}$	Transmit Clock Width	36		ns
$t_{SIHFCLK}$	Transmit Clock Period	80		ns
$t_{SISCLKW}$	Clock Width	9		ns
t_{SISCLK}	Clock Period	20		ns

[1] The serial clock, data and frame sync signals can come from any of the DAI pins.The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

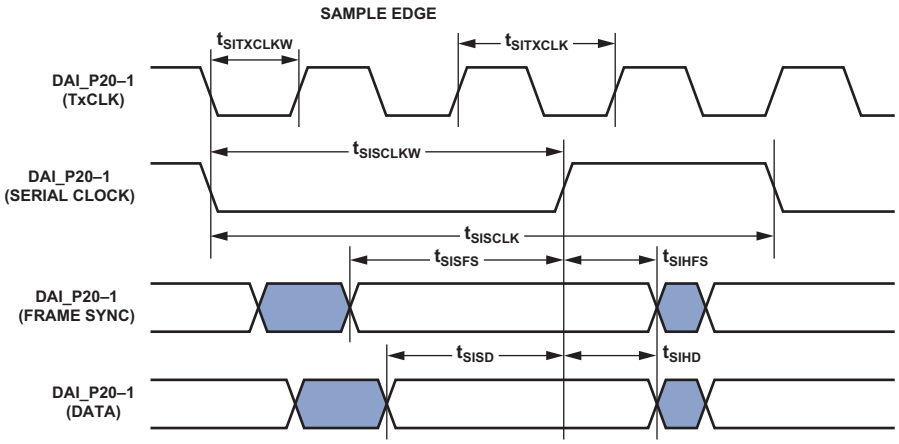


Figure 34. S/PDIF Transmitter Input Timing

Oversampling Clock (HFCLK) Switching Characteristics

The S/PDIF transmitter has an oversampling clock. This HFCLK input is divided down to generate the biphase clock.

Table 42. Over Sampling Clock (HFCLK) Switching Characteristics

Parameter	Max	Unit
HFCLK Frequency for HFCLK = 384 × Frame Sync	Oversampling Ratio × Frame Sync <= $1/t_{SIHFCLK}$	MHz
HFCLK Frequency for HFCLK = 256 × Frame Sync	49.2	MHz
Frame Rate (FS)	192.0	kHz

S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver.

Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the TBD × FS clock.

Table 43. S/PDIF Receiver Internal Digital PLL Mode Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	LRCLK Delay After Serial Clock		5	ns
t_{HOFSI}	LRCLK Hold After Serial Clock	–2		ns
t_{DDTI}	Transmit Data Delay After Serial Clock		5	ns
t_{HDTI}	Transmit Data Hold After Serial Clock	–2		ns
t_{SCLKIW}[1]	Transmit Serial Clock Width	40		ns

[1] Serial clock frequency is TBD x Frame Sync where FS = the frequency of LRCLK.

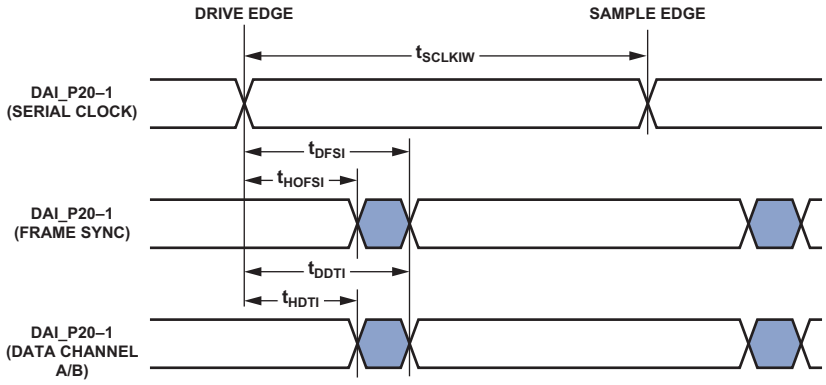


Figure 35. S/PDIF Receiver Internal Digital PLL Mode Timing

SPI Interface—Master

The ADSP-2146x contains two SPI ports. Both primary and secondary are available through DPI only. The timing provided in Table 44 and Table 45 applies to both.

Table 44. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	8.2		ns
t_{HSPIDM}	SPICLK Last Sampling Edge to Data Input Not Valid	2		ns
Switching Characteristics				
$t_{SPICLKM}$	Serial Clock Cycle	$8 \times t_{PCLK} - 2$		ns
t_{SPICHM}	Serial Clock High Period	$4 \times t_{PCLK} - 2$		ns
t_{SPICLM}	Serial Clock Low Period	$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		2.5	ns
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$4 \times t_{PCLK} - 2$		ns
t_{SDSCIM}	DPI Pin (SPI Device Select) Low to First SPICLK Edge	$4 \times t_{PCLK} - 2$		ns
t_{HDSM}	Last SPICLK Edge to DPI Pin (SPI Device Select) High	$4 \times t_{PCLK} - 2$		ns
t_{SPITDM}	Sequential Transfer Delay	$4 \times t_{PCLK} - 1$		ns

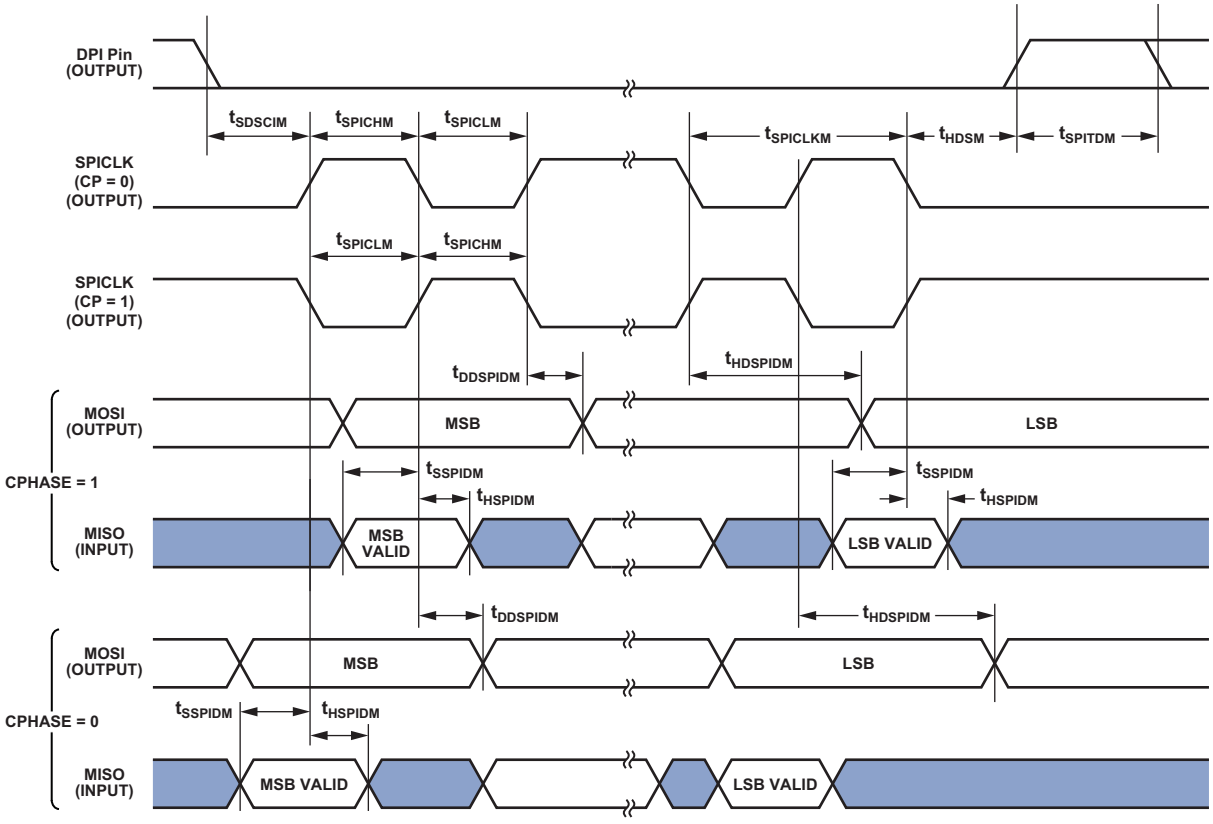


Figure 36. SPI Master Timing

SPI Interface—Slave

Table 45. SPI Interface Protocol—Slave Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SPICLKS}$	Serial Clock Cycle	$4 \times t_{PCLK} - 2$		ns
t_{SPICHS}	Serial Clock High Period	$2 \times t_{PCLK} - 2$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{PCLK} - 2$		ns
t_{SDSCO}	$\overline{SPIDS}$ Assertion to First SPICLK Edge, CPHASE = 0 or CPHASE = 1	$2 \times t_{PCLK}$		ns
t_{HDS}	Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted, CPHASE = 0	$2 \times t_{PCLK}$		ns
t_{SSPIDS}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	2		ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	2		ns
t_{SDPPW}	$\overline{SPIDS}$ Deassertion Pulse Width (CPHASE = 0)	$2 \times t_{PCLK}$		ns
Switching Characteristics				
t_{DSOE}	$\overline{SPIDS}$ Assertion to Data Out Active	0	6.8	ns
t_{DSOE}[1]	$\overline{SPIDS}$ Assertion to Data Out Active (SPI2)	0	8	ns
t_{DSDHI}	$\overline{SPIDS}$ Deassertion to Data High Impedance	0	6.8	ns
t_{DSDHI}[1]	$\overline{SPIDS}$ Deassertion to Data High Impedance (SPI2)	0	8.6	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		9.5	ns
$t_{HDSPIDS}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$2 \times t_{PCLK}$		ns
t_{DSOV}	$\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0)		$5 \times t_{PCLK}$	ns

[1] The timing for these parameters applies when the SPI is routed through the signal routing unit. For more information, see the processor hardware reference, "Serial Peripheral Interface Port" chapter.

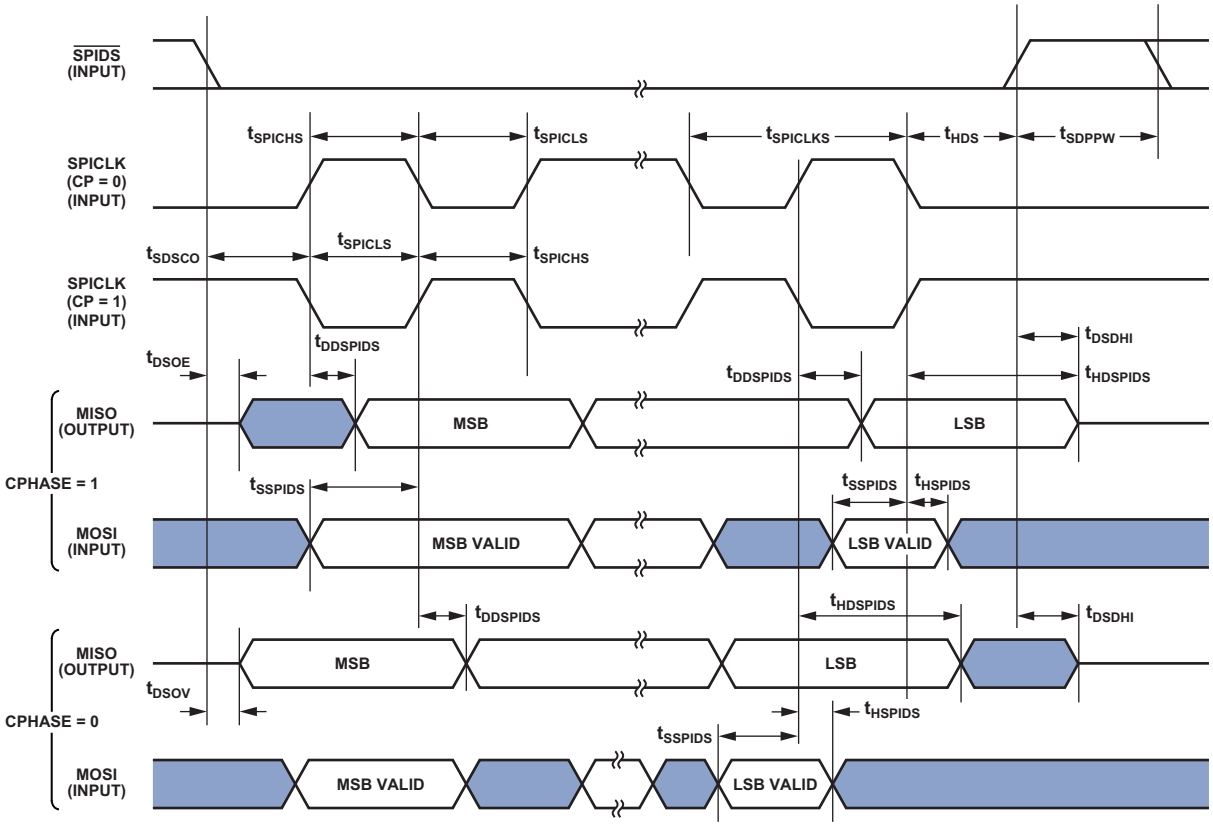


Figure 37. SPI Slave Timing

Media Local Bus

All the numbers given are applicable for all speed modes (1024Fs, 512Fs and 256Fs for 3-pin; 512Fs and 256Fs for 5-pin) unless otherwise specified. Please refer to MediaLB specification document rev 3.0 for more details.

Table 46. MLB Interface, 3-pin Specifications

Parameter		Min	Typ	Max	Unit
Three-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	1024Fs		20.3		ns
	512Fs		40		ns
	256Fs		81		ns
t_{MCKL}	MLBCLK Low Time				
	1024Fs	6.1			ns
	512Fs	14			ns
	256Fs	30			ns
t_{MCKH}	MLBCLK High Time				
	1024Fs	9.3			ns
	512Fs	14			ns
	256Fs	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})				
	1024Fs			1	ns
	512Fs/256Fs			3	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})				
	1024Fs			1	ns
	512Fs/256Fs			3	ns
t_{MPWV}[1]	MLBCLK Pulse Width Variation				
	1024Fs			0.7	nspp
	512Fs/256			2.0	nspp
t_{DSMCF}	DAT/SIG Input Setup Time	1			ns
t_{DHMCF}	DAT/SIG Input Hold Time	0			ns
t_{MCFDZ}	DAT/SIG Output Time to Three-state	0		t_{MCKL}	ns
t_{MCDRV}	DAT/SIG Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MDZH}[2]	Bus Hold Time				
	1024Fs	2			ns
	512Fs/256	4			ns
C_{MLB}	DAT/SIG Pin Load				
	1024Fs			40	pf
	512Fs/256			60	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak(pp).
[2] The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

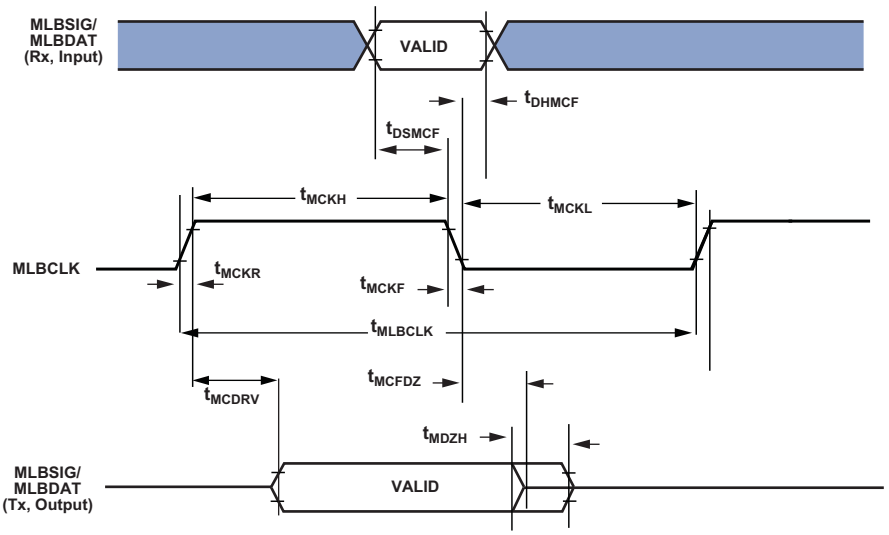


Figure 38. MLB Timing (3-Pin Interface)

Table 47. MLB Interface, 5-pin Specifications

Parameter		Min	Typ	Max	Unit
Five-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	512Fs		40		ns
	256Fs		81		ns
t_{MCKL}	MLBCLK Low Time				
	512Fs	15			ns
	256Fs	30			ns
t_{MCKH}	MLBCLK High Time				
	512Fs	15			ns
	256Fs	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})			6	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})			6	ns
t_{MPWV}[1]	MLBCLK Pulse Width Variation			2	nspp
t_{DSMCF}[2]	DAT/SIG Input Setup Time	3			ns
t_{DHMCF}	DAT/SIG Input Hold Time	5			ns
t_{MCDRV}	DS/DO Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MCRDL}[3]	DO/SO Low From MLBCLK High				
	512Fs			10	ns
	256Fs			20	ns
C_{MLB}	DS/DO Pin Load			40	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp).
[2] Gate Delays due to OR'ing logic on the pins must be accounted for.
[3] When a node is not driving valid data onto the bus, the MLBSO and MLBDO output lines shall remain low. If the output lines can float at anytime, including while in reset, external pull-down resistors are required to keep the outputs from corrupting the MediaLB signal lines when not being driven.

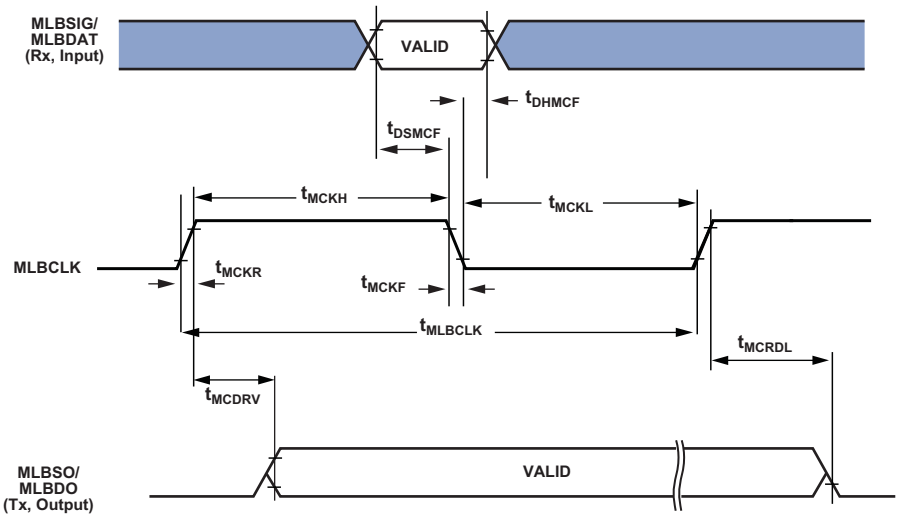


Figure 39. MLB Timing (5-Pin Interface)

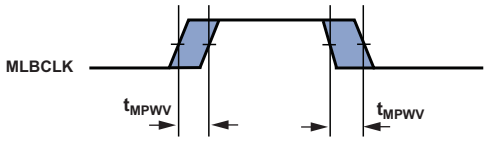


Figure 40. MLB 3-Pin and 5-Pin MLBCLK Pulse Width Variation Timing

Universal Asynchronous Receiver-Transmitter (UART) Port—Receive and Transmit Timing

Figure 41 describes UART port receive and transmit operations. The maximum baud rate is PCLK/16 where PCLK = 1/tPCLK. As shown in Figure 41 there is some latency between the generation of internal UART interrupts and the external data operations. These latencies are negligible at the data transmission rates for the UART.

Table 48. UART Port

Parameter		Min	Max	Unit
Timing Requirement				
t_{RXD}[1]	Incoming Data Pulse Width	$16 \times t_{PCLK}-1$		ns
Switching Characteristic				
t_{TXD}1	Outgoing Data Pulse Width	$16 \times t_{PCLK}-1$		ns

[1] UART signals RXD and TXD are routed through DPI P14-1 pins using the SRU.

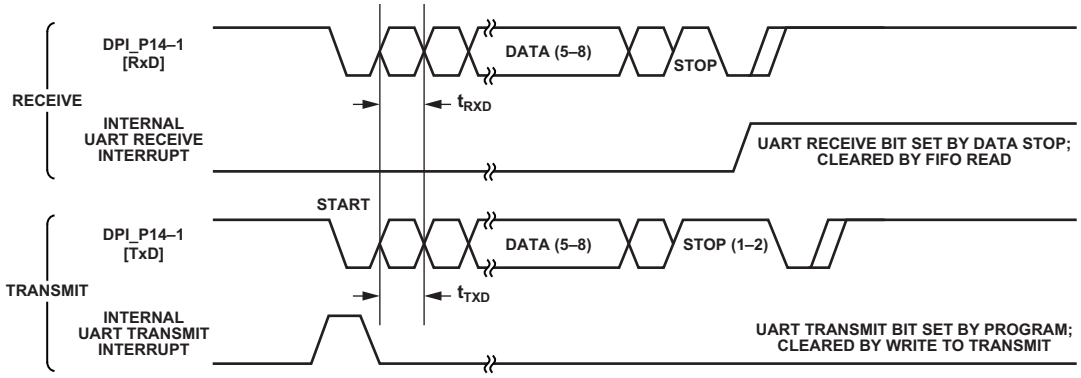


Figure 41. UART Port—Receive and Transmit Timing

TWI Controller Timing

Table 49 and Figure 42 provide timing information for the TWI interface. Input Signals (SCL, SDA) are routed to the DPI_P14–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 49. Characteristics of the SDA and SCL Bus Lines for F/S-Mode TWI Bus Devices[1]

Parameter		Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency	0	100	0	400	kHz
t_{HDSTA}	Hold Time (repeated) Start Condition. After This Period, the First Clock Pulse is Generated.	4.0		0.6		µs
t_{LOW}	Low Period of the SCL Clock	4.7		1.3		µs
t_{HIGH}	High Period of the SCL Clock	4.0		0.6		µs
t_{SUSTA}	Setup Time for a Repeated Start Condition	4.7		0.6		µs
t_{HDDAT}	Data Hold Time for TWI-bus Devices	0		0		µs
t_{SUDAT}	Data Setup Time	250		100		ns
t_{SUSTO}	Setup Time for Stop Condition	4.0		0.6		µs
t_{BUF}	Bus Free Time Between a Stop and Start Condition	4.7		1.3		µs
t_{SP}	Pulse Width of Spikes Suppressed By the Input Filter	n/a	n/a	0	50	ns

[1] All values referred to V_{IHmin} and V_{ILmax} levels. For more information, see Electrical Characteristics on page 20.

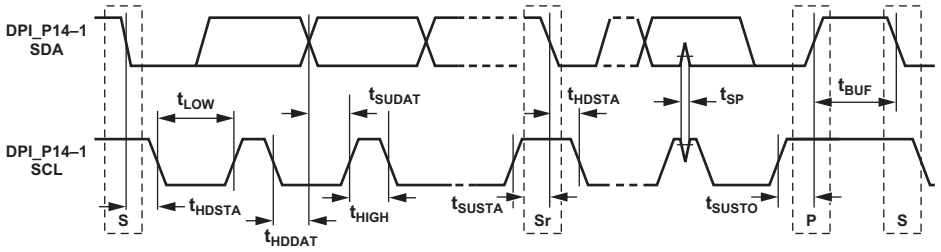


Figure 42. Fast and Standard Mode Timing on the TWI Bus

JTAG Test Access Port and Emulation

Table 50. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4 \times t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		7	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = AMI_DATA, DDR2_DATA, CLKCFG1-0, BOOTCFG2-0 RESET, DAI, DPI, FLAG3-0.
[2] System Outputs = AMI_ADDR/DATA, DDR2_ADDR/DATA, AMI_CTRL, DDR2_CTRL, DAI, DPI, FLAG3-0, $\overline{\text{EMU}}$.

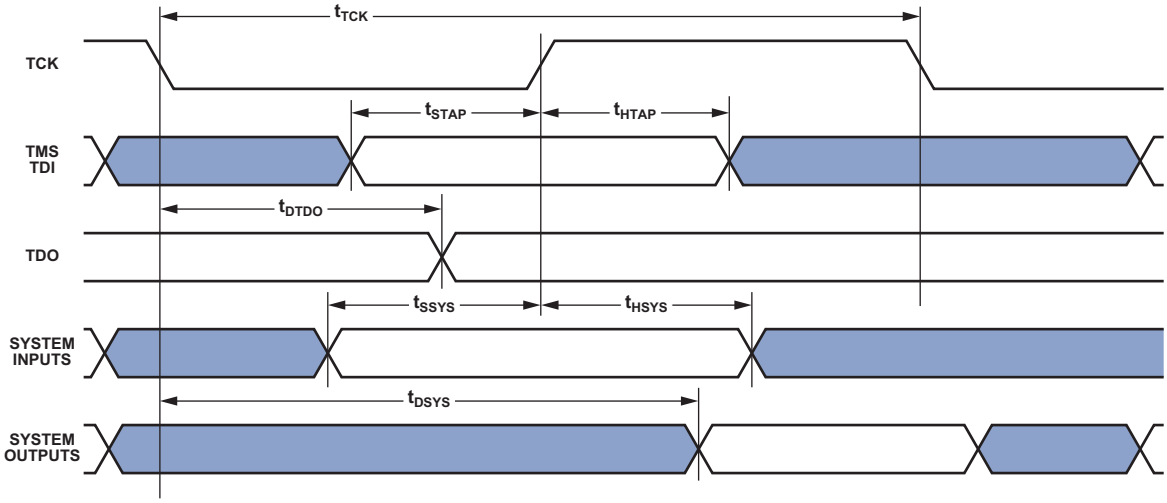


Figure 43. IEEE 1149.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 44 shows typical I-V characteristics for the output drivers of the ADSP-2146x. The curves represent the current drive capability of the output drivers as a function of output voltage.

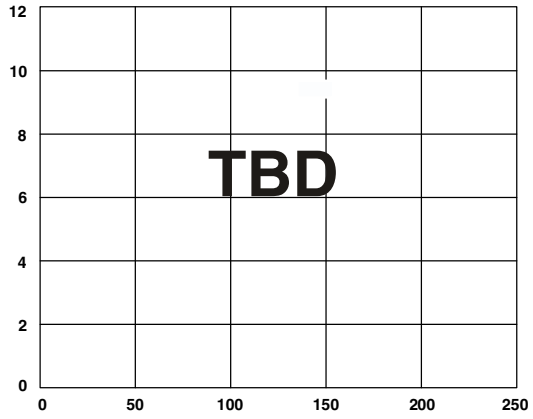
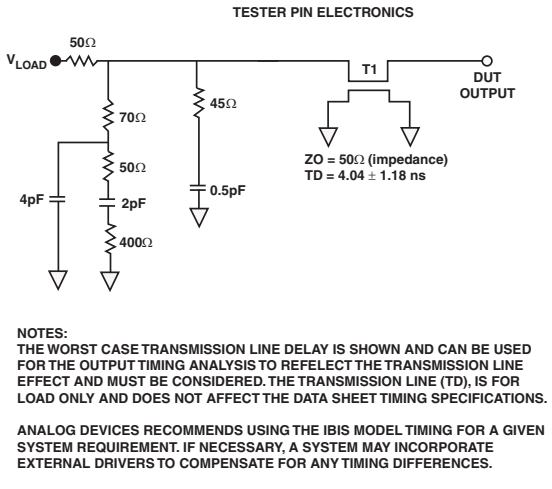


Figure 44. Typical Drive at Junction Temperature

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 17 on Page 26 through Table 50 on Page 58. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 45.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 46. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD), IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 45. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

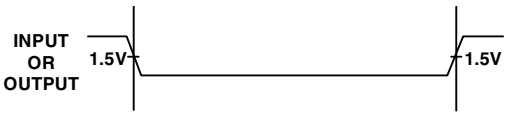


Figure 46. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 45). Figure 49 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 47, Figure 48, and Figure 49 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

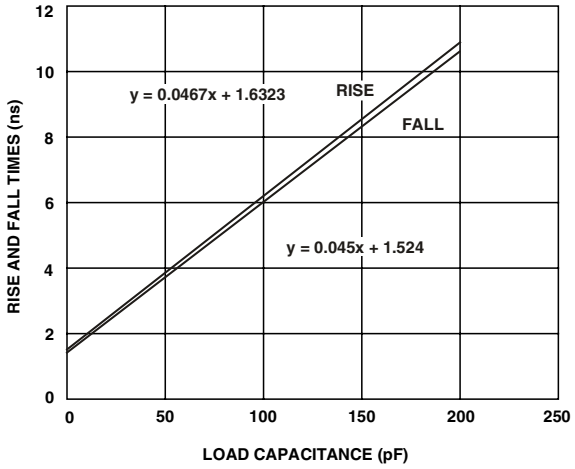


Figure 47. Typical Output Rise/Fall Time (20% to 80%, V_{DD_EXT} = Max)

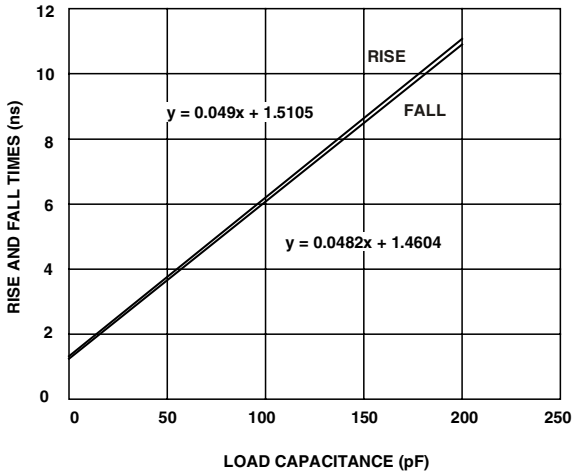


Figure 48. Typical Output Rise/Fall Time (20% to 80%, V_{DD_EXT} = Min)

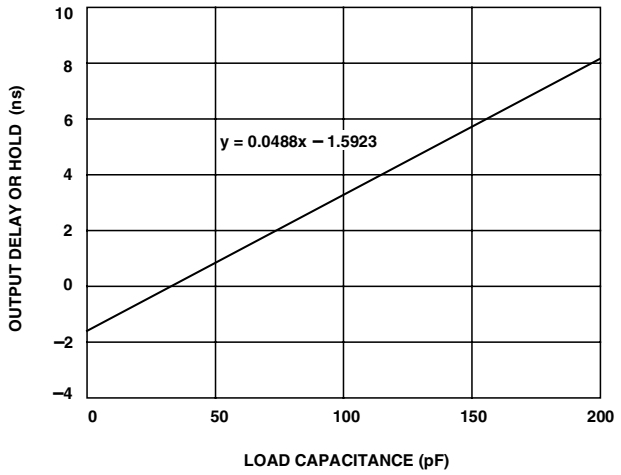


Figure 49. Typical Output Delay or Hold vs. Load Capacitance (at Ambient Temperature)

THERMAL CHARACTERISTICS

The ADSP-2146x processor is rated for performance over the temperature range specified in Operating Conditions on Page 19.

Table 51 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-7 (CSP_BGA). The junction-to-case measurement complies with MIL- STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature °C

T_{CASE} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the Typical value from Table 51.

P_D = power dissipation

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature °C

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heatsink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations. Note that the thermal characteristics values provided in Table 51 are modeled values.

Table 51. Thermal Characteristics for 324-Lead CSP_BGA

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	TBD	°C/W
θ_{JMA}	Airflow = 1 m/s	TBD	°C/W
θ_{JMA}	Airflow = 2 m/s	TBD	°C/W
θ_{JC}		TBD	°C/W
Ψ_{JT}	Airflow = 0 m/s	TBD	°C/W
Ψ_{JMT}	Airflow = 1 m/s	TBD	°C/W
Ψ_{JMT}	Airflow = 2 m/s	TBD	°C/W

CSP_BGA BALL ASSIGNMENT – ADSP-21462W/ADSP-21465W/ADSP-21469W

Table 52 lists the CSP_BGA ball names. For default DAI and DPI routing, see the processor hardware reference manual.

Table 52. CSP_BGA Ball Assignment (Alphabetically by Signal)

Signal	Ball No.	Signal	Ball	Signal	Ball	Signal	Ball
AGND	H02	CLK_CFG1	G02	DDR2_CKE	E01	DPI_P09	N01
AMI_ACK	R10	CLKIN	L01	$\overline{\text{DDR2_CLK0}}$	A07	DPI_P10	N02
AMI_ADDR0	V16	DAI_P01	R06	DDR2_CLK0	B07	DPI_P11	N03
AMI_ADDR01	U16	DAI_P02	V05	$\overline{\text{DDR2_CLK1}}$	A13	DPI_P12	N04
AMI_ADDR02	T16	DAI_P03	R07	DDR2_CLK1	B13	DPI_P13	M03
AMI_ADDR03	R16	DAI_P04	R03	$\overline{\text{DDR2_CS0}}$	C01	DPI_P14	M04
AMI_ADDR04	V15	DAI_P05	U05	$\overline{\text{DDR2_CS1}}$	D01	$\overline{\text{EMU}}$	K02
AMI_ADDR05	U15	DAI_P06	T05	$\overline{\text{DDR2_CS2}}$	C02	FLAG0	R08
AMI_ADDR06	T15	DAI_P07	V06	$\overline{\text{DDR2_CS3}}$	D02	FLAG1	V07
AMI_ADDR07	R15	DAI_P08	V02	DDR2_DATA0	B02	FLAG2	U07
AMI_ADDR08	V14	DAI_P09	R05	DDR2_DATA01	A02	FLAG3	T07
AMI_ADDR09	U14	DAI_P10	V04	DDR2_DATA02	B03	GND	A01
AMI_ADDR10	T14	DAI_P11	U04	DDR2_DATA03	A03	GND	A18
AMI_ADDR11	R14	DAI_P12	T04	DDR2_DATA04	B05	GND	C04
AMI_ADDR12	V13	DAI_P13	U06	DDR2_DATA05	A05	GND	C06
AMI_ADDR13	U13	DAI_P14	U02	DDR2_DATA06	B06	GND	C08
AMI_ADDR14	T13	DAI_P15	R04	DDR2_DATA07	A06	GND	D05
AMI_ADDR15	R13	DAI_P16	V03	DDR2_DATA08	B08	GND	D07
AMI_ADDR16	V12	DAI_P17	U03	DDR2_DATA09	A08	GND	D09
AMI_ADDR17	U12	DAI_P18	T03	DDR2_DATA10	B09	GND	D10
AMI_ADDR18	T12	DAI_P19	T06	DDR2_DATA11	A09	GND	D17
AMI_ADDR19	R12	DAI_P20	T02	DDR2_DATA12	A11	GND	E03
AMI_ADDR20	V11	DDR2_ADDR0	D13	DDR2_DATA13	B11	GND	E05
AMI_ADDR21	U11	DDR2_ADDR01	C13	DDR2_DATA14	A12	GND	E12
AMI_ADDR22	T11	DDR2_ADDR02	D14	DDR2_DATA15	B12	GND	E13
AMI_ADDR23	R11	DDR2_ADDR03	C14	DDR2_DM0	C03	GND	E16
AMI_DATA0	U18	DDR2_ADDR04	B14	DDR2_DM1	C11	GND	F01
AMI_DATA1	T18	DDR2_ADDR05	A14	DDR2_DQS0	A04	GND	F02
AMI_DATA2	R18	DDR2_ADDR06	D15	$\overline{\text{DDR2_DQS0}}$	B04	GND	F04
AMI_DATA3	P18	DDR2_ADDR07	C15	DDR2_DQS1	A10	GND	F14
AMI_DATA4	V17	DDR2_ADDR08	B15	$\overline{\text{DDR2_DQS1}}$	B10	GND	F16
AMI_DATA5	U17	DDR2_ADDR09	A15	DDR2_ODT	B01	GND	G03
AMI_DATA6	T17	DDR2_ADDR10	D16	$\overline{\text{DDR2_RAS}}$	C09	GND	G04
AMI_DATA7	R17	DDR2_ADDR11	C16	$\overline{\text{DDR2_WE}}$	C10	GND	G05
$\overline{\text{AMI_MS0}}$	T10	DDR2_ADDR12	B16	DPI_P01	R02	GND	G07
$\overline{\text{AMI_MS1}}$	U10	DDR2_ADDR13	A16	DPI_P02	U01	GND	G08
$\overline{\text{AMI_RD}}$	J04	DDR2_ADDR14	B17	DPI_P03	T01	GND	G09
$\overline{\text{AMI_WR}}$	V10	DDR2_ADDR15	A17	DPI_P04	R01	GND	G10
BOOT_CFG0	J02	DDR2_BA0	C18	DPI_P05	P01	GND	G11
BOOT_CFG1	J03	DDR2_BA1	C17	DPI_P06	P02	GND	G12
BOOT_CFG2	Ho3	DDR2_BA2	B18	DPI_P07	P03	GND	G15
CLK_CFG0	G01	$\overline{\text{DDR2_CAS}}$	C07	DPI_P08	P04	GND	H04

Table 52. CSP_BGA Ball Assignment (Alphabetically by Signal) (Continued)

Signal	Ball No.	Signal	Ball	Signal	Ball	Signal	Ball
GND	H07	GND	V01	V_{DD_DDR2}	E04	V_{DD_INT}	F12
GND	H08	GND	V18	V_{DD_DDR2}	E07	V_{DD_INT}	F13
GND	H09	LACK_0	K17	V_{DD_DDR2}	E10	V_{DD_INT}	G06
GND	H10	LACK_1	P17	V_{DD_DDR2}	E11	V_{DD_INT}	G13
GND	H11	LCLK_0	J18	V_{DD_DDR2}	E17	V_{DD_INT}	H05
GND	H12	LCLK_1	N18	V_{DD_DDR2}	F03	V_{DD_INT}	H06
GND	J01	LDAT0_0	E18	V_{DD_DDR2}	F05	V_{DD_INT}	H13
GND	J07	LDAT0_1	F17	V_{DD_DDR2}	F15	V_{DD_INT}	H14
GND	J08	LDAT0_2	F18	V_{DD_DDR2}	G14	V_{DD_INT}	J06
GND	J09	LDAT0_3	G17	V_{DD_DDR2}	G16	V_{DD_INT}	J13
GND	J10	LDAT0_4	G18	V_{DD_EXT}	H15	V_{DD_INT}	K06
GND	J11	LDAT0_5	H16	V_{DD_EXT}	H18	V_{DD_INT}	K13
GND	J12	LDAT0_6	H17	V_{DD_EXT}	J05	V_{DD_INT}	L06
GND	J14	LDAT0_7	J16	V_{DD_EXT}	J15	V_{DD_INT}	L13
GND	J17	LDAT1_0	K18	V_{DD_EXT}	K14	V_{DD_INT}	M06
GND	K05	LDAT1_1	L16	V_{DD_EXT}	L05	V_{DD_INT}	M13
GND	K07	LDAT1_2	L17	V_{DD_EXT}	M14	V_{DD_INT}	N06
GND	K08	LDAT1_3	L18	V_{DD_EXT}	M18	V_{DD_INT}	N07
GND	K09	LDAT1_4	M16	V_{DD_EXT}	N05	V_{DD_INT}	N08
GND	K10	LDAT1_5	M17	V_{DD_EXT}	N10	V_{DD_INT}	N09
GND	K11	LDAT1_6	N16	V_{DD_EXT}	P06	V_{DD_INT}	N13
GND	K12	LDAT1_7	P16	V_{DD_EXT}	P08	V_{REF}	D04
GND	L07	MLBCLK	K03	V_{DD_EXT}	P10	V_{REF}	D11
GND	L08	MLBDAT	K04	V_{DD_EXT}	P12	XTAL	K01
GND	L09	MLBDO	L02	V_{DD_EXT}	P14		
GND	L10	MLBSIG	L03	V_{DD_EXT}	P15		
GND	L11	MLBSO	L04	V_{DD_EXT}	T08		
GND	L12	$\overline{\text{RESET}}$	M01	V_{DD_EXT}	T09		
GND	L14	$\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$	M02	V_{DD_EXT}	U08		
GND	M05	TCK	K15	V_{DD_EXT}	U09		
GND	M07	TDI	L15	V_{DD_EXT}	V08		
GND	M08	TDO	M15	V_{DD_EXT}	V09		
GND	M09	THD_M	N12	V_{DD_INT}	D12		
GND	M10	THD_P	N11	V_{DD_INT}	E06		
GND	M11	TMS	K16	V_{DD_INT}	E08		
GND	M12	$\overline{\text{TRST}}$	N15	V_{DD_INT}	E09		
GND	N14	VDD_A	H01	V_{DD_INT}	E14		
GND	N17	V_{DD_DDR2}	C05	V_{DD_INT}	E15		
GND	P05	V_{DD_DDR2}	C12	V_{DD_INT}	F06		
GND	P07	V_{DD_DDR2}	D03	V_{DD_INT}	F07		
GND	P09	V_{DD_DDR2}	D06	V_{DD_INT}	F08		
GND	P11	V_{DD_DDR2}	D08	V_{DD_INT}	F09		
GND	P13	V_{DD_DDR2}	D18	V_{DD_INT}	F10		
GND	R09	V_{DD_DDR2}	E02	V_{DD_INT}	F11		

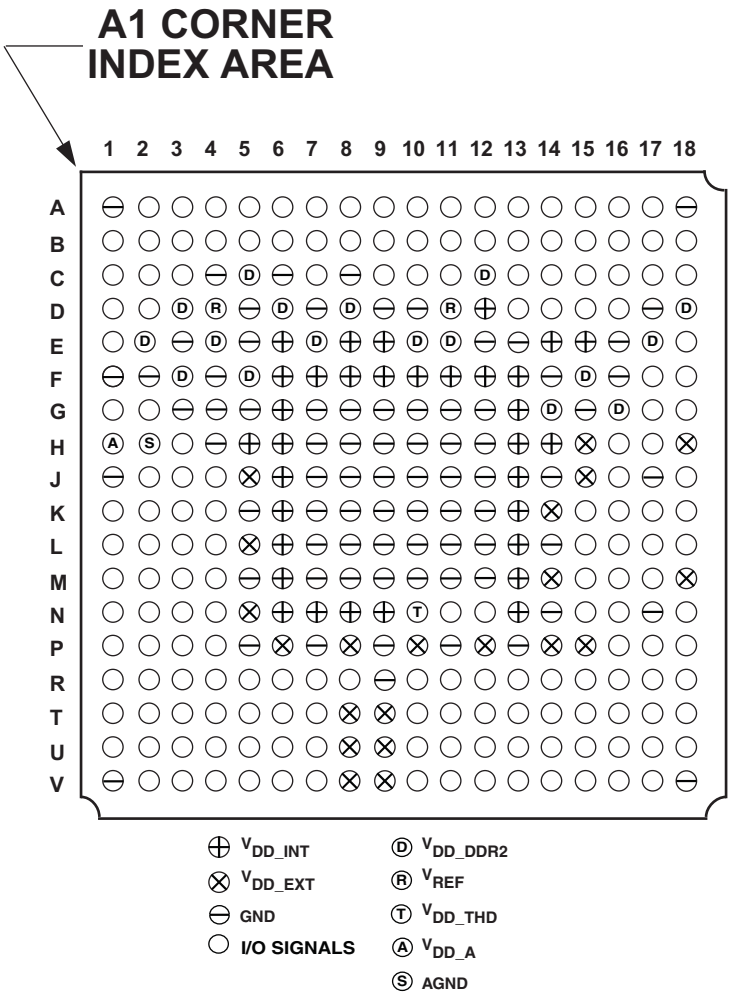


Figure 50. ADSP-21462W/ADSP-21465W/ADSP-21469W Ball Configuration – Pin Out

CSP_BGA BALL ASSIGNMENT - ADSP-21467/ADSP-21469

Table 53 lists the ball names.

Table 53. CSP_BGA Ball Assignment (Alphabetically by Signal)

Signal	Ball No.	Signal	Ball	Signal	Ball	Signal	Ball
AGND	H02	CLK_CFG1	G02	DDR2_CKE	E01	DPI_P09	N01
AMI_ACK	R10	CLKIN	L01	$\overline{\text{DDR2_CLK0}}$	A07	DPI_P10	N02
AMI_ADDR0	V16	DAI_P01	R06	DDR2_CLK0	B07	DPI_P11	N03
AMI_ADDR01	U16	DAI_P02	V05	$\overline{\text{DDR2_CLK1}}$	A13	DPI_P12	N04
AMI_ADDR02	T16	DAI_P03	R07	DDR2_CLK1	B13	DPI_P13	M03
AMI_ADDR03	R16	DAI_P04	R03	$\overline{\text{DDR2_CS0}}$	C01	DPI_P14	M04
AMI_ADDR04	V15	DAI_P05	U05	$\overline{\text{DDR2_CS1}}$	D01	$\overline{\text{EMU}}$	K02
AMI_ADDR05	U15	DAI_P06	T05	$\overline{\text{DDR2_CS2}}$	C02	FLAG0	R08
AMI_ADDR06	T15	DAI_P07	V06	$\overline{\text{DDR2_CS3}}$	D02	FLAG1	V07
AMI_ADDR07	R15	DAI_P08	V02	DDR2_DATA0	B02	FLAG2	U07
AMI_ADDR08	V14	DAI_P09	R05	DDR2_DATA01	A02	FLAG3	T07
AMI_ADDR09	U14	DAI_P10	V04	DDR2_DATA02	B03	GND	A01
AMI_ADDR10	T14	DAI_P11	U04	DDR2_DATA03	A03	GND	A18
AMI_ADDR11	R14	DAI_P12	T04	DDR2_DATA04	B05	GND	C04
AMI_ADDR12	V13	DAI_P13	U06	DDR2_DATA05	A05	GND	C06
AMI_ADDR13	U13	DAI_P14	U02	DDR2_DATA06	B06	GND	C08
AMI_ADDR14	T13	DAI_P15	R04	DDR2_DATA07	A06	GND	D05
AMI_ADDR15	R13	DAI_P16	V03	DDR2_DATA08	B08	GND	D07
AMI_ADDR16	V12	DAI_P17	U03	DDR2_DATA09	A08	GND	D09
AMI_ADDR17	U12	DAI_P18	T03	DDR2_DATA10	B09	GND	D10
AMI_ADDR18	T12	DAI_P19	T06	DDR2_DATA11	A09	GND	D17
AMI_ADDR19	R12	DAI_P20	T02	DDR2_DATA12	A11	GND	E03
AMI_ADDR20	V11	DDR2_ADDR0	D13	DDR2_DATA13	B11	GND	E05
AMI_ADDR21	U11	DDR2_ADDR01	C13	DDR2_DATA14	A12	GND	E12
AMI_ADDR22	T11	DDR2_ADDR02	D14	DDR2_DATA15	B12	GND	E13
AMI_ADDR23	R11	DDR2_ADDR03	C14	DDR2_DM0	C03	GND	E16
AMI_DATA0	U18	DDR2_ADDR04	B14	DDR2_DM1	C11	GND	F01
AMI_DATA1	T18	DDR2_ADDR05	A14	DDR2_DQS0	A04	GND	F02
AMI_DATA2	R18	DDR2_ADDR06	D15	$\overline{\text{DDR2_DQS0}}$	B04	GND	F04
AMI_DATA3	P18	DDR2_ADDR07	C15	DDR2_DQS1	A10	GND	F14
AMI_DATA4	V17	DDR2_ADDR08	B15	$\overline{\text{DDR2_DQS1}}$	B10	GND	F16
AMI_DATA5	U17	DDR2_ADDR09	A15	DDR2_ODT	B01	GND	G03
AMI_DATA6	T17	DDR2_ADDR10	D16	$\overline{\text{DDR2_RAS}}$	C09	GND	G04
AMI_DATA7	R17	DDR2_ADDR11	C16	$\overline{\text{DDR2_WE}}$	C10	GND	G05
$\overline{\text{AMI_MS0}}$	T10	DDR2_ADDR12	B16	DPI_P01	R02	GND	G07
$\overline{\text{AMI_MS1}}$	U10	DDR2_ADDR13	A16	DPI_P02	U01	GND	G08
$\overline{\text{AMI_RD}}$	J04	DDR2_ADDR14	B17	DPI_P03	T01	GND	G09
$\overline{\text{AMI_WR}}$	V10	DDR2_ADDR15	A17	DPI_P04	R01	GND	G10
BOOT_CFG0	J02	DDR2_BA0	C18	DPI_P05	P01	GND	G11
BOOT_CFG1	J03	DDR2_BA1	C17	DPI_P06	P02	GND	G12
BOOT_CFG2	Ho3	DDR2_BA2	B18	DPI_P07	P03	GND	G15
CLK_CFG0	G01	$\overline{\text{DDR2_CAS}}$	C07	DPI_P08	P04	GND	H04

Table 53. CSP_BGA Ball Assignment (Alphabetically by Signal) (Continued)

Signal	Ball No.	Signal	Ball	Signal	Ball	Signal	Ball
GND	H07	GND	V01	V_{DD_DDR2}	E04	V_{DD_INT}	F12
GND	H08	GND	V18	V_{DD_DDR2}	E07	V_{DD_INT}	F13
GND	H09	LACK_0	K17	V_{DD_DDR2}	E10	V_{DD_INT}	G06
GND	H10	LACK_1	P17	V_{DD_DDR2}	E11	V_{DD_INT}	G13
GND	H11	LCLK_0	J18	V_{DD_DDR2}	E17	V_{DD_INT}	H05
GND	H12	LCLK_1	N18	V_{DD_DDR2}	F03	V_{DD_INT}	H06
GND	J01	LDAT0_0	E18	V_{DD_DDR2}	F05	V_{DD_INT}	H13
GND	J07	LDAT0_1	F17	V_{DD_DDR2}	F15	V_{DD_INT}	H14
GND	J08	LDAT0_2	F18	V_{DD_DDR2}	G14	V_{DD_INT}	J06
GND	J09	LDAT0_3	G17	V_{DD_DDR2}	G16	V_{DD_INT}	J13
GND	J10	LDAT0_4	G18	V_{DD_EXT}	H15	V_{DD_INT}	K06
GND	J11	LDAT0_5	H16	V_{DD_EXT}	H18	V_{DD_INT}	K13
GND	J12	LDAT0_6	H17	V_{DD_EXT}	J05	V_{DD_INT}	L06
GND	J14	LDAT0_7	J16	V_{DD_EXT}	J15	V_{DD_INT}	L13
GND	J17	LDAT1_0	K18	V_{DD_EXT}	K14	V_{DD_INT}	M06
GND	K05	LDAT1_1	L16	V_{DD_EXT}	L05	V_{DD_INT}	M13
GND	K07	LDAT1_2	L17	V_{DD_EXT}	M14	V_{DD_INT}	N06
GND	K08	LDAT1_3	L18	V_{DD_EXT}	M18	V_{DD_INT}	N07
GND	K09	LDAT1_4	M16	V_{DD_EXT}	N05	V_{DD_INT}	N08
GND	K10	LDAT1_5	M17	V_{DD_EXT}	N10	V_{DD_INT}	N09
GND	K11	LDAT1_6	N16	V_{DD_EXT}	P06	V_{DD_INT}	N13
GND	K12	LDAT1_7	P16	V_{DD_EXT}	P08	V_{REF}	D04
GND	L07	NC	K03	V_{DD_EXT}	P10	V_{REF}	D11
GND	L08	NC	K04	V_{DD_EXT}	P12	XTAL	K01
GND	L09	NC	L02	V_{DD_EXT}	P14		
GND	L10	NC	L03	V_{DD_EXT}	P15		
GND	L11	NC	L04	V_{DD_EXT}	T08		
GND	L12	$\overline{\text{RESET}}$	M01	V_{DD_EXT}	T09		
GND	L14	$\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$	M02	V_{DD_EXT}	U08		
GND	M05	TCK	K15	V_{DD_EXT}	U09		
GND	M07	TDI	L15	V_{DD_EXT}	V08		
GND	M08	TDO	M15	V_{DD_EXT}	V09		
GND	M09	THD_M	N12	V_{DD_INT}	D12		
GND	M10	THD_P	N11	V_{DD_INT}	E06		
GND	M11	TMS	K16	V_{DD_INT}	E08		
GND	M12	$\overline{\text{TRST}}$	N15	V_{DD_INT}	E09		
GND	N14	VDD_A	H01	V_{DD_INT}	E14		
GND	N17	V_{DD_DDR2}	C05	V_{DD_INT}	E15		
GND	P05	V_{DD_DDR2}	C12	V_{DD_INT}	F06		
GND	P07	V_{DD_DDR2}	D03	V_{DD_INT}	F07		
GND	P09	V_{DD_DDR2}	D06	V_{DD_INT}	F08		
GND	P11	V_{DD_DDR2}	D08	V_{DD_INT}	F09		
GND	P13	V_{DD_DDR2}	D18	V_{DD_INT}	F10		
GND	R09	V_{DD_DDR2}	E02	V_{DD_INT}	F11		

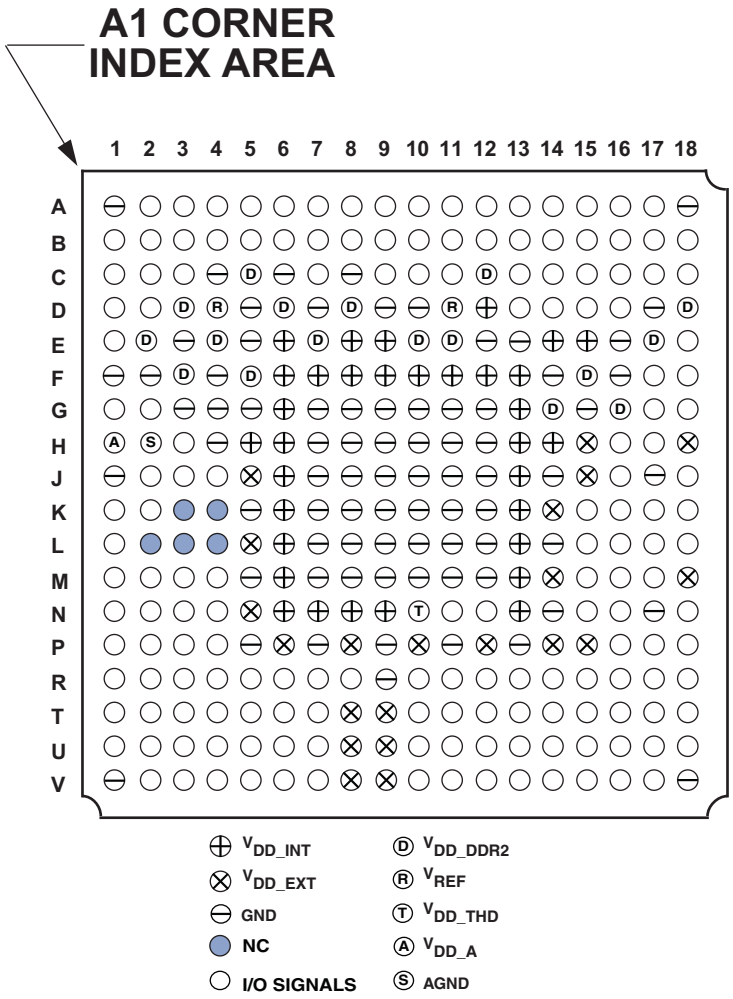
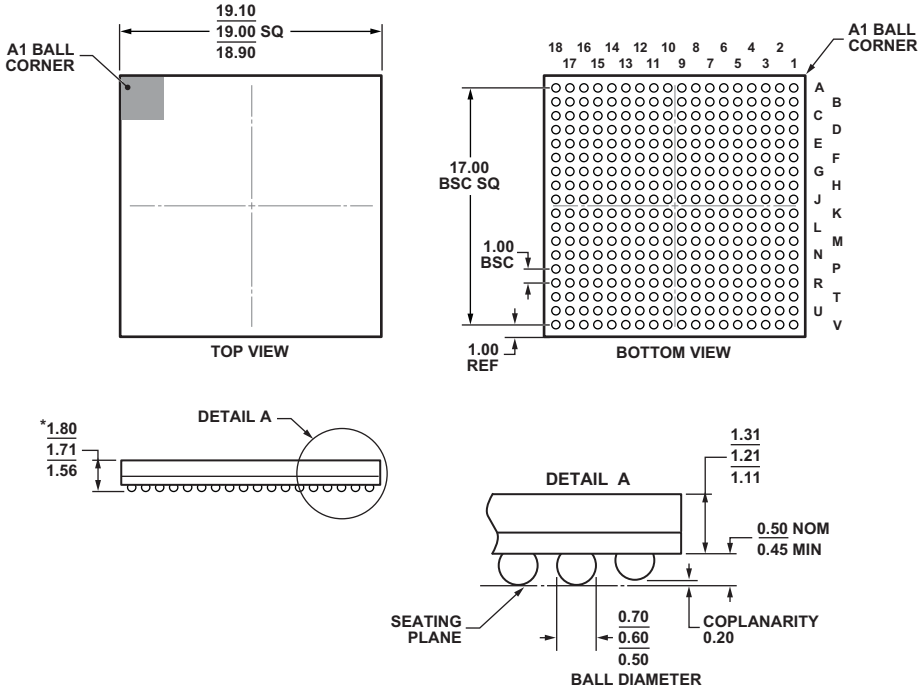


Figure 51. ADSP-21467/ADSP-21469 Ball Configuration - Pin Out

OUTLINE DIMENSIONS

The ADSP-2146x processors are available in a 19 mm by 19 mm CSP_BGA lead-free package.



*COMPLIANT TO JEDEC STANDARDS MO-192-AAG-1 WITH THE EXCEPTION TO PACKAGE HEIGHT.

Figure 52. 324-Ball Plastic Ball Grid Array [CSP_BGA] (BC-324-1)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

The following table is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard.*

Package	Package Ball Attach Type	Package Metal Pad	Package Solder Mask Opening	Package Ball Pad Size
324-Ball CSP_BGA (BC-324-1)	Solder Mask Defined	0.60 mm on laminate	0.43 mm diameter	0.6 mm diameter

AUTOMOTIVE PRODUCTS

The ADSP-21462W, ADSP-21465W, and ADSP-21469W are available for automotive applications with controlled manufacturing. Note that these special models may have specifications that differ from the general release models.

The automotive grade products shown in Table 54 are available for use in automotive applications. Contact your local ADI account representative or authorized ADI product distributor for specific product ordering information. Note that all automotive products are RoHS compliant.

Table 54. Automotive Products

Model [1]	Temperature Range[2]	On-Chip SRAM	ROM	Package Description	Package Option
AD21462WBCZ3xx	–40°C to +85°C	5M bit	N/A	324-Ball Grid Array (CSP_BGA)	BC-324-1
AD21465WBCZ3xx	–40°C to +85°C	5M bit	4M bit	324-Ball Grid Array (CSP_BGA)	BC-324-1
AD21469WBCZ3xx	–40°C to +85°C	5M bit	N/A	324-Ball Grid Array (CSP_BGA)	BC-324-1

[1] Z =RoHS Compliant Part
[2] Referenced temperature is ambient temperature.

ORDERING GUIDE

Model [1]	Temperature Range[2]	On-Chip SRAM	ROM	Package Description	Package Option
ADSP-21462BBCZ-ENG	–40 °C to +85 °C	5 Mbit	4 Mbit	324-Ball Grid Array (CSP_BGA)	BC-324-1
ADSP-21467KBCZ-ENG[3]	0 °C to +70 °C	5 Mbit	4 Mbit	324-Ball Grid Array (CSP_BGA)	BC-324-1
ADSP-21469KBCZ-ENG	0 °C to +70 °C	5 Mbit	N/A	324-Ball Grid Array (CSP_BGA)	BC-324-1

[1] Z =RoHS Compliant Part.
[2] Referenced temperature is ambient temperature.
[3] Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at www.analog.com/SHARC.

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