LM4911/LM4911Q Boomer® Audio Power Amplifier Series Stereo 40mW Low Noise Headphone Amplifier with Selectable Capacitive Coupled or OCL Output

Check for Samples: LM4911, LM4911Q

FEATURES

- OCL or Capacitively Coupled Outputs (Patent Pending)
- External Gain-Setting Capability
- Available in Space-Saving VSSOP and WSON Packages
- Ultra Low Current Shutdown Mode
- Mute Mode Allows Fast Turn-on (1ms) with Less Than 1mV Change on Outputs
- 2V - 5.5V Operation
- Ultra Low Noise
- LM4911QMM is an Automotive Grade Product that is AEC-Q100 Grade 2 Qualified.

APPLICATIONS

- Portable CD Players
- PDAs
- Portable Electronics Devices
- Automotive

KEY SPECIFICATIONS

- PSRR at 217Hz and 1kHz 65 dB (typ)
- Output Power at 1kHz with V_{DD} = 2.4V, 1% THD+N into a 16Ω Load 25 mW (typ)
- Output Power at 1kHz with V_{DD} = 3V, 1% THD+N into a 16Ω Load 40 mW (typ)
- Shutdown Current 2.0 µA (max)
- Output Voltage Change on Release from Shutdown V_{DD} = 2.4V, R_L = 16Ω (C-Coupled) 1 mV (max)
- Mute Current 100 µA (max)

DESCRIPTION

The LM4911/LM4911Q is an stereo audio power amplifier capable of delivering 40mW per channel of continuous average power into a 16Ω load or 25mW per channel into a 32Ω load at 1% THD+N from a 3V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. Since the LM4911/LM4911Q does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems. In addition, the LM4911/LM4911Q may be configured for either single-ended capacitively coupled outputs or for OCL outputs (patent pending).

Block Diagram

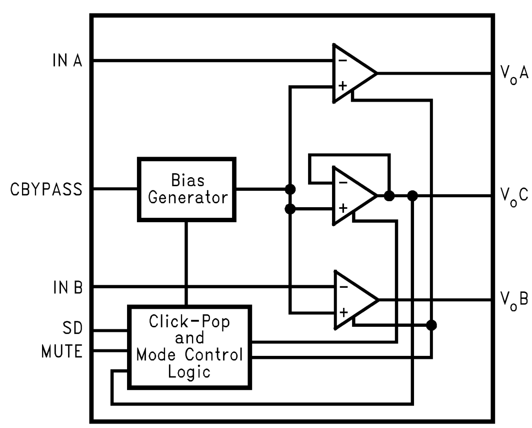

Figure 1. Block Diagram

DESCRIPTION (CONTINUED)

The LM4911/LM4911Q features a low-power consumption shutdown mode and a power mute mode that allows for faster turn on time with less than 1mV voltage change at outputs on release. Additionally, the LM4911/LM4911Q features an internal thermal shutdown protection mechanism.

The LM4911/LM4911Q is unity gain stable and may be configured with external gain-setting resistors.

A Q-grade version is available for automotive applications. It is AEC-Q100 grade 2 qualified and packaged in a 10–pin VSSOP package (LM4911QMM).

Typical Application

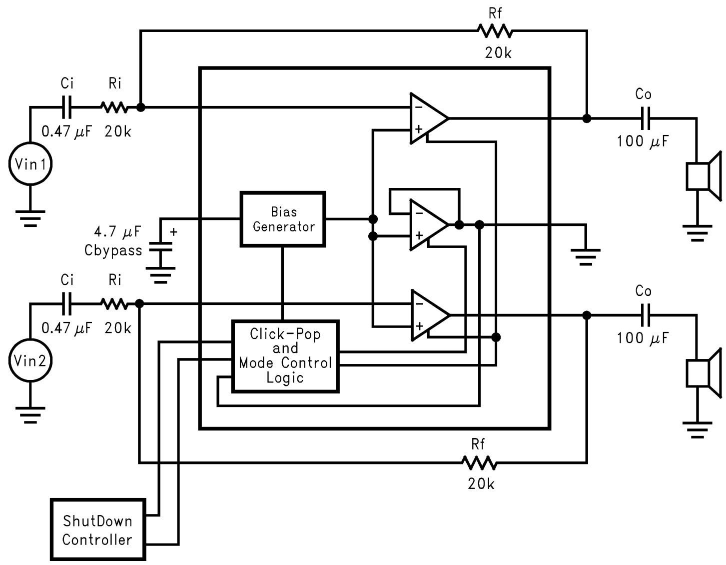

Figure 2. Typical Capacitive Coupled Output Configuration Circuit

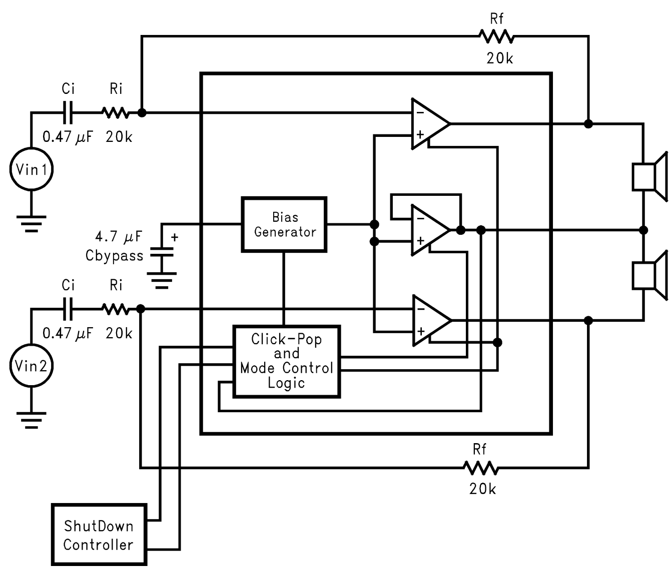

Figure 3. Typical OCL Output Configuration Circuit

Connection Diagram

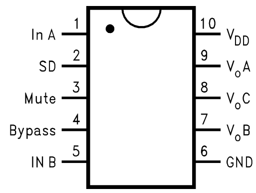

Figure 4. VSSOP Package (Top View)
See Package Number DGS0010A

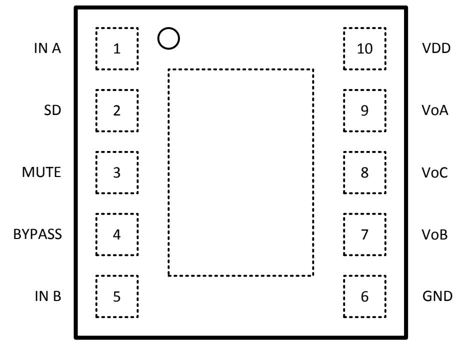

Figure 5. WSON Package (Top View)
See Package Number NGY0010A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage		-0.3V to V_{DD} + 0.3V
Power Dissipation (3)		Internally Limited
ESD Susceptibility (4)		2000V
ESD Susceptibility (5)		200V
Junction Temperature		150°C
Thermal Resistance	θ_{JC} (VSSOP)	56°C/W
	θ_{JA} (VSSOP)	190°C/W
	θ_{JA} (WSON) (6)	63°C/W
	θ_{JA} (WSON) (6)	12°C/W

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional but do not ensure specific performance limits.*Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensures specific performance limits. This assumes that the device is within the *Operating Ratings*. Specifications are not ensured for parameters where no limit is given; however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower. For the LM4911/LM4911Q, see power derating currents for more information.
(4) Human body model, 100pF discharged through a 1.5kΩ resistor.
(5) Machine Model, 220pF-240pF discharged through all pins.
(6) The NGY0010A package has its exposed-DAP soldered to an exposed 1.2in^2 area of 1oz. Printed circuit board copper.

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$ (LM4911MM)	$-40°C \le T_A \le 85°C$
	$T_{MIN} \le T_A \le T_{MAX}$ (LM4911QMM)	$-40°C \le T_A \le 105°C$
Supply Voltage (V_{DD})		$2V \le V_{CC} \le 5.5V$

Electrical Characteristics V_{DD} = 5.0V [(1)(2)(3)]

The following specifications apply for V_{DD} = 5V, R_L = 16Ω, and C_B = 4.7µF unless otherwise specified. Limits apply to T_A = 25°C.

Symbol	Parameter	Conditions	LM4911		LM4911Q		Units (Limits)
			Typ [(4)]	Limit [(5)]	Typ [(4)]	Limit [(5)]	
I_{DD}	Quiescent Current	V_{IN} = 0V, I_O = 0A					
		T_A = +25°C	2	5	2	5	mA (max)
		T_A = –40°C to +105°C				6	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND	0.1	2	0.1	2	µA (max)
I_M	Mute Current	V_{MUTE} = V_{DD}, C-Coupled					
		T_A = +25°C	50	100	50	100	µA (max)
		T_A = –40°C to +105°C				150	µA (max)
V_{SDIH}	Shutdown Voltage Input High	T_A = –40°C to +105°C	1.8			1.8	V
V_{SDIL}	Shutdown Voltage Input Low	T_A = –40°C to +105°C	0.4			0.4	V
V_{MIH}	Mute Voltage Input High	T_A = –40°C to +105°C	1.8			1.8	V
V_{MIL}	Mute Voltage Input Low	T_A = –40°C to +105°C	0.4			0.4	V
P_O	Output Power	THD ≤ 1%, f 1kHz					
		OCL, $_{RLOAD}$ = 16Ω	80				mW (max)
		LM4911/LM4911QLD OCL, R_{LOAD} = 16Ω [(6)]	145				mW (max)
		OCL, R_{LOAD} = 32Ω	80				mW (max)
		C-CUPL, R_{LOAD} = 16Ω					
		T_A = +25°C	145	134	145		mW (min)
		T_A = –40°C to +105°C				130	mW (min)
		C-CUPL, R_{LOAD} = 32Ω	85				mW (max)
THD+N	Total Harmonic Distortion + Noise	P_O = 15.3mW, f = 1kHz	0.1	0.5	0.1	0.5	% (max) [(7)]
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV sine p-p f = 1kHz [(8)]	65		65		dB
V_{ON}	Output Noise Voltage	BW = 20Hz to 20kHz, A-weighted	10		10		µV

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional but do not ensure specific performance limits.*Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensures specific performance limits. This assumes that the device is within the *Operating Ratings*. Specifications are not ensured for parameters where no limit is given; however, the typical value is a good indication of device performance.
(3) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(4) Typicals are measured at 25°C and represent the parametric norm.
(5) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(6) The NGY0010A package has its exposed-DAP soldered to an exposed 1.2in^2 area of 1oz. Printed circuit board copper.
(7) The limit is specified over the temperature range of –40°C to +85°C.
(8) 10Ω terminated input.

Electrical Characteristics V_{DD} = 3.3V (1)(2)(3)

The following specifications apply for V_{DD} = 3.3V, R_L = 16Ω, and C_B = 4.7µF unless otherwise specified. Limits apply to T_A = 25°C.

Symbol	Parameter	Conditions	LM4911		LM4911Q		Units (Limits)
			Typ (4)	Limit (5)	Typ (4)	Limit (5)	
I_{DD}	Quiescent Current	V_{IN} = 0V, I_O = 0A					
		T_A = +25°C	1.5	3	1.5	3	mA (max)
		T_A = –40°C to +105°C				4	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND					
		T_A = +25°C	0.1	2	0.1	2	µA (max)
		T_A = –40°C to +105°C				4	µA (max)
I_M	Mute Current	V_{MUTE} = V_{DD}, C-Coupled					
		T_A = +25°C	50	100	50	100	µA (max)
		T_A = –40°C to +105°C				125	µA (max)
V_{SDIH}	Shutdown Voltage Input High	T_A = –40°C to +105°C	1.8			1.8	V
V_{SDIL}	Shutdown Voltage Input Low	T_A = –40°C to +105°C	0.4			0.4	V
V_{MIH}	Mute Voltage Input High	T_A = –40°C to +105°C	1.8			1.8	V
V_{MIL}	Mute Voltage Input Low	T_A = –40°C to +105°C	0.4			0.4	V
P_O	Output Power	THD ≤ 1%, `C-CUPL, R_L = 16Ω					
		T_A = +25°C	60	55	60	55	mW (min)
		T_A = –40°C to +105°C				50	mW (min)
THD+N	Total Harmonic Distortion + Noise	P_O = 15.3mW, f = 1kHz	0.1	0.5	0.1	0.5	% (max) (6)
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV sine p-p f = 1kHz (7)	65		65		dB
V_{ON}	Output Noise Voltage	BW = 20Hz to 20kHz, A-weighted	10		10		µV

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional but do not ensure specific performance limits.*Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensures specific performance limits. This assumes that the device is within the *Operating Ratings*. Specifications are not ensured for parameters where no limit is given; however, the typical value is a good indication of device performance.
(3) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(4) Typicals are measured at 25°C and represent the parametric norm.
(5) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(6) The limit is specified over the temperature range of –40°C to +85°C.
(7) 10Ω terminated input.

Electrical Characteristics V_{DD} = 3.0V [(1)(2)(3)]

The following specifications apply for V_{DD} = 3.0V, R_L = 16Ω, and C_B = 4.7µF unless otherwise specified. Limits apply to T_A = 25°C.

Symbol	Parameter	Conditions	LM4911		LM4911Q		Units (Limits)
			Typ [(4)]	Limit [(5)]	Typ [(4)]	Limit [(5)]	
I_{DD}	Quiescent Current	V_{IN} = 0V, I_O = 0A					
		T_A = +25°C	1.5	3	1.5	3	mA (max)
		T_A = –40°C to +105°C				4	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND	0.1	2	0.1	2	µA (max)
I_M	Mute Current	V_{MUTE} = V_{DD}, C-Coupled					
		T_A = +25°C	50	100	50	100	µA (max)
		T_A = –40°C to +105°C				120	µA (max)
V_{SDIH}	Shutdown Voltage Input High	T_A = –40°C to +105°C	1.8			1.8	V
V_{SDIL}	Shutdown Voltage Input Low	T_A = –40°C to +105°C	0.4			0.4	V
V_{MIH}	Mute Voltage Input High	T_A = –40°C to +105°C	1.8			1.8	V
V_{MIL}	Mute Voltage Input Low	T_A = –40°C to +105°C	0.4			0.4	V
P_O	Output Power	THD ≤ 1%; C-CUPL, R_L = 16Ω					
		T_A = +25°C	40		40	35	mW (min)
		T_A = –40°C to +105°C				30	mW (min)
		THD ≤ 1%, f = 1kHz, R_L = 32Ω	25				mW (min)
THD+N	Total Harmonic Distortion + Noise	P_O = 15.3mW, f = 1kHz	0.1	0.5	0.1	0.5	% (max) [(6)]
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV sine p-p f = 1kHz [(7)]	65		65		dB
V_{ON}	Output Noise Voltage	BW = 20 Hz to 20kHz, A-weighted	10		10		µV

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional but do not ensure specific performance limits.*Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensures specific performance limits. This assumes that the device is within the *Operating Ratings*. Specifications are not ensured for parameters where no limit is given; however, the typical value is a good indication of device performance.
(3) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(4) Typicals are measured at 25°C and represent the parametric norm.
(5) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(6) The limit is specified over the temperature range of –40°C to +85°C.
(7) 10Ω terminated input.

Electrical Characteristics V_{DD} = 2.4V (1)(2)(3)

The following specifications apply for V_{DD} = 2.4V, R_L = 16Ω, and C_B = 4.7µF unless otherwise specified. Limits apply to T_A = 25°C.

Symbol	Parameter	Conditions	LM4911		LM4911Q		Units (Limits)
			Typ (4)	Limit (5)	Typ (4)	Limit (5)	
I_{DD}	Quiescent Current	V_{IN} = 0V, I_O = 0A					
		T_A = +25°C	1.5	3	1.5	3	mA (max)
		T_A = –40°C to +105°C				4	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND	0.1	2	0.1	2	µA (max)
I_M	Mute Current	V_{MUTE} = V_{DD}, C-Coupled					
		T_A = +25°C	40	80	40	80	µA (max)
		T_A = –40°C to +105°C				100	µA (max)
V_{SDIH}	Shutdown Voltage Input High	T_A = –40°C to +105°C	1.8			1.8	V
V_{SDIL}	Shutdown Voltage Input Low	T_A = –40°C to +105°C	0.4			0.4	V
V_{MIH}	Mute Voltage Input High	T_A = –40°C to +105°C	1.8			1.8	V
V_{MIL}	Mute Voltage Input Low		0.4			0.4	V
P_O	Output Power	THD = 1%; C-CUPL, R_L = 16Ω					
		T_A = +25°C	25		25	20	mW (min)
		T_A = –40°C to +105°C				15	mW (min)
		THD ≤1%; R_L = 32Ω, f = 1kHz	12		12		
THD+N	Total Harmonic Distortion + Noise	P_O = 15.3mW, f = 1kHz	0.1	0.5	0.1	0.5	% (max) (6)
T_{WU}	Wake Up Time	OCL	0.5		0.5		s
		C-Coupled, C_O = 100µF	2		2		s
T_{UM}	Un-mute Time	C-Coupled, C_O= 100µF	0.01	0.02	0.01	0.02	s (max)
V_{OSD}	Output Voltage Change on Release from Shutdown	C-Coupled, C_O= 100µF		1		1	mV (max)
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV sine p-p f = 1kHz (7)	65		65		dB
V_{ON}	Output Noise Voltage	BW = 20 Hz to 20kHz, A-weighted	10		10		dB

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional but do not ensure specific performance limits.*Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensures specific performance limits. This assumes that the device is within the *Operating Ratings*. Specifications are not ensured for parameters where no limit is given; however, the typical value is a good indication of device performance.
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(4) Typicals are measured at 25°C and represent the parametric norm.
(5) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(6) The limit is specified over the temperature range of –40°C to +85°C.
(7) 10Ω terminated input.

External Components Description

(Figure 2)

Components		Functional Description
1.	R_I	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high-pass filter with C_i at $f_c = 1/(2\pi R_i C_i)$.
2.	C_I	Input coupling capacitor which blocks the DC voltage at the amplifier's input terminals. Also creates a high-pass filter with R_i at $f_c = 1/(2\pi R_i C_i)$. Refer to the section Proper Selection of External Components, for an explanation of how to determine the value of C_i.
3.	R_f	Feedback resistance which sets the closed-loop gain in conjunction with R_i.
4.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the Power Supply section for information concerning proper placement and selection of the supply bypass capacitor.
5.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, Proper Selection of External Components, for information concerning proper placement and selection of C_B
6.	C_o	Output coupling capacitor which blocks the DC voltage at the amplifier's output. Forms a high pass filter with R_L at $f_o = 1/(2\pi R_L C_o)$

Typical Performance Characteristics

THD+N vs Frequency

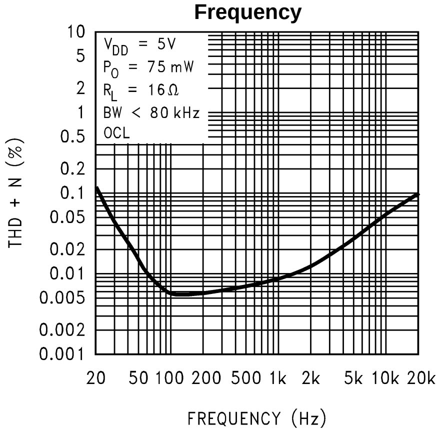

Figure 6.

THD+N vs Frequency

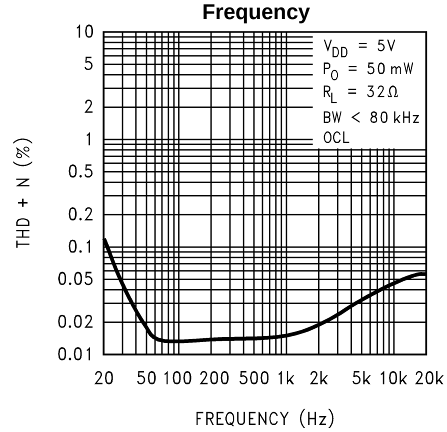

Figure 7.

THD+N vs Frequency

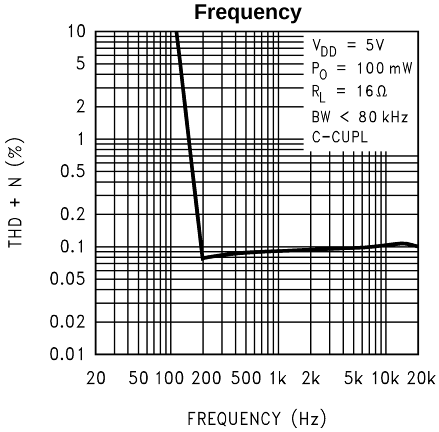

Figure 8.

THD+N vs Frequency

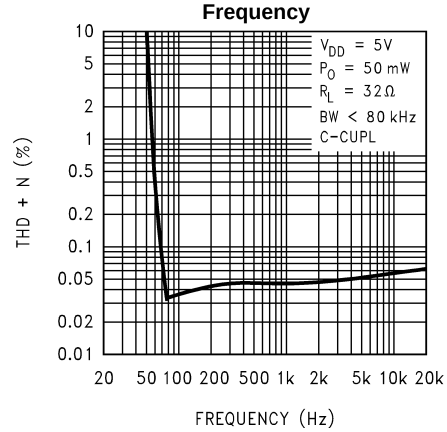

Figure 9.

THD+N vs Frequency

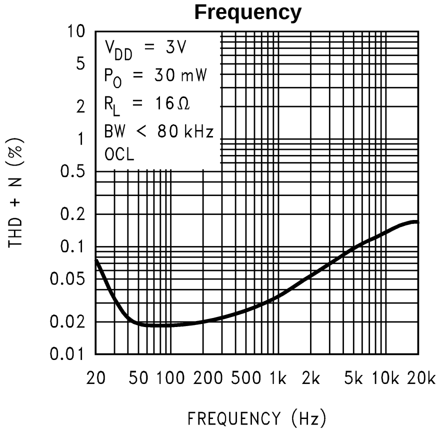

Figure 10.

THD+N vs Frequency

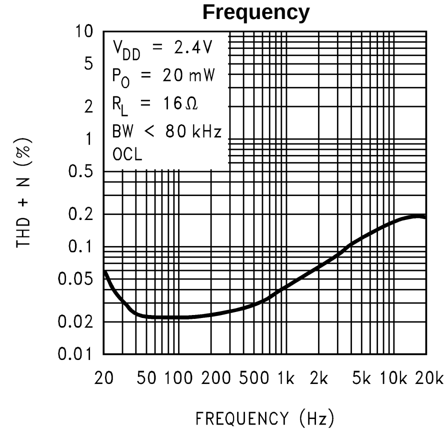

Figure 11.

Typical Performance Characteristics (continued)

THD+N vs Frequency

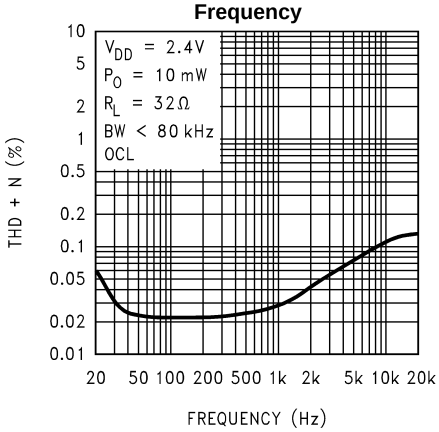

Figure 12.

THD+N vs Frequency

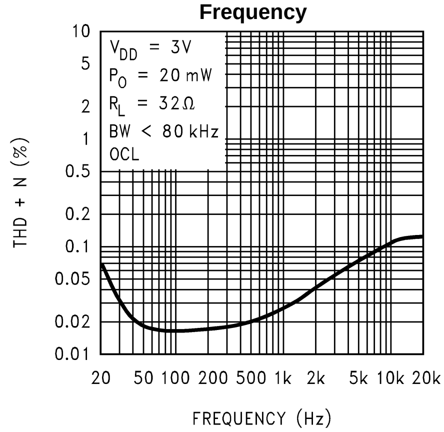

Figure 13.

THD+N vs Frequency

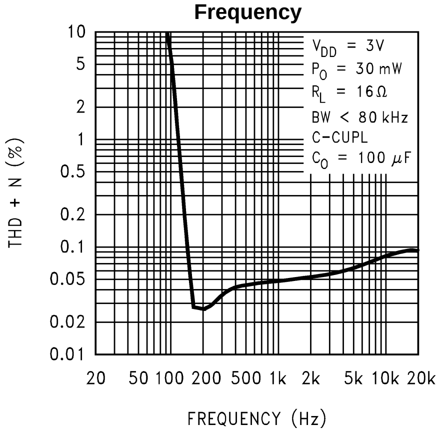

Figure 14.

THD+N vs Frequency

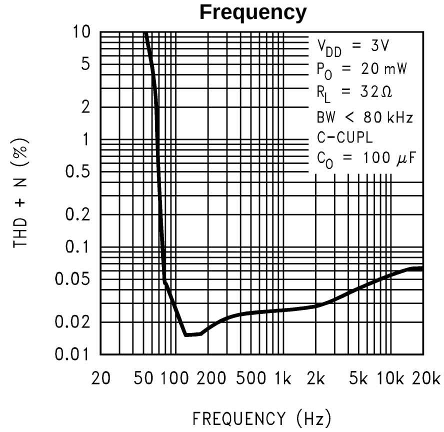

Figure 15.

THD+N vs Frequency

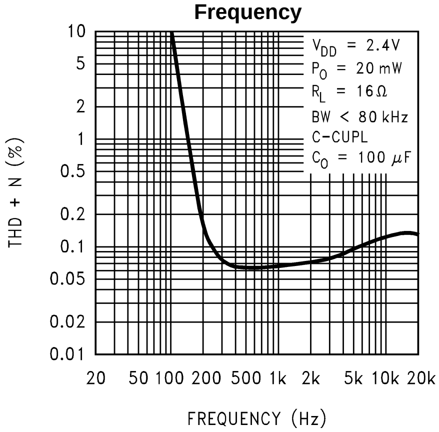

Figure 16.

THD+N vs Frequency

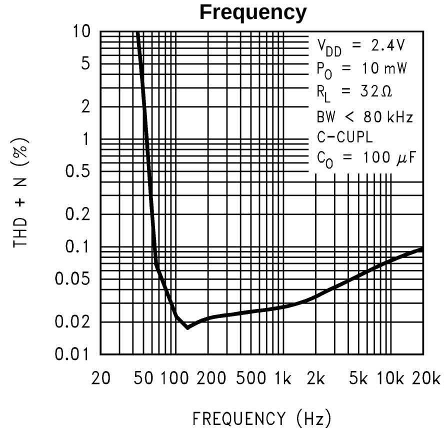

Figure 17.

Typical Performance Characteristics (continued)

THD+N vs Output Power

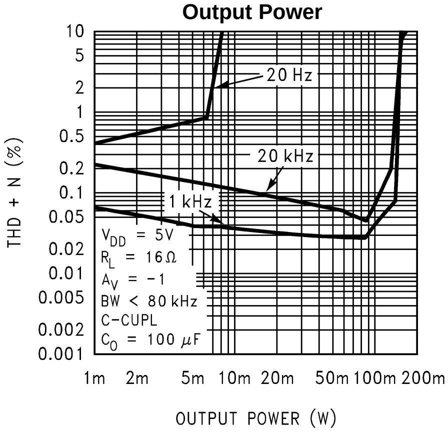

Figure 18.

THD+N vs Output Power

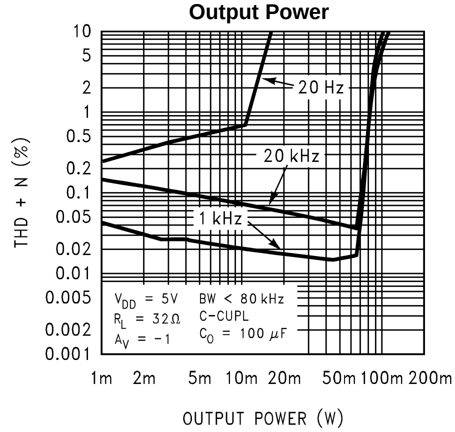

Figure 19.

THD+N vs Output Power

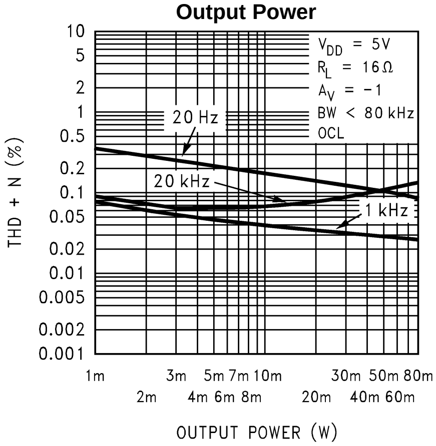

Figure 20.

THD+N vs Output Power

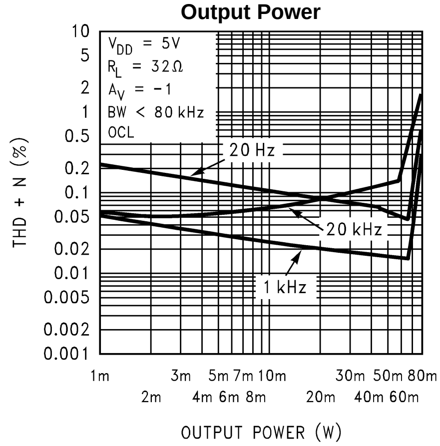

Figure 21.

THD+N vs Output Power

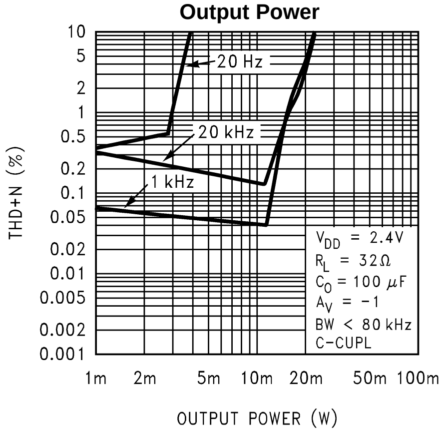

Figure 22.

THD+N vs Output Power

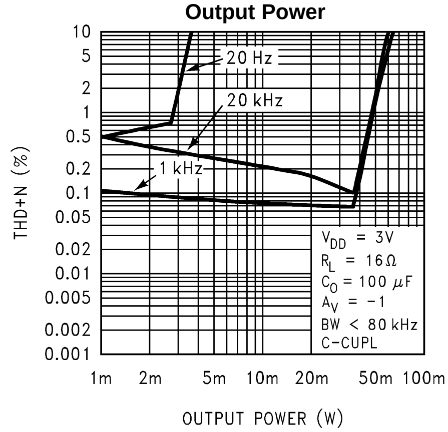

Figure 23.

Typical Performance Characteristics (continued)

THD+N vs Output Power

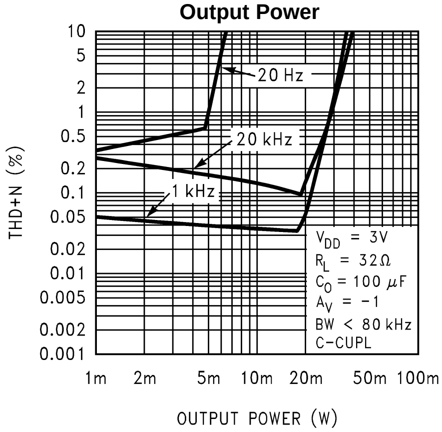

Figure 24.

THD+N vs Output Power

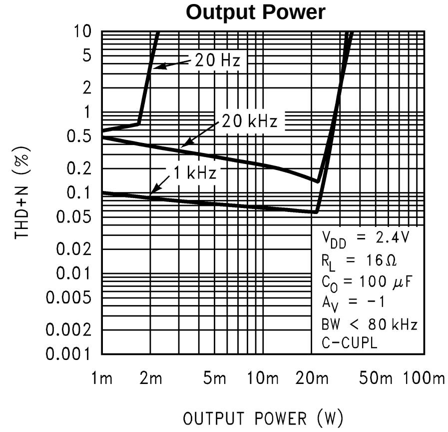

Figure 25.

Output Resistance vs Load Resistance

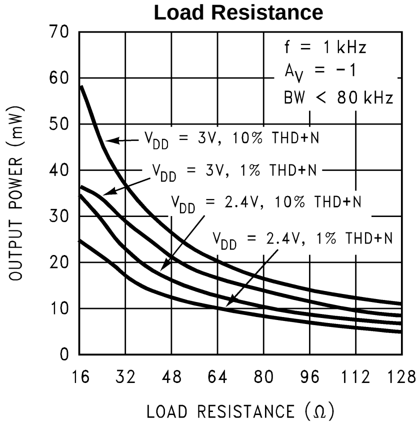

Figure 26.

Output Power vs Supply Voltage

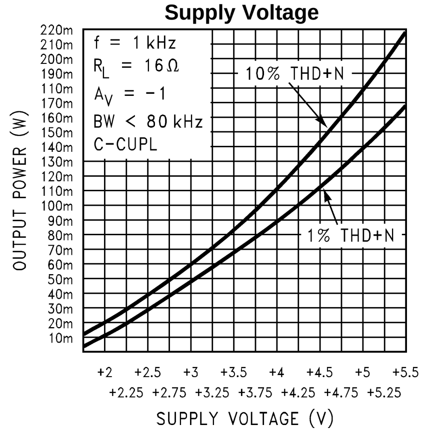

Figure 27.

Output Power vs Supply Voltage

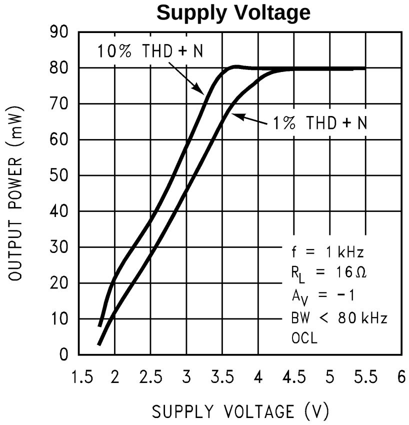

Figure 28.

Output Power vs Supply Voltage

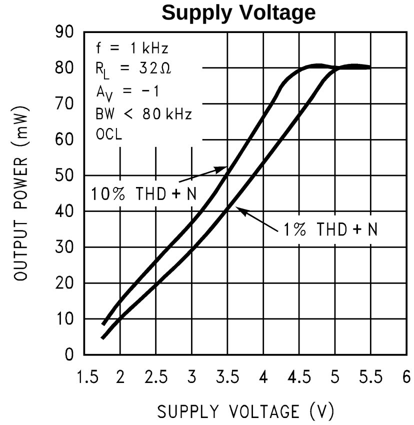

Figure 29.

Typical Performance Characteristics (continued)

Output Power vs Supply Voltage

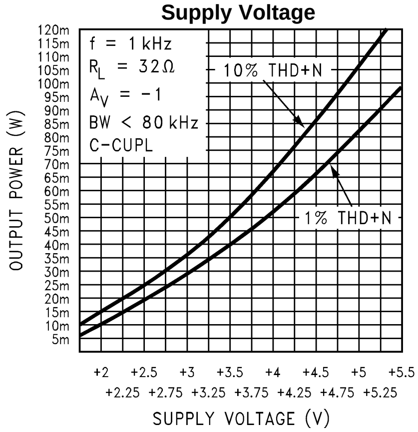

Figure 30.

Output Power vs Load Resistance

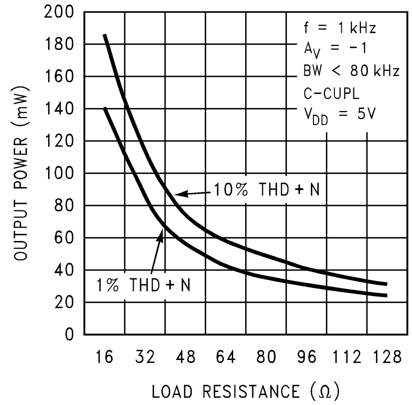

Figure 31.

Output Power vs Load Resistance

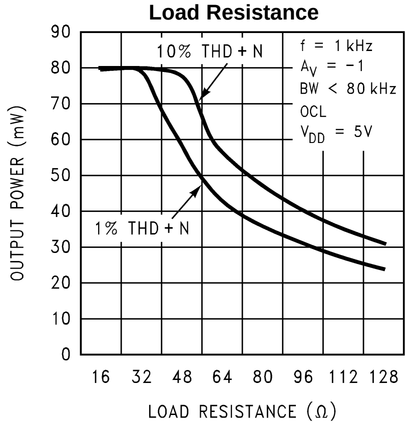

Figure 32.

Power Dissipation vs. Output Power

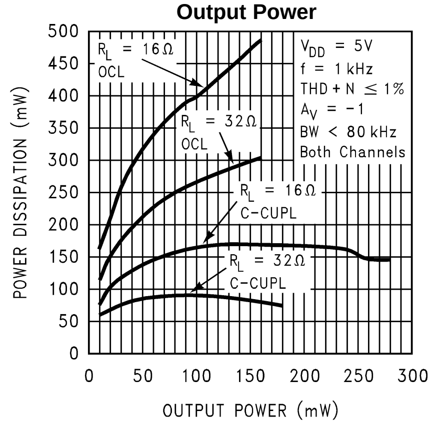

Figure 33.

Power Dissipation vs. Output Power

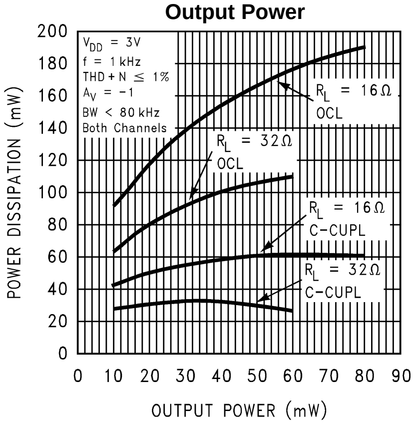

Figure 34.

Power Dissipation vs Output Power

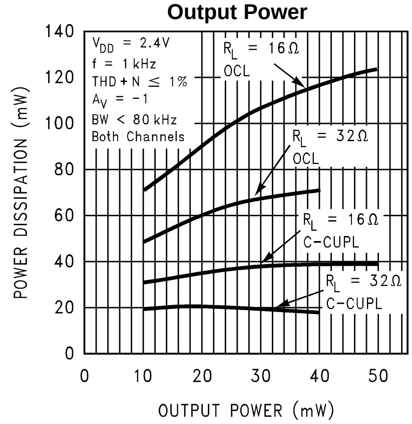

Figure 35.

Typical Performance Characteristics (continued)

Channel Separation

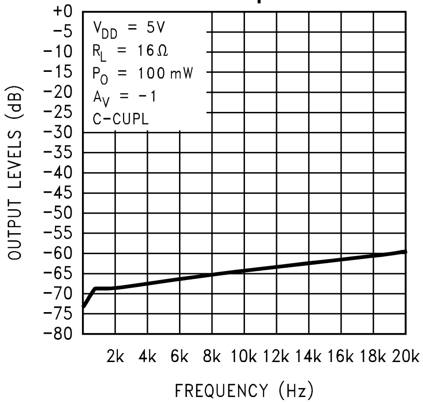

Figure 36.

Channel Separation

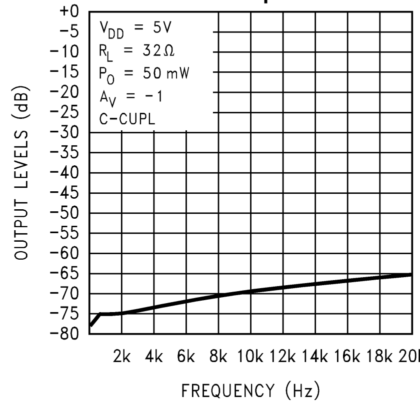

Figure 37.

Channel Separation

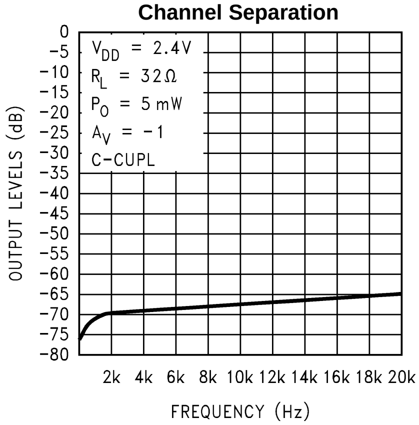

Figure 38.

Channel Separation

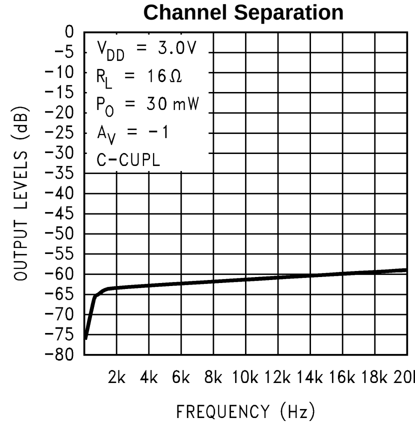

Figure 39.

Channel Separation

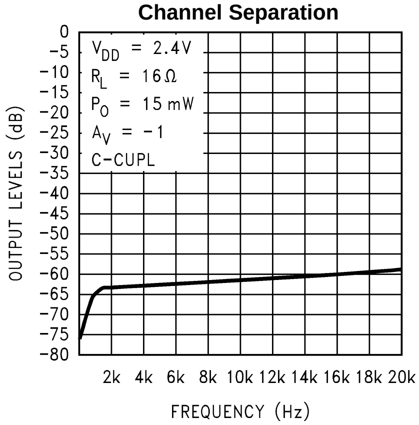

Figure 40.

Channel Separation

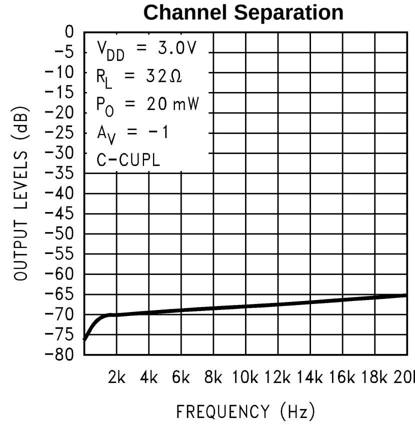

Figure 41.

Typical Performance Characteristics (continued)

Power Supply Rejection Ratio

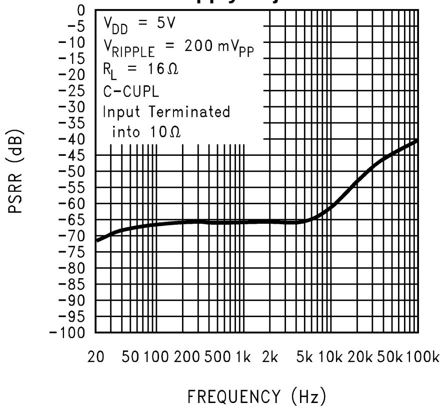

Figure 42.

Power Supply Rejection Ratio

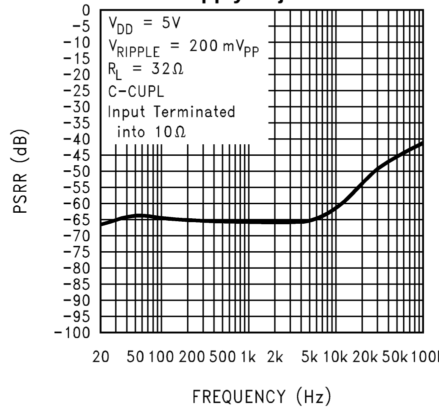

Figure 43.

Power Supply Rejection Ratio

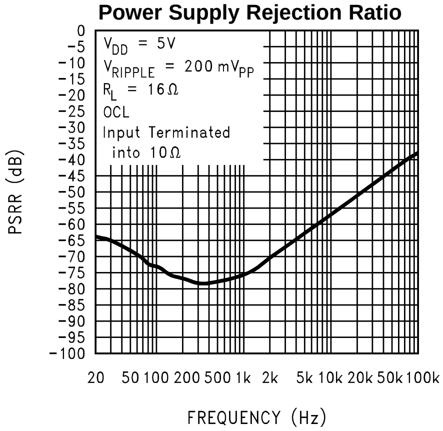

Figure 44.

Power Supply Rejection Ratio

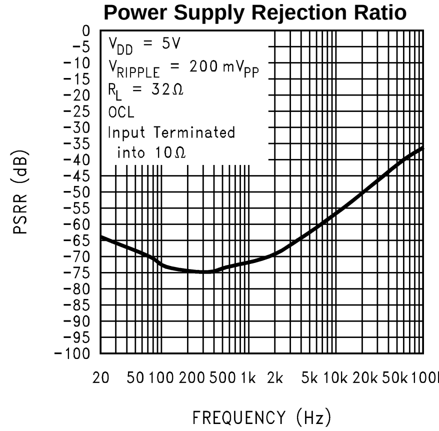

Figure 45.

Power Supply Rejection Ratio

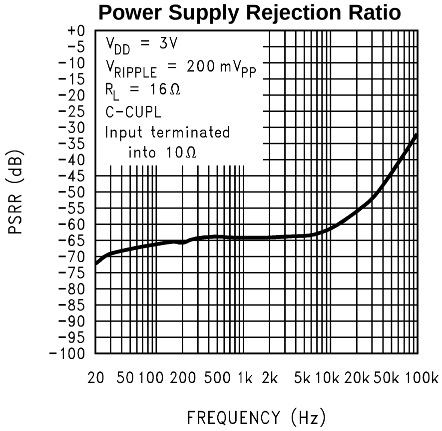

Figure 46.

Power Supply Rejection Ratio

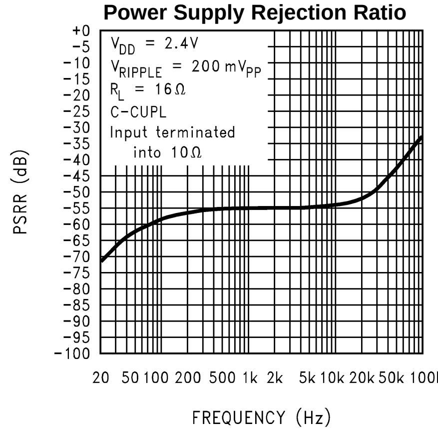

Figure 47.

Typical Performance Characteristics (continued)

Power Supply Rejection Ratio

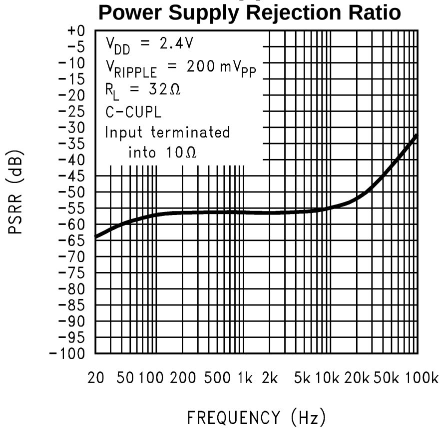

Figure 48.

Power Supply Rejection Ratio

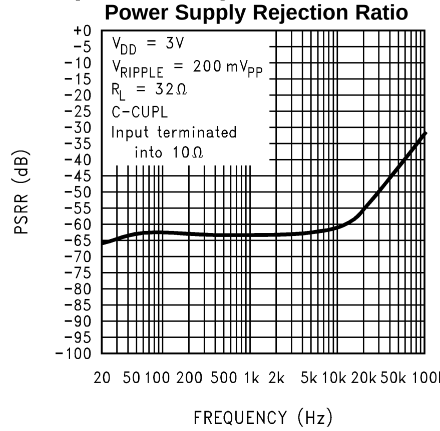

Figure 49.

Frequency Response vs Input Capacitor Size

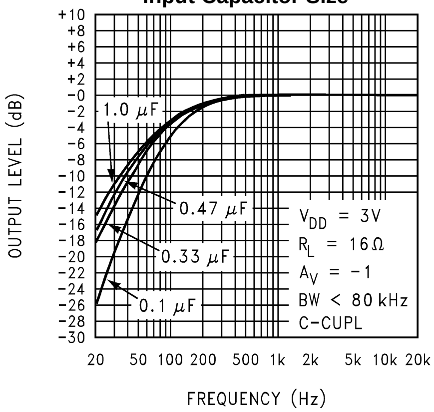

Figure 50.

Frequency Response vs Input Capacitor Size

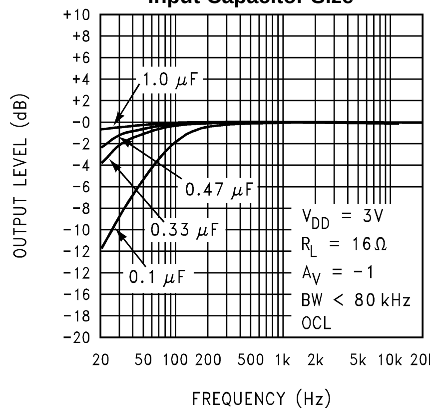

Figure 51.

Open Loop Frequency Response

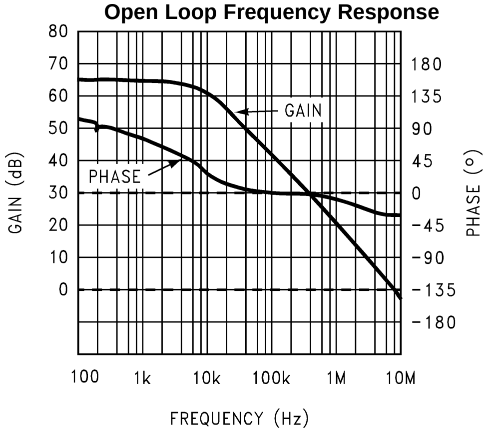

Figure 52.

Supply Voltage vs Supply Current

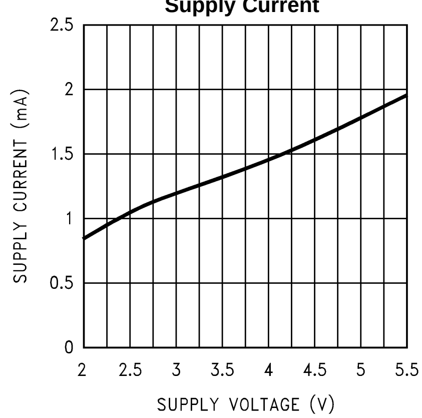

Figure 53.

Typical Performance Characteristics (continued)

Clipping Voltage vs Supply Voltage

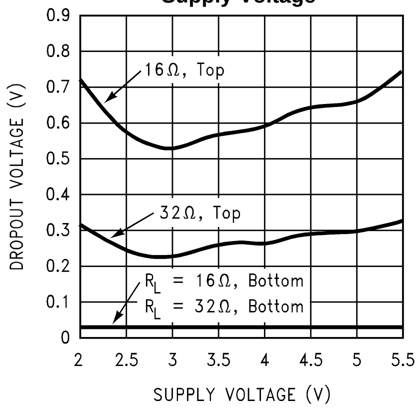

Figure 54.

Noise Floor

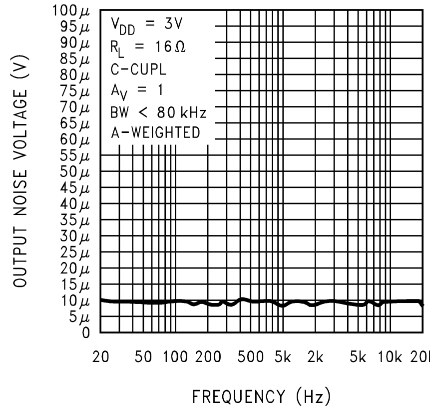

Figure 55.

Shutdown Hysteresis Voltage, Vdd=5V

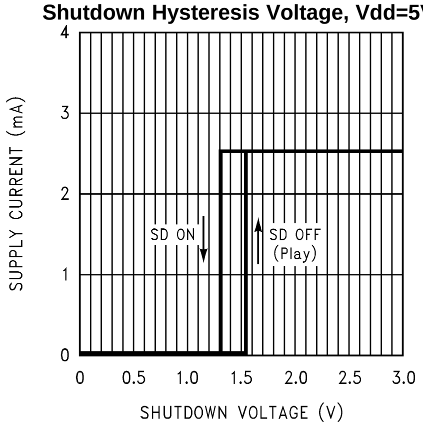

Figure 56.

Shutdown Hysteresis Voltage, Vdd=3V

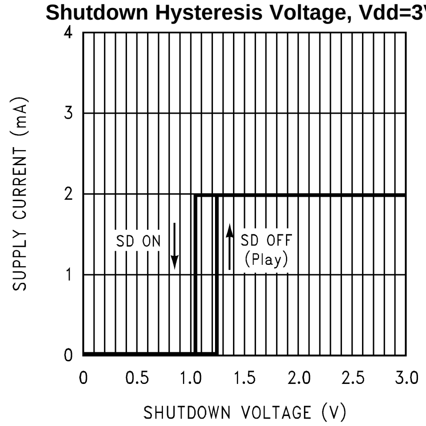

Figure 57.

Power Derating Curve

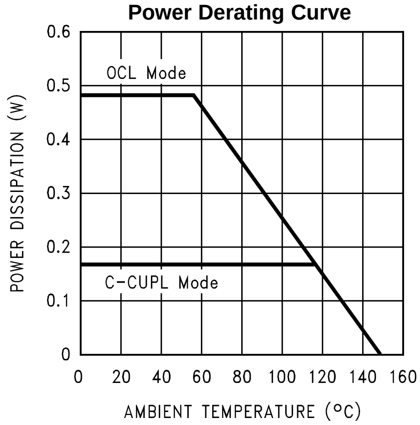

Figure 58.

Typical Performance Characteristics LM4911/LM4911Q Specific Characteristics

The NGY0010A package has its exposed-DAP soldered to an exposed 1.2in^2 area of 1oz. Printed circuit board copper.

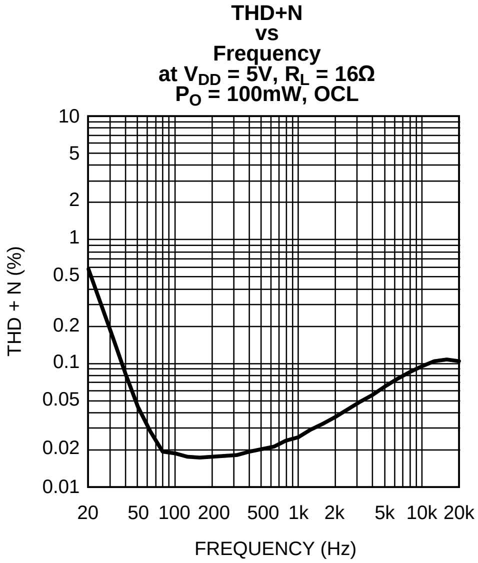

Figure 59.

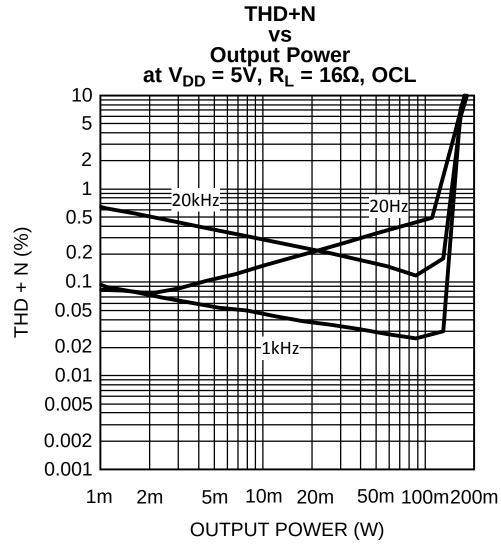

Figure 60.

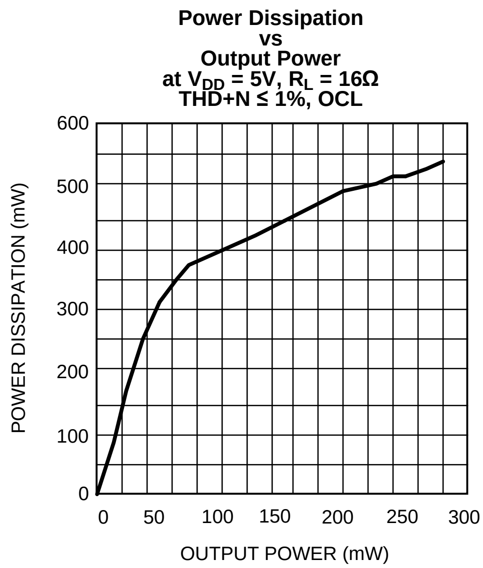

Figure 61.

APPLICATION INFORMATION

AMPLIFIER CONFIGURATION EXPLANATION

As shown in Figure 1, the LM4911/LM4911Q has three operational amplifiers internally. Two of the amplifier's have externally configurable gain while the other amplifier is internally fixed at the bias point acting as a unity-gain buffer. The closed-loop gain of the two configurable amplifiers is set by selecting the ratio of R_f to R_i. Consequently, the gain for each channel of the IC is:

$$A_{VD} = -(R_f / R_i)$$

By driving the loads through outputs V_oA and V_oB with V_oC acting as a buffered bias voltage the LM4911/LM4911Q does not require output coupling capacitors. The classical single-ended amplifier configuration where one side of the load is connected to ground requires large, expensive output coupling capacitors.

A configuration such as the one used in the LM4911/LM4911Q has a major advantage over single supply, single-ended amplifiers. Since the outputs V_oA, V_oB, and V_oC are all biased at 1/2 V_{DD}, no net DC voltage exists across each load. This eliminates the need for output coupling capacitors which are required in a single-supply, single-ended amplifier configuration. Without output coupling capacitors in a typical single-supply, single-ended amplifier, the bias voltage is placed across the load resulting in both increased internal IC power dissipation and possible loudspeaker damage.

OUTPUT CAPACITOR vs. CAPACITOR COUPLED

The LM4911/LM4911Q is an stereo audio power amplifier capable of operating in two distinct output modes: capacitor coupled (C-CUPL) or output capacitor-less (OCL). The LM4911/LM4911Q may be run in capacitor coupled mode by using a coupling capacitor on each single-ended output (V_oA and V_oB) and connecting V_oC to ground. This output coupling capacitor blocks the half supply voltage to which the output amplifiers are typically biased and couples the audio signal to the headphones or other single-ended (SE) load. The signal return to circuit ground is through the headphone jack's sleeve.

The LM4911/LM4911Q can also eliminate these output coupling capacitors by running in OCL mode. Unless shorted to ground, VoC is internally configured to apply a ½ V_{DD} bias voltage to a stereo headphone jack's sleeve. This voltage matches the bias voltage present on V_oA and V_oB outputs that drive the headphones. The headphones operate in a manner similar to a bridge-tied load (BTL). Because the same DC voltage is applied to both headphone speaker terminals this results in no net DC current flow through the speaker. AC current flows through a headphone speaker as an audio signal's output amplitude increases on the speaker's terminal.

The headphone jack's sleeve is not connected to circuit ground when used in OCL mode. Using the headphone output jack as a line-level output will place the LM4911/LM4911Q's ½ V_{DD} bias voltage on a plug's sleeve connection. This presents no difficulty when the external equipment uses capacitively coupled inputs. For the very small minority of equipment that is DC coupled, the LM4911/LM4911Q monitors the current supplied by the amplifier that drives the headphone jack's sleeve. If this current exceeds $500mA_{PK}$, the amplifier is shutdown, protecting the LM4911/LM4911Q and the external equipment.

MODE SELECT DETAIL

The LM4911/LM4911Q may be set up to operate in one of two modes: OCL and cap-coupled. The default state of the LM4911/LM4911Q at power up is cap-coupled. During initial power up or return from shutdown, the LM4911/LM4911Q must detect the correct mode of operation (OCL or cap-coupled) by sensing the status of the V_OC pin. When the bias voltage of the part ramps up to 60mV (as seen on the Bypass pin), an internal comparator detects the status of V_OC; and at 80mV, latches that value in place. Ramp up of the bias voltage will proceed at a different rate from this point on depending upon operating mode. OCL mode will ramp up about 11 times faster than cap-coupled. Shutdown is not a valid command during this time period (T_{WU}) and should not enabled to ensure a proper power on reset (POR) signal. In addition, the slew rate of V_{DD} must be greater than 2.5V/ms to ensure reliable POR. Recommended power up timing is shown in Figure 63 along with proper usage of Shutdown and Mute. The mode select circuit is suspended during C_B discharge time.

The circuit shown in Figure 62 presents an applications solution to the problem of using different supply voltages with different turn-on times in a system with the LM4911/LM4911Q. This circuit shows the LM4911/LM4911Q with a 25-50kΩ pull-up resistor connected from the shutdown pin to V_{DD}. The shutdown pin of the LM4911/LM4911Q is also being driven by an open drain output of an external microcontroller on a separate supply. This circuit ensures that shutdown is disabled when powering up the LM4911/LM4911Q by either allowing shutdown to be high before the LM4911/LM4911Q powers on (the microcontroller powers up first) or allows shutdown to ramp up with V_{DD} (the LM4911/LM4911Q powers up first). This will ensure the LM4911/LM4911Q powers up properly and enters the correct mode of operation (cap-coupled or OCL).

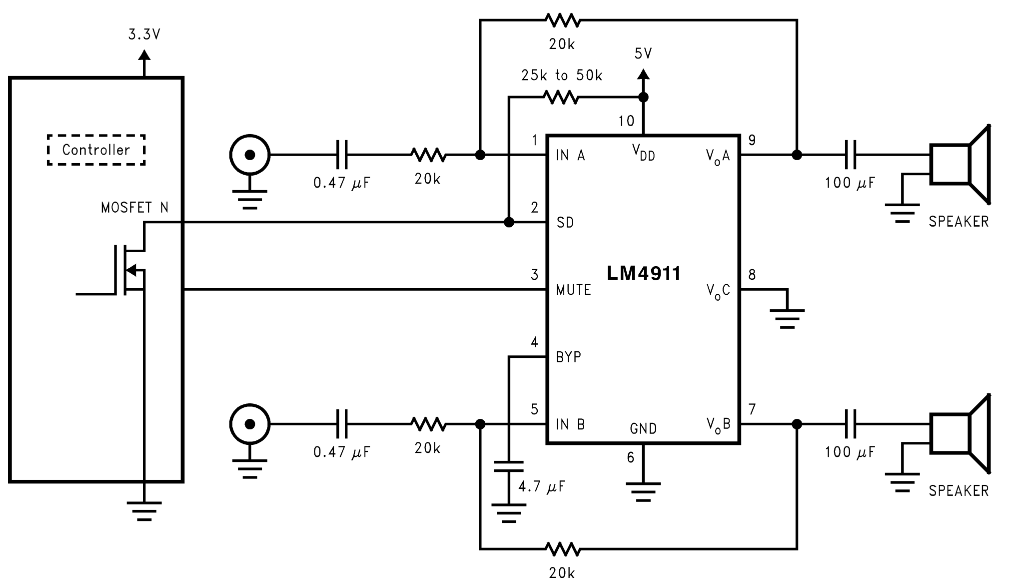

Figure 62. Recommended Circuit for Different Supply Turn-On Timing

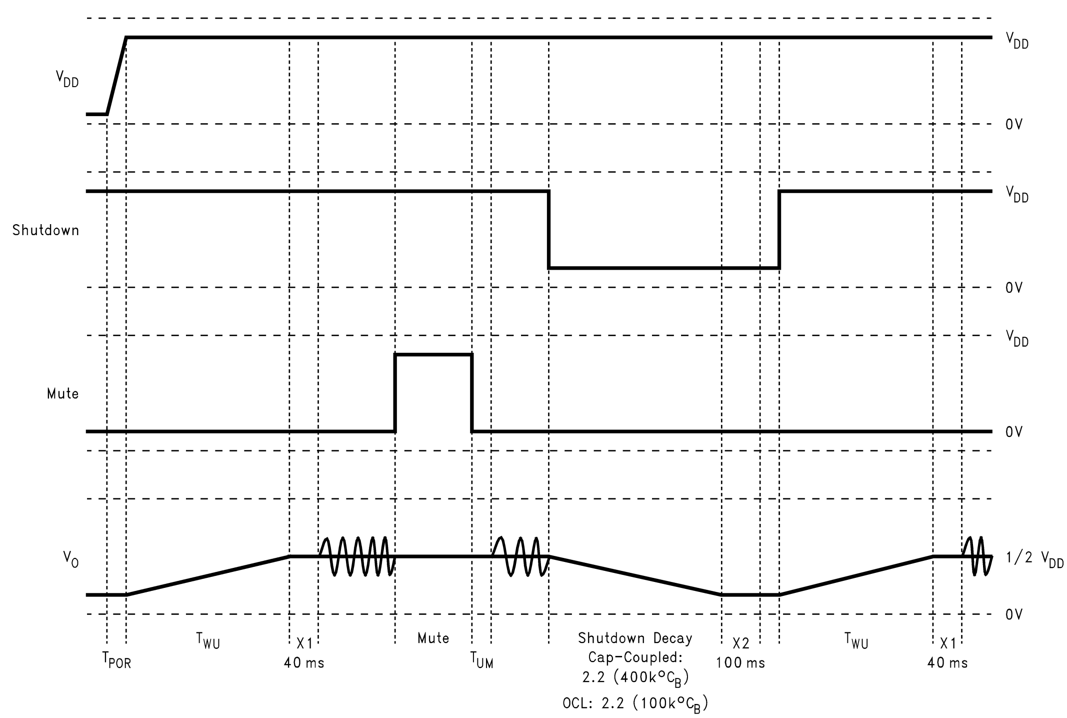

Figure 63. Turn-On, Shutdown, and Mute Timing for Cap-Coupled Mode

POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier and must be thoroughly understood to ensure a successful design. When operating in capacitor-coupled mode, Equation 1 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \tag{1}$$

Since the LM4911/LM4911Q has two operational amplifiers in one package, the maximum internal power dissipation point is twice that of the number which results from Equation 1. From Equation 1, assuming a 3V power supply and an 32Ω load, the maximum power dissipation point is 14mW per amplifier. Thus the maximum package dissipation point is 28mW.

When operating in OCL mode, the maximum power dissipation increases due to the use of the third amplifier as a buffer and is given in Equation 2:

$$P_{DMAX} = 4(V_{DD})^2 / (\pi^2 R_L) \tag{2}$$

The maximum power dissipation point obtained from either Equation 1 or Equation 2 must not be greater than the power dissipation that results from Equation 3:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \tag{3}$$

For package DGS0010A, θ_{JA} = 190°C/W; for package NGY0010A, θ_{JA} = 63°C/W. T_{JMAX} = 150°C for the LM4911/LM4911Q. Depending on the ambient temperature, T_A, of the system surroundings, Equation 3 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 1 or Equation 2 is greater than that of Equation 3, then either the supply voltage must be decreased, the load impedance increased or T_A reduced. For the typical application of a 3V power supply, with a 32Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 144°C provided that device operation is around the maximum power dissipation point. Thus, for typical applications, power dissipation is not an issue. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature may be increased accordingly. Refer to the Typical Performance Characteristics curves for power dissipation information for lower output powers.

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATIONS

The LM4911/LM4911Q's exposed-DAP (die attach paddle) package (WSON) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane, and surrounding air.

The WSON package should have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad may be connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area. Further detailed and specific information concerning PCB layout, fabrication, and mounting an WSON package is available from TI's Package Engineering Group under application note AN-1187 (SNOA401).

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is important for low noise performance and high power supply rejection. The capacitor location on the power supply pins should be as close to the device as possible.

Typical applications employ a 3V regulator with 10mF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4911/LM4911Q. A bypass capacitor value in the range of 0.1µF to 1µF is recommended for C_S.

MICRO POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the LM4911/LM4911Q's shutdown function. Activate micro-power shutdown by applying a logic-low voltage to the SHUTDOWN pin. When active, the LM4911/LM4911Q's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The trigger point varies depending on supply voltage and is shown in the Shutdown Hysteresis Voltage graphs in the Typical Performance Characteristics section. The low 0.1µA(typ) shutdown current is achieved by applying a voltage that is as near as ground as possible to the SHUTDOWN pin. A voltage that is higher than ground may increase the shutdown current. There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 100kΩ pull-up resistor between the SHUTDOWN pin and V_{DD}. Connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by opening the switch. Closing the switch connects the SHUTDOWN pin to ground, activating micro-power shutdown.

The switch and resistor specifies that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull-up resistor.

Shutdown enable/disable times are controlled by a combination of C_B and V_{DD}. Larger values of C_B results in longer turn on/off times from Shutdown. Smaller V_{DD} values also increase turn on/off time for a given value of C_B. Longer shutdown times also improve the LM4911/LM4911Q's resistance to click and pop upon entering or returning from shutdown. For a 2.4V supply and C_B = 4.7µF, the LM4911/LM4911Q requires about 2 seconds to enter or return from shutdown. This longer shutdown time enables the LM4911/LM4911Q to have virtually zero pop and click transients upon entering or release from shutdown.

Smaller values of C_B will decrease turn-on time, but at the cost of increased pop and click and reduced PSRR. Since shutdown enable/disable times increase dramatically as supply voltage gets below 2.2V, this reduced turn-on time may be desirable if extreme low supply voltage levels are used as this would offset increases in turn-on time caused by the lower supply voltage. This technique is not recommended for OCL mode since shutdown enable/disable times are very fast (0.5s) independent of supply voltage.

When in cap-coupled mode, some restrictions on the usage of Mute are in effect when entering or returning from shutdown. These restrictions require Mute not be toggled immediately following a return or entrance to shutdown for a brief period. These periods are shown as X1 and X2 and are discussed in greater detail in the Mute section as well as shown in Figure 63.

MUTE

When in C-CUPL mode, the LM4911/LM4911Q also features a mute function that enables extremely fast turn-on/turn-off with a minimum of output pop and click with a low current consumption (≤ 100µA). The mute function leaves the outputs at their bias level, thus resulting in higher power consumption than shutdown mode, but also provides much faster turn on/off times. Mute mode is enabled by providing a logic high signal on the MUTE pin in the opposite manner as the shutdown function described above. Threshold voltages and activation techniques match those given for the shutdown function as well.

Mute may not appear to function when the LM4911/LM4911Q is used to drive high impedance loads. This is because the LM4911/LM4911Q relies on a typical headphone load (16-32Ω) to reduce input signal feedthrough through the input and feedback resistors. Mute attenuation can thus be calculated by the following formula:

Mute Attenuation (dB) = $20\text{Log}(R_L / (R_i+R_F))$

Parallel load resistance may be necessary to achieve satisfactory Mute levels when the application load is known to be high impedance.

The mute function is not necessary when the LM4911/LM4911Q is operating in OCL mode since the shutdown function operates quickly in OCL mode with less power consumption than mute.

Mute may be enabled during shutdown transitions, but should not be toggled for a brief period immediately after exiting or entering shutdown. These brief time periods are labeled X1 (time after returning from shutdown) and X2 (time after entering shutdown) and are shown in the timing diagram given in Figure 63. X1 occurs immediately following a return from shutdown (T_{WU}) and lasts 40ms±25%. X2 occurs after the part is placed in shutdown and the decay of the bias voltage has occurred (2.2*400k*C_B for cap-coupled and 2.2*100k*C_B for

OCL) and lasts for 100ms±25%. The timing of these transition periods relative to X1 and X2 is also shown in Figure 63. Mute should not be toggled during these time periods, but may be made during the shutdown transitions or any other time the part is in normal operation (while in cap-coupled mode - Mute is not valid in OCL mode). Failure to operate mute correctly may result in much higher click and pop values or failure of the device to mute at all.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4911/LM4911Q is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4911/LM4911Q is unity-gain stable which gives the designer maximum system flexibility. The LM4911/LM4911Q should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than $1V_{rms}$ are available from sources such as audio codecs. Very large values should not be used for the gain-setting resistors. Values for R_i and R_f should be less than 1MΩ. Please refer to the section, Audio Power Amplifier Design, for a more complete explanation of proper gain selection

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in Figure 2 and Figure 3. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response and turn-on time.

SELECTION OF INPUT CAPACITOR SIZE

Amplifying the lowest audio frequencies requires a high value input coupling capacitor, C_i. A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the headphones used in portable systems have little ability to reproduce signals below 60Hz. Applications using headphones with this limited frequency response reap little improvement by using a high value input capacitor.

In addition to system cost and size, turn on time is affected by the size of the input coupling capacitor C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage. This charge comes from the output via the feedback Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on time can be minimized. A small value of C_i (in the range of 0.1µF to 0.39µF), is recommended.

AUDIO POWER AMPLIFIER DESIGN

A 25mW/32Ω AUDIO AMPLIFIER

Given:	
Power Output	25mWrms
Load Impedance	32Ω
Input Level	1Vrms
Input Impedance	20kΩ

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the Typical Performance Characteristics section, the supply rail can be easily found.

3V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4911/LM4911Q to reproduce peak in excess of 25mW without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the Power Dissipation section.

Once the power dissipation equations have been addressed, the required gain can be determined from Equation 1.

$$A_V \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (4)$$

From Equation 3, the minimum A_V is 0.89; use A_V = 1. Since the desired input impedance is 20kΩ, and with a A_V gain of 1, a ratio of 1:1 results from for R_f to R_i. The values are chosen with R_i = 20kΩ and R_f = 20kΩ. The final design step is to address the bandwidth requirements which must be stated as a pair of -3dB frequency points. Five times away from a -3dB point is 0.17dB down from passband response which is better than the required ± 0.25dB specified.

f_L = 100Hz/5 = 20Hz

f_H = 20kHz * 5 = 100kHz

As stated in the External Components section, R_i in conjunction with C_i creates a

C_i ≥ 1 / (2π * 20kΩ * 20Hz) = 0.397µF; use 0.39µF.

The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_V. With an A_V = 1 and f_H = 100kHz, the resulting GBWP = 100kHz which is much smaller than the LM4911/LM4911Q GBWP of 10MHz. This figure displays that is a designer has a need to design an amplifier with higher differential gain, the LM4911/LM4911Q can still be used without running into bandwidth limitations.

Figure 62 shows an optional resistor connected between the amplifier output that drives the headphone jack sleeve and ground. This resistor provides a ground path that suppressed power supply hum. This hum may occur in applications such as notebook computers in a shutdown condition and connected to an external powered speaker. The resistor's 100Ω value is a suggested starting point. Its final value must be determined based on the tradeoff between the amount of noise suppression that may be needed and minimizing the additional current drawn by the resistor (25mA for a 100Ω resistor and a 5V supply).

ESD PROTECTION

As stated in the Absolute Maximum Ratings, the LM4911/LM4911Q has a maximum ESD susceptibility rating of 2000V. For higher ESD voltages, the addition of a PCDN042 dual transil (from California Micro Devices), as shown in Figure 64, will provide additional protection.

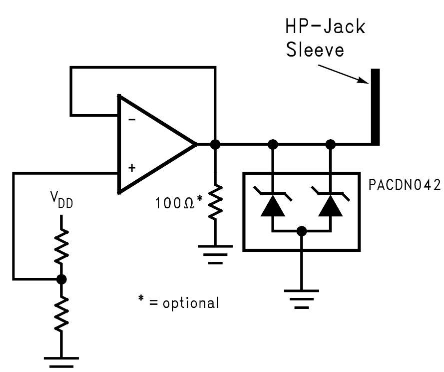

Figure 64. The PCDN042 provides additional ESD protection beyond the 2000V shown in the Absolute Maximum Ratings for the V_OC output

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM4911MM/NOPB	Active	Production	VSSOP (DGS) | 10	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	GA3
LM4911MM/NOPB.A	Active	Production	VSSOP (DGS) | 10	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	GA3
LM4911QMM/NOPB	Active	Production	VSSOP (DGS) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	GC9
LM4911QMM/NOPB.A	Active	Production	VSSOP (DGS) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	GC9
LM4911QMMX/NOPB	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	GC9
LM4911QMMX/NOPB.A	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	GC9

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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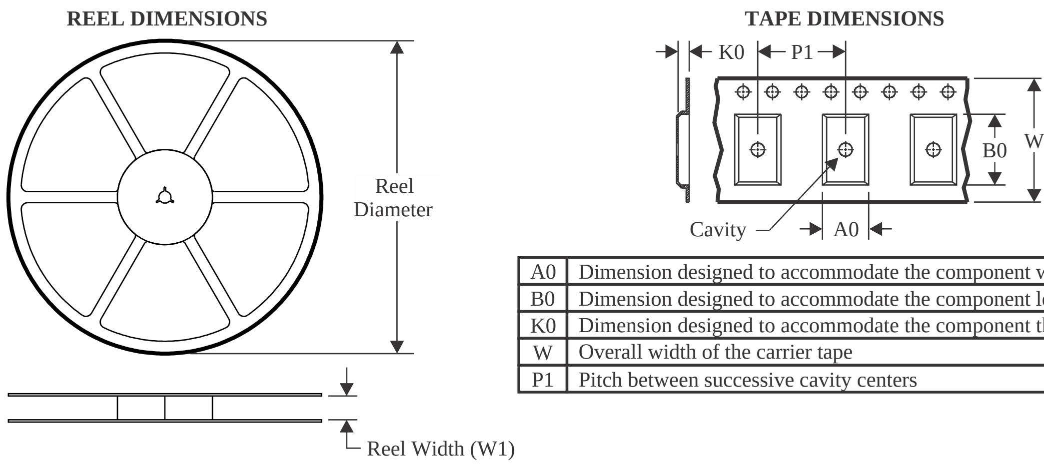
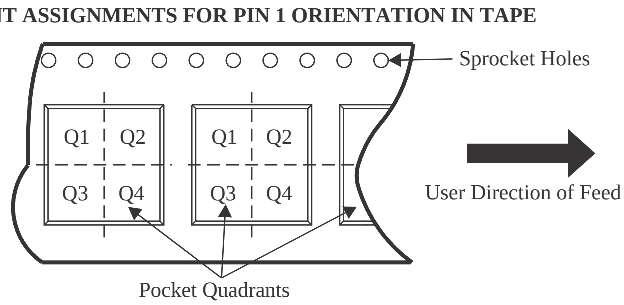
TAPE AND REEL INFORMATION



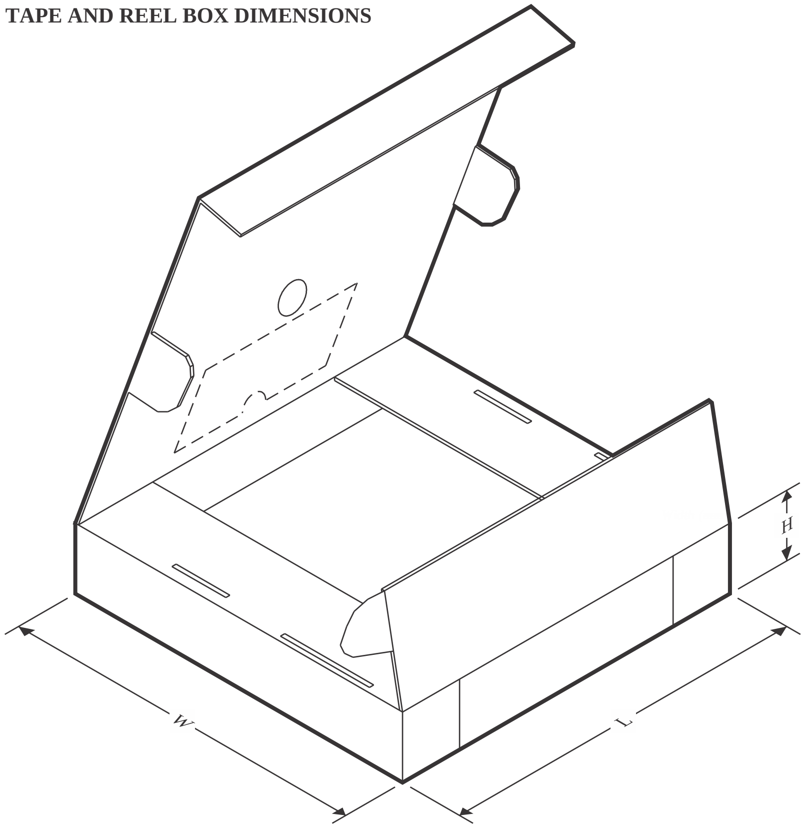
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

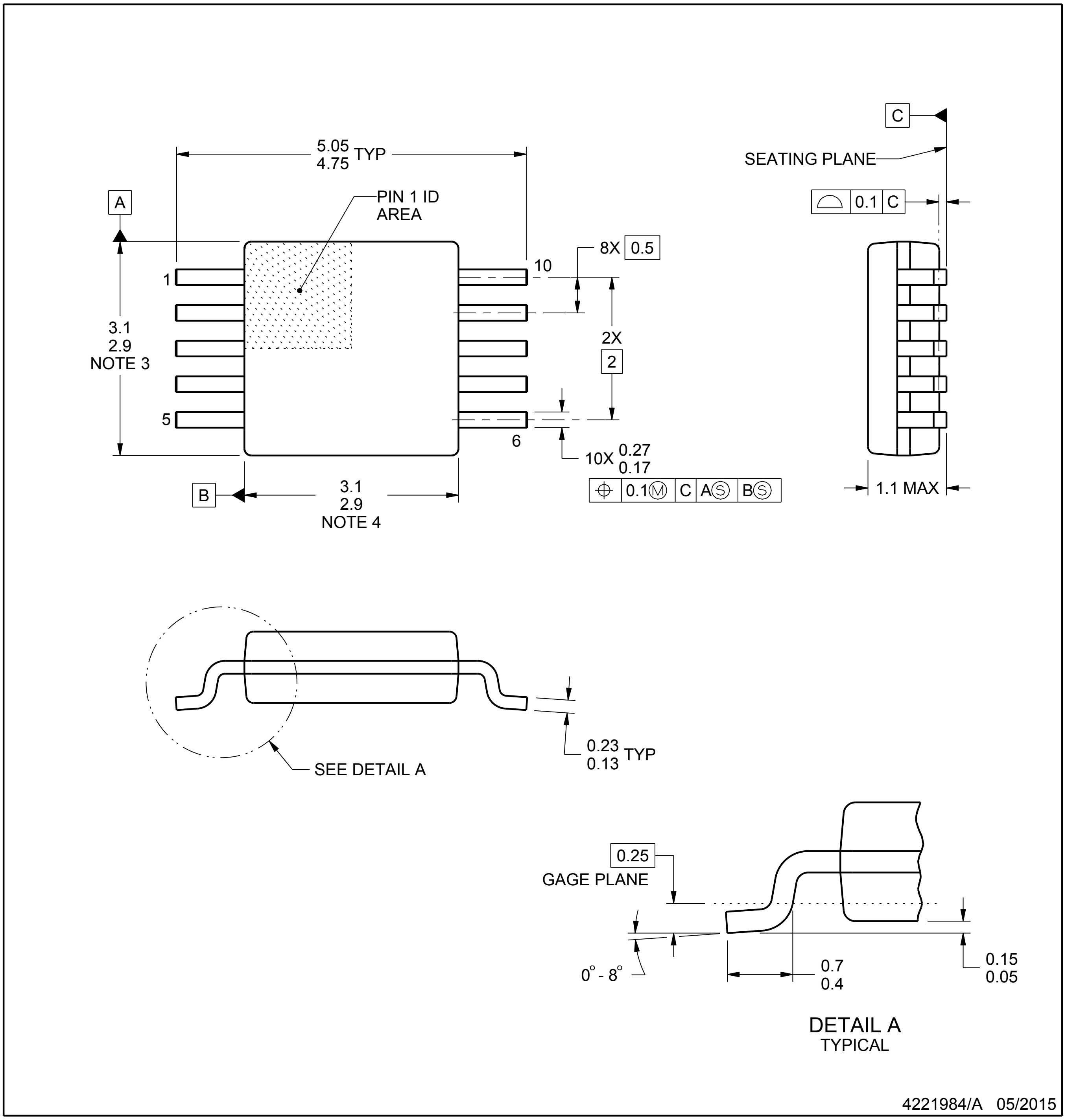
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4911MM/NOPB	VSSOP	DGS	10	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4911QMM/NOPB	VSSOP	DGS	10	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4911QMMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



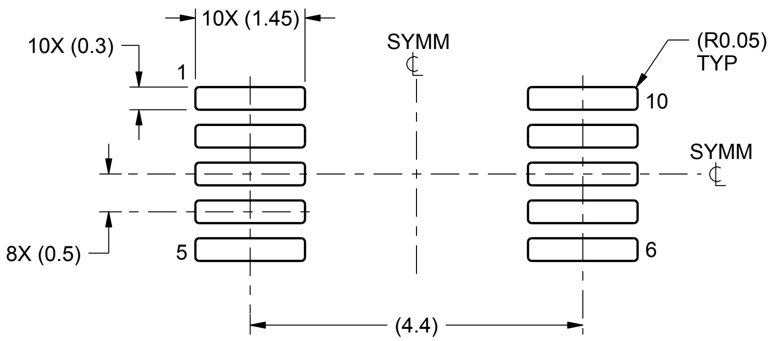
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4911MM/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LM4911QMM/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LM4911QMMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0

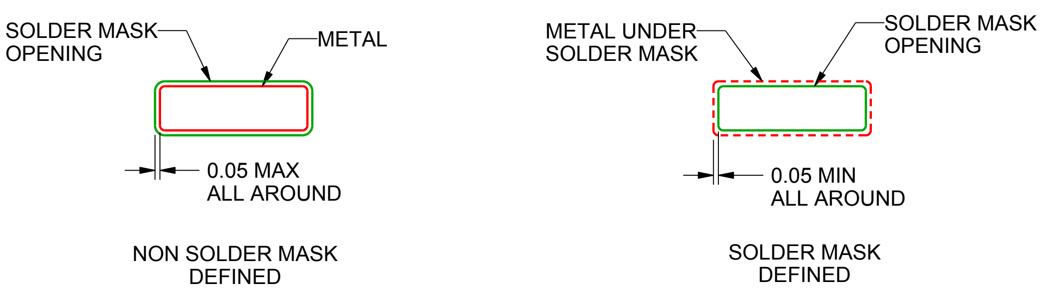


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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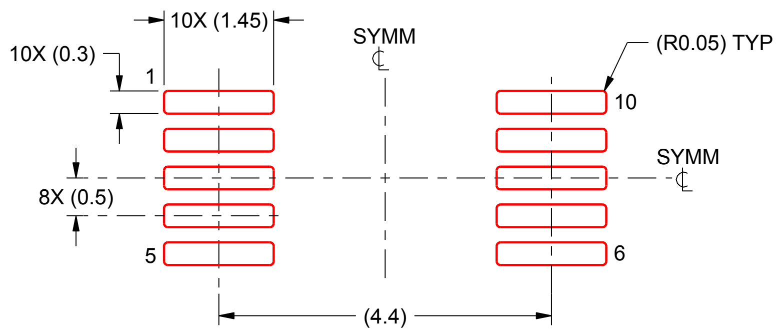
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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