South Sea Semiconductor

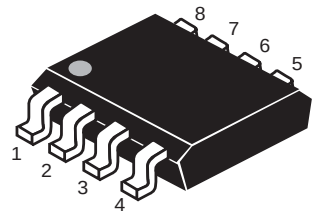
SSM8405

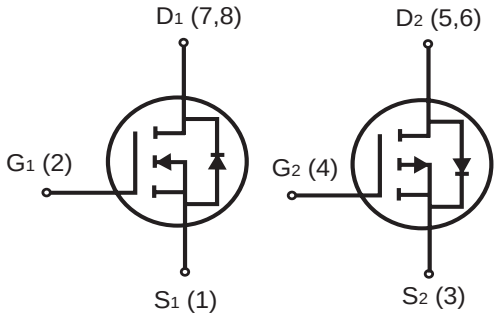
Dual Enhancement Mode MOSFET

Product Summary (N-Channel)		
V_{DS} (V)	I_D (A)	$R_{DS(ON)}$ (mΩ) Max
30V	7A	25 @V_{GS} = 10V
		40 @V_{GS} = 4.5V

Product Summary (P-Channel)		
V_{DS} (V)	I_D (A)	$R_{DS(ON)}$ (mΩ) Max
-30V	-5A	45 @V_{GS} = -10V
		60 @V_{GS} = -4.5V

SO-8





ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)					
Parameter		Symbol	N-Channel Limited	P-Channel Limited	Unit
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	±22	±22	
Drain Current-Continuous @ Ta	25 °C	I_D	7	-5	A
	70 °C		6	-4.5	
-Pulsed [b]		I_{DM}	30	-20	
Drain-Source Diode Forward Current [a]		I_S	1.6	-1.6	
Maximum Power Dissipation [a]	Ta=25 °C	P_D	2.0		W
	Ta=70 °C		1.44		
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C
THERMAL CHRACTERISTICS					
Thermal Resistance, Junction-to-Ambient [a]		$R_{\theta JA}$	62.5		°C/W

South Sea Semiconductor, September 2005 (Rev 2.0)

N-Channel Electrical Characteristics (T_A = 25°C unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V, V_{GS}=0V			1	μA
Gate-Body Leakage	I_{GSS}	V_{GS}=±22V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} I_D=250μA	1	1.5	2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=6.6A		20	25	mΩ
		V_{GS}=4.5V, I_D=5A		35	40	
On-State Drain Current	$I_{D(ON)}$	V_{DS}=5V, V_{GS}=4.5V	20			A
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=6.6A		10		S
Input Capacitance	C_{ISS}	V_{DS}=15V		766	853	pF
Output Capacitance	C_{OSS}	V_{GS}=0V		142	166	
Reverse Transfer Capacitance	C_{RSS}	f=1.0MHz		98	122	
Turn-On Delay Time	$t_{D(ON)}$	V_{DD}=15V,		7.5	10	ns
Rise Time	t_r	I_D=6.6A,		27.5	35	
Turn-Off Delay Time	$t_{D(OFF)}$	V_{GS}=10V,		12	22	
Fall Time	t_f	R_{GEN}=3Ω		7.5	12	
Total Gate Charge	Q_g	V_{DS}=10V, I_D=6.6A, V_{GS}=10V		14	18	nC
		V_{DS}=10V, I_D=6.6A, V_{GS}=4.5V		6	10	
Gate-Source Charge	Q_{gs}	V_{DS}=15V I_D=6.6A, V_{GS}=10V		2.3	4	
Gate-Drain Charge	Q_{gd}			4	6	
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_D=1.6A		0.8	1.2	V

P-Channel Electrical Characteristics (T_A = 25°C unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-24V, V_{GS}=0V			-1	μA
Gate-Body Leakage	I_{GSS}	V_{GS}=±22V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} I_D=-250μA	-1	-1.5	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-5A		35	45	mΩ
		V_{GS}=-4.5V, I_D=-4A		50	60	
On-State Drain Current	$I_{D(ON)}$	V_{DS}=-5V, V_{GS}=-10V	20			A
Forward Transconductance	g_{FS}	V_{DS}=-5V, I_D=-5A		10		S
Input Capacitance	C_{ISS}	V_{DS}=-15V		720	845	pF
Output Capacitance	C_{OSS}	V_{GS}=0V		155	185	
Reverse Transfer Capacitance	C_{RSS}	f=1.0MHz		90	125	
Gate Resistance	Rg	V_{GS}=0V, V_{DS}=0V, f=1.0MHz		3.5		
Turn-On Delay Time	$t_{D(ON)}$	V_{DD}=-15V,		4.5	14	ns
Rise Time	t_r	V_{GS}=-10V,		8	30	
Turn-Off Delay Time	$t_{D(OFF)}$	R_{GEN}=3Ω,		47	75	
Fall Time	t_f	R_L=2.7Ω		22.5	35	
Total Gate Charge	Q_g	V_{DS}=-15V, I_D=-5A, V_{GS}=-10V		14	16	nC
		V_{DS}=-15V, I_D=-5A, V_{GS}=-4.5V		7	10	
Gate-Source Charge	Q_{gs}	V_{DS}=-15V, I_D=-5A, V_{GS}=-10V		1.5	2.8	
Gate-Drain Charge	Q_{gd}			4.2	6	
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_D=-1.6A		-0.8	-1.2	V

Notes：

a. Surface Mounted on FR4 Board, t ≤10 sec.

b. Pulse Test：Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

c. Guaranteed by design, not subject to production testing.

N-Channel

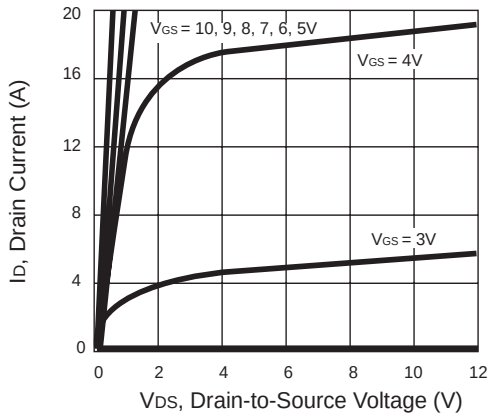


Figure 1. Output Characteristics

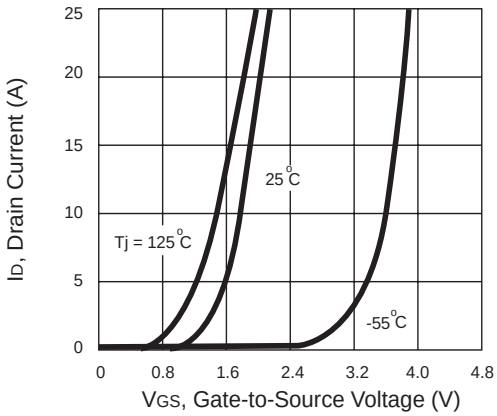


Figure 2. Thansfer Characteristics

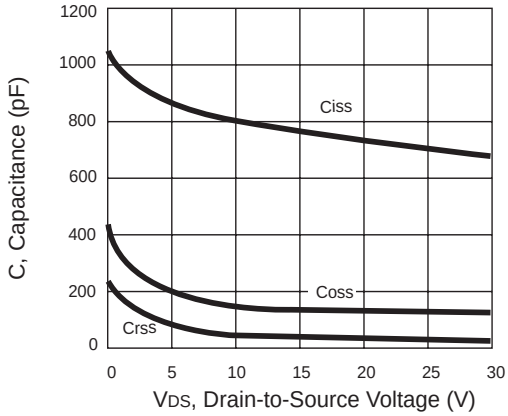
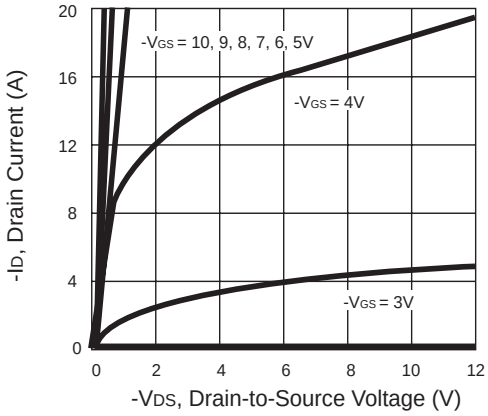


Figure 3. Capacitance

P-Channel



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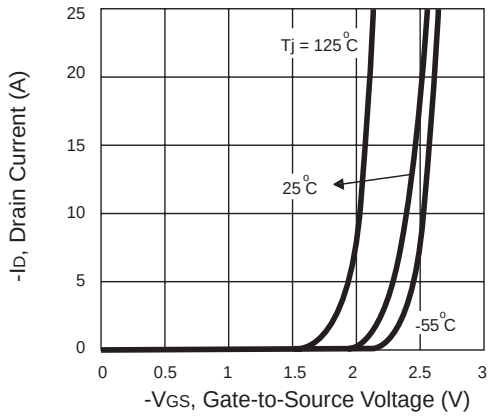
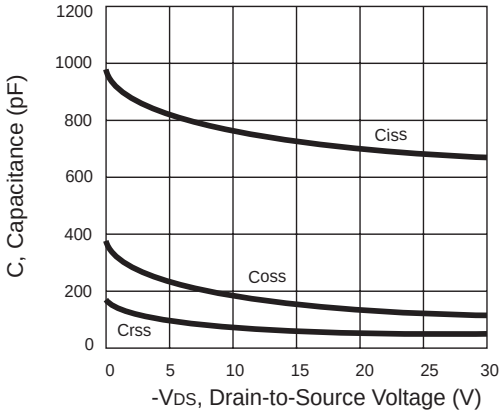


Figure 2. Thansfer Characteristics



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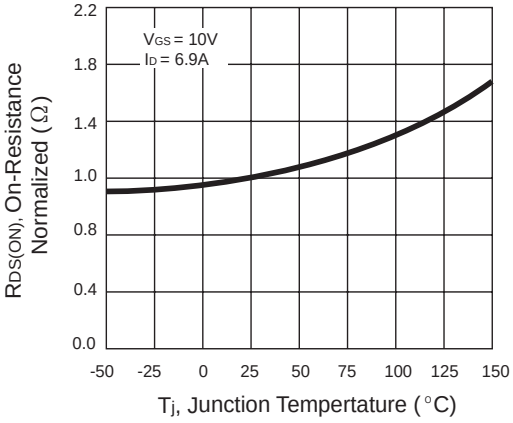


Figure 4. On-Resistance Variation with Temperature

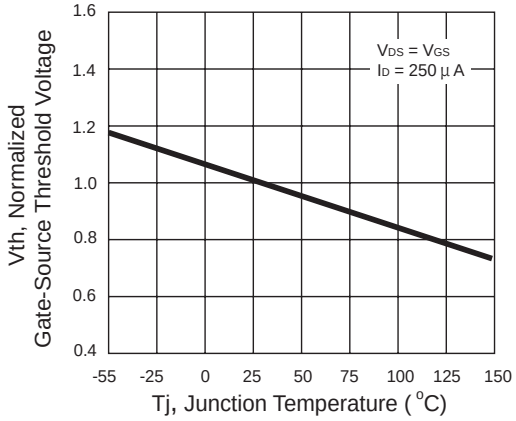


Figure 5. Gate Threshold Variation with Temperature

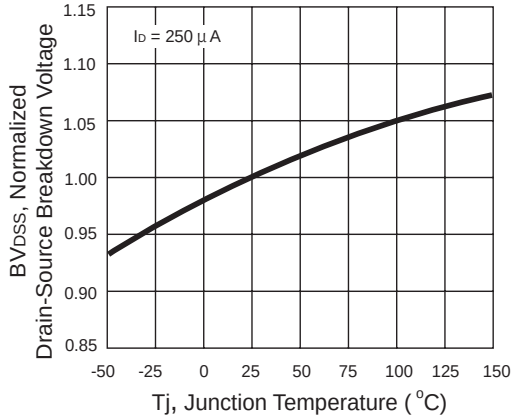
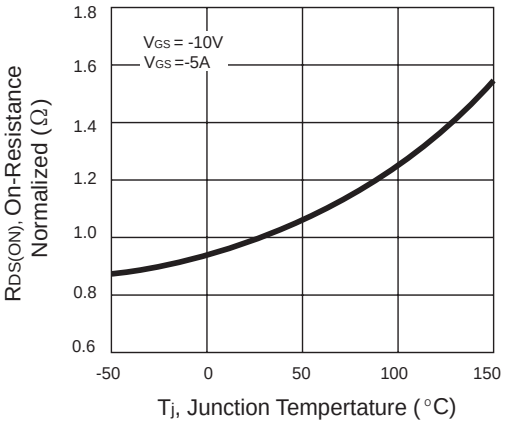


Figure 6. Breakdown Voltage Variation with Temperature

P-Channel



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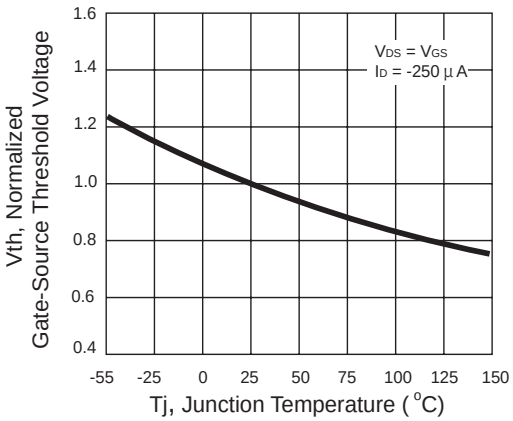

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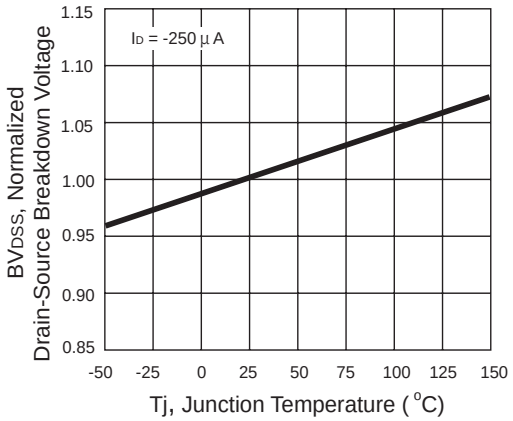

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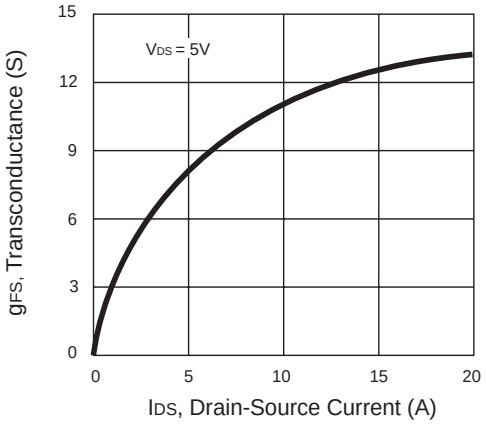


Figure 7. Transconductance Variation with Drain Current

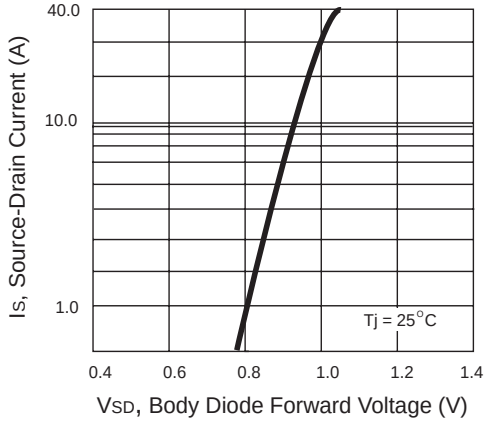


Figure 8. Body Diode Forward Voltage Variation with Source Current

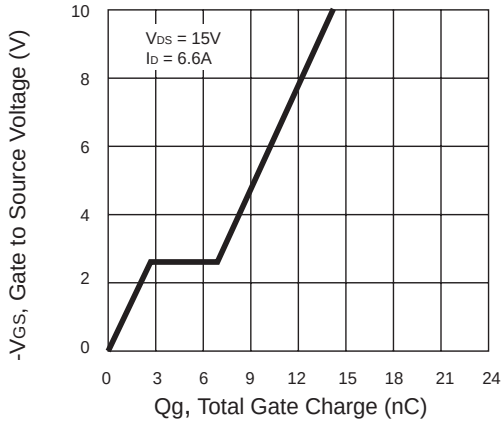
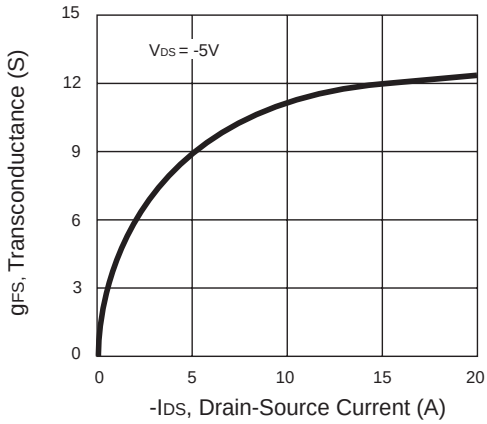


Figure 9. Gate Charge

P-Channel



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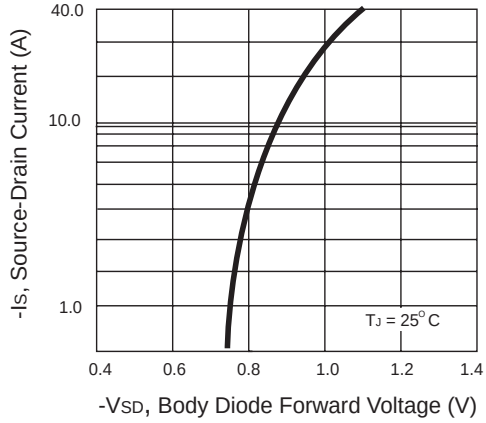

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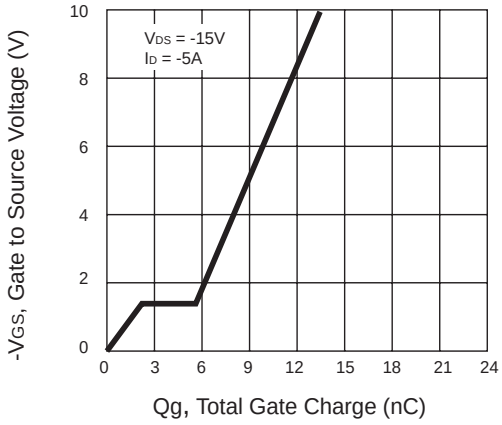

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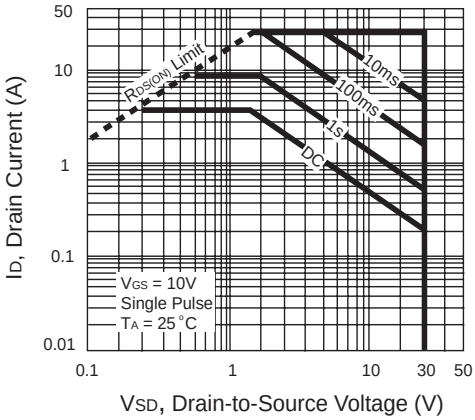
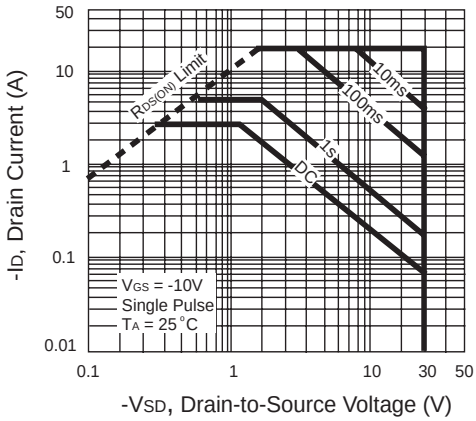


Figure 10. Maximum Safe Operating Area

P-Channel



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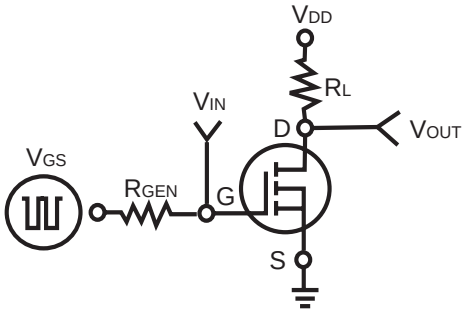


Figure 11. Switching Test Circuit

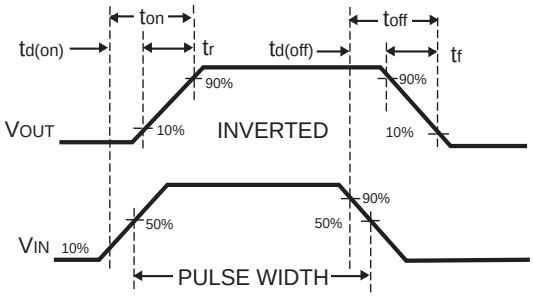


Figure 12. Switching Waveforms

N-Channel

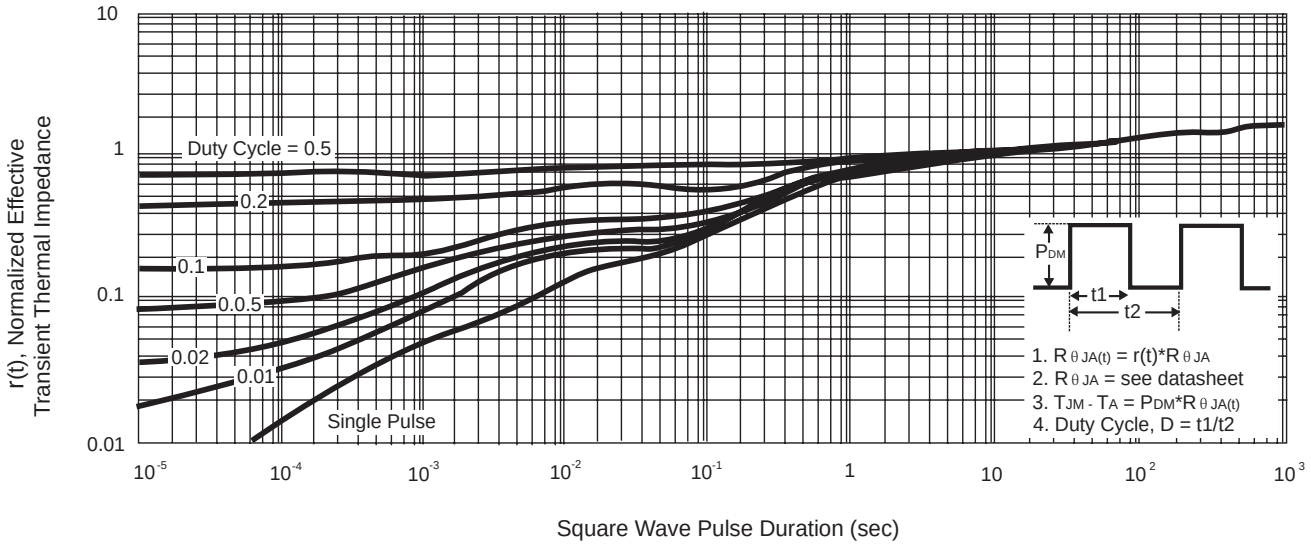


Figure 13. Normalized Thermal Transient Impedance Curve

P-Channel

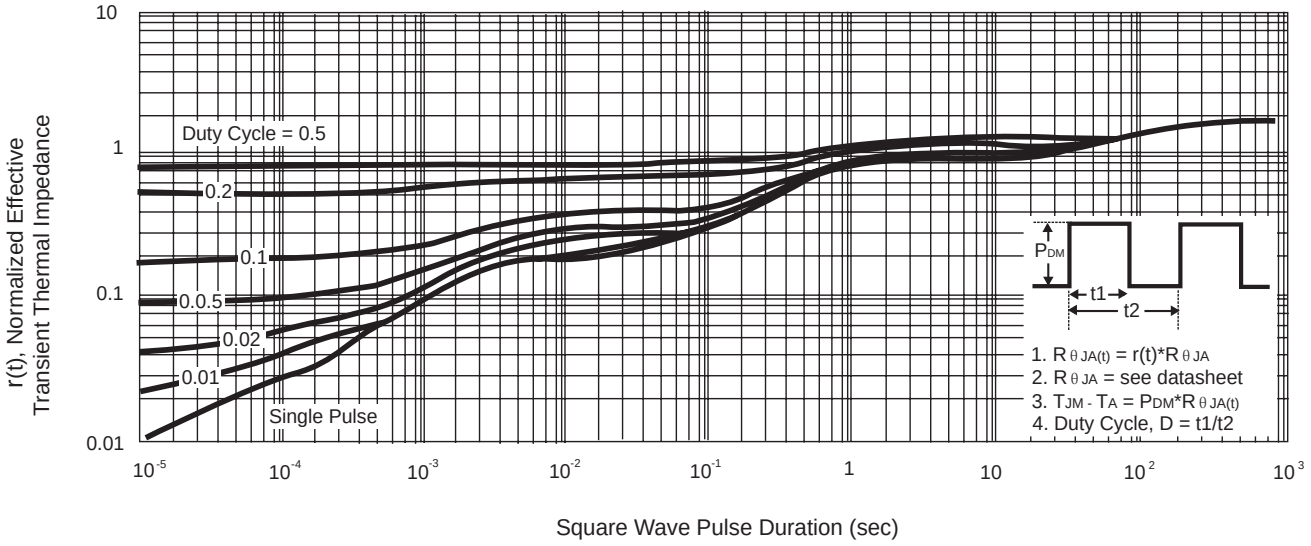
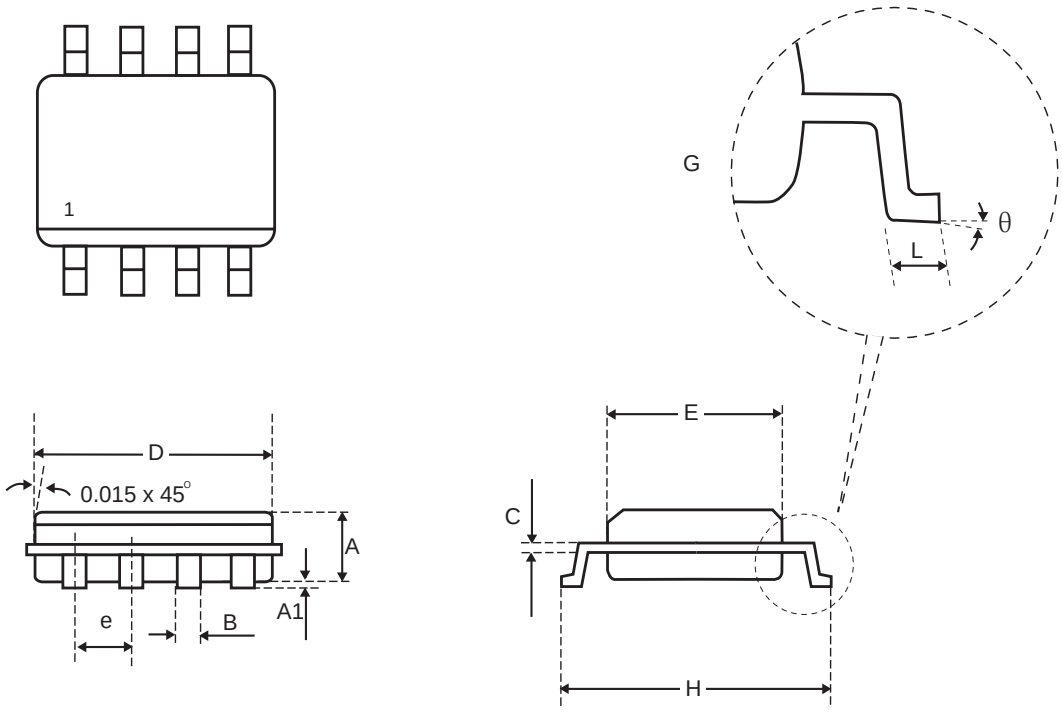


Figure 13. Normalized Thermal Transient Impedance Curve

Package Outline Dimensions

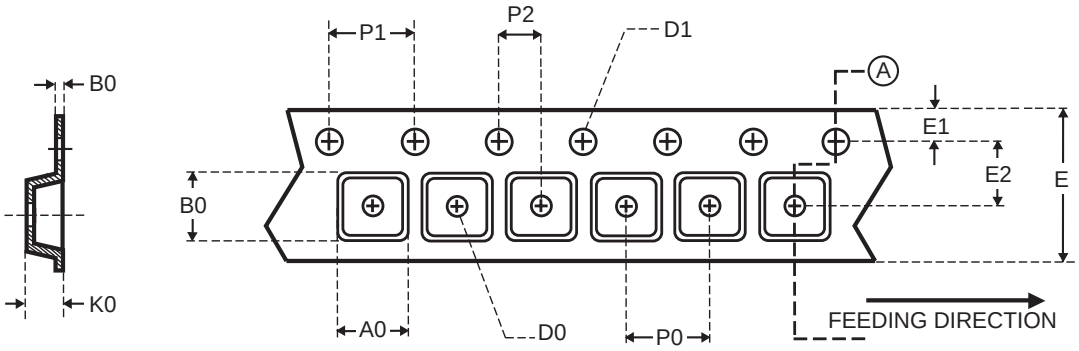
SO-8



SYMBOLS	MILLIMETERS		INCHES	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
B	0.41 Typ.		0.016 Typ.	
C	0.20 Typ.		0.008 Typ.	
D	4.80	4.98	0.189	0.196
E	3.81	3.99	0.150	0.157
e	1.25 Typ.		0.05 Typ.	
H	5.79	6.20	0.228	0.244
L	0.41	1.27	0.016	0.050
θ	0°	8°	0°	8°

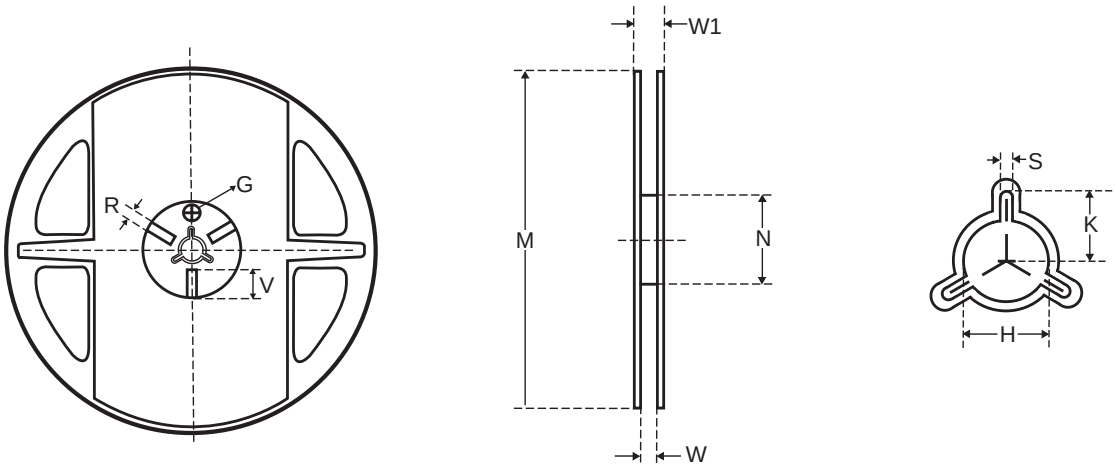
Carrier Tape & Reel Dimensions

SO-8



Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SOP 8N 150 mil	6.40	5.20	2.10	ψ1.50 (Min.)	ψ1.50 +0.10 −0.10	12.00 ±0.30	1.75	5.50 ± 0.05	8.00	4.00	2.00 ± 0.05	0.30 ± 0.05

UNIT：mm



Tape size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ψ330	330 ± 1	62 ±1.5	12.4 ± 0.2	16.8 −0.4	ψ12.75 ±0.15	–	2.0 ±0.15	–	–	–

UNIT：mm